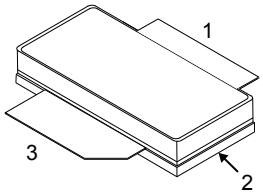
life.augmented

ST24180

Datasheet

180 W, 32 V, 2.3 to 2.5 GHz RF power LDMOS transistor



B2

Pin connection	
Pin	**Connection**
1	Gate
2	Source (bottom side)
3	Drain

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
ST24180	2350 MHz	32 V	180 W	15.3 dB	48%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internal input matching for ease of use
- Large positive and negative gate/source voltage range for improved class C operation
- In compliance with the European Directive 2002/95/EC

Applications

- RF energy
- Industrial, scientific and medical (ISM)

Description

The ST24180 is a 180 W, internally-matched LDMOS FET designed for multiple uses, especially for RF energy applications such as cooking, heating and medical with frequencies from 2400 to 2500 MHz. It is qualified for operations requiring up to 32 V.

STPOWER

Product status link
ST24180

Product summary	
Order code	ST24180
Marking	ST24180
Package	B2
Packing	Tape and Reel 13"
Base / Bulk	120 / 120

1 Electrical ratings

Table 1. Absolute maximum ratings (+25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	-6 to +10	V
V_{DD}	Drain supply voltage	32	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Junction-case thermal resistance T_{CASE} = +85 °C , T_J = +200 °C, DC test	0.35	°C/W

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to JESD22-A114)	2

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. Static

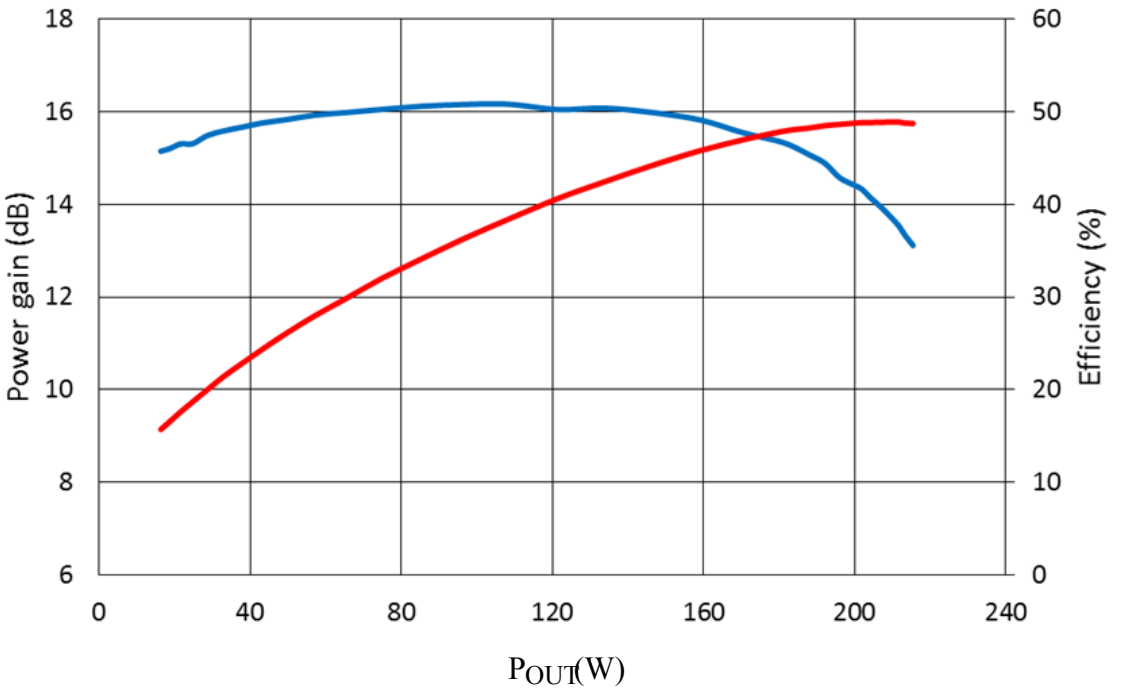
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 100 µA	65			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 28 V			1	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = 10 V			1	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 28 V, I_D = 600 µA	1.5		2.5	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_D = 1.55 A			0.22	V

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	V_{DD} = 32 V, I_{DQ} = 0.8 A, f = 2350 MHz, PW = 10 µs, DC = 10% (see Figure 1. Power gain and drain efficiency vs output power (at 2350 MHz) and Figure 3. Test circuit (f = 2350 MHz))	-	180	-	W
Gain	Power gain		-	15.3	-	dB
Efficiency	Drain efficiency		-	48	-	%
VSWR	Load mismatch	P_{OUT} = 180 W, all phases	-		10:1	

2.1 Electrical characteristics (curves)

Figure 1. Power gain and drain efficiency vs output power (at 2350 MHz)



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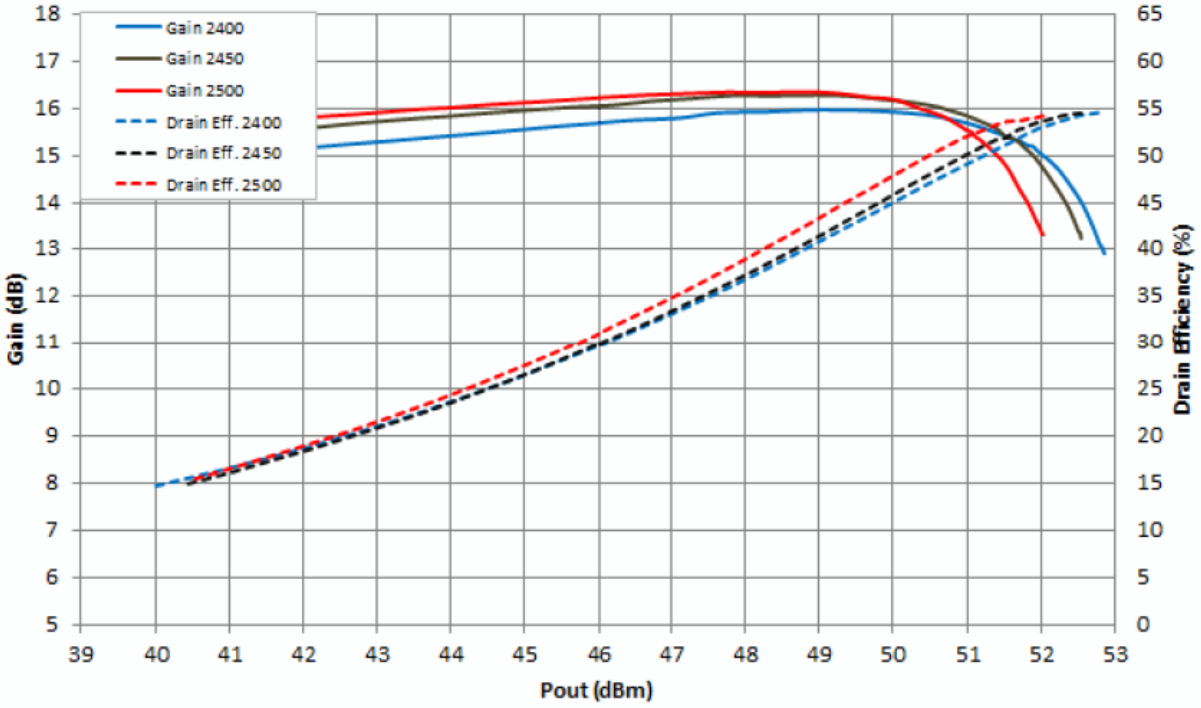
Note: V_{DD} = 32 V, I_{DQ} = 800 mA, pulse width = 10 µs, duty cycle = 10%

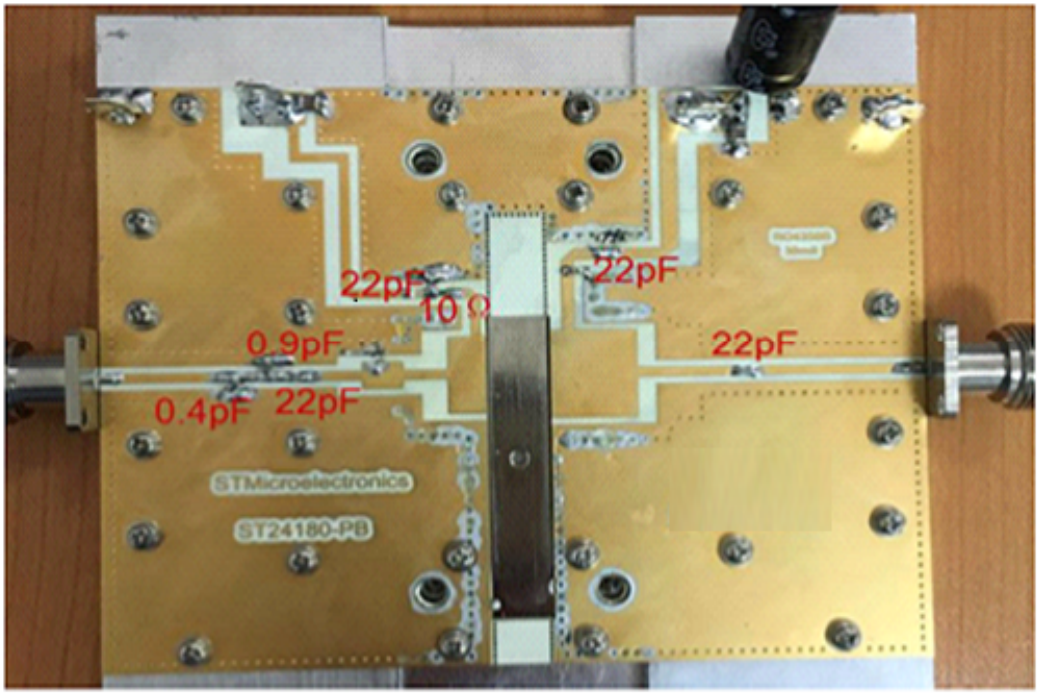
Figure 2. **Power gain and drain efficiency vs output power (2400 - 2500 MHz)**



Note: *V_{DD} = 28 V, I_{DQ} = 800 mA, pulse width = 10 µs, duty cycle = 10%*

3 Test circuits

Figure 3. **Test circuit (f = 2350 MHz)**



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 B2 package information

Figure 4. B2 package outline

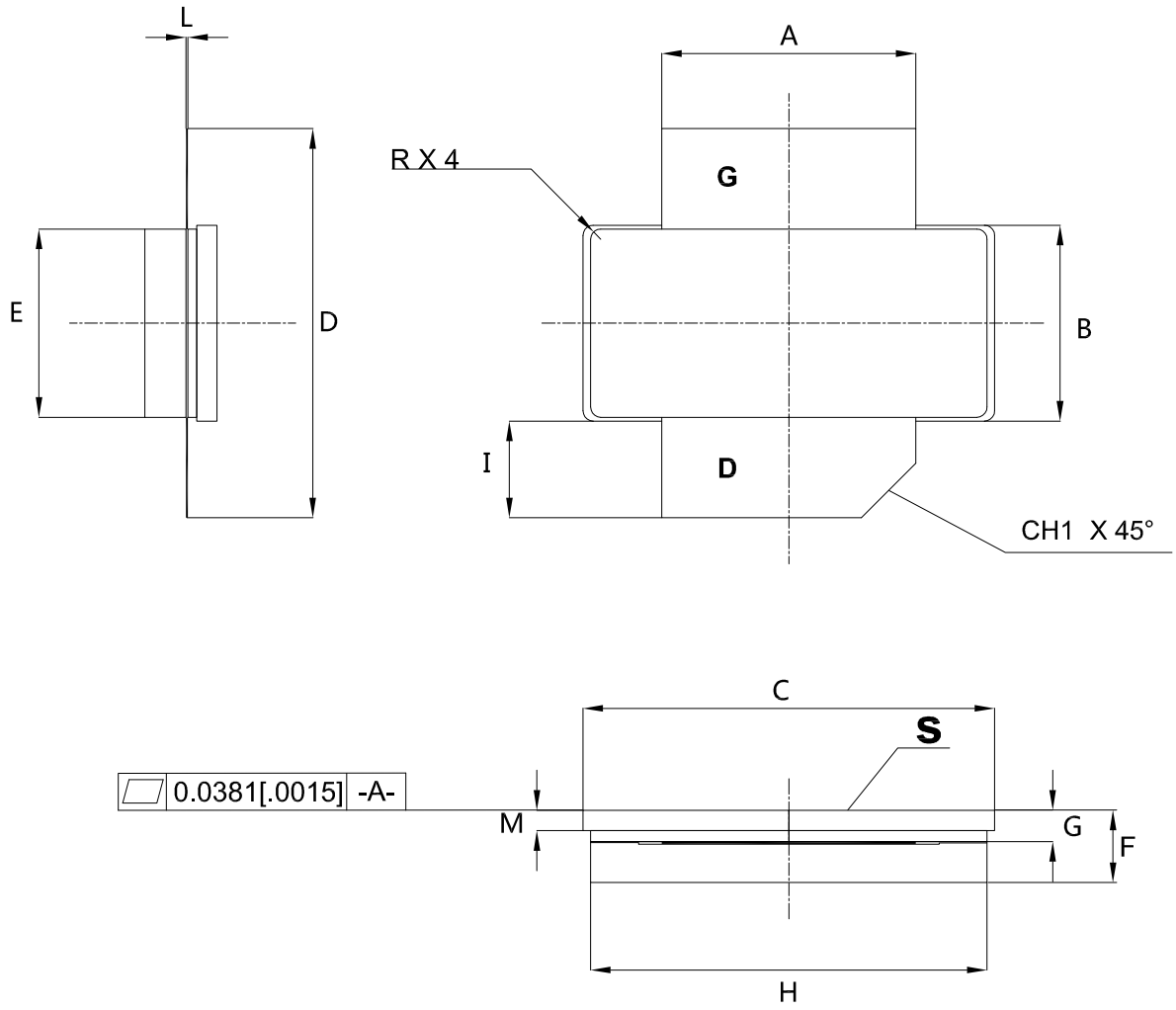


Table 6. **B2 mechanical data**

Symbol	Millimetres		
	Min	Typ	Max
A	12.57	12.7	12.83
B	9.65	9.78	9.91
C	20.44	20.57	20.70
D	19.31	19.44	19.57
E	9.27	9.40	9.53
F	3.23	3.61	3.99
G	1.44	1.57	1.70
H	19.68	19.81	19.94
I	4.70	4.83	4.96
L	0.07	0.10	0.15
M	0.89	1.02	1.15
CH1		2.72	
R		0.51	

Revision history

Table 7. **Document revision history**

Date	Version	Changes
01-Oct-2018	1	Initial release
16-Oct-2020	2	Updated Section Product status / summary, Table 5. Dynamic and Section 4.1 B2 package information.

Contents

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