

# AWR1243 单芯片 77 和 79GHz FMCW 收发器

## 1 器件概述

### 1.1 特性

- FMCW 收发器
  - 集成式 PLL、发送器、接收器、基带和 A2D
  - 76 至 81GHz 覆盖范围，具有 4GHz 的可用带宽
  - 四个接收通道
  - 三个发送通道（对于 AWR1243，可以同时使用两个通道；对于 AWR1243P，可以同时使用全部三个通道）
  - 基于分数 N PLL 的超精确线性调频脉冲引擎
  - TX 功率：12dBm
  - RX 噪声系数：
    - 14dB（76 至 77GHz）
    - 15dB（77 至 81GHz）
  - 1MHz 时的相位噪声：
    - -95dBc/Hz（76 至 77GHz）
    - -93dBc/Hz（77 至 81GHz）
- 内置的校准和自检
  - 内置的固件 (ROM)
  - 针对频率和温度进行自校准的系统
- 主机接口
  - 通过 SPI 与外部处理器进行控制连接
  - 通过 MIPI D-PHY 和 CSI2 V1.1 与外部处理器进行数据连接
  - 用于故障报告的中断
- 以 ASIL B 级为目标
- 符合 AECQ100 标准
- AWR1243 高级特性
  - 嵌入式自监控，无需使用主机处理器
  - 复基带架构
  - 可以选择级联多个器件以增加通道数
  - 嵌入式干扰检测功能
- 电源管理
  - 内置的 LDO 网络，可增强 PSRR
  - I/O 支持双电压 3.3V/1.8V
- 时钟源
  - 支持外部驱动、频率为 40MHz 的时钟（方波/正弦波）
  - 支持 40MHz 晶体与负载电容器相连接
- 轻松的硬件设计
  - 0.65mm 间距、161 引脚 10.4mm × 10.4mm 覆晶 BGA 封装，可实现轻松组装和低成本 PCB 设计
  - 小尺寸解决方案
- 支持汽车运行温度范围

### 1.2 应用

- 自动公路驾驶
- 自动紧急刹车
- 自适应巡航控制
- 使用级联配置的成像雷达

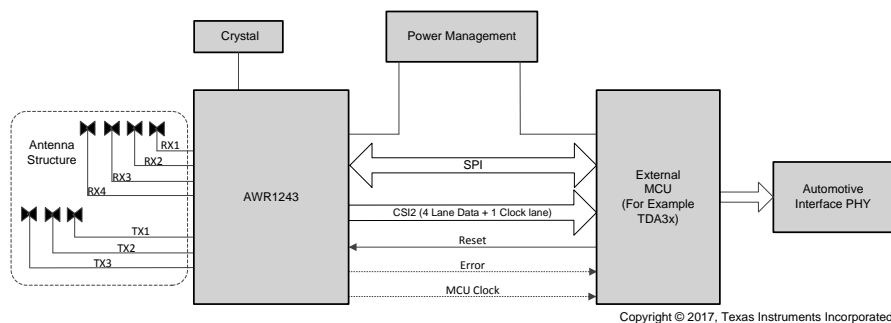


图 1-1. 适用于汽车应用的雷达传感器传感器

### 1.3 说明

AWR1243 器件是一款能够在 76 至 81GHz 频带内运行的集成式单芯片 FMCW 收发器。该器件在极小的封装中实现了前所未有的集成度。AWR1243 是适用于汽车领域中的低功耗、自监控、超精确雷达系统的理想解决方案。



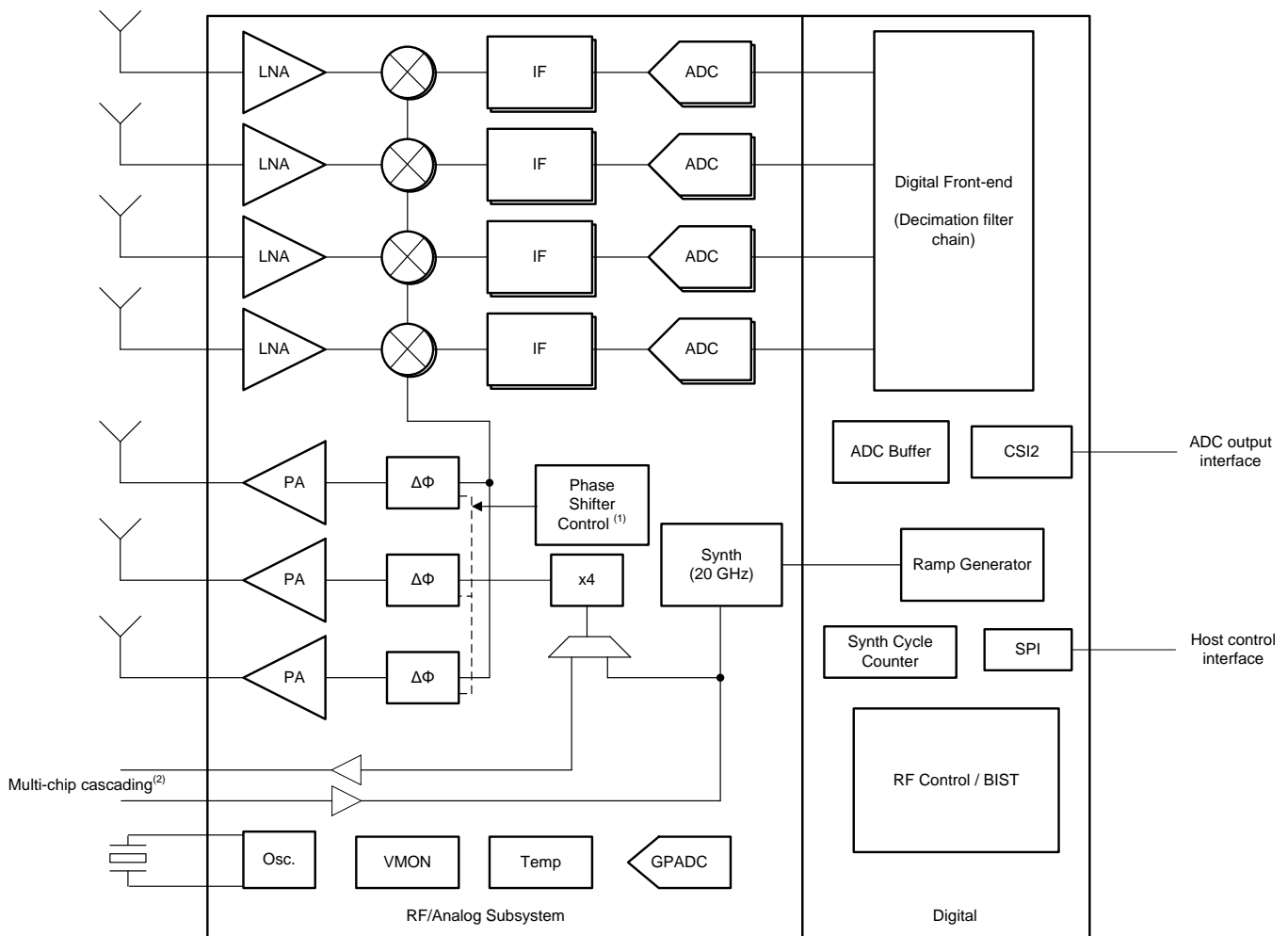
AWR1243 器件是一种自包含 FMCW 收发器单芯片解决方案，能够简化 76 至 81GHz 频带中的汽车雷达传感器实施。它构建在 TI 的低功耗 45nm RFCMOS 工艺之上，从而实现了一个具有内置 PLL 和模数转换器的单片实施 3TX、4RX 系统。简单编程模型更改可支持各种传感器实施（近距离、中距离和远距离），并且能够进行动态重新配置，从而实现多模式传感器。此外，该器件作为完整的平台解决方案进行提供，该解决方案包括硬件参考设计、软件驱动程序、样例配置、API 指南以及用户文档。

器件信息<sup>(1)</sup>

器件编号	封装	封装尺寸
AWR1243FBIGABLQ1 (托盘)	FCBGA (161)	10.4mm x 10.4mm
XA1243PBGABL (托盘)		
AWR1243FBIGABLRQ1 (卷)		

(1) 更多信息请参见 节 9, 机械封装和可订购产品信息。

## 1.4 功能框图



(1) 相移控制:

- 为 AWR1243 提供了 0°/180° BPM
- 为 AWR1243P 提供了 0°/180° BPM 和 5.625° 分辨率控制选项

(2) AWR1243P 提供了多芯片级联功能。

## 内容

<b>1</b>	<b>器件概述</b> .....	<b>1</b>	6.1	Overview .....	<b>33</b>
1.1	特性 .....	1	6.2	Functional Block Diagram .....	<b>33</b>
1.2	应用 .....	1	6.3	Subsystems .....	<b>34</b>
1.3	说明 .....	1	6.4	Other Subsystems.....	<b>38</b>
1.4	功能框图 .....	2	<b>7</b>	<b>Applications, Implementation, and Layout</b> .....	<b>40</b>
<b>2</b>	<b>修订历史记录</b> .....	<b>4</b>	7.1	Application Information .....	<b>40</b>
<b>3</b>	<b>Device Comparison</b> .....	<b>6</b>	7.2	Short-, Medium-, and Long-Range Radar .....	<b>40</b>
3.1	Related Products .....	7	7.3	Imaging Radar using Cascade Configuration .....	<b>41</b>
<b>4</b>	<b>Terminal Configuration and Functions</b> .....	<b>8</b>	7.4	Reference Schematic .....	<b>41</b>
4.1	Pin Diagram .....	8	7.5	Layout .....	<b>43</b>
4.2	Signal Descriptions.....	12	<b>8</b>	<b>Device and Documentation Support</b> .....	<b>48</b>
<b>5</b>	<b>Specifications</b> .....	<b>16</b>	8.1	Device Nomenclature .....	<b>48</b>
5.1	Absolute Maximum Ratings .....	16	8.2	Tools and Software .....	<b>49</b>
5.2	ESD Ratings .....	16	8.3	Documentation Support .....	<b>49</b>
5.3	Power-On Hours (POH).....	16	8.4	Community Resources .....	<b>50</b>
5.4	Recommended Operating Conditions.....	17	8.5	商标.....	<b>50</b>
5.5	Power Supply Specifications .....	17	8.6	静电放电警告 .....	<b>50</b>
5.6	Power Consumption Summary.....	18	8.7	Export Control Notice .....	<b>50</b>
5.7	RF Specification.....	19	8.8	Glossary .....	<b>50</b>
5.8	Thermal Resistance Characteristics for FCBGA Package [ABL0161] .....	20	<b>9</b>	<b>Mechanical, Packaging, and Orderable Information</b> .....	<b>51</b>
5.9	Timing and Switching Characteristics .....	21	9.1	Packaging Information .....	<b>51</b>
<b>6</b>	<b>Detailed Description</b> .....	<b>33</b>			

## 2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from May 1, 2017 to October 31, 2018 (from * Revision (May 2017) to A Revision)	Page
• 将 RX 噪声系数从“15dB (76 至 77GHz)”更新成了“14dB (76 至 77GHz)”	<a href="#">1</a>
• 将 RX 噪声系数从“16dB (77 至 81GHz)”更新成了“15dB (77 至 81GHz)”	<a href="#">1</a>
• 将 1MHz 时的相位噪声从“-94dBc/Hz (76 至 77GHz)”更新成了“-95dBc/Hz (76 至 77GHz)”	<a href="#">1</a>
• 将 1MHz 时的相位噪声从“-91dBc/Hz (77 至 81GHz)”更新成了“-93dBc/Hz (77 至 81GHz)”	<a href="#">1</a>
• 将“特性”中的“符合 ASIL B 级要求”更新/更改成了“以 ASIL B 级为目标”	<a href="#">1</a>
• 删除了“具有内部振荡器的 40.0MHz 晶体”项目	<a href="#">1</a>
• 更新/更改了时钟源子项目	<a href="#">1</a>
• 在“应用”中添加了“使用级联配置的成像雷达”应用范围	<a href="#">1</a>
• 更新/更改了“适用于汽车 应用的雷达传感器”	<a href="#">1</a>
• 在“器件信息”中添加了新的可订购部件号	<a href="#">2</a>
• 更新了功能方框图中的 RX 和 TX 连接	<a href="#">2</a>
• 更新/更改了功能框图	<a href="#">2</a>
• Added AWR1243P to Device Features Comparison	<a href="#">6</a>
• Updated/Changed Device Features Comparison ASIL for AWR1243P, AWR1243, and AWR1642 from "B-Capable" to "B-Targeted"	<a href="#">6</a>
• Added "Max complex sampling rate (MSPS)" to Device Features Comparison	<a href="#">6</a>
• Changed AWR1243 and AWR1443 Product status from AI to PD	<a href="#">6</a>
• Corrected A10 pin to "VOUT_14APLL"	<a href="#">9</a>
• Added DEFAULT PULL STATUS column to Signal Descriptions	<a href="#">12</a>
• Added footnote to Chip-to-chip cascading synchronization signals	<a href="#">12</a>
• Combined FM_CW_CLKOUT and FM_CW_SYNCOUT Descriptions	<a href="#">12</a>
• Added text to SYNC_IN Description in Signal Descriptions table	<a href="#">12</a>
• Added footnote to WARM_RESET	<a href="#">13</a>
• Updated/Changed CLKP and CLKM descriptions in <i>Signal Descriptions</i>	<a href="#">13</a>
• Changed HBM ESD value from $\pm 1000$ V to $\pm 2000$ V and CDM ESD value from $\pm 250$ V to $\pm 500$ V	<a href="#">16</a>
• Added footnote to $V_{(ESD)}$	<a href="#">16</a>
• Completely updated Recommended Operating Conditions	<a href="#">17</a>
• Updated Power Supply Rails Characteristics footnote	<a href="#">17</a>
• Added footnote to Power Supply Rails Characteristics	<a href="#">17</a>
• Completely updated Ripple Specifications table	<a href="#">18</a>
• Added footnote to Maximum Current Ratings at Power Terminals	<a href="#">18</a>
• Updated footnote to Maximum Current Ratings at Power Terminals	<a href="#">18</a>
• Updated Average Power Consumption at Power Terminals	<a href="#">18</a>
• Updated 76 to 77 GHz Noise Figure in RF Specification from "15 dB" to "14 dB"	<a href="#">19</a>
• Updated 76 to 77 GHz Noise Figure in RF Specification from "16 dB" to "15 dB"	<a href="#">19</a>
• Added footnote to RF Specification	<a href="#">19</a>
• Changed 1-dB compression point from "-5 dBm" to "-8 dBm"	<a href="#">19</a>
• Updated RF Specification	<a href="#">19</a>
• Removed IQ gain mismatch from RF Specification	<a href="#">19</a>
• Added multiple row to RF Specification Receiver	<a href="#">19</a>
• Updated In-band and Out-of-band TYP value	<a href="#">19</a>
• Added FM_CW_CLKOUT, FM_CW_SYNCOUT, FM_CW_SYNCIN1, and FM_CW_SYNCIN2 to RF Specification	<a href="#">19</a>
• Modified all values for 20 GHz SYNC IN signal (FM_CW_SYNCIN)	<a href="#">19</a>
• Updated footnote in RF Specification	<a href="#">20</a>
• Removed 1v4 signal from Device Wakeup	<a href="#">21</a>
• Updated Device Wake-up Sequence	<a href="#">21</a>
• Updated Synchronized Frame Triggering text	<a href="#">21</a>
• Added text to Synchronized Frame Triggering	<a href="#">22</a>
• Added Synchronized Frame Triggering subsection	<a href="#">22</a>
• Removed $T_{Lag}$ from Frame Trigger Timing table	<a href="#">22</a>
• Updated/Changed Crystal Implementation	<a href="#">23</a>
• Updated Crystal Implementation note	<a href="#">23</a>
• Updated/Changed $f_p$ Parallel resonance crystal frequency from "40, 50" to "40"	<a href="#">23</a>
• Updated/Changed Frequency tolerance from "-50 and 50" to "-200 to 200"	<a href="#">23</a>

• Added <i>External Clock Electrical Characteristics</i> .....	<a href="#">24</a>
• Added External Clock Mode Specifications .....	<a href="#">24</a>
• Completely updated External Clock Mode Specifications .....	<a href="#">24</a>
• Updated External Clock Mode Specifications Frequency from "40, 50 MHz" to "40 MHz" .....	<a href="#">24</a>
• Updated/Changed SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output) .....	<a href="#">25</a>
• Updated/Changed SPI Slave Mode Timing Requirements (SPICLK = input, SPISIMO = input, and SPISOMI = output) .....	<a href="#">26</a>
• Added LVDS Interface Configuration .....	<a href="#">28</a>
• Updated LVDS Interface Lane Config image .....	<a href="#">28</a>
• Updated Timing Parameters .....	<a href="#">28</a>
• Updated LVDS Electrical Characteristics .....	<a href="#">29</a>
• Updated Camera Serial Interface (CSI) .....	<a href="#">31</a>
• Removed $T_{\text{CLK-SETTLE}}$ and $T_{\text{HS-SETTLE}}$ .....	<a href="#">31</a>
• Updated/Changed <i>Clock Subsystem</i> diagram .....	<a href="#">35</a>
• Added AWR1243P information to Transmit Subsystem text. ....	<a href="#">36</a>
• Updated/Changed Transmit Subsystem (Per Channel) .....	<a href="#">36</a>
• Updated/Changed Recieve Subsystem text from "...cutoff frequencies above 350 kHz..." to "...cutoff frequencies above 175 kHz..." .....	<a href="#">36</a>
• Updated Host Interface text .....	<a href="#">38</a>
• Updated text in "A2D Data Format Over CSI2 Interface" .....	<a href="#">38</a>
• Added Imaging Radar using Cascade Configuration .....	<a href="#">41</a>
• Removed Low-Noise LDO Circuitry image .....	<a href="#">41</a>
• Updated Device Nomenclature .....	<a href="#">49</a>

### 3 Device Comparison

**Table 3-1. Device Features Comparison**

FUNCTION	AWR1243P	AWR1243	AWR1443	AWR1642
Number of receivers	4	4	4	4
Number of transmitters	3 <sup>(1)</sup>	3	3	2
On-chip memory	—	—	576KB	1.5MB
ASIL	B-Targeted	B-Targeted	—	B-Targeted
Max I/F (Intermediate Frequency) (MHz)	15	15	5	5
Max real sampling rate (Msps)	37.5	37.5	12.5	12.5
Max complex sampling rate (Msps)	18.75	18.75	6.25	6.25
Processor				
MCU (R4F)	—	—	Yes	Yes
DSP (C674x)	—	—	—	Yes
Peripherals				
Serial Peripheral Interface (SPI) ports	1	1	1	2
Quad Serial Peripheral Interface (QSPI)	—	—	Yes	Yes
Inter-Integrated Circuit (I <sup>2</sup> C) interface	—	—	1	1
Controller Area Network (DCAN) interface	—	—	Yes	Yes
CAN FD	—	—	—	Yes
Trace	—	—	—	Yes
PWM	—	—	—	Yes
Hardware In Loop (HIL/DMM)	—	—	—	Yes
GPADC	—	—	Yes	Yes
LVDS/Debug	Yes	Yes	Yes	Yes
CSI2	Yes	Yes	—	—
Hardware accelerator	—	—	Yes	—
1-V bypass mode	Yes	Yes	Yes	Yes
Cascade (20-GHz sync)	Yes	—	—	—
JTAG	—	—	Yes	Yes
Number of Tx that can be simultaneously used	3	2	2	2
Per chirp configurable Tx phase shifter	Yes	—	—	—
Product status <sup>(2)</sup>	PRODUCT PREVIEW (PP), ADVANCE INFORMATION (AI), or PRODUCTION DATA (PD)	AI	PD	PD

- (1) 3 Tx Simultaneous operation is supported only in AWR1243P with 1V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin.
- (2) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

### 3.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

**mmWave Sensors** TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for automotive applications.

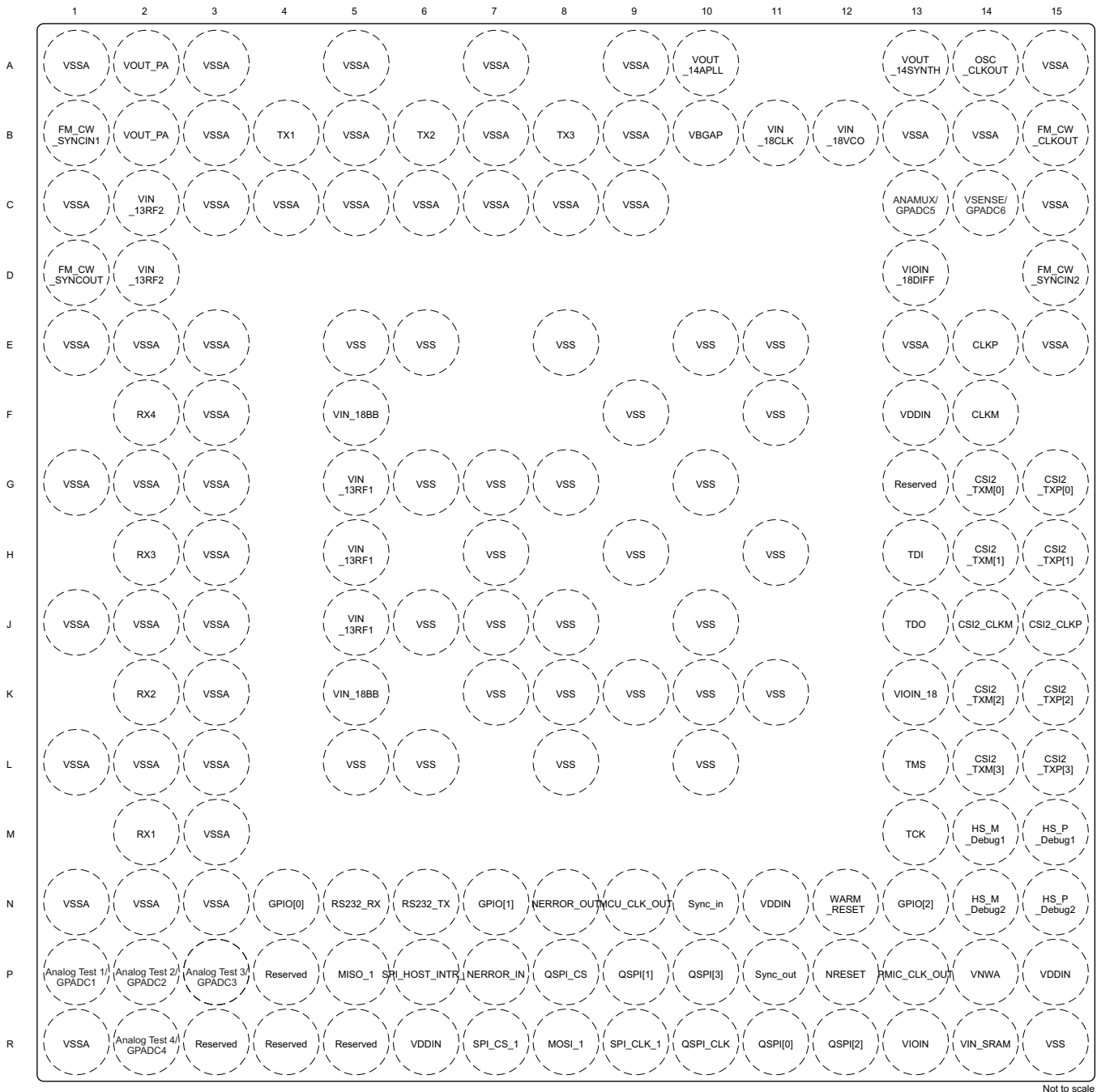
**Automotive mmWave Sensors** TI's automotive mmWave sensor portfolio offers high-performance radar front end to ultra-high resolution, small and low-power single-chip radar solutions. TI's scalable sensor portfolio enables design and development of ADAS system solution for every performance, application and sensor configuration ranging from comfort functions to safety functions in all vehicles.

**Companion Products for AWR1243** Review products that are frequently purchased or used in conjunction with this product.

## 4 Terminal Configuration and Functions

### 4.1 Pin Diagram

Figure 4-1 shows the pin locations for the 161-pin FCBGA package. Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5 show the same pins, but split into four quadrants.



Not to scale

Figure 4-1. Pin Diagram



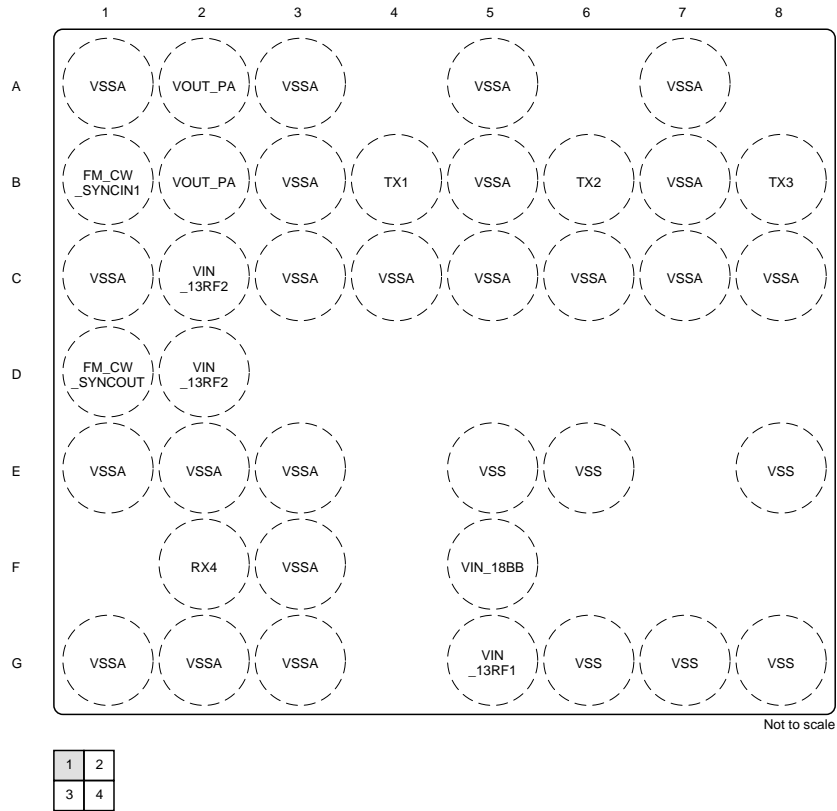


Figure 4-2. Top Left Quadrant

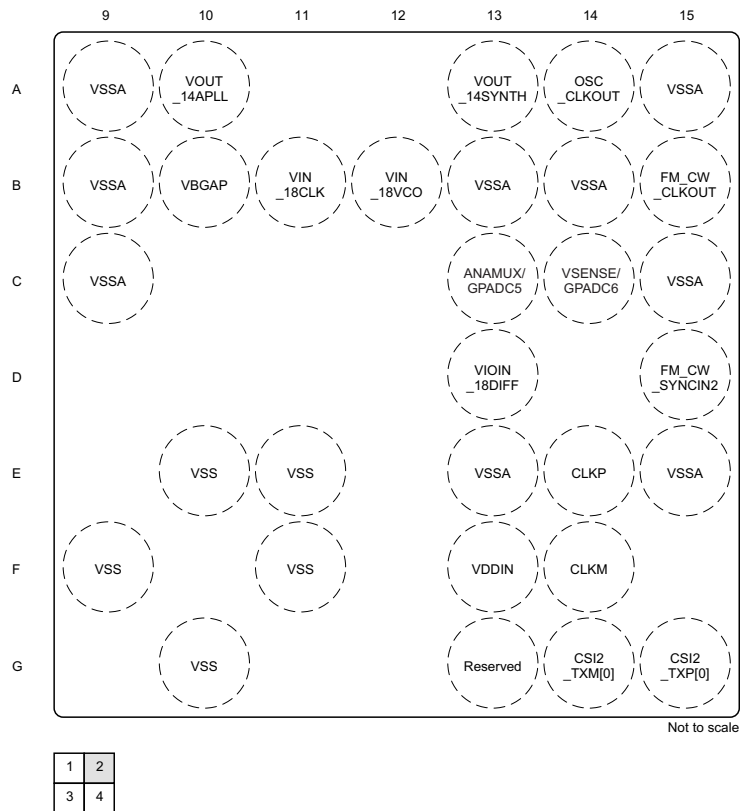
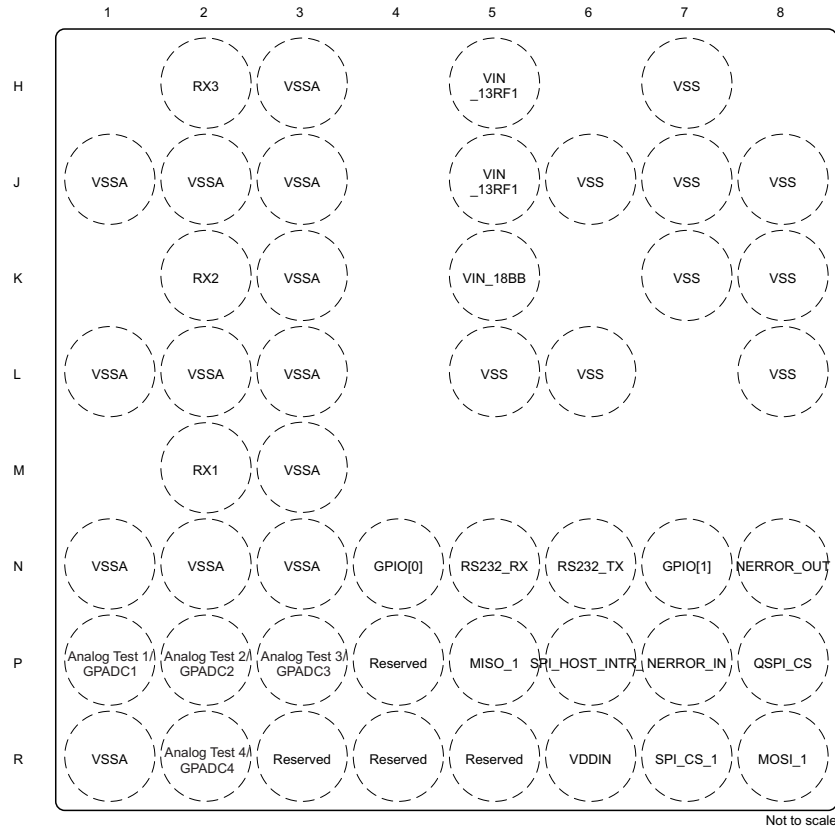
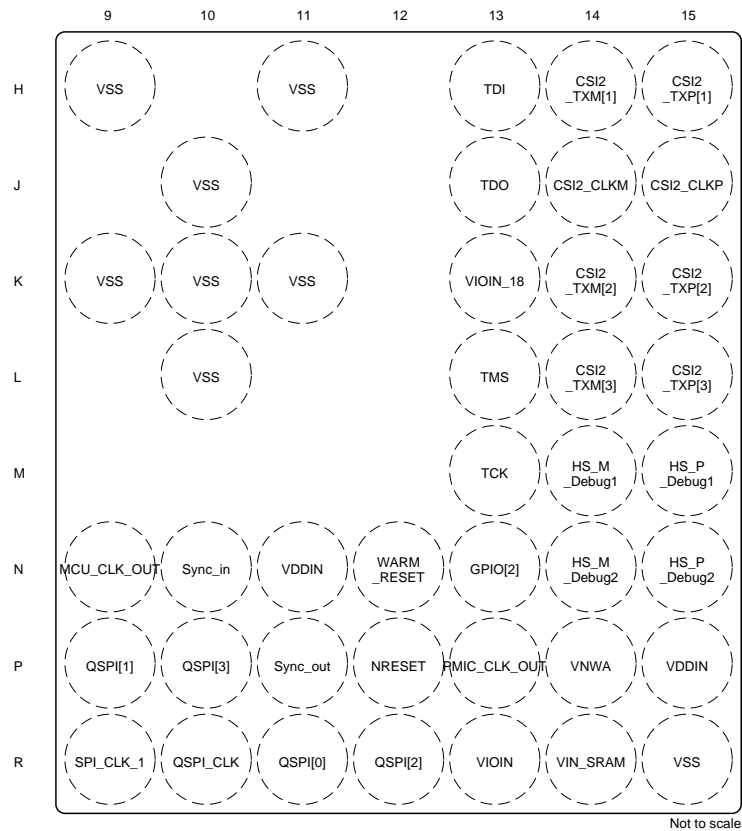


Figure 4-3. Top Right Quadrant



1	2
3	4

**Figure 4-4. Bottom Left Quadrant**



Not to scale

1	2
3	4

Figure 4-5. Bottom Right Quadrant

## 4.2 Signal Descriptions

Table 4-1 lists the pins by function and describes that function.

**Table 4-1. Signal Descriptions**

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
Transmitters	TX1	B4	O	—	Single-ended transmitter1 o/p
	TX2	B6	O	—	Single-ended transmitter2 o/p
	TX3	B8	O	—	Single-ended transmitter3 o/p
Receivers	RX1	M2	I	—	Single-ended receiver1 i/p
	RX2	K2	I	—	Single-ended receiver2 i/p
	RX3	H2	I	—	Single-ended receiver3 i/p
	RX4	F2	I	—	Single-ended receiver4 i/p
CSI2 TX	CSI2_TXP[0]	G15	O	—	Differential data Out – Lane 0
	CSI2_TXM[0]	G14	O	—	
	CSI2_CLKP	J15	O	—	Differential clock Out
	CSI2_CLKM	J14	O	—	
	CSI2_TXP[1]	H15	O	—	Differential data Out – Lane 1
	CSI2_TXM[1]	H14	O	—	
	CSI2_TXP[2]	K15	O	—	Differential data Out – Lane 2
	CSI2_TXM[2]	K14	O	—	
	CSI2_TXP[3]	L15	O	—	Differential data Out – Lane 3
	CSI2_TXM[3]	L14	O	—	
	HS_DEBUG1_P	M15	O	—	Differential debug port 1
	HS_DEBUG1_M	M14	O	—	
	HS_DEBUG2_P	N15	O	—	Differential debug port 2
HS_DEBUG2_M	N14	O	—		
Chip-to-chip cascading synchronization signals <sup>(2)</sup>	FM_CW_CLKOUT	B15	O	—	20-GHz single-ended output. Modulated waveform
	FM_CW_SYNCOOUT	D1			
	FM_CW_SYNCIN1	B1	I	—	
	FM_CW_SYNCIN2	D15			
Reference clock	OSC_CLKOUT	A14	O	—	Reference clock output from clocking subsystem after cleanup PLL. Can be used by slave chip in multichip cascading
System synchronization	SYNC_OUT	P11	O	Pull Down	Low-frequency frame synchronization signal output. Can be used by slave chip in multichip cascading
	SYNC_IN	N10	I	Pull Down	Low-frequency frame synchronization signal input. This signal could also be used as a hardware trigger for frame start
SPI control interface from external MCU (default slave mode)	SPI_CS_1	R7	I	Pull Up	SPI chip select
	SPI_CLK_1	R9	I	Pull Down	SPI clock
	MOSI_1	R8	I	Pull Up	SPI data input
	MISO_1	P5	O	Pull Up	SPI data output
	SPI_HOST_INTR_1	P6	O	Pull Down	SPI interrupt to host
	RESERVED	R3, R4, R5, P4		—	

(1) Status of PULL structures associated with the IO after device POWER UP.

(2) Cascading feature is available only in the AWR1243P variant.

**Table 4-1. Signal Descriptions (continued)**

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
Reset	NRESET	P12	I	Open Drain	Power on reset for chip. Active low
	WARM_RESET <sup>(3)</sup>	N12	IO	Open Drain	Open-drain fail-safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.
Safety	NERROR_OUT	N8	O	Open Drain	Open-drain fail-safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.
	NERROR_IN	P7	I	Open Drain	Fail-safe input to the device. Error output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by firmware
JTAG	TMS	L13	I	Pull Up	JTAG port for TI internal development
	TCK	M13	I	Pull Down	
	TDI	H13	I	Pull Up	
	TDO	J13	O	—	
Reference oscillator	CLKP	E14	I	—	In XTAL mode: Differential port for reference crystal In External clock mode: Single ended input reference clock port (Output CLKM is grounded in this case)
	CLKM	F14	O	—	
Band-gap voltage	VBGAP	B10	O	—	

(3) For the AWR1243 WARM\_RESET can be used as an output only pin for status indication.

Table 4-1. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
Power supply	VDDIN	F13,N11,P15,R6	POW	—	1.2-V digital power supply
	VIN_SRAM	R14	POW	—	1.2-V power rail for internal SRAM
	VNWA	P14	POW	—	1.2-V power rail for SRAM array back bias
	VIOIN	R13	POW	—	I/O supply (3.3-V or 1.8-V): All CMOS I/Os would operate on this supply.
	VIOIN_18	K13	POW	—	1.8-V supply for CMOS IO
	VIN_18CLK	B11	POW	—	1.8-V supply for clock module
	VIOIN_18DIFF	D13	POW	—	1.8-V supply for CSI2 port
	Reserved	G13	POW	—	No connect
	VIN_13RF1	G5,J5,H5	POW	—	1.3-V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board
	VIN_13RF2	C2,D2	POW	—	
	VIN_18BB	K5,F5	POW	—	1.8-V Analog baseband power supply
	VIN_18VCO	B12	POW	—	1.8-V RF VCO supply
	VSS	E5,E6,E8,E10,E11,F9,F11,G6,G7,G8,G10,H7,H9,H11,J6,J7,J8,J10,K7,K8,K9,K10,K11,L5,L6,L8,L10,R15	GND	—	Digital ground
VSSA	A1,A3,A5,A7,A9,A15,B3,B5,B7,B9,B13,B14,C1,C3,C4,C5,C6,C7,C8,C9,C15,E1,E2,E3,E13,E15,F3,G1,G2,G3,H3,J1,J2,J3,K3,L1,L2,L3,M3,N1,N2,N3,R1	GND	—	Analog ground	
Internal LDO output/inputs	VOUT_14APLL	A10	O	—	
	VOUT_14SYNTH	A13	O	—	
	VOUT_PA	A2,B2	IO	—	When internal PA LDO is used this pin provides the output voltage of the LDO. When the internal PA LDO is bypassed and disabled 1V supply should be fed on this pin. This is mandatory in 3TX simultaneous use case.
External clock out	PMIC_CLK_OUT	P13	O	—	Dithered clock input to PMIC
	MCU_CLK_OUT	N9	O	—	Programmable clock given out to external MCU or the processor
General-purpose I/Os	GPIO[0]	N4	IO	Pull Down	General-purpose IO
	GPIO[1]	N7	IO	Pull Down	General-purpose IO
	GPIO[2]	N13	IO	Pull Down	General-purpose IO

**Table 4-1. Signal Descriptions (continued)**

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
QSPI for Serial Flash <sup>(4)</sup>	QSPI_CS	P8	O	Pull Up	Chip-select output from the device. Device is a master connected to serial flash slave.
	QSPI_CLK	R10	O	Pull Down	Clock output from the device. Device is a master connected to serial flash slave.
	QSPI[0]	R11	IO	Pull Down	Data IN/OUT
	QSPI[1]	P9	IO	Pull Down	Data IN/OUT
	QSPI[2]	R12	IO	Pull Up	Data IN/OUT
	QSPI[3]	P10	IO	Pull Up	Data IN/OUT
Flash programming and RS232 UART <sup>(4)</sup>	RS232_TX	N6	O	Pull Down	UART pins for programming external flash in preproduction/debug hardware.
	RS232_RX	N5	I	Pull Up	
Test and Debug output for preproduction phase. Can be pinned out on production hardware for field debug	Analog Test1 / GPADC1	P1	IO	—	GP ADC channel 1
	Analog Test2 / GPADC2	P2	IO	—	GP ADC channel 2
	Analog Test3 / GPADC3	P3	IO	—	GP ADC channel 3
	Analog Test4 / GPADC4	R2	IO	—	GP ADC channel 4
	ANAMUX / GPADC5	C13	IO	—	GP ADC channel 5
	VSENSE / GPADC6	C14	IO	—	GP ADC channel 6

(4) This option is for development/debug in preproduction phase. Can be disabled by firmware pin mux setting.

## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		MIN	MAX	UNIT
VDDIN	1.2 V digital power supply	-0.5	1.4	V
VIN_SRAM	1.2 V power rail for internal SRAM	-0.5	1.4	V
VNWA	1.2 V power rail for SRAM array back bias	-0.5	1.4	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	-0.5	3.8	V
VIOIN_18	1.8 V supply for CMOS IO	-0.5	2	V
VIN_18CLK	1.8 V supply for clock module	-0.5	2	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	-0.5	2	V
VIN_13RF1	1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board.	-0.5	1.45	V
VIN_13RF2				
VIN_13RF1	1-V Internal LDO bypass mode. Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	-0.5	1.4	V
VIN_13RF2				
VIN_18BB	1.8-V Analog baseband power supply	-0.5	2	V
VIN_18VCO supply	1.8-V RF VCO supply	-0.5	2	V
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	-0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input	VIOIN + 20% up to 20% of signal period		
CLKP, CLKM	Input ports for reference crystal	-0.5	2	V
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	-20	20	mA
T <sub>J</sub>	Operating junction temperature range	-40	125	°C
T <sub>STG</sub>	Storage temperature range after soldered onto PC board	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V<sub>SS</sub>, unless otherwise noted.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011 <sup>(2)</sup>	±500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) Corner pins are rated as ±750 V

### 5.3 Power-On Hours (POH)<sup>(1)</sup>

JUNCTION TEMPERATURE (T <sub>J</sub> )	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
-40°C	100% duty cycle	1.2	600 (6%)
75°C			2000 (20%)
95°C			6500 (65%)
125°C			900 (9%)

- (1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.



## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIN	1.2 V digital power supply	1.14	1.2	1.32	V
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	3.15	3.3	3.45	V
		1.71	1.8	1.89	
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.9	V
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	1.71	1.8	1.9	V
VIN_13RF1	1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board	1.23	1.3	1.36	V
VIN_13RF2					
VIN_13RF1 (1-V Internal LDO bypass mode)		0.95	1	1.05	V
VIN_13RF2 (1-V Internal LDO bypass mode)					
VIN18BB	1.8-V Analog baseband power supply	1.71	1.8	1.9	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.9	V
V <sub>IH</sub>	Voltage Input High (1.8 V mode)	1.17			V
	Voltage Input High (3.3 V mode)	2.25			
V <sub>IL</sub>	Voltage Input Low (1.8 V mode)			0.3*VIOIN	V
	Voltage Input Low (3.3 V mode)			0.62	
V <sub>OH</sub>	High-level output threshold (I <sub>OH</sub> = 6 mA)	VIOIN – 450			mV
V <sub>OL</sub>	Low-level output threshold (I <sub>OL</sub> = 6 mA)				450
NRESET SOP[2:0]	V <sub>IL</sub> (1.8V Mode)			0.2	V
	V <sub>IH</sub> (1.8V Mode)	0.96			
	V <sub>IL</sub> (3.3V Mode)			0.3	
	V <sub>IH</sub> (3.3V Mode)	1.57			

## 5.5 Power Supply Specifications

Table 5-1 describes the four rails from an external power supply block of the AWR1243 device.

**Table 5-1. Power Supply Rails Characteristics**

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, CSI2	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.3 V (or 1 V in internal LDO bypass mode) <sup>(1)</sup>	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM

(1) Three simultaneous transmitter operation is supported only in 1-V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin.

The 1.3V (1.0V) and 1.8V power supply ripple specifications mentioned in [Table 5-2](#) are defined to meet a target spur level of  $-105\text{dBc}$  (RF Pin =  $-15\text{dBm}$ ) at the RX. The spur and ripple levels have a dB to dB relationship, for example, a 1dB increase in supply ripple leads to a  $\sim 1\text{dB}$  increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

**Table 5-2. Ripple Specifications**

FREQUENCY (kHz)	RF RAIL		VCO/IF RAIL
	1.0 V (INTERNAL LDO BYPASS) ( $\mu\text{V}_{\text{RMS}}$ )	1.3 V ( $\mu\text{V}_{\text{RMS}}$ )	1.8 V ( $\mu\text{V}_{\text{RMS}}$ )
137.5	744	648	83
275	4	76	21
550	3	22	11
1100	2	4	6
2200	11	82	13
4400	13	93	19
6600	22	117	29

## 5.6 Power Consumption Summary

[Table 5-3](#) and [Table 5-4](#) summarize the power consumption at the power terminals.

**Table 5-3. Maximum Current Ratings at Power Terminals**

PARAMETER	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
Current consumption	VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			500	mA
	VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3V (or 1V in LDO Bypass mode) rail when only 2 transmitters are used <sup>(1)</sup>			2000	
	VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8V rail			850	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail			50	

(1) 3 Transmitters can simultaneously be deployed only in AWR1243P device with 1V / LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin. In this case the peak 1V supply current goes up to 2500 mA.

**Table 5-4. Average Power Consumption at Power Terminals**

PARAMETER	CONDITION		DESCRIPTION	MIN	TYP	MAX	UNIT
Average power consumption	1.0-V internal LDO bypass mode	1TX, 4RX	Sampling: 16.66 MSps complex Transceiver, 40-ms frame time, 512 chirps, 512 samples/chirp, 8.5- $\mu\text{s}$ interchirp time (50% duty cycle) Data Port: MIPI-CSI-2		1.62		W
		2TX, 4RX			1.79		
		3TX, 4RX			1.98		
	1.3-V internal LDO enabled mode	1TX, 4RX			1.8		
		2TX, 4RX			2.01		

## 5.7 RF Specification

over recommended operating conditions and with run time calibrations enabled(unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT	
Receiver	Noise figure	76 to 77 GHz	14		dB	
		77 to 81 GHz	15			
	1-dB compression point (Out Of Band) <sup>(1)</sup>			-8		dBm
	Maximum gain			48		dB
	Gain range			24		dB
	Gain step size			2		dB
	Image Rejection Ratio (IMRR)			30		dB
	IF bandwidth <sup>(2)</sup>				15	MHz
	A2D sampling rate (real)				37.5	Msp/s
	A2D sampling rate (complex)				18.75	Msp/s
	A2D resolution			12		Bits
	Return loss (S11)			<-10		dB
	Gain mismatch variation (over temperature)			±0.5		dB
	Phase mismatch variation (over temperature)			±3		°
		In-band IIP2	RX gain = 30dB IF = 1.5, 2 MHz at -12 dBFS		16	dBm
RX gain = 24dB IF = 10 kHz at -10dBm, 1.9 MHz at -30 dBm			24	dBm		
Idle Channel Spurs			-90		dBFS	
Transmitter	Output power			12	dBm	
	Amplitude noise			-145	dBc/Hz	
Clock subsystem	Frequency range		76		81 GHz	
	Ramp rate				100 MHz/μs	
	Phase noise at 1-MHz offset	76 to 77 GHz		-95		dBc/Hz
77 to 81 GHz			-93			
20 GHz SYNC OUT signal (FM_CW_CL KOUT and FM_CW_SY NCOOUT) <sup>(3)</sup>	Frequency range		19		20.25 GHz	
	Output Power			7	dBm	
	Return loss			-10	dB	
	Impedance			50	Ω	
20 GHz SYNC IN signal (FM_CW_SY NCIN) <sup>(4)(3)</sup>	Frequency range		19		20.25 GHz	
	Input Power			1	dBm	
	Return loss			-10	dB	
	Impedance			50	Ω	

(1) 1-dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone below the lowest HPF cut-off frequency (50 kHz).

(2) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)

HPF1	HPF2
175, 235, 350, 700	350, 700, 1400, 2800

The filtering performed by the digital baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

(3) Cascading feature is available only in AWR1243P variant.

(4) Below +3dBm, there may be SNR degradation. Below -10dBm, there may be TX power level drop.

Figure 5-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

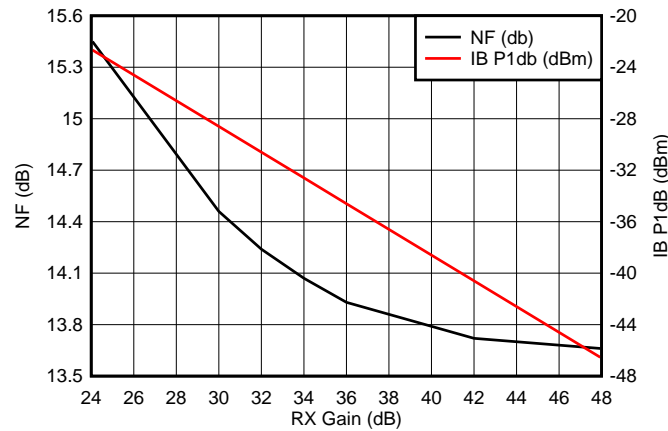


Figure 5-1. Noise Figure, In-band P1dB vs Receiver Gain

## 5.8 Thermal Resistance Characteristics for FCBGA Package [ABL0161]<sup>(1)</sup>

THERMAL METRICS <sup>(2)</sup>		°C/W <sup>(3) (4)</sup>
R $\theta_{JC}$	Junction-to-case	4.92
R $\theta_{JB}$	Junction-to-board	6.57
R $\theta_{JA}$	Junction-to-free air	22.3
R $\theta_{JMA}$	Junction-to-moving air	N/A <sup>(1)</sup>
Psi $_{JT}$	Junction-to-package top	4.92
Psi $_{JB}$	Junction-to-board	6.4

(1) N/A = not applicable

(2) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(3) °C/W = degrees Celsius per watt.

(4) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R $\theta_{JC}$ ] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

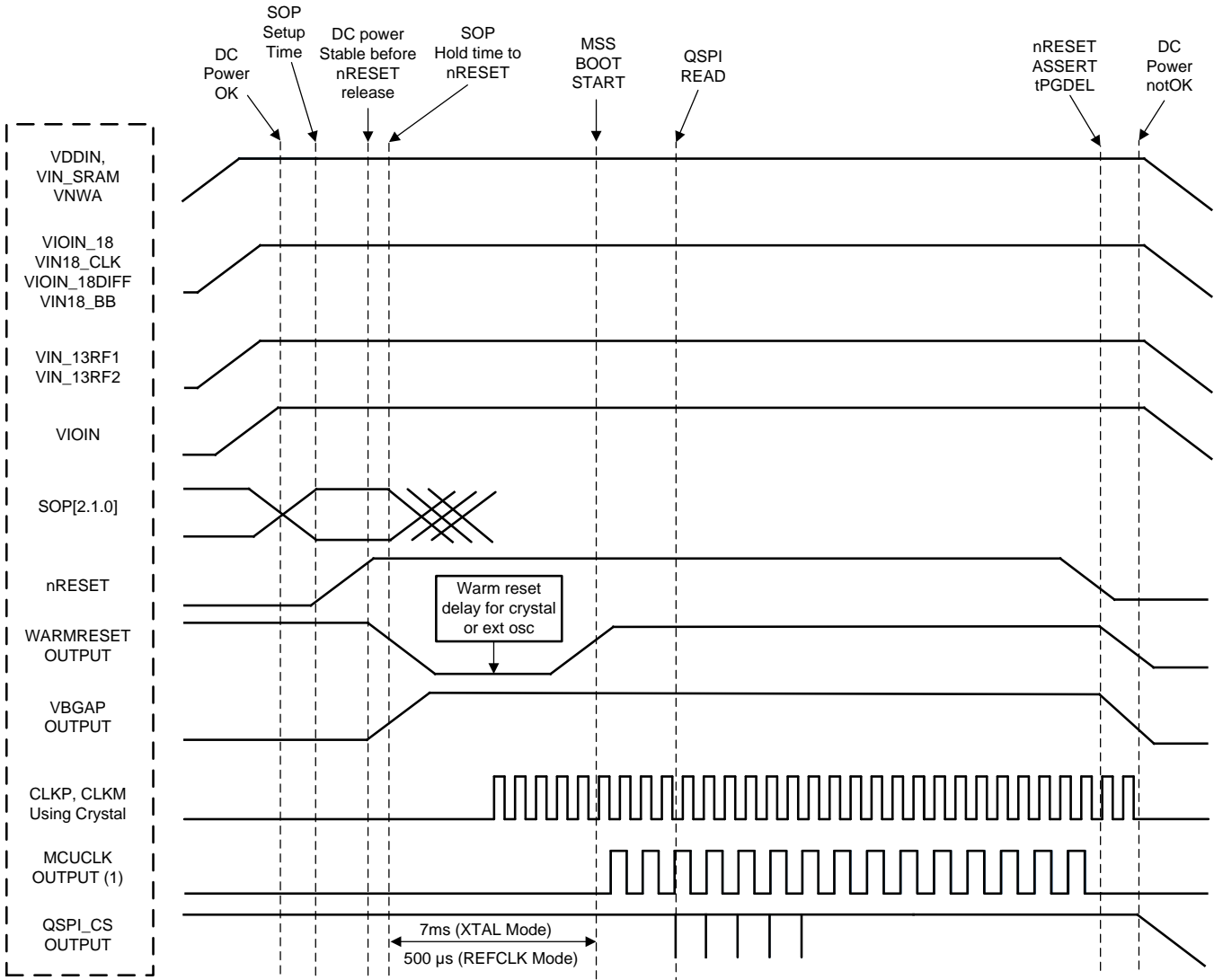
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

A junction temperature of 125°C is assumed.

## 5.9 Timing and Switching Characteristics

### 5.9.1 Power Supply Sequencing and Reset Timing

The AWR1243 device expects all external voltage rails and SOP lines to be stable before reset is deasserted. Figure 5-2 describes the device wake-up sequence.



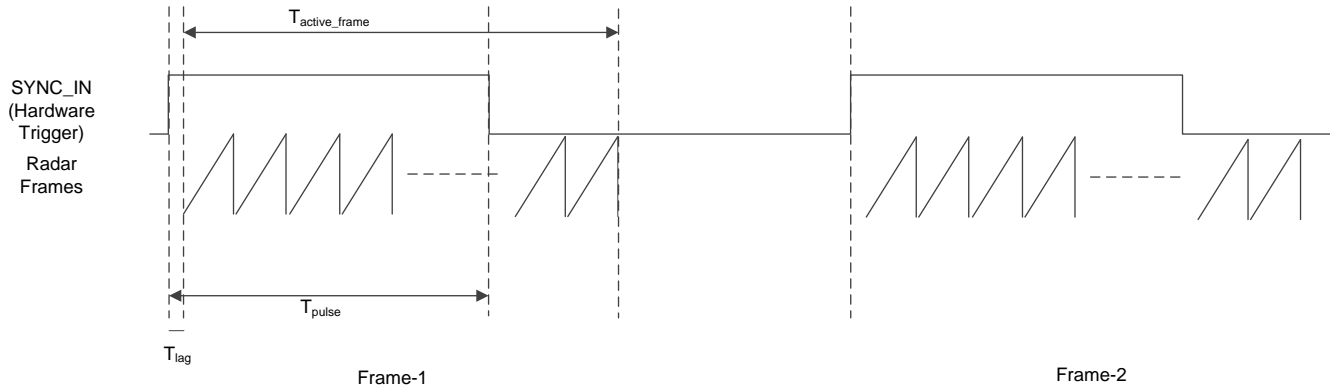
- (1) MCU\_CLK\_OUT in autonomous mode, where AWR1243 application is booted from the serial flash, MCU\_CLK\_OUT is not enabled by default by the device bootloader.

Figure 5-2. Device Wake-up Sequence

### 5.9.2 Synchronized Frame Triggering

The AWR1243 device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC\_IN signal to start radar frames. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.

The periodicity of the external SYNC\_IN pulse should be always greater than the programmed frame periodic in the frame configurations in all instances.



**Figure 5-3. Sync In Hardware Trigger**

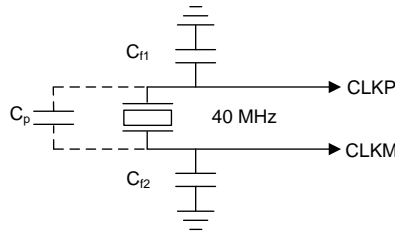
**Table 5-5. Frame Trigger Timing**

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$T_{active\_frame}$	Active frame duration	User defined		ns
$T_{pulse}$		25	$< T_{active\_frame}$	

### 5.9.3 Input Clocks and Oscillators

#### 5.9.3.1 Clock Specifications

An external crystal is connected to the device pins. [Figure 5-4](#) shows the crystal implementation.



**Figure 5-4. Crystal Implementation**

#### NOTE

The load capacitors, C<sub>f1</sub> and C<sub>f2</sub> in [Figure 5-4](#), should be chosen such that [Equation 1](#) is satisfied. C<sub>L</sub> in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins. Note that C<sub>f1</sub> and C<sub>f2</sub> include the parasitic capacitances due to PCB routing.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

[Table 5-6](#) lists the electrical characteristics of the clock crystal.

**Table 5-6. Crystal Electrical Characteristics (Oscillator Mode)**

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f <sub>P</sub>	Parallel resonance crystal frequency		40		MHz
C <sub>L</sub>	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	-40		150	°C
Frequency tolerance	Crystal frequency tolerance <sup>(1)(2)</sup>	-200		200	ppm
Drive level			50	200	μW

(1) The crystal manufacturer's specification must satisfy this requirement.

(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40-MHz clock is fed externally. [Table 5-7](#) lists the electrical characteristics of the external clock signal.

**Table 5-7. External Clock Mode Specifications**

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC- coupled square wave Phase Noise referred to 40 MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	DC- $t_{\text{rise/fall}}$			10	ns
	Phase Noise at 1 kHz			-132	dBc/Hz
	Phase Noise at 10 kHz			-143	dBc/Hz
	Phase Noise at 100 kHz			-152	dBc/Hz
	Phase Noise at 1 MHz			-153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	-50		50	ppm



## 5.9.4 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

### 5.9.4.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Table 5-9 and Table 5-10 assume the operating conditions stated in Table 5-8. Table 5-9, Table 5-10, and Figure 5-5 describe the timing and switching characteristics of the MibSPI.

**Table 5-8. SPI Timing Conditions**

		MIN	TYP	MAX	UNIT
Input Conditions					
$t_R$	Input rise time	1		3	ns
$t_F$	Input fall time	1		3	ns
Output Conditions					
$C_{LOAD}$	Output load capacitance	2		15	pF

**Table 5-9. SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)<sup>(1)(2)(3)</sup>**

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK <sup>(4)</sup>	25			ns
2 <sup>(5)</sup>	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	10			ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	10			
3 <sup>(5)</sup>	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	10			ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	10			
4 <sup>(5)</sup>	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)			10	
5 <sup>(5)</sup>	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	2			
4 <sup>(5)</sup>	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)			10	
5 <sup>(5)</sup>	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	2			

(1) The MASTER bit (SPIGCRx.0) is cleared ( where x = 0 or 1 ).

(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.

(3)  $t_{c(MSS\_VCLK)}$  = master subsystem clock time =  $1 / f_{(MSS\_VCLK)}$ . For more details, see the [Technical Reference Manual](#).

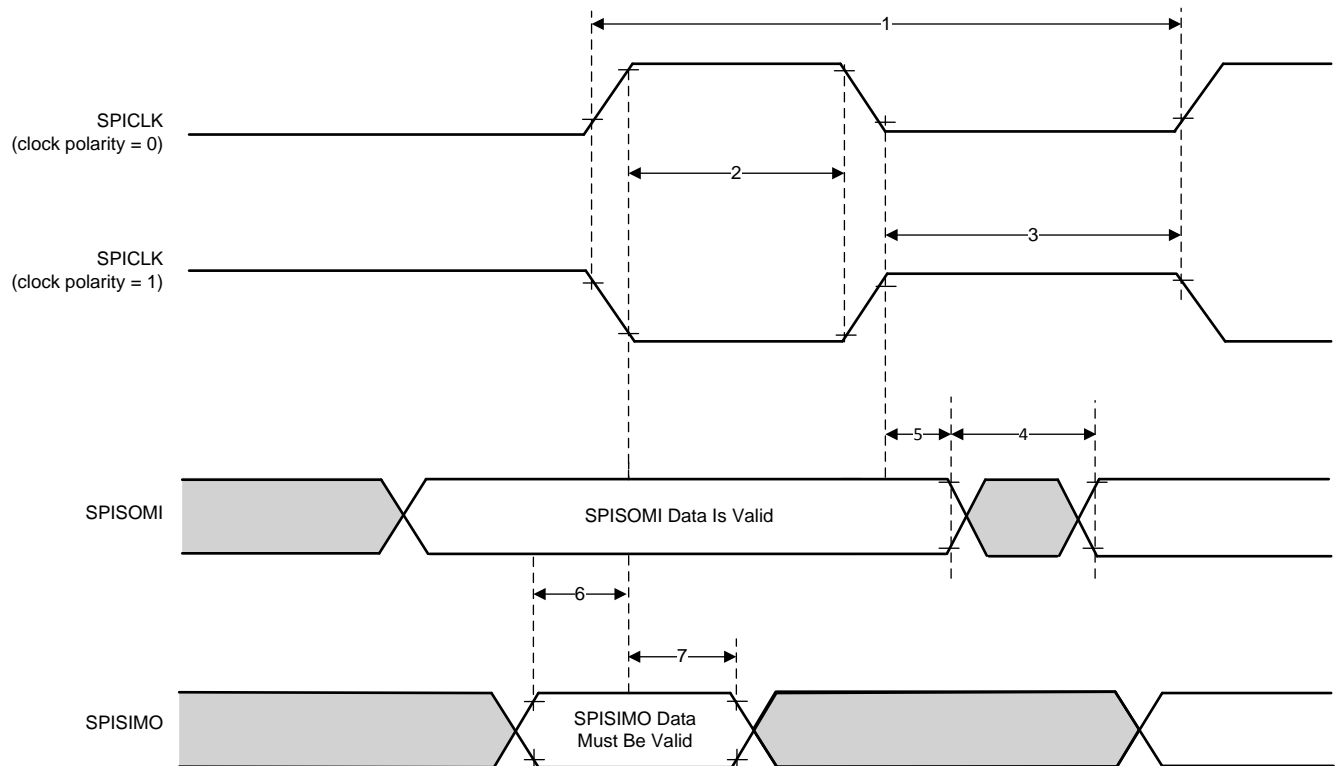
(4) When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255:  $t_{c(SPC)S} \geq (PS + 1)t_{c(MSS\_VCLK)} \geq 25$  ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0:  $t_{c(SPC)S} = 2t_{c(MSS\_VCLK)} \geq 25$  ns.

(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

**Table 5-10. SPI Slave Mode Timing Requirements (SPICLK = input, SPISIMO = input, and SPISOMI = output)**

NO.		MIN	TYP	MAX	UNIT
6 <sup>(1)</sup>	$t_{su}(SIMO-SPCL)S$ Setup time, SPISIMO before SPICLK low (clock polarity = 0)	3			ns
	$t_{su}(SIMO-SPCH)S$ Setup time, SPISIMO before SPICLK high (clock polarity = 1)	3			
7 <sup>(1)</sup>	$t_h(SPCL-SIMO)S$ Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	0			ns
	$t_h(SPCL-SIMO)S$ Hold time, SPISIMO data valid after SPICLK low (clock polarity = 1)	0			
6 <sup>(1)</sup>	$t_{su}(SIMO-SPCL)S$ Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	3			ns
	$t_{su}(SIMO-SPCH)S$ Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	3			
7 <sup>(1)</sup>	$t_h(SPCL-SIMO)S$ Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	1			ns
	$t_h(SPCL-SIMO)S$ Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	1			

(1) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).



**Figure 5-5. SPI Slave Mode External Timing**

### 5.9.4.2 Typical Interface Protocol Diagram (Slave Mode)

1. Host should ensure that there is a delay of at least two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 5-6 shows the SPI communication timing of the typical interface protocol.

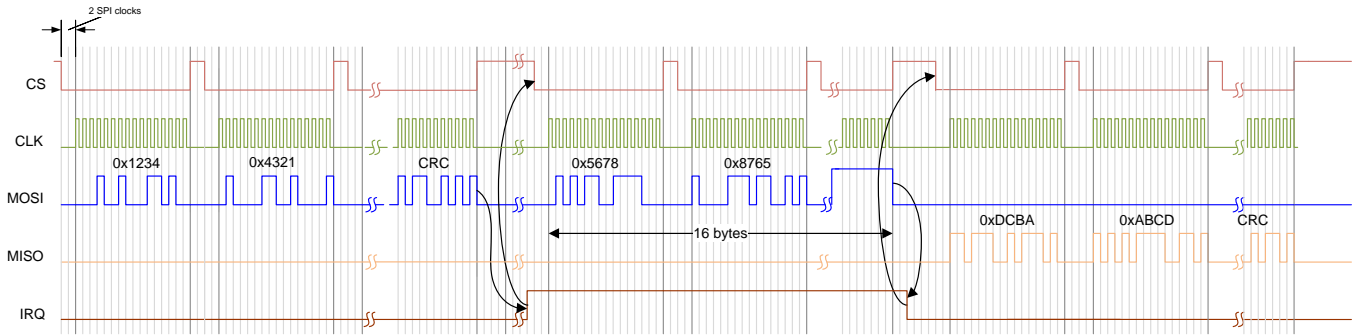


Figure 5-6. SPI Communication

### 5.9.5 LVDS Interface Configuration

The AWR1243 supports seven differential LVDS IOs/Lanes to support debug where raw ADC data could be extracted. The lane configuration supported is four Data lanes (LVDS\_TXP/M), one Bit Clock lane (LVDS\_CLKP/M) one Frame clock lane (LVDS\_FRCLKP/M). The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

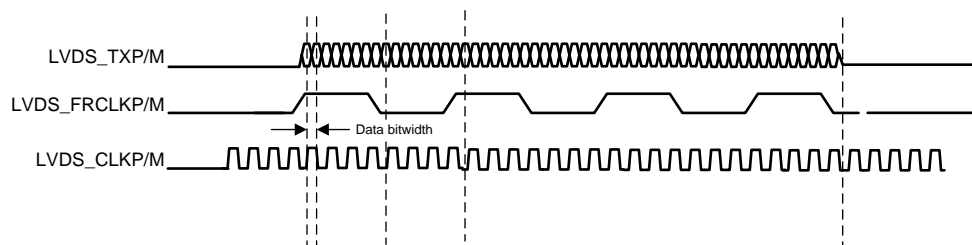


Figure 5-7. LVDS Interface Lane Configuration And Relative Timings

#### 5.9.5.1 LVDS Interface Timings

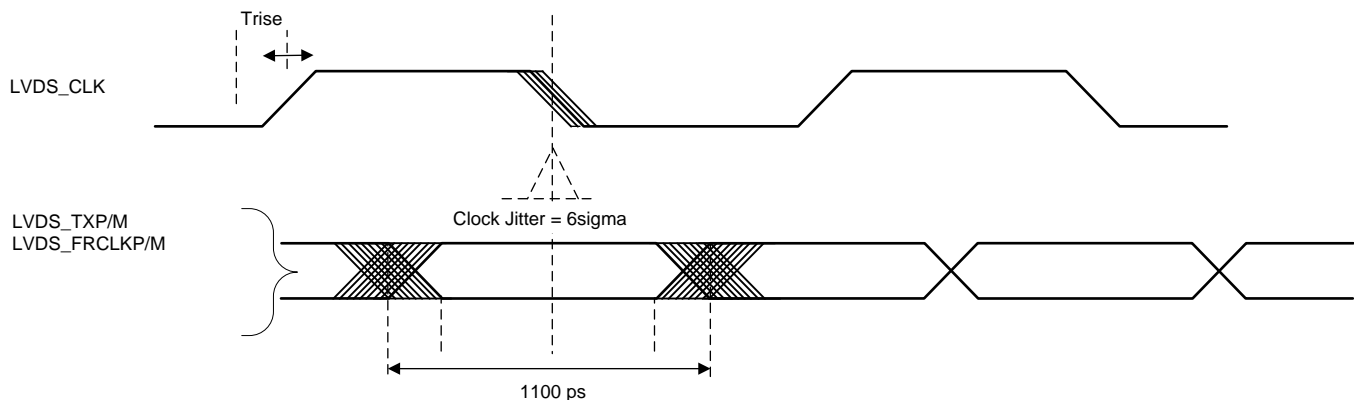


Figure 5-8. Timing Parameters

**Table 5-11. LVDS Electrical Characteristics**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 $\Omega$ resistive load between differential pairs	250		450	mV
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps		330		ps
Jitter (pk-pk)	900 Mbps		80		ps

## 5.9.6 General-Purpose Input/Output

Table 5-12 lists the switching characteristics of output timing relative to load capacitance.

**Table 5-12. Switching Characteristics for Output Timing versus Load Capacitance ( $C_L$ )<sup>(1)(2)</sup>**

PARAMETER		TEST CONDITIONS	VIOIN = 1.8V	VIOIN = 3.3V	UNIT	
$t_r$	Max rise time	Slew control = 0	$C_L = 20$ pF	2.8	3.0	ns
			$C_L = 50$ pF	6.4	6.9	
			$C_L = 75$ pF	9.4	10.2	
$t_f$	Max fall time		$C_L = 20$ pF	2.8	2.8	ns
			$C_L = 50$ pF	6.4	6.6	
			$C_L = 75$ pF	9.4	9.8	
$t_r$	Max rise time	Slew control = 1	$C_L = 20$ pF	3.3	3.3	ns
			$C_L = 50$ pF	6.7	7.2	
			$C_L = 75$ pF	9.6	10.5	
$t_f$	Max fall time		$C_L = 20$ pF	3.1	3.1	ns
			$C_L = 50$ pF	6.6	6.6	
			$C_L = 75$ pF	9.6	9.6	

(1) Slew control, which is configured by PADxx\_CFG\_REG, changes behavior of the output driver (faster or slower output slew rate).

(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

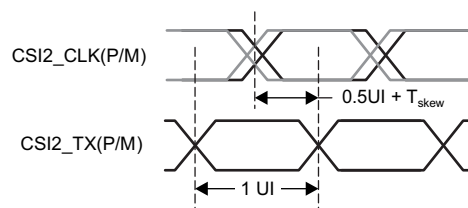
### 5.9.7 Camera Serial Interface (CSI)

The CSI is a MIPI D-PHY compliant interface for connecting this device to a camera receiver module. This interface is made of four differential lanes; each lane is configurable for carrying data or clock. The polarity of each wire of a lane is also configurable. Table 5-13, Figure 5-9, Figure 5-10, and Figure 5-11 describe the clock and data timing of the CSI. The clock is always ON once the CSI IP is enabled. Hence it remains in HS mode.

**Table 5-13. CSI Switching Characteristics**

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
HPTX						
HSTX <sub>DBR</sub>	Data bit rate	(1/2/4 data lane PHY)	150		600	Mbps
f <sub>CLK</sub>	DDR clock frequency	(1/2/4 data lane PHY)	75		300	MHz
ΔV <sub>CMTX(LF)</sub>	Common-level variation				50	mV
t <sub>R</sub> and t <sub>F</sub>	20% to 80% rise time and fall time				0.3	UI
LPTX DRIVER						
t <sub>EOT</sub>	Time from start of THS-TRAIL period to start of LP-11 state				105 + 12*UI	ns
DATA-CLOCK Timing Specification						
UINOM	Nominal Unit Interval		1.67		13.33	ns
UIINST,MIN	Minimum instantaneous Unit Interval		1.131			ns
TSKEW[TX]	Data to clock skew measured at transmitter		-0.15		0.15	UIINST, MIN
CSI2 TIMING SPECIFICATION						
T <sub>CLK-PRE</sub>	Time that the HS clock shall be driven by the transmitter before any associated data lane beginning the transition from LP to HS mode.		8			ns
T <sub>CLK-PREPARE</sub>	Time that the transmitter drives the clock lane LP-00 line state immediately before the HS-0 line state starting the HS transmission.		38		95	ns
T <sub>CLK-PREPARE</sub> + T <sub>CLK-ZERO</sub>	T <sub>CLK-PREPARE</sub> + time that the transmitter drives the HS-0 state before starting the clock.		300			ns
T <sub>EOT</sub>	Transmitted time interval from the start of T <sub>HS-TRAIL</sub> or T <sub>CLKTRAIL</sub> to the start of the LP-11 state following a HS burst.				105 ns + 12*UI	ns
T <sub>HS-PREPARE</sub>	Time that the transmitter drives the data lane LP-00 line state immediately before the HS-0 line state starting the HS transmission		40 + 4*UI		85 + 6*UI	ns
T <sub>HS-PREPARE</sub> + T <sub>HS-ZERO</sub>	T <sub>HS-PREPARE</sub> + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.		145 ns + 10*UI			ns
T <sub>HS-EXIT</sub>	Time that the transmitter drives LP-11 following a HS burst.		100			ns
T <sub>HS-TRAIL</sub>	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst		max(8*UI, 60 ns + 4*UI)			ns
T <sub>LPX</sub>	Transmitted length of any low-power state period		50			ns



**Figure 5-9. Clock and Data Timing in HS Transmission**

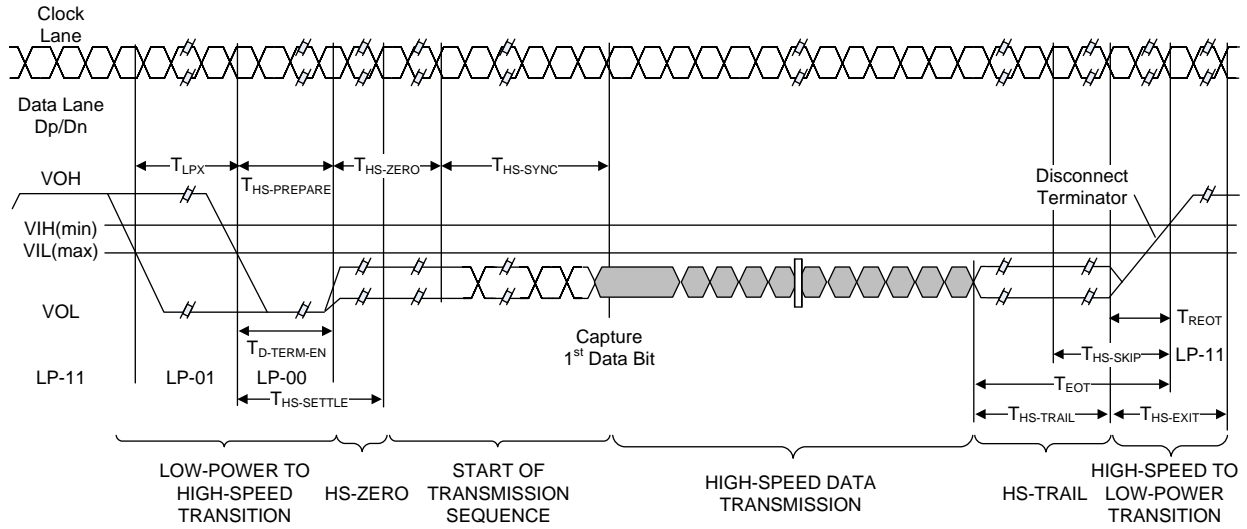
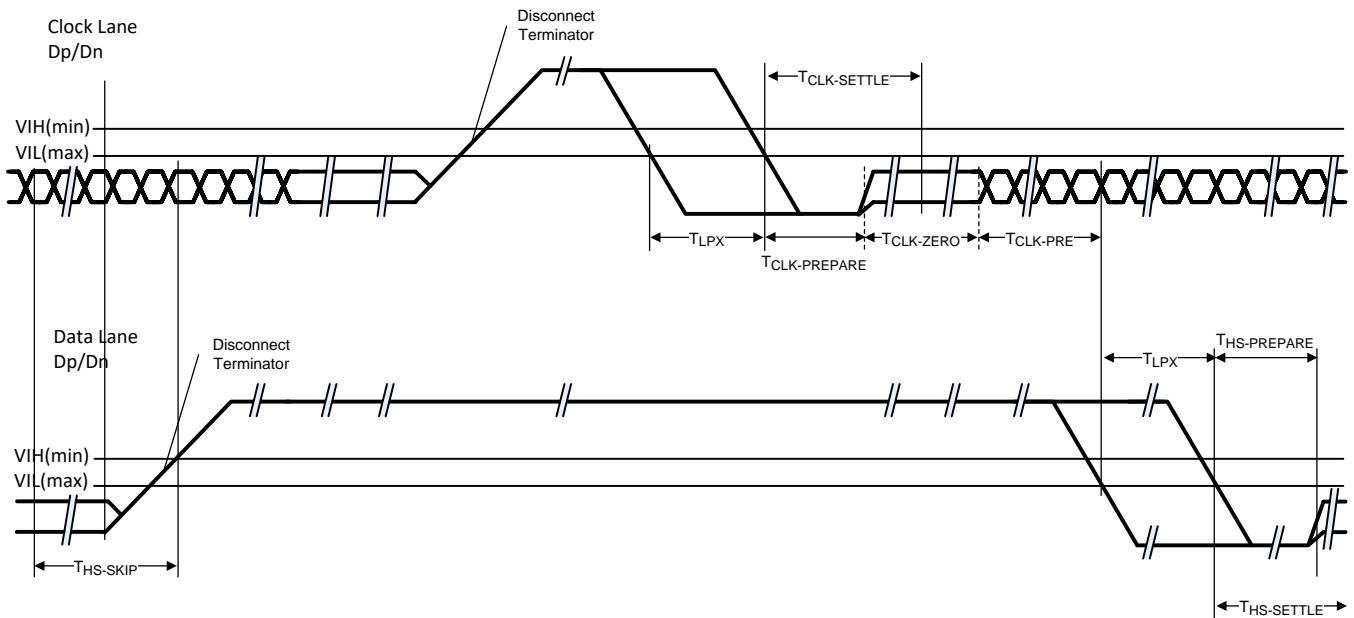


Figure 5-10. High-Speed Data Transmission Burst



(1) The HS to LP transition of the CLK does not actually take place since the CLK is always ON in HS mode.

Figure 5-11. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

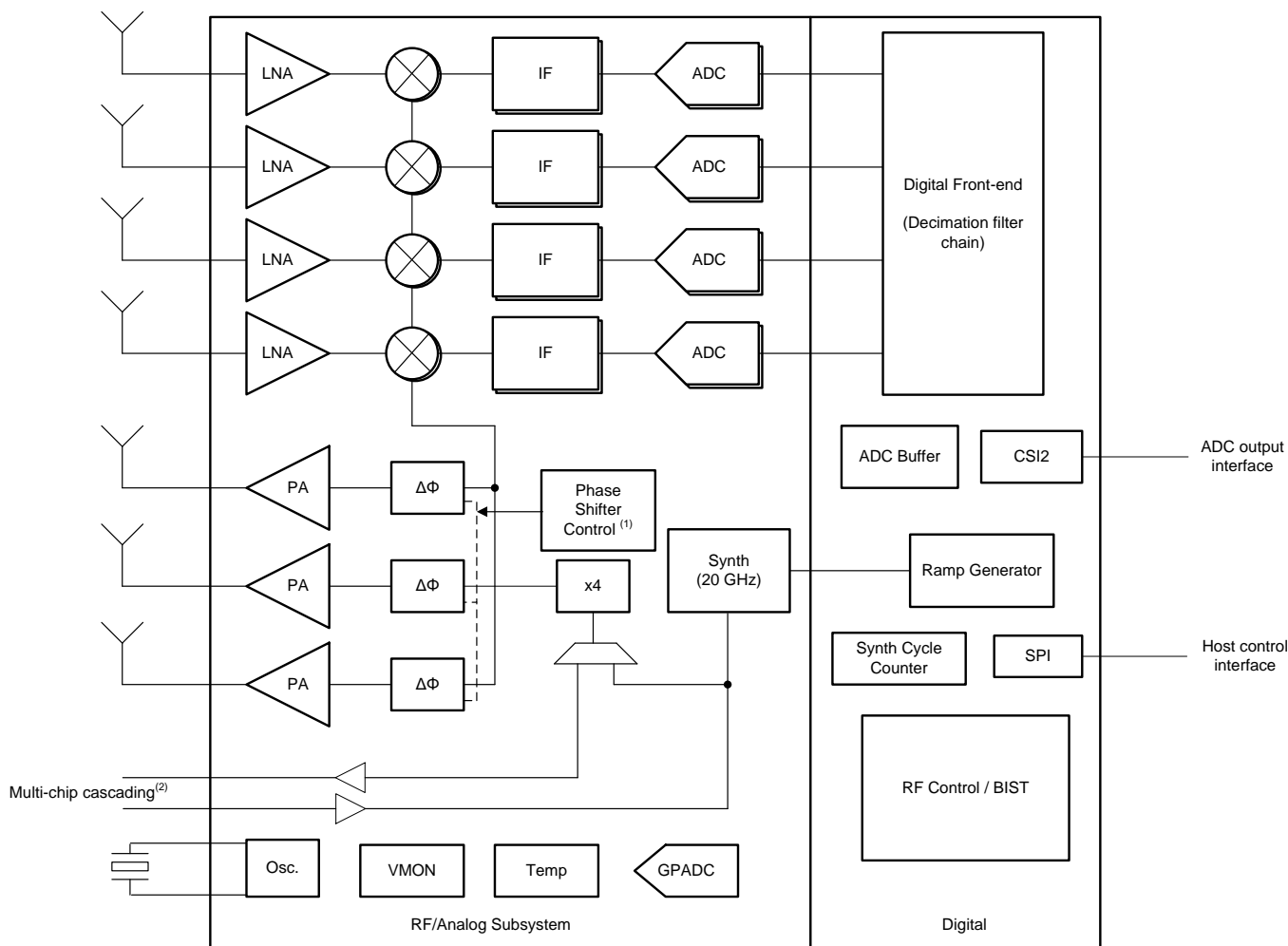


## 6 Detailed Description

### 6.1 Overview

The AWR1243 device is a single-chip highly integrated 77-GHz transceiver and front end that includes three transmit and four receive chains. The device can be used in long-range automotive radar applications such as automatic emergency braking and automatic adaptive cruise control. The AWR1243 has extremely small form factor and provides ultra-high resolution with very low power consumption. This device, when used with the TDA3X or TD2X, offers higher levels of performance and flexibility through a programmable digital signal processor (DSP); thus addressing the standard short-, mid-, and long-range automotive radar applications.

### 6.2 Functional Block Diagram



- (1) Phase Shift Control:
- 0° / 180° BPM for AWR1243
  - 0° / 180° BPM and 5.625° resolution control option for AWR1243P

### 6.3 Subsystems

### 6.3.1 *RF and Analog Subsystem*

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated simultaneously for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

Please note that AWR1243 device supports simultaneous operation of 2 transmitters and AWR1243P device supports simultaneous operation of 3 transmitters.

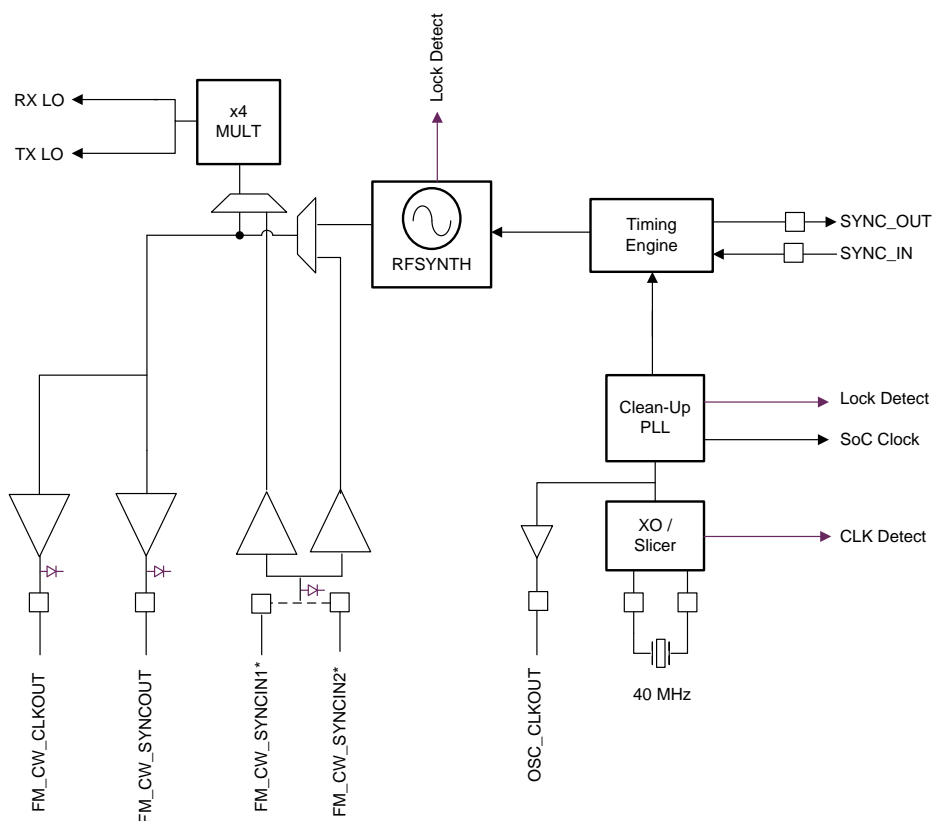
### 6.3.1.1 Clock Subsystem

The AWR1243 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The output of the RF synthesizer is available at the device pin boundary for multichip cascaded configuration. The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 6-1 describes the clock subsystem.



\* These pins are 20GHz LO input pins. Connect LO to one pin while grounding the other pin.

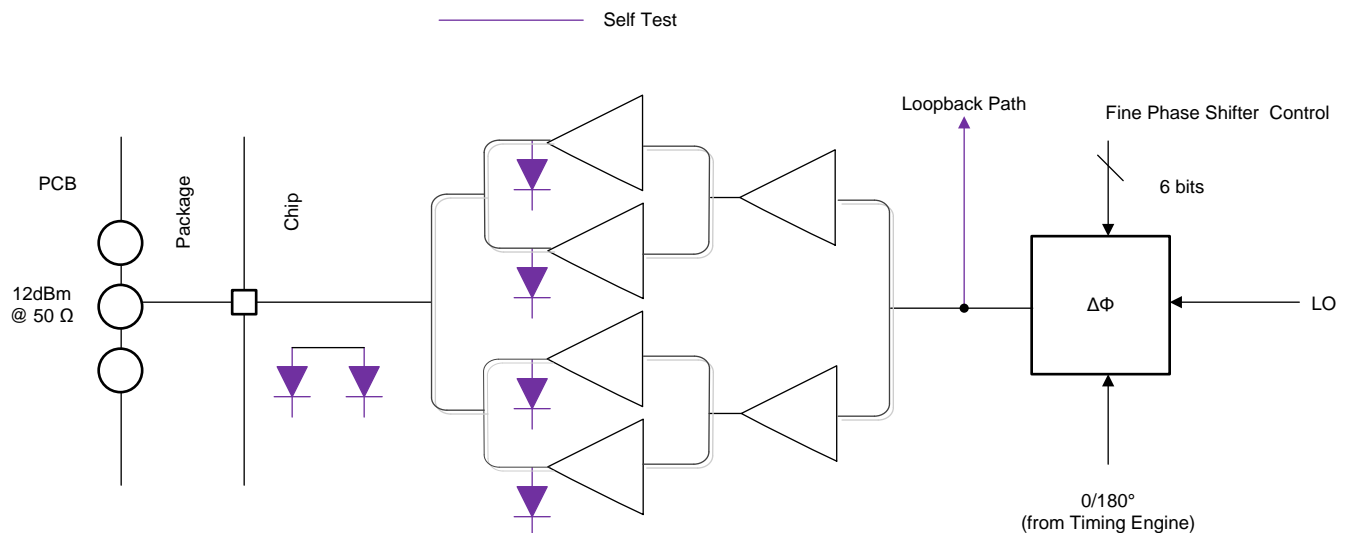
Figure 6-1. Clock Subsystem

### 6.3.1.2 Transmit Subsystem

The AWR1243 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. A maximum of two transmit chains can be operational at the same time (while all three can be used simultaneously for AWR1243P). However all three chains can be operated together in a time-multiplexed fashion. The device supports binary phase modulation for MIMO radar and interference mitigation. For AWR1243P, additional phase shifters are associated with Tx channels, and these can be programmed on a per chirp basis.

Each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

Figure 6-2 describes the transmit subsystem.



**Figure 6-2. Transmit Subsystem (Per Channel)**

### 6.3.1.3 Receive Subsystem

The AWR1243 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the AWR1243 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The AWR1243 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 15 MHz.

Figure 6-3 describes the receive subsystem.

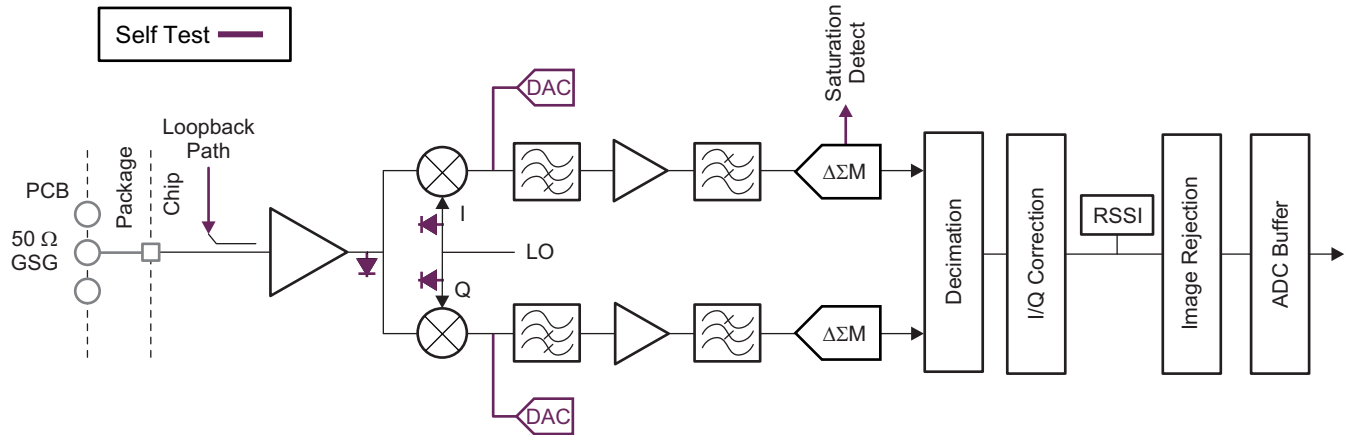


Figure 6-3. Receive Subsystem (Per Channel)

### 6.3.2 Host Interface

The AWR1243 device communicates with the host radar processor over the following main interfaces:

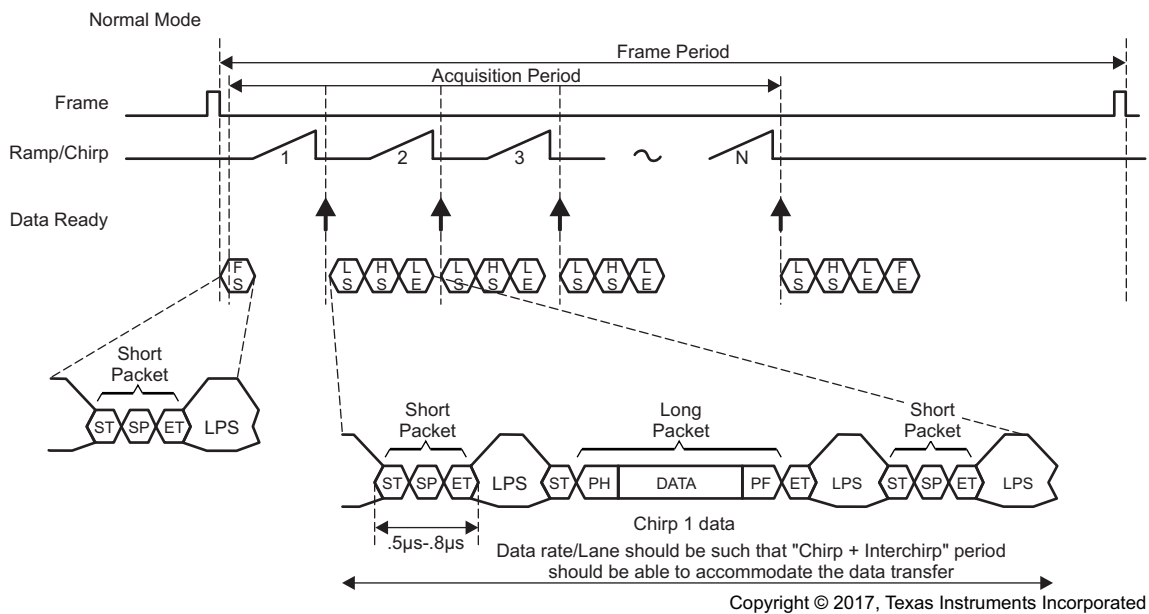
- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (slave) for host control along with HOST INTR pin for async events. . All radio control commands (and response) flow through this interface.
- Data – High-speed serial port following the MIPI CSI2 format. Four data and one clock lane (all differential). Data from different receive channels can be multiplexed on a single data lane to optimize board routing. This is a unidirectional interface used for data transfer only.
- Reset – Active-low reset for device wakeup from host
- Out-of-band interrupt
- Error – Used for notifying the host in case the radio controller detects a fault

### 6.4 Other Subsystems

#### 6.4.1 A2D Data Format Over CSI2 Interface

The AWR1243 device uses MIPI D-PHY / CSI2-based format to transfer the raw A2D samples to the external MCU. This is shown in Figure 6-4.

- Supports four data lanes
- CSI-2 data rate scalable from 150 Mbps to 600 Mbps per lane
- Virtual channel based
- CRC generation



Frame Start – CSI2 VSYNC Start Short Packet  
 Line Start – CSI2 HSYNC Start Short Packet  
 Line End – CSI2 HSYNC End Short Packet  
 Frame End – CSI2 VSYNC End Short Packet

Figure 6-4. CSI-2 Transmission Format

The data payload is constructed with the following three types of information:

- Chirp profile information
- The actual chirp number
- A2D data corresponding to chirps of all four channels
  - Interleaved fashion
- Chirp quality data (configurable)

The payload is then split across the four physical data lanes and transmitted to the receiving D-PHY. The data packet packing format is shown in [Figure 6-5](#)

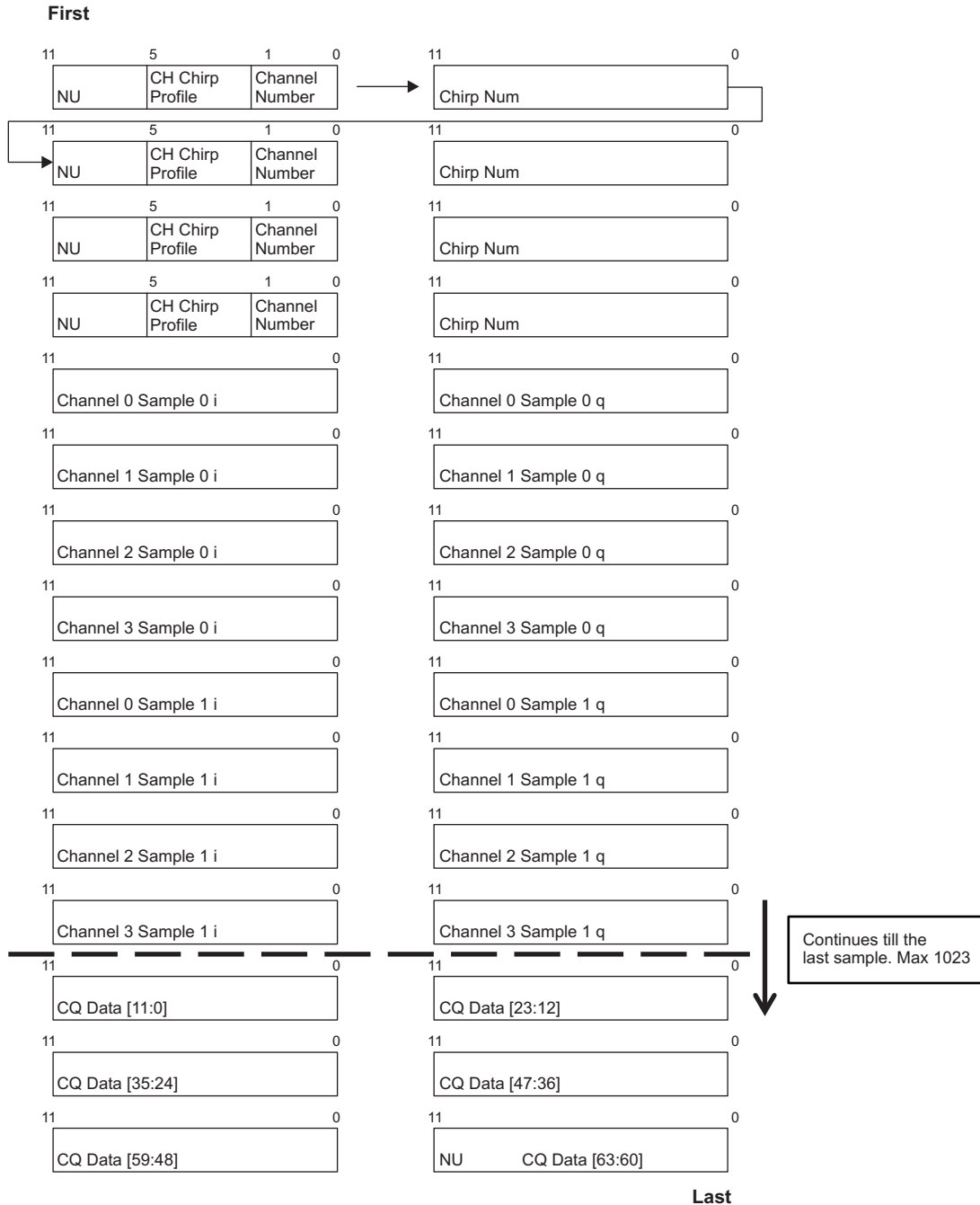


Figure 6-5. Data Packet Packing Format for 12-Bit Complex Configuration

## 7 Applications, Implementation, and Layout

### NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Application Information

A typical application addresses the standard short-, mid-, long-range, and high-performance imaging radar applications with this radar front end and external programmable MCU. Figure 7-1 shows a short-, medium-, or long-range radar application.

### 7.2 Short-, Medium-, and Long-Range Radar

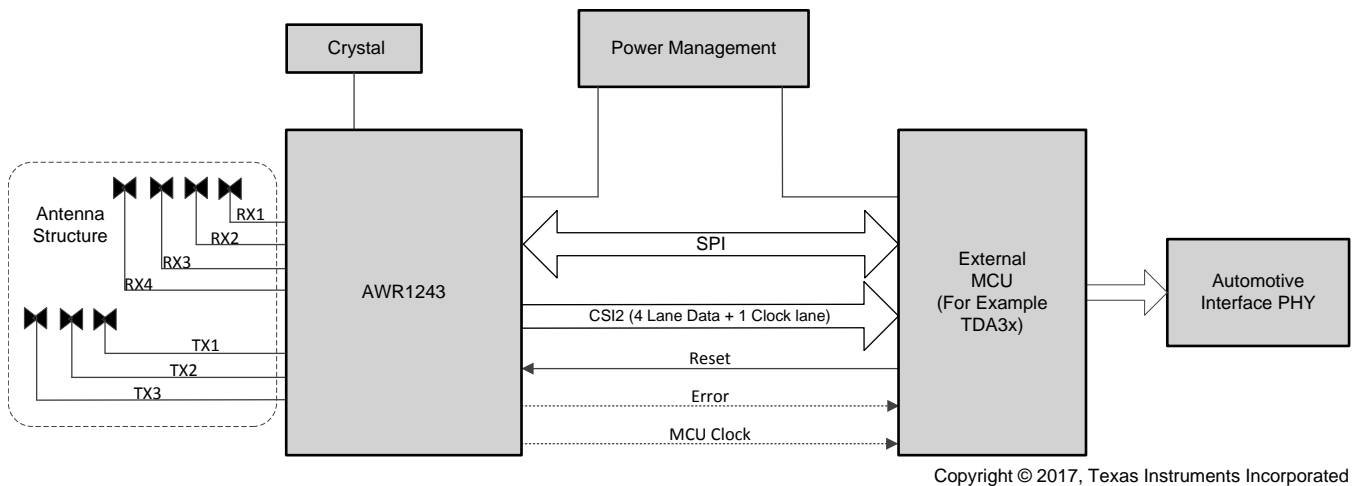
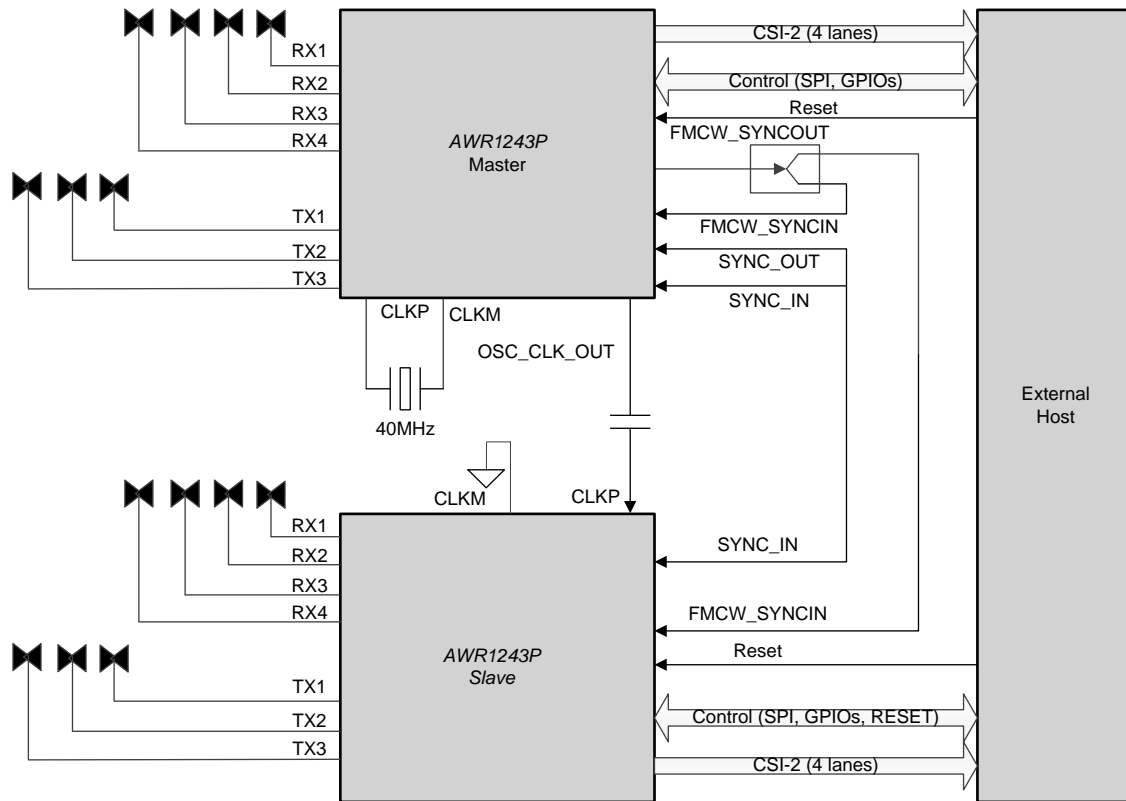


Figure 7-1. Short-, Medium-, and Long-Range Radar

### 7.3 Imaging Radar using Cascade Configuration





Copyright © 2017, Texas Instruments Incorporated

Figure 7-2. Imaging Radar using Cascade Configuration

## 7.4 Reference Schematic

Figure 7-3 shows the reference schematic for the AWR1243 device.

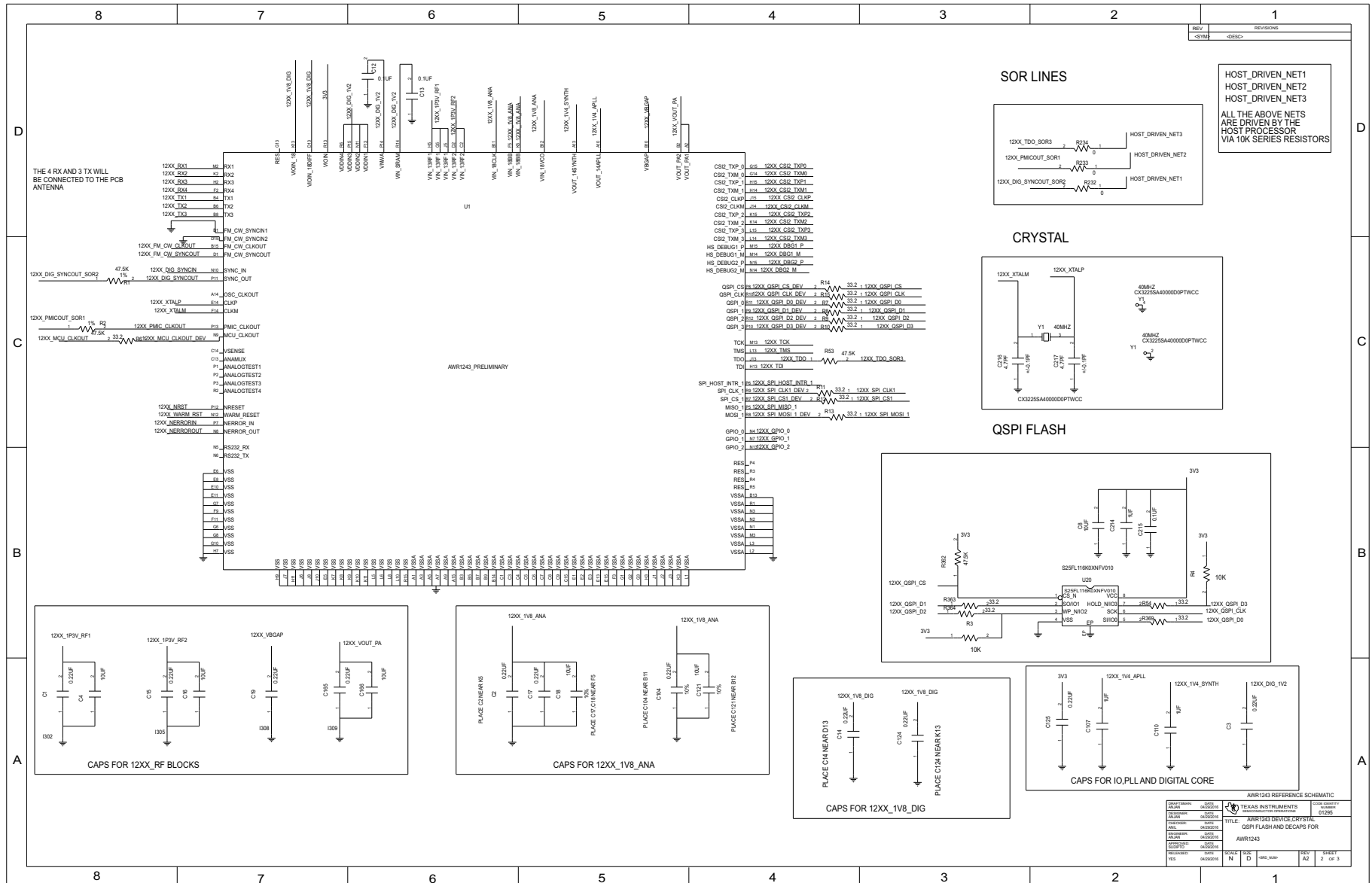


Figure 7-3. AWR1243 Reference Schematic

## 7.5 Layout

The top layer routing, top layer closeup, and bottom layer routing are shown in [Figure 7-4](#), [Figure 7-5](#), and [Figure 7-6](#), respectively.

## 7.5.1 Layout Guidelines

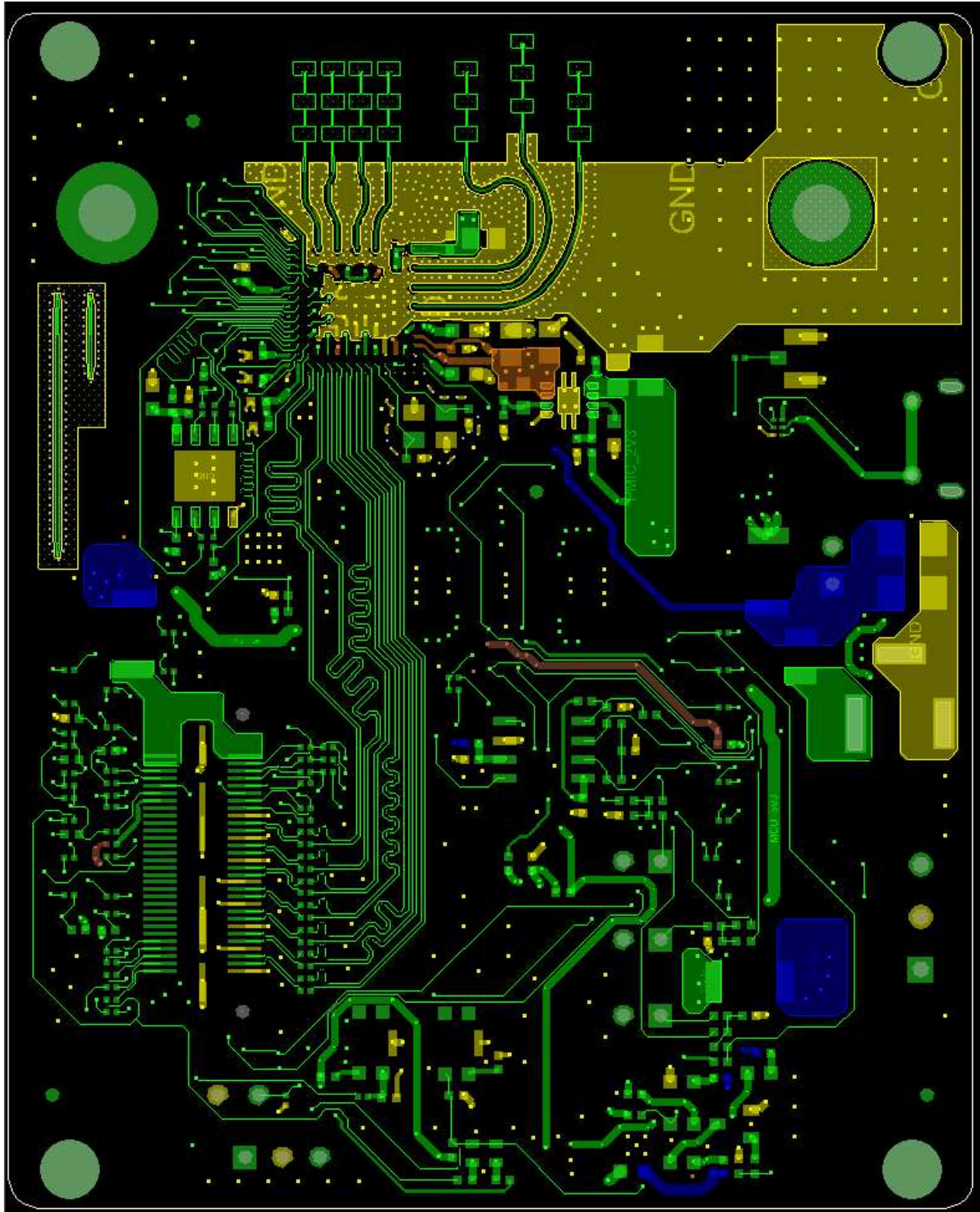


Figure 7-4. Top Layer Routing

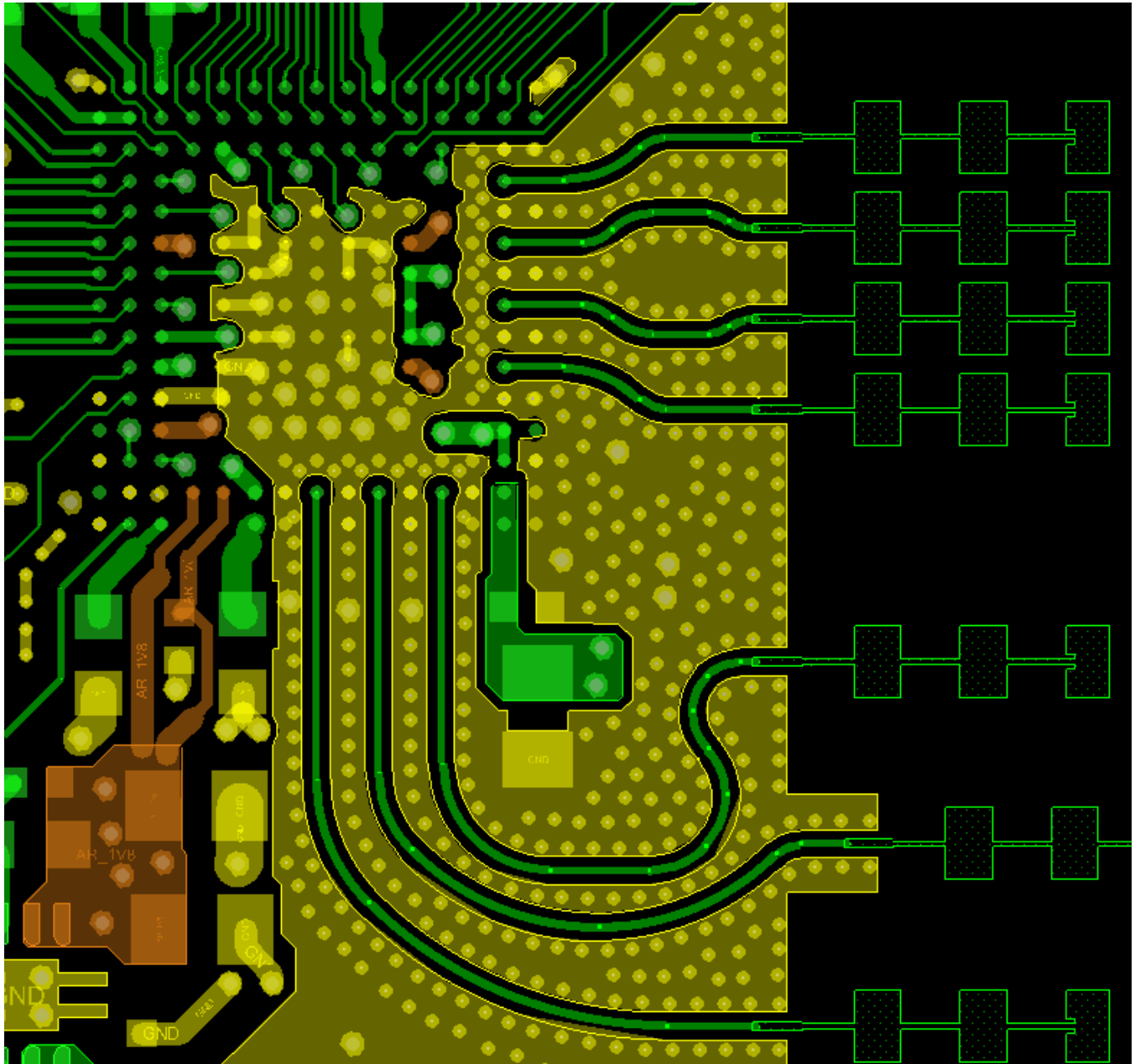


Figure 7-5. Top Layer Routing Closeup

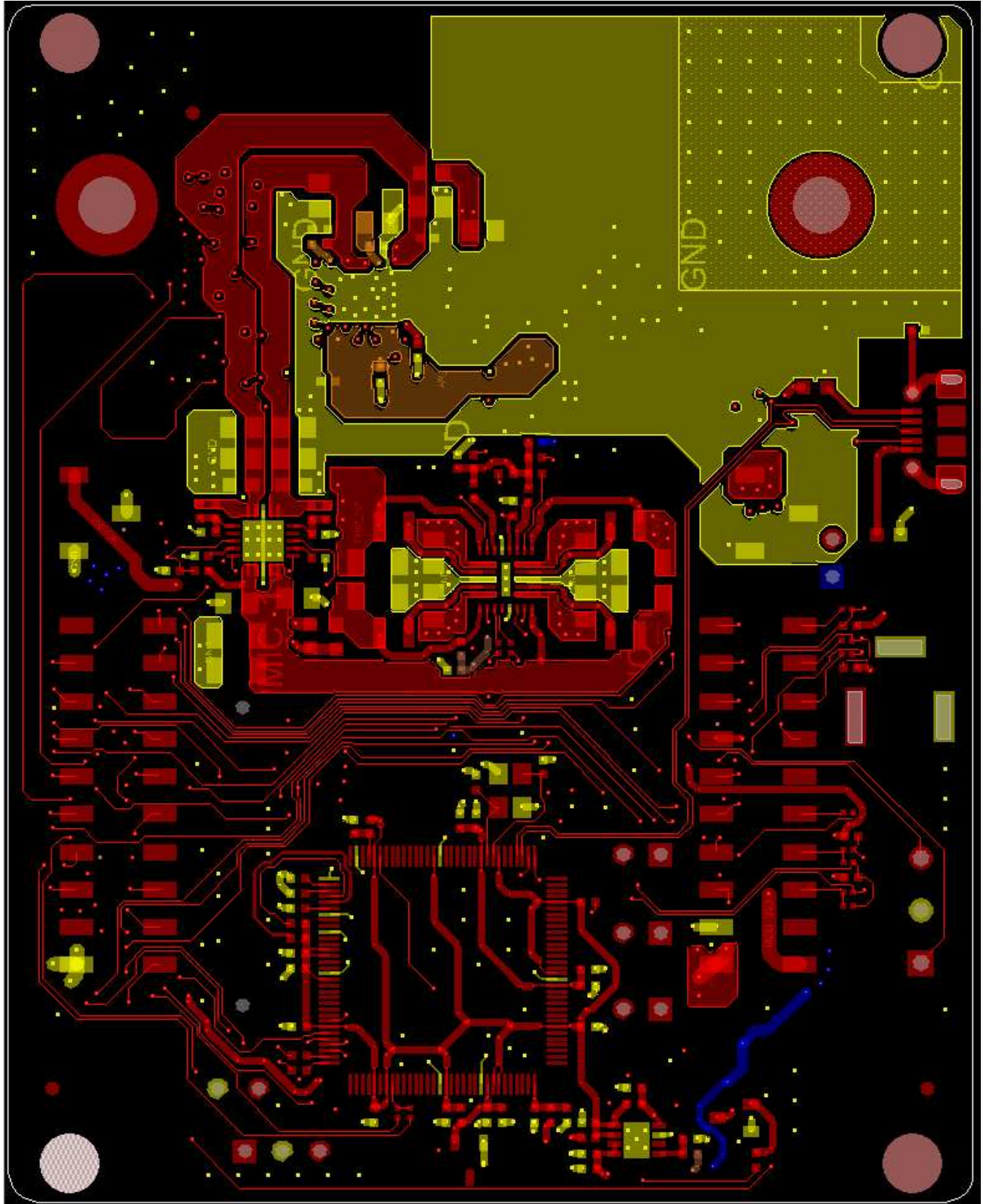


Figure 7-6. Bottom Layer Routing

### 7.5.2 Stackup Details

Layer	Stack up	Description	Type	Base Thickness	Processed Thickness	$\epsilon_r$	Copper Coverage
1		Rogers 4835 4mil coreH/1 Low Pro	Rogers 4835	0.689	2.067		100.000
2		Iteq IT 180A Prepreg 1080	Dielectric	4.000	4.000	3.480	
		Iteq IT 180A Prepreg 1080	Dielectric	1.260	1.260		73.000
		Iteq IT 180A Prepreg 1080	Dielectric	4.195	2.830	3.700	
3		Iteq IT 180A Prepreg 1080	Dielectric	4.195	2.830	3.700	
		Iteq IT 180A 28 mil core 1/1	FR4	1.260	1.260		69.000
4	Iteq IT 180A Prepreg 1080	Dielectric	28.000	28.000	4.280		
	Iteq IT 180A Prepreg 1080	Dielectric	1.260	1.260		48.000	
	Iteq IT 180A Prepreg 1080	Dielectric	4.195	2.691	3.700		
	Iteq IT 180A Prepreg 1080	Dielectric	4.195	2.691	3.700		
5	Iteq IT 180A Prepreg 1080	Dielectric	4.195	2.691	3.700		
	Iteq IT 180A 4 mil core 1/H	FR4	1.260	1.260		72.000	
6	Iteq IT 180A 4 mil core 1/H	FR4	4.000	4.000	3.790		
			0.689	2.067		100.000	

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

### 8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AWR1243*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

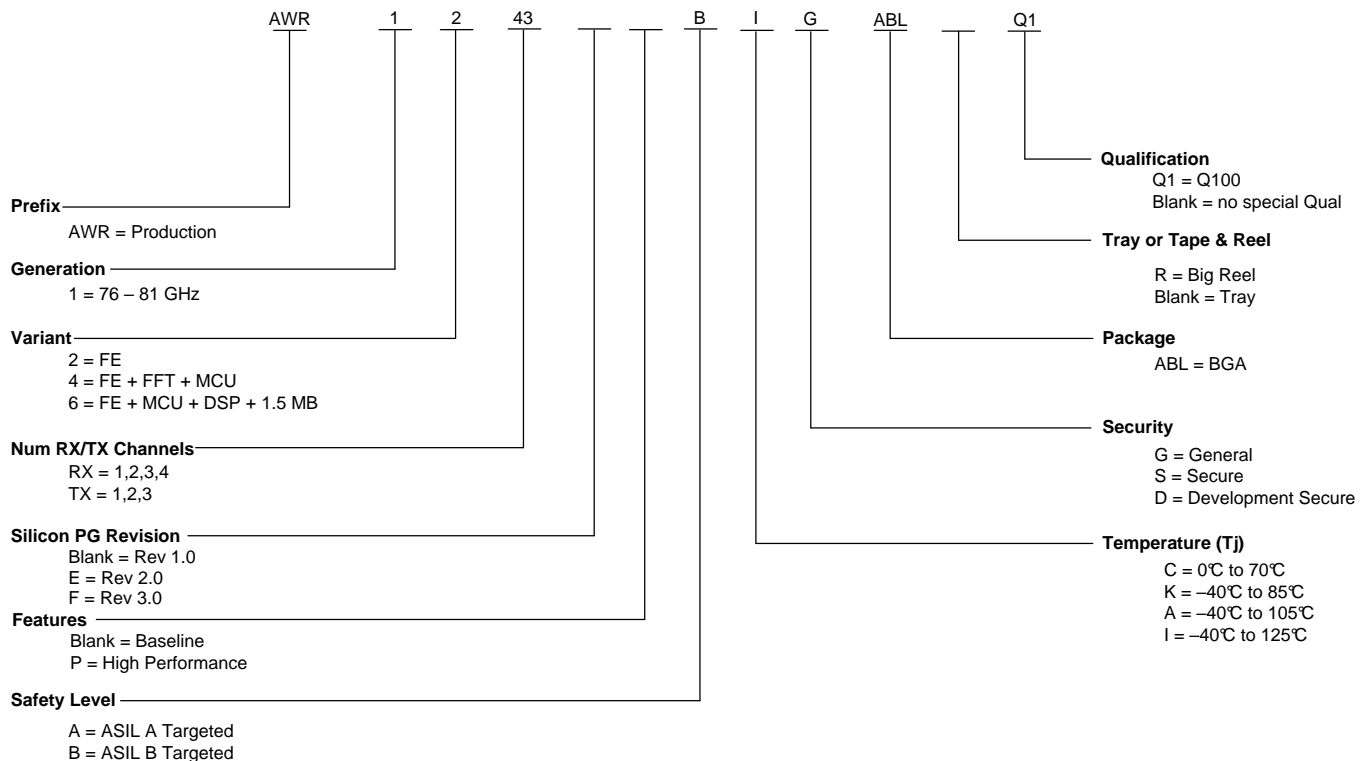
Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161), the temperature range (for example, blank is the default commercial temperature range). [Figure 8-1](#) provides a legend for reading the complete device name for any *AWR1243* device.

For orderable part numbers of *AWR1243* devices in the ABL0161 package types, see the Package Option Addendum of this document, the TI website ([www.ti.com](http://www.ti.com)), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [AWR1243 Device Errata Silicon Revision 1.0 and 2.0](#).





**Figure 8-1. Device Nomenclature**

## 8.2 Tools and Software

### Development Tools

**AWR1243 Cascade Application Note** Describes TI's cascaded mmWave radar system.

### Models

**AWR1243 BSDL Model** Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

**AWR1x43 IBIS Model** IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

**AWR1243 Checklist for Schematic Review, Layout Review, Bringup/Wakeup** A set of steps in spreadsheet form to select system functions and pinmux options. Specific EVM schematic and layout notes to apply to customer engineering. A bringup checklist is suggested for customers.

## 8.3 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](http://ti.com) (AWR1243). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

### Errata

**AWR1243 Device Errata** Describes known advisories, limitations, and cautions on silicon and provides workarounds.

## 8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.


**TI Embedded Processors Wiki** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.5 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

## 8.6 静电放电警告

 ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 8.8 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

### 9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

#### CAUTION

The following package information is subject to change without notice.

## 重要声明和免责声明




TI 均以“原样”提供技术性及其可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2018 德州仪器半导体技术（上海）有限公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AWR1243FBIGABLQ1	ACTIVE	FC/CSP	ABL	161	176	RoHS & Green	Call TI   SNAGCU	Level-3-260C-168 HR	-40 to 125	AWR1243 IG 964FC C ABL G1	
AWR1243FBIGABLRQ1	ACTIVE	FC/CSP	ABL	161	1000	RoHS & Green	Call TI   SNAGCU	Level-3-260C-168 HR	-40 to 125	AWR1243 IG 964FC C ABL G1	
XA1243FPBGABL	ACTIVE	FC/CSP	ABL	161	1	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

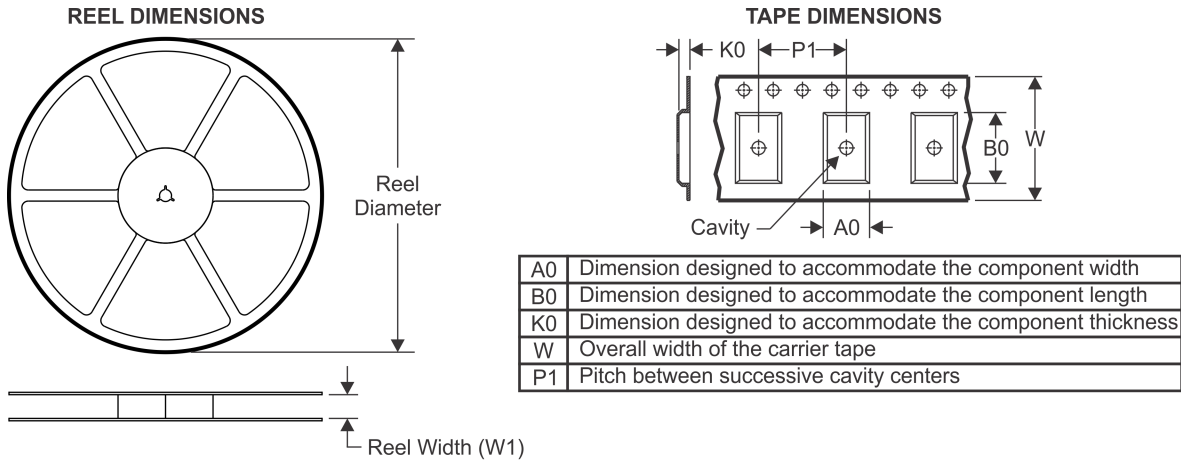
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AWR1243FBIGABLRQ1	FC/CSP	ABL	161	1000	330.0	24.4	10.7	10.7	1.65	16.0	24.0	Q1

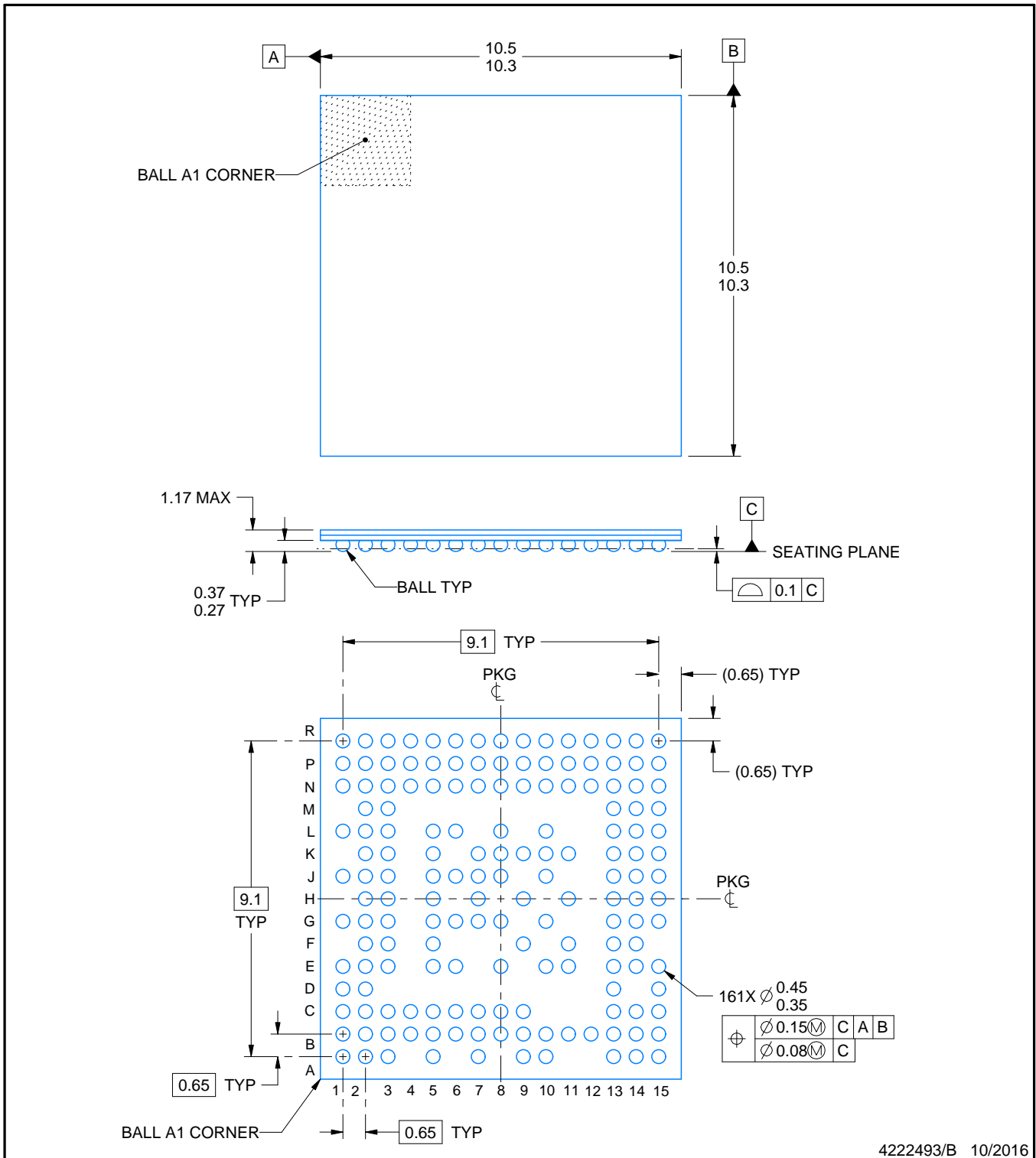
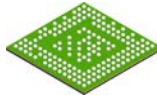
TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AWR1243FBIGABLRQ1	FC/CSP	ABL	161	1000	336.6	336.6	41.3





NOTES:

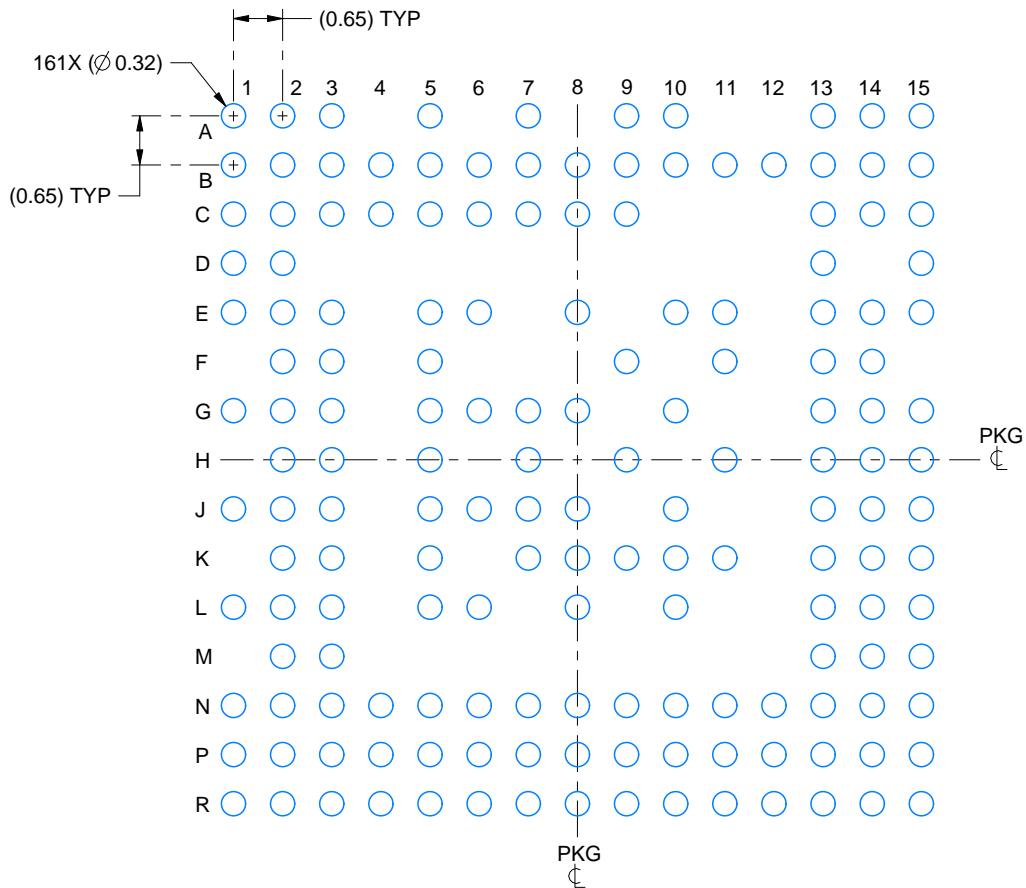
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

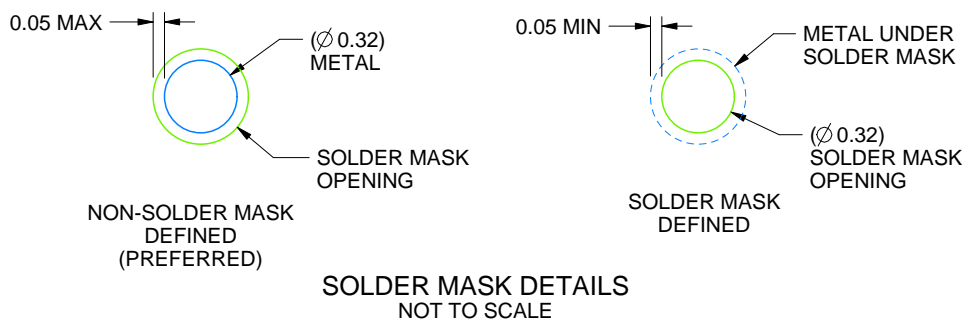
ABL0161A

FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4222493/B 10/2016

NOTES: (continued)

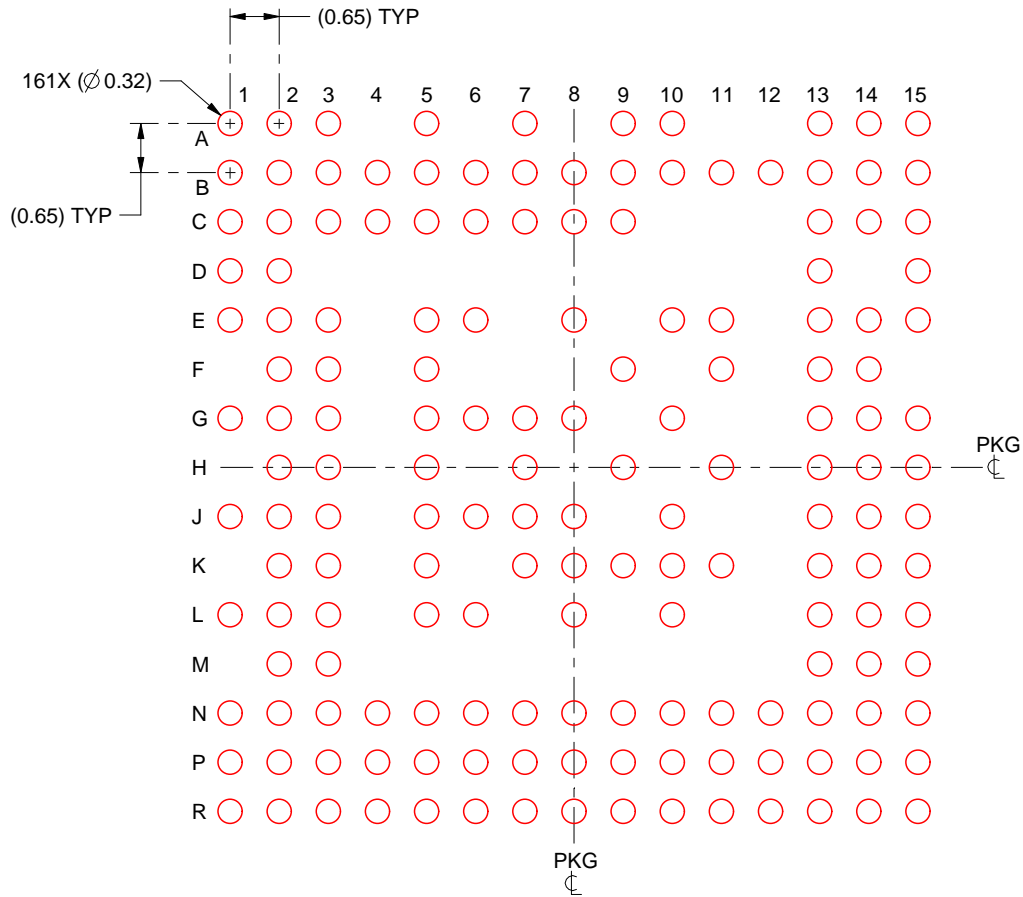
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

# EXAMPLE STENCIL DESIGN

## ABL0161A

## FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4222493/B 10/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## 重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 或 [ti.com.cn](https://www.ti.com.cn) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2021 德州仪器半导体技术（上海）有限公司