AWR1843AOP 单芯片 77GHz 和 79GHz FMCW 雷达传感器

1 特性

- FMCW 收发器
  - 集成 4 个接收器和 3 个发送器的封装天线 (AOP)
  - 集成 PLL、发送器、接收器、基带和 ADC
  - 76GHz 至 81GHz 的覆盖范围，具有 4GHz 的可用带宽
  - 基于分数 N PLL 的超精确线性调频脉冲引擎
  - TX 功率：16dBm
  - RX 噪声系数：10dB（76 至 81GHz）
  - 1MHz 时的相位噪声：
    - 95dBc/Hz（76 至 77GHz）
    - 93dBc/Hz（77 至 81GHz）
- 内置校准和自检（监控）
  - 基于 Arm® Cortex®-R4F 的无线电控制系统
  - 内置固件 (ROM)
  - 针对频率和温度进行自校准的系统
- 用于 FMCW 信号处理的 C674x DSP
- 片上存储器：2MB RAM
- 用于物体跟踪和分类、AUTOSAR 和接口控制的 Arm Cortex-R4F 微控制器
  - 支持自主模式（从 QSPI 闪存加载用户应用）
- 主机接口
  - CAN（两个实例，其中一个是 CAN-FD）
- 为用户应用提供的其他接口
  - 多达 6 个通用 ADC 通道
  - 多达 2 个 SPI 端口
  - 多达 2 个 UART
  - I^2C
  - GPIO
  - 用于原始 ADC 数据和调试仪表的双通道 LVDS 接口
- 以符合功能安全标准为目标
  - 专为功能安全应用开发
  - 将提供相关文档来协助进行符合 ISO 26262 标准的功能安全系统设计
  - 以硬件完整性高达 ASIL-B 级为目标
  - 安全相关认证
    - 计划通过 TUV Sud 的 ISO 26262 认证
- 符合 AEC-Q100 标准
- AWR1843AOP 高级特性
  - 嵌入式自监控，无需使用主机处理器
  - 复基带架构
  - 嵌入式干扰检测功能
  - 发送路径中的可编程相位旋转器，用于实现波束形成
- 电源管理
  - 内置 LDO 网络，可增强 PSRR
  - I/O 支持双电压 3.3V/1.8V
- 时钟源
  - 支持频率为 40MHz 的外部振荡器
  - 支持外部驱动、频率为 40MHz 的时钟（方波/正弦波）
  - 支持 40MHz 晶体与负载电容器相连接
- 轻松的硬件设计
  - 0.8mm 间距、180 引脚 15mm × 15mm 覆晶 BGA 封装 (ALP)，可实现轻松组装和低成本 PCB 设计
  - 小解决方案尺寸

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2 应用

- 盲点检测
- 变道辅助
- 侧向来车警示
- 泊车辅助
- 占位检测
- 手势识别
- 车门开启器应用

3 说明

AWR1843AOP 是一款能够在 76GHz 至 81GHz 频带内运行的封装天线器件。该器件采用 TI 的低功耗 45nm RFCMOS 工艺进行构建，并且在超小封装中实现了出色的集成度。AWR1843AOP 是适用于汽车领域中低功耗、自监控、超精确雷达系统的理想解决方案。

它集成了一个 DSP 子系统，该子系统包含 TI 用于雷达信号处理的高性能 C674x DSP。该器件包含一个 BIST 处理器子系统，该子系统负责无线电配置、控制和校准。此外，该器件还包含用于汽车连接的用户可编程 Arm Cortex-R4F。硬件加速器区块 (HWA) 可执行雷达处理，并减轻 DSP 上的负载，从而执行更高级的算法。简单编程模型更改可支持各种传感器应用，并且能够进行动态重新配置，从而实现多模式传感器。此外，该器件作为完整的平台解决方案进行提供，该解决方案包括硬件参考设计、软件驱动程序、样例配置、API 指南以及用户文档。

器件信息

器件型号	封装(1)	封装尺寸	托盘/卷带包装
XA1843ARBGALP	FCBGA (180)	15mm × 15mm	托盘

(1) 更多信息请参阅 节 12，*机械封装和可订购产品信息*。

3.1 Functional Block Diagram

图 3-1 is functional block diagram for the device.

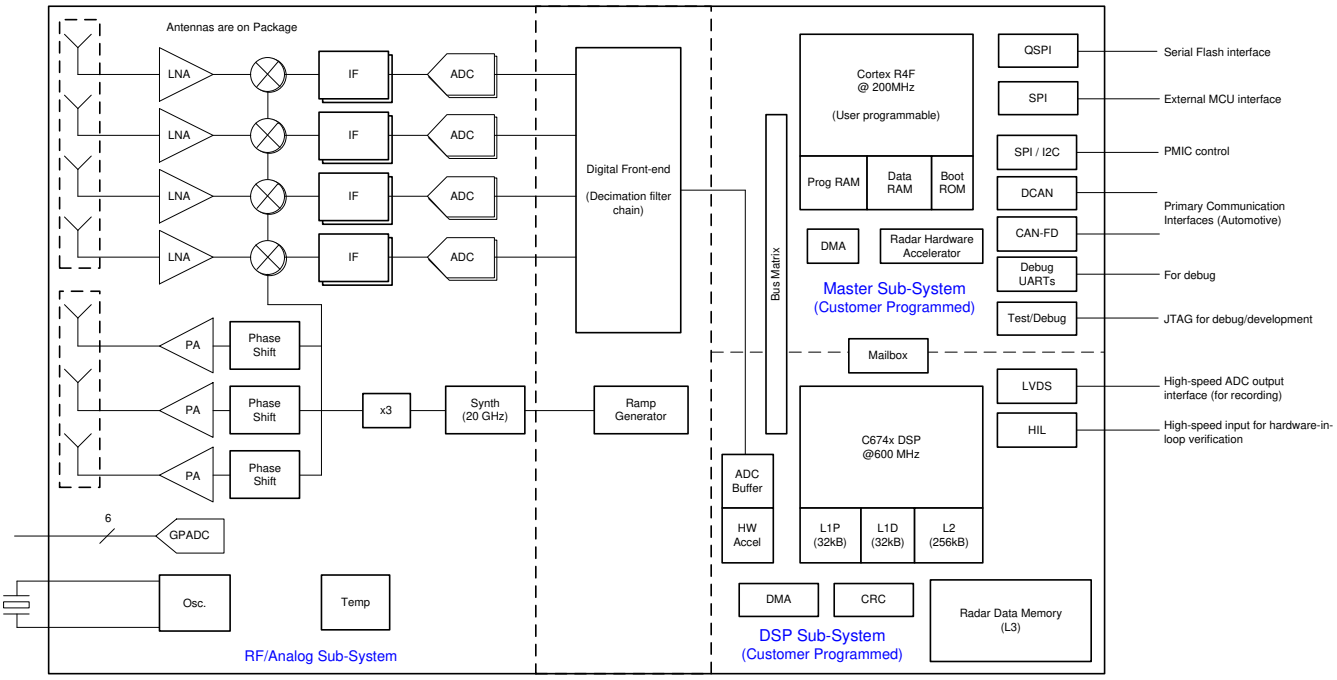

图 3-1. Functional Block Diagram

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4 Revision History

DATE	REVISION	NOTES
March 2021	*	Initial Release

5 Device Comparison

表 5-1 shows a comparison between devices, highlighting the differences.

表 5-1. Device Features Comparison

FUNCTION		AWR6843AOP	AWR1843AOP	AWR1843	AWR1642	AWR1443
Antenna on Package (AOP)		Yes	Yes	—	—	—
Number of receivers		4	4	4	4	4
Number of transmitters		3(1)	3(1)	3(1)	2	3
RF frequency range		60 to 64 GHz	76 to 81 GHz	76 to 81 GHz	76 to 81 GHz	76 to 81 GHz
On-chip memory		1.75MB	2MB	2MB	1.5MB	576KB
Max I/F (Intermediate Frequency) (MHz)		10	10	10	5	5
Max real sampling rate (Msps)		25	25	25	12.5	12.5
Max complex sampling rate (Msps)		12.5	12.5	12.5	6.25	6.25
Processors						
MCU (Arm Cortex-R4F)		Yes	Yes	Yes	Yes	Yes
DSP (C674x)		Yes	Yes	Yes	Yes	—
Peripherals						
Serial Peripheral Interface (SPI) ports		2	2	2	2	1
Quad Serial Peripheral Interface (QSPI)		Yes	Yes	Yes	Yes	Yes
Inter-Integrated Circuit (I^2C) interface		1	1	1	1	1
Controller Area Network (DCAN) interface		—	1	1	1	1
Controller Area Network (CAN-FD) interface		2	1	1	—	—
Trace		Yes	Yes	Yes	Yes	—
PWM		Yes	Yes	Yes	Yes	—
Hardware In Loop (HIL/DMM)		Yes	Yes	Yes	Yes	—
GPADC		Yes	Yes	Yes	Yes	Yes
LVDS/Debug		Yes	Yes	Yes	Yes	Yes
Hardware accelerator		Yes	Yes	Yes	—	Yes
1-V bypass mode		Yes	Yes	Yes	Yes	Yes
JTAG		Yes	Yes	Yes	Yes	Yes
Product status	Product Preview (PP), Advance Information (AI), or Production Data (PD)	AI(2)	AI(2)	PD(3)	PD(3)	PD(3)

(1) 3 Tx Simultaneous operation is supported only with 1-V LDO bypass and PA LDO disable mode. In this mode, the 1-V supply needs to be fed on the VOUT PA pin.
(2) ADVANCE INFORMATION for pre-production products; subject to change without notice.
(3) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty.

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5.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave Sensors	TI’s mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for automotive applications.
Automotive mmWave Sensors	TI’s automotive mmWave sensor portfolio offers high-performance radar front end to ultra-high resolution, small and low-power single-chip radar solutions. TI’s scalable sensor portfolio enables design and development of ADAS system solution for every performance, application and sensor configuration ranging from comfort functions to safety functions in all vehicles.
Companion Products for AWR1843AOP	Review products that are frequently purchased or used in conjunction with this product.
Reference Designs for AWR1843AOP	TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

6 Terminal Configuration and Functions

6.1 Pin Diagram

图 6-1 shows the pin locations for the 180-pin 15 × 15 mm FCBGA package.

	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
V	VSSA	VSSA	RS232_RX	VDDIN	VNWA	MCU_CLKOUT	VIN_SRAM	VIOIN_18	PMIC_CLKOUT	VIOIN	VDDIN	VNWA	VIN_SRAM	DP2	VDDIN	DP4	VPP	VSS	V
U	VSSA	VSSA	RS232_TX	NERROR_OUT	NERROR_IN	WARM_RESET	SYNC_IN	NRESET	TDO	TDI	TMS	DP0	DP1	DP3	DMM_SYNC	DMM_CLK	VIOIN_18DIFF	VSS	U
T	GPADC_4	VSSA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TCK	LVDS_FRCLKM	LVDS_FRCLKP	T
R	GPADC_3	VSSA	VSSA													VSS	LVDS_CLKM	LVDS_CLKP	R
P	GPADC_1	GPADC_2	VSSA													VSS	LVDS_TXP[1]	LVDS_TXM[1]	P
N	VSSA	VSSA	VSSA													VSS	LVDS_TXP[0]	LVDS_TXM[0]	N
M	VIN_18BB	VIN_18BB	VIN_18BB													SYNC_OUT	GPIO_0	DP5	M
L	VSSA	VSSA	VSSA													GPIO_1	DP6	DP7	L
K	VSSA	VSSA	VSSA													GPIO_2	QSPI[3]	VIOIN_18	K
J	VIN_13RF1	VIN_13RF1	VIN_13RF1													QSPI[2]	QSPI_CS_N	VDDIN	J
H	VIN_13RF2	VIN_13RF2	VIN_13RF2													QSPI[0]	QSPI_CLK	VIOIN	H
G	VOUT_PA	VOUT_PA	VOUT_PA													SPIB_MISO	QSPI[1]	SPIB_MOSI	G
F	VSSA	VSSA	VSSA													VSS	SPIA_MOSI	VIOIN_18	F
E	VSSA	VSSA	VSSA													VSS	SPIB_CLK	VDDIN	E
D	VSSA	VSSA	VSSA													SPIB_CS_N	SPIA_CLK	SPIA_MISO	D
C	VIN_18CLK	VSSA	VSSA	VIN_18CLK	VSSA	VSSA	VSSA	VIN_18VCO	GPADC_6	GPADC_5	VSSA	VSSA	VSSA	DP14	DP10	DP8	SPIA_CS_N	VNWA	C
B	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	CLKM	VSSA	DP15	DP12	DP9	SPI_HOST_INTR	VIOIN_18	B
A	VSSA	VSSA	VBGAP	VSSA	OSC_CLKOUT	VSSA	VIN_18VCO	VSSA	VOUT_14APLL	VOUT_14SYNTH	VSSA	CLKP	VSSA	VIN_SRAM	DP13	DP11	VSS	VSS	A
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

图 6-1. Pin Diagram

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6.2 Pin Attributes

表 6-1. Pin Attributes (ALP180A Package)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
M2	GPIO_0	GPIO_13	0xFFFFEA04	0	IO	Output Disabled	Pull Down
		GPIO_0		1	IO		
		PMIC_CLKOUT		2	O		
		ADC_VALID		7	O		
		EPWM1B		10	O		
		ePWM2A		11	O		
L3	GPIO_1	GPIO_16	0xFFFFEA08	0	IO	Output Disabled	Pull Down
		GPIO_1		1	IO		
		SYNC_OUT		2	O		
		ADC_VALID		7	O		
		DMM_MUX_IN		12	I		
		SPIB_CS_N_1		13	IO		
		SPIB_CS_N_2		14	IO		
		EPWM1SYNCI		15	I		
K3	GPIO_2	GPIO_26	0xFFFFEA64	0	IO	Output Disabled	Pull Down
		GPIO_2		1	IO		
		OSC_CLKOUT		2	O		
		MSS_UARTB_TX		7	O		
		BSS_UART_TX		8	O		
		SYNC_OUT		9	O		
		PMIC_CLKOUT		10	O		
		CHIRP_START		11	O		
		CHIRP_END		12	O		
		FRAME_START		13	O		
U7	GPIO_31 (DP0)	TRACE_DATA_0	0xFFFFEA7C	0	O	Output Disabled	Pull Down
		GPIO_31		1	IO		
		DMM0		2	I		
		MSS_UARTA_TX		4	IO		
U6	GPIO_32 (DP1)	TRACE_DATA_1	0xFFFFEA80	0	O	Output Disabled	Pull Down
		GPIO_32		1	IO		
		DMM1		2	I		
V5	GPIO_33 (DP2)	TRACE_DATA_2	0xFFFFEA84	0	O	Output Disabled	Pull Down
		GPIO_33		1	IO		
		DMM2		2	I		

表 6-1. Pin Attributes (ALP180A Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
U5	GPIO_34 (DP3)	TRACE_DATA_3	0xFFFFEA88	0	O	Output Disabled	Pull Down
		GPIO_34		1	IO		
		DMM3		2	I		
		EPWM3SYNCO		4	O		
V3	GPIO_35 (DP4)	TRACE_DATA_4	0xFFFFEA8C	0	O	Output Disabled	Pull Down
		GPIO_35		1	IO		
		DMM4		2	I		
		EPWM2SYNCO		4	O		
M1	GPIO_36 (DP5)	TRACE_DATA_5	0xFFFFEA90	0	O	Output Disabled	Pull Down
		GPIO_36		1	IO		
		DMM5		2	I		
		MSS_UARTB_TX		5	O		
L2	GPIO_37 (DP6)	TRACE_DATA_6	0xFFFFEA94	0	O	Output Disabled	Pull Down
		GPIO_37		1	IO		
		DMM6		2	I		
		BSS_UART_TX		5	O		
L1	GPIO_38 (DP7)	TRACE_DATA_7	0xFFFFEA98	0	O	Output Disabled	Pull Down
		GPIO_38		1	IO		
		DMM7		2	I		
		DSS_UART_TX		5	O		
C3	GPIO_39 (DP8)	TRACE_DATA_8	0xFFFFEA9C	0	O	Output Disabled	Pull Down
		GPIO_39		1	IO		
		DMM8		2	I		
		CAN_FD_TX		4	O		
		EPWM1SYNCI		5	I		
B3	GPIO_40 (DP9)	TRACE_DATA_9	0xFFFFEAA0	0	O	Output Disabled	Pull Down
		GPIO_40		1	IO		
		DMM9		2	I		
		CAN_FD_RX		4	I		
		EPWM1SYNCO		5	O		
C4	GPIO_41 (DP10)	TRACE_DATA_10	0xFFFFEAA4	0	O	Output Disabled	Pull Down
		GPIO_41		1	IO		
		DMM10		2	I		
		EPWM3A		4	O		

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表 6-1. Pin Attributes (ALP180A Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
A3	GPIO_42 (DP11)	TRACE_DATA_11	0xFFFFEAA8	0	O	Output Disabled	Pull Down
		GPIO_42		1	IO		
		DMM11		2	I		
		EPWM3B		4	O		
B4	GPIO_43 (DP12)	TRACE_DATA_12	0xFFFFEAAC	0	O	Output Disabled	Pull Down
		GPIO_43		1	IO		
		DMM12		2	I		
		EPWM1A		4	O		
		CAN_FD_TX		5	O		
A4	GPIO_44 (DP13)	TRACE_DATA_13	0xFFFFEAB0	0	O	Output Disabled	Pull Down
		GPIO_44		1	IO		
		DMM13		2	I		
		EPWM1B		4	O		
		CAN_FD_RX		5	I		
C5	GPIO_45 (DP14)	TRACE_DATA_14	0xFFFFEAB4	0	O	Output Disabled	Pull Down
		GPIO_45		1	IO		
		DMM14		2	I		
		EPWM2A		4	O		
B5	GPIO_46 (DP15)	TRACE_DATA_15	0xFFFFEAB8	0	O	Output Disabled	Pull Down
		GPIO_46		1	IO		
		DMM15		2	I		
		EPWM2B		4	O		
U3	GPIO_47 (DMM_CLK)	TRACE_CLK	0xFFFFEABC	0	O	Output Disabled	Pull Down
		GPIO_47		1	IO		
		DMM_CLK		2	I		
U4	DMM_SYNC	TRACE_CTL	0xFFFFEAC0	0	O	Output Disabled	Pull Down
		DMM_SYNC		2	I		
V13	MCU_CLKOUT	GPIO_25	0xFFFFEA60	0	IO	Output Disabled	Pull Down
		MCU_CLKOUT		1	O		
		CHIRP_START		2	O		
		CHIRP_END		6	O		
		FRAME_START		7	O		
		EPWM1A		12	O		
U14	NERROR_IN	NERROR_IN	0xFFFFEA44	0	I	Input	
U15	NERROR_OUT	NERROR_OUT	0xFFFFEA4C	0	O	Hi-Z (Open Drain)	

表 6-1. Pin Attributes (ALP180A Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
V10	PMIC_CLKOUT	SOP[2]	0xFFFFEA68	During Power Up	I	Output Disabled	Pull Down
		GPIO_27		0	IO		
		PMIC_CLKOUT		1	O		
		CHIRP_START		6	O		
		CHIRP_END		7	O		
		FRAME_START		8	O		
		EPWM1B		11	O		
		EPWM2A		12	O		
H3	QSPI[0]	GPIO_8	0xFFFFEA2C	0	IO	Output Disabled	Pull Down
		QSPI[0]		1	IO		
		SPIB_MISO		2	IO		
G2	QSPI[1]	GPIO_9	0xFFFFEA30	0	IO	Output Disabled	Pull Down
		QSPI[1]		1	I		
		SPIB_MOSI		2	IO		
		SPIB_CS_N_2		8	IO		
J3	QSPI[2]	GPIO_10	0xFFFFEA34	0	IO	Output Disabled	Pull Down
		QSPI[2]		1	I		
		CAN_FD_TX		8	O		
K2	QSPI[3]	GPIO_11	0xFFFFEA38	0	IO	Output Disabled	Pull Down
		QSPI[3]		1	I		
		CAN_FD_RX		8	I		
H2	QSPI_CLK	GPIO_7	0xFFFFEA3C	0	IO	Output Disabled	Pull Down
		QSPI_CLK		1	O		
		SPIB_CLK		2	IO		
		DSS_UART_TX		6	O		
J2	QSPI_CS_N	GPIO_6	0xFFFFEA40	0	IO	Output Disabled	Pull Up
		QSPI_CS_N		1	O		
		SPIB_CS_N		2	IO		
V16	RS232_RX	GPIO_15	0xFFFFEA74	0	IO	Input Enabled	Pull Up
		RS232_RX		1	I		
		MSS_UARTA_RX		2	I		
		BSS_UART_TX		6	IO		
		MSS_UARTB_RX		7	IO		
		CAN_FD_RX		8	I		
		I2C_SCL		9	IO		
		EPWM2A		10	O		
		EPWM2B		11	O		
		EPWM3A		12	O		

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表 6-1. Pin Attributes (ALP180A Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
U16	RS232_TX	GPIO_14	0xFFFFEA78	0	IO	Output Enabled	
		RS232_TX		1	O		
		MSS_UARTA_TX		5	IO		
		MSS_UARTB_TX		6	IO		
		BSS_UART_TX		7	IO		
		CAN_FD_TX		10	O		
		I2C_SDA		11	IO		
		EPWM1A		12	O		
		EPWM1B		13	O		
		NDMM_EN		14	I		
		EPWM2A		15	O		
D2	SPIA_CLK	GPIO_3	0xFFFFEA14	0	IO	Output Disabled	Pull Up
		SPIA_CLK		1	IO		
		CAN_FD_RX		6	I		
		DSS_UART_TX		7	O		
C2	SPIA_CS_N	GPIO_30	0xFFFFEA18	0	IO	Output Disabled	Pull Up
		SPIA_CS_N		1	IO		
		CAN_FD_TX		6	O		
D1	SPIA_MISO	GPIO_20	0xFFFFEA10	0	IO	Output Disabled	Pull Up
		SPIA_MISO		1	IO		
		CAN_FD_TX		2	O		
F2	SPIA_MOSI	GPIO_19	0xFFFFEA0C	0	IO	Output Disabled	Pull Up
		SPIA_MOSI		1	IO		
		CAN_FD_RX		2	I		
		DSS_UART_TX		8	O		
E2	SPIB_CLK	GPIO_5	0xFFFFEA24	0	IO	Output Disabled	Pull Up
		SPIB_CLK		1	IO		
		MSS_UARTA_RX		2	I		
		MSS_UARTB_TX		6	O		
		BSS_UART_TX		7	O		
		CAN_FD_RX		8	I		
D3	SPIB_CS_N	GPIO_4	0xFFFFEA28	0	IO	Output Disabled	Pull Up
		SPIB_CS_N		1	IO		
		MSS_UARTA_TX		2	O		
		MSS_UARTB_TX		6	O		
		BSS_UART_TX		7	IO		
		QSPI_CLK_EXT		8	I		
		CAN_FD_TX		9	O		

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表 6-1. Pin Attributes (ALP180A Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
G3	SPIB_MISO	GPIO_22	0xFFFFEA20	0	IO	Output Disabled	Pull Up
		SPIB_MISO		1	IO		
		I2C_SCL		2	IO		
		DSS_UART_TX		6	O		
G1	SPIB_MOSI	GPIO_21	0xFFFFEA1C	0	IO	Output Disabled	Pull Up
		SPIB_MOSI		1	IO		
		I2C_SDA		2	IO		
B2	SPI_HOST_INTR	GPIO_12	0xFFFFEA00	0	IO	Output Disabled	Pull Down
		SPI_HOST_INTR		1	O		
		ADC_VALID		2	O		
		SPIB_CS_N_1		6	IO		
U12	SYNC_IN	GPIO_28	0xFFFFEA6C	0	IO	Output Disabled	Pull Down
		SYNC_IN		1	I		
		MSS_UARTB_RX		6	IO		
		DMM_MUX_IN		7	I		
		SYNC_OUT		9	O		
M3	SYNC_OUT	SOP[1]	0xFFFFEA70	During Power Up	I	Output Disabled	Pull Down
		GPIO_29		0	IO		
		SYNC_OUT		1	O		
		DMM_MUX_IN		9	I		
		SPIB_CS_N_1		10	IO		
		SPIB_CS_N_2		11	IO		
T3	TCK	GPIO_17	0xFFFFEA50	0	IO	Input Enabled	Pull Down
		TCK		1	I		
		MSS_UARTB_TX		2	O		
		CAN_FD_TX		8	O		
U9	TDI	GPIO_23	0xFFFFEA58	0	IO	Input Enabled	Pull Up
		TDI		1	I		
		MSS_UARTA_RX		2	I		
U10	TDO	SOP[0]	0xFFFFEA5C	During Power Up	I	Output Enabled	
		GPIO_24		0	IO		
		TDO		1	O		
		MSS_UARTA_TX		2	O		
		MSS_UARTB_TX		6	O		
		BSS_UART_TX		7	O		
		NDMM_EN		9	I		

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表 6-1. Pin Attributes (ALP180A Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
U8	TMS	GPIO_18	0xFFFFEA54	0	IO	Input Enabled	Pull Down
		TMS		1	I		
		BSS_UART_TX		2	O		
		CAN_FD_RX		6	I		
U13	WARM_RESET	WARM_RESET	0xFFFFEA48	0	IO	Hi-Z Input (Open Drain)	
R2	LVDS_CLKM	LVDS_CLKM			O		
R1	LVDS_CLKP	LVDS_CLKP			O		
N2	LVDS_TXP[0]	LVDS_TXP[0]			O		
N1	LVDS_TXM[0]	LVDS_TXM[0]			O		
P2	LVDS_TXP[1]	LVDS_TXP[1]			O		
P1	LVDS_TXM[1]	LVDS_TXM[1]			O		
T1	LVDS_FRCLKP	LVDS_FRCLKP			O		
T2	LVDS_FRCLKM	LVDS_FRCLKM			O		
U11	NRESET	NRESET			I		
A7	CLKP	CLKP			I		
B7	CLKM	CLKM			I		
A14	OSC_CLKOUT	OSC_CLKOUT			O		
A16	VBGAP	VBGAP			O		
E1	VDDIN	VDDIN			PWR		
J1	VDDIN	VDDIN			PWR		
V4	VDDIN	VDDIN			PWR		
V8	VDDIN	VDDIN			PWR		
V15	VDDIN	VDDIN			PWR		
A5	VIN_SRAM	VIN_SRAM			PWR		
V6	VIN_SRAM	VIN_SRAM			PWR		
V12	VIN_SRAM	VIN_SRAM			PWR		
C1	VNWA	VNWA			PWR		
V7	VNWA	VNWA			PWR		
V14	VNWA	VNWA			PWR		
H1	VIOIN	VIOIN			PWR		
V9	VIOIN	VIOIN			PWR		
B1	VIOIN_18	VIOIN_18			PWR		
F1	VIOIN_18	VIOIN_18			PWR		
K1	VIOIN_18	VIOIN_18			PWR		
V11	VIOIN_18	VIOIN_18			PWR		
C15	VIN_18CLK	VIN_18CLK			PWR		
C18	VIN_18CLK	VIN_18CLK			PWR		
U2	VIOIN_18DIFF	VIOIN_18DIFF			PWR		

表 6-1. Pin Attributes (ALP180A Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
V2	VPP	VPP			PWR		
J16	VIN_13RF1	VIN_13RF1			PWR		
J17	VIN_13RF1	VIN_13RF1			PWR		
J18	VIN_13RF1	VIN_13RF1			PWR		
H16	VIN_13RF2	VIN_13RF2			PWR		
H17	VIN_13RF2	VIN_13RF2			PWR		
H18	VIN_13RF2	VIN_13RF2			PWR		
M16	VIN_18BB	VIN_18BB			PWR		
M17	VIN_18BB	VIN_18BB			PWR		
M18	VIN_18BB	VIN_18BB			PWR		
A12	VIN_18VCO	VIN_18VCO			PWR		
C11	VIN_18VCO	VIN_18VCO			PWR		
A1	VSS	VSS			GND		
A2	VSS	VSS			GND		
E3	VSS	VSS			GND		
F3	VSS	VSS			GND		
N3	VSS	VSS			GND		
P3	VSS	VSS			GND		
R3	VSS	VSS			GND		
T4	VSS	VSS			GND		
T5	VSS	VSS			GND		
T6	VSS	VSS			GND		
T7	VSS	VSS			GND		
T8	VSS	VSS			GND		
T9	VSS	VSS			GND		
T10	VSS	VSS			GND		
T11	VSS	VSS			GND		
T12	VSS	VSS			GND		
T13	VSS	VSS			GND		
T14	VSS	VSS			GND		
T15	VSS	VSS			GND		
T16	VSS	VSS			GND		
U1	VSS	VSS			GND		
V1	VSS	VSS			GND		
A6	VSSA	VSSA			GND		
A8	VSSA	VSSA			GND		
A11	VSSA	VSSA			GND		
A13	VSSA	VSSA			GND		
A15	VSSA	VSSA			GND		

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表 6-1. Pin Attributes (ALP180A Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
A17	VSSA	VSSA			GND		
A18	VSSA	VSSA			GND		
B6	VSSA	VSSA			GND		
B8	VSSA	VSSA			GND		
B9	VSSA	VSSA			GND		
B10	VSSA	VSSA			GND		
B11	VSSA	VSSA			GND		
B12	VSSA	VSSA			GND		
B13	VSSA	VSSA			GND		
B14	VSSA	VSSA			GND		
B15	VSSA	VSSA			GND		
B16	VSSA	VSSA			GND		
B17	VSSA	VSSA			GND		
B18	VSSA	VSSA			GND		
C6	VSSA	VSSA			GND		
C7	VSSA	VSSA			GND		
C8	VSSA	VSSA			GND		
C12	VSSA	VSSA			GND		
C13	VSSA	VSSA			GND		
C14	VSSA	VSSA			GND		
C16	VSSA	VSSA			GND		
C17	VSSA	VSSA			GND		
D16	VSSA	VSSA			GND		
D17	VSSA	VSSA			GND		
D18	VSSA	VSSA			GND		
E16	VSSA	VSSA			GND		
E17	VSSA	VSSA			GND		
E18	VSSA	VSSA			GND		
F16	VSSA	VSSA			GND		
F17	VSSA	VSSA			GND		
F18	VSSA	VSSA			GND		
K16	VSSA	VSSA			GND		
K17	VSSA	VSSA			GND		
K18	VSSA	VSSA			GND		
L16	VSSA	VSSA			GND		
L17	VSSA	VSSA			GND		
L18	VSSA	VSSA			GND		
N16	VSSA	VSSA			GND		
N17	VSSA	VSSA			GND		

表 6-1. Pin Attributes (ALP180A Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5] [9]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
N18	VSSA	VSSA			GND		
P16	VSSA	VSSA			GND		
R16	VSSA	VSSA			GND		
R17	VSSA	VSSA			GND		
T17	VSSA	VSSA			GND		
U17	VSSA	VSSA			GND		
U18	VSSA	VSSA			GND		
V17	VSSA	VSSA			GND		
V18	VSSA	VSSA			GND		
A10	VOUT_14APLL	VOUT_14APLL			O		
A9	VOUT_14SYNTH	VOUT_14SYNTH			O		
G16	VOUT_PA	VOUT_PA			IO		
G17	VOUT_PA	VOUT_PA			IO		
G18	VOUT_PA	VOUT_PA			IO		
P18	Analog Test1 / GPADC1	Analog Test1 / GPADC1			IO		
P17	Analog Test2 / GPADC2	Analog Test2 / GPADC2			IO		
R18	Analog Test3 / GPADC3	Analog Test3 / GPADC3			IO		
T18	Analog Test4 / GPADC4	Analog Test4 / GPADC4			IO		
C9	ANAMUX / GPADC5	ANAMUX / GPADC5			IO		
C10	VSENSE / GPADC6	VSENSE / GPADC6			IO		

The following list describes the table column headers:

1. **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 1).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 1).
4. **PINCNTL ADDRESS:** MSS Address for PinMux Control
5. **MODE:** Multiplexing mode number: value written to PinMux Cntl register to select specific Signal name for this Ball number. Mode column has bit range value.
6. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - IO = Input or Output
7. **BALL RESET STATE:** The state of the terminal after supplies are stable after power-on-reset (NRESET) is asserted
8. **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
   - Pull Up: Internal pullup
   - Pull Down: Internal pulldown

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- An empty box means No pull.

9. Pin Mux Control Value maps to lower 4 bits of register.

IO MUX registers are available in the MSS memory map and the respective mapping to device pins is as follows:

表 6-2. PAD IO Control Registers

Default Pin/Ball Name	Package Ball /Pin (Address)	Pin Mux Config Register
SPI_HOST_INTR	B2	0xFFFFEA00
GPIO_0	M2	0xFFFFEA04
GPIO_1	L3	0xFFFFEA08
SPIA_MOSI	F2	0xFFFFEA0C
SPIA_MISO	D1	0xFFFFEA10
SPIA_CLK	D2	0xFFFFEA14
SPIA_CS_N	C2	0xFFFFEA18
SPIB_MOSI	G1	0xFFFFEA1C
SPIB_MISO	G3	0xFFFFEA20
SPIB_CLK	E2	0xFFFFEA24
SPIB_CS_N	D3	0xFFFFEA28
QSPI[0]	H3	0xFFFFEA2C
QSPI[1]	G2	0xFFFFEA30
QSPI[2]	J3	0xFFFFEA34
QSPI[3]	K2	0xFFFFEA38
QSPI_CLK	H2	0xFFFFEA3C
QSPI_CS_N	J2	0xFFFFEA40
NERROR_IN	U14	0xFFFFEA44
WARM_RESET	U13	0xFFFFEA48
NERROR_OUT	U15	0xFFFFEA4C
TCK	T3	0xFFFFEA50
TMS	U8	0xFFFFEA54
TDI	U9	0xFFFFEA58
TDO	U10	0xFFFFEA5C
MCU_CLKOUT	V13	0xFFFFEA60
GPIO_2	K3	0xFFFFEA64
PMIC_CLKOUT	V10	0xFFFFEA68
SYNC_IN	U12	0xFFFFEA6C

表 6-2. PAD IO Control Registers (continued)

Default Pin/Ball Name	Package Ball /Pin (Address)	Pin Mux Config Register
SYNC_OUT	M3	0xFFFFEA70
RS232_RX	V16	0xFFFFEA74
RS232_TX	U16	0xFFFFEA78
GPIO_31	U7	0xFFFFEA7C
GPIO_32	U6	0xFFFFEA80
GPIO_33	V5	0xFFFFEA84
GPIO_34	U5	0xFFFFEA88
GPIO_35	V3	0xFFFFEA8C
GPIO_36	M1	0xFFFFEA90
GPIO_37	L2	0xFFFFEA94
GPIO_38	L1	0xFFFFEA98
GPIO_39	C3	0xFFFFEA9C
GPIO_40	B3	0xFFFFEAA0
GPIO_41	C4	0xFFFFEAA4
GPIO_42	A3	0xFFFFEAA8
GPIO_43	B4	0xFFFFEAAC
GPIO_44	A4	0xFFFFEAB0
GPIO_45	C5	0xFFFFEAB4
GPIO_46	B5	0xFFFFEAB8
GPIO_47	U3	0xFFFFEABC
DMM_SYNC	U4	0xFFFFEAC0

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The register layout is as follows:

表 6-3. PAD IO Register Bit Descriptions

BIT	FIELD	TYPE	RESET (POWER ON DEFAULT)	DESCRIPTION
31-11	NU	RW	0	Reserved
10	SC	RW	0	IO slew rate control: 0 = Higher slew rate 1 = Lower slew rate
9	PUPDSEL	RW	0	Pullup/PullDown Selection 0 = Pull Down 1 = Pull Up (This field is valid only if Pull Inhibit is set as '0')
8	PI	RW	0	Pull Inhibit/Pull Disable 0 = Enable 1 = Disable
7	OE_OVERRIDE	RW	1	Output Override
6	OE_OVERRIDE_CTRL	RW	1	Output Override Control: (A '1' here overrides any o/p manipulation of this IO by any of the peripheral block hardware it is associated with for example a SPI Chip select)
5	IE_OVERRIDE	RW	0	Input Override
4	IE_OVERRIDE_CTRL	RW	0	Input Override Control: (A '1' here overrides any i/p value on this IO with a desired value)
3-0	FUNC_SEL	RW	1	Function select for Pin Multiplexing (Refer to the Pin Mux Sheet)

6.3 Signal Descriptions

Note

All IO pins of the device (except NERROR IN, NERROR_OUT, and WARM_RESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

Note

The GPIO state during the power supply ramp is not ensured. In case the GPIO is used in the application where the state of the GPIO is critical, even when NRESET is low , a tri-state buffer should be used to isolate the GPIO output from the radar device and a pull resister used to define the required state in the application. The NRESET signal to the radar device could be used to control the output enable (OE) of the tri-state buffer.

6.3.1 Pin Functions - Digital and Analog [ALP Package]

表 6-4 lists the pins by function and describes that function.

表 6-4. Pin Functions - Digital and Analog [ALP Package]

NAME	I/O	DESCRIPTION	NO.
DIGITAL			
BSS_UART_TX	O	Debug UART Transmit [Radar Block]	D3, E2, K3, L2, U8, U10, U16, V16
CAN_FD_RX	I	CAN FD (MCAN) Receive Signal	A4, B3, D2, E2, F2, K2, U8, V16
CAN_FD_TX	O	CAN FD (MCAN) Transmit Signal	B4, C2, C3, D1, D3, J3, T3, U16
DMM0	I	Debug Interface (Hardware In Loop) - Data Line	U7
DMM1	I	Debug Interface (Hardware In Loop) - Data Line	U6
DMM2	I	Debug Interface (Hardware In Loop) - Data Line	V5
DMM3	I	Debug Interface (Hardware In Loop) - Data Line	U5
DMM4	I	Debug Interface (Hardware In Loop) - Data Line	V3
DMM5	I	Debug Interface (Hardware In Loop) - Data Line	M1
DMM6	I	Debug Interface (Hardware In Loop) - Data Line	L2
DMM7	I	Debug Interface (Hardware In Loop) - Data Line	L1
DMM8	I	Debug Interface (Hardware In Loop) - Data Line	C3
DMM9	I	Debug Interface (Hardware In Loop) - Data Line	B3
DMM10	I	Debug Interface (Hardware In Loop) - Data Line	C4
DMM11	I	Debug Interface (Hardware In Loop) - Data Line	A3
DMM12	I	Debug Interface (Hardware In Loop) - Data Line	B4
DMM13	I	Debug Interface (Hardware In Loop) - Data Line	A4
DMM14	I	Debug Interface (Hardware In Loop) - Data Line	C5
DMM15	I	Debug Interface (Hardware In Loop) - Data Line	B5
DMM_CLK	I	Debug Interface (Hardware In Loop) - Clock	U3
DMM_MUX_IN	I	Debug Interface (Hardware In Loop) Mux Select between DMM1 and DMM2 (Two Instances)	L3, M3, U12
DMM_SYNC	I	Debug Interface (Hardware In Loop) - Sync	U4
DSS_UART_TX	O	Debug UART Transmit [DSP]	D2, F2, G3, H2, L1

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表 6-4. Pin Functions - Digital and Analog [ALP Package] (continued)

NAME	I/O	DESCRIPTION	NO.
EPWM1A	O	PWM Module 1 - Output A	B4, U16, V13
EPWM1B	O	PWM Module 1 - Output B	A4, M2, U16, V10
EPWM1SYNCI	I	PWM Module 1 - Sync Input	C3, L3
EPWM1SYNCO	I	PWM Module 1 - Sync Output	B3
EPWM2A	O	PWM Module 2- Output A	C5, M2, U16, V10, V16
EPWM2B	O	PWM Module 2 - Output B	B5, V16
EPWM2SYNCO	O	PWM Module 2 - Sync Output	V3
EPWM3A	O	PWM Module 3 - Output A	C4, V16
EPWM3B	O	PWM Module 3 - Output A	A3
EPWM3SYNCO	O	PWM Module 3 - Sync Output	U5
GPIO_0	IO	General-purpose I/O	M2
GPIO_1	IO	General-purpose I/O	L3
GPIO_2	IO	General-purpose I/O	K3
GPIO_3	IO	General-purpose I/O	D2
GPIO_4	IO	General-purpose I/O	D3
GPIO_5	IO	General-purpose I/O	E2
GPIO_6	IO	General-purpose I/O	J2
GPIO_7	IO	General-purpose I/O	H2
GPIO_8	IO	General-purpose I/O	H3
GPIO_9	IO	General-purpose I/O	G2
GPIO_10	IO	General-purpose I/O	J3
GPIO_11	IO	General-purpose I/O	K2
GPIO_12	IO	General-purpose I/O	B2
GPIO_13	IO	General-purpose I/O	M2
GPIO_14	IO	General-purpose I/O	U16
GPIO_15	IO	General-purpose I/O	V16
GPIO_16	IO	General-purpose I/O	L3
GPIO_17	IO	General-purpose I/O	T3
GPIO_18	IO	General-purpose I/O	U8
GPIO_19	IO	General-purpose I/O	F2
GPIO_20	IO	General-purpose I/O	D1
GPIO_21	IO	General-purpose I/O	G1
GPIO_22	IO	General-purpose I/O	G3
GPIO_23	IO	General-purpose I/O	U9
GPIO_24	IO	General-purpose I/O	U10
GPIO_25	IO	General-purpose I/O	V13
GPIO_26	IO	General-purpose I/O	K3
GPIO_27	IO	General-purpose I/O	V10
GPIO_28	IO	General-purpose I/O	U12
GPIO_29	IO	General-purpose I/O	M3
GPIO_30	IO	General-purpose I/O	C2, D2
GPIO_31	IO	General-purpose I/O	U7
GPIO_32	IO	General-purpose I/O	U6
GPIO_33	IO	General-purpose I/O	V5
GPIO_34	IO	General-purpose I/O	U5

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表 6-4. Pin Functions - Digital and Analog [ALP Package] (continued)

NAME	I/O	DESCRIPTION	NO.
GPIO_35	IO	General-purpose I/O	V3
GPIO_36	IO	General-purpose I/O	M1
GPIO_37	IO	General-purpose I/O	L2
GPIO_38	IO	General-purpose I/O	L1
GPIO_39	IO	General-purpose I/O	C3
GPIO_40	IO	General-purpose I/O	B3
GPIO_41	IO	General-purpose I/O	C4
GPIO_42	IO	General-purpose I/O	A3
GPIO_43	IO	General-purpose I/O	B4
GPIO_44	IO	General-purpose I/O	A4
GPIO_45	IO	General-purpose I/O	C5
GPIO_46	IO	General-purpose I/O	B5
GPIO_47	IO	General-purpose I/O	U3
I2C_SCL	IO	I2C Clock	G3, V16
I2C_SDA	IO	I2C Data	G1, U16
LVDS_TXP[0]	O	Differential data Out – Lane 0	N2
LVDS_TXM[0]	O	Differential data Out – Lane 0	N1
LVDS_TXP[1]	O	Differential data Out – Lane 1	P2
LVDS_TXM[1]	O	Differential data Out – Lane 1	P1
LVDS_CLKP	O	Differential clock Out	R1
LVDS_CLKM	O	Differential clock Out	R2
LVDS_FRCLKP	O	Differential Frame Clock	T1
LVDS_FRCLKM	O	Differential Frame Clock	T2
MCU_CLKOUT	O	Programmable clock given out to external MCU or the processor	V13
MSS_UARTA_RX	I	Master Subsystem - UART A Receive	E2, U9, V16
MSS_UARTA_TX	O	Master Subsystem - UART A Transmit	D3, U7, U10, U16
MSS_UARTB_RX	IO	Master Subsystem - UART B Receive	U12, V16
MSS_UARTB_TX	O	Master Subsystem - UART B Transmit	D3, E2, K3, M1, T3, U10, U16
NDMM_EN	I	Debug Interface (Hardware In Loop) Enable - Active Low Signal	U10, U16
NERROR_IN	I	Failsafe input to the device. Nerror output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by Firmware	U14
NERROR_OUT	O	Open drain fail safe output signal. Connected to PMIC/ Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.	U15
PMIC_CLKOUT	O	Output Clock from AWR6843AOP device for PMIC	K3, M2, V10
QSPI[0]	IO	QSPI Data Line #0 (Used with Serial Data Flash)	H3
QSPI[1]	I	QSPI Data Line #1 (Used with Serial Data Flash)	G2
QSPI[2]	I	QSPI Data Line #2 (Used with Serial Data Flash)	J3
QSPI[3]	I	QSPI Data Line #3 (Used with Serial Data Flash)	K2
QSPI_CLK	O	QSPI Clock (Used with Serial Data Flash)	H2
QSPI_CLK_EXT	I	QSPI Clock (Used with Serial Data Flash)	D3
QSPI_CS_N	O	QSPI Chip Select (Used with Serial Data Flash)	J2
RS232_RX	I	Debug UART (Operates as Bus Master) - Receive Signal	V16
RS232_TX	O	Debug UART (Operates as Bus Master) - Transmit Signal	U16
SOP[0]	I	Sense On Power - Line#0	U10

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表 6-4. Pin Functions - Digital and Analog [ALP Package] (continued)

NAME	I/O	DESCRIPTION	NO.
SOP[1]	I	Sense On Power - Line#1	M3
SOP[2]	I	Sense On Power - Line#2	V10
SPIA_CLK	IO	SPI Channel A - Clock	D2
SPIA_CS_N	IO	SPI Channel A - Chip Select	C2
SPIA_MISO	IO	SPI Channel A - Master In Slave Out	D1
SPIA_MOSI	IO	SPI Channel A - Master Out Slave In	F2
SPIB_CLK	IO	SPI Channel B - Clock	E2, H2
SPIB_CS_N	IO	SPI Channel B Chip Select (Instance ID 0)	D3, J2
SPIB_CS_N_1	IO	SPI Channel B Chip Select (Instance ID 1)	B2, L3, M3
SPIB_CS_N_2	IO	SPI Channel B Chip Select (Instance ID 2)	G2, L3, M3
SPIB_MISO	IO	SPI Channel B - Master In Slave Out	G3, H3
SPIB_MOSI	IO	SPI Channel B - Master Out Slave In	G1, G2
SPI_HOST_INTR	O	Out of Band Interrupt to an external host communicating over SPI	B2
SYNC_IN	I	Low frequency Synchronization signal input	U12
SYNC_OUT	O	Low Frequency Synchronization Signal output	K3, L3, M3, U12
TCK	I	JTAG Test Clock	T3
TDI	I	JTAG Test Data Input	U9
TDO	O	JTAG Test Data Output	U10
TMS	I	JTAG Test Mode Signal	U8
TRACE_CLK	O	Debug Trace Output - Clock	U3
TRACE_CTL	O	Debug Trace Output - Control	U4
TRACE_DATA_0	O	Debug Trace Output - Data Line	U7
TRACE_DATA_1	O	Debug Trace Output - Data Line	U6
TRACE_DATA_2	O	Debug Trace Output - Data Line	V5
TRACE_DATA_3	O	Debug Trace Output - Data Line	U5
TRACE_DATA_4	O	Debug Trace Output - Data Line	V3
TRACE_DATA_5	O	Debug Trace Output - Data Line	M1
TRACE_DATA_6	O	Debug Trace Output - Data Line	L2
TRACE_DATA_7	O	Debug Trace Output - Data Line	L1
TRACE_DATA_8	O	Debug Trace Output - Data Line	C3
TRACE_DATA_9	O	Debug Trace Output - Data Line	B3
TRACE_DATA_10	O	Debug Trace Output - Data Line	C4
TRACE_DATA_11	O	Debug Trace Output - Data Line	A3
TRACE_DATA_12	O	Debug Trace Output - Data Line	B4
TRACE_DATA_13	O	Debug Trace Output - Data Line	A4
TRACE_DATA_14	O	Debug Trace Output - Data Line	C5
TRACE_DATA_15	O	Debug Trace Output - Data Line	B5
FRAME_START	O	Pulse signal indicating the start of each frame	K3, V10, V13
CHIRP_START	O	Pulse signal indicating the start of each chirp	K3, V10, V13
CHIRP_END	O	Pulse signal indicating the end of each chirp	K3, V10, V13
ADC_VALID	O	When high, indicating valid ADC samples	B2, L3, M2
WARM_RESET	IO	Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.	U13
ANALOG			
NRESET	I	Power on reset for chip. Active low	U11

表 6-4. Pin Functions - Digital and Analog [ALP Package] (continued)

NAME	I/O	DESCRIPTION	NO.
CLKP	I	In XTAL mode: Differential port for reference crystal In External clock mode: Single ended input reference clock port	A7
CLKM	I	In XTAL mode: Differential port for reference crystal In External clock mode: Connect this port to ground	B7
OSC_CLKOUT	O	Reference clock output from clocking sub system after cleanup PLL (1.4-V output voltage swing).	A14, K3
VBGAP	O	Device's Band Gap Reference Output	A16
VDDIN	Power	1.2V digital power supply	E1, J1, V4, V8, V15
VIN_SRAM	Power	1.2V power rail for internal SRAM	A5, V6, V12
VNWA	Power	1.2V power rail for SRAM array back bias	C1, V7, V14
VIOIN	Power	I/O Supply (3.3V or 1.8V): All CMOS I/Os would operate on this supply	H1, V9
VIOIN_18	Power	1.8V supply for CMOS IO	B1, F1, K1, V11
VIN_18CLK	Power	1.8V supply for clock module	C15, C18
VIOIN_18DIFF	Power	1.8V supply for LVDS port	U2
VPP	Power	Voltage supply for fuse chain	V2
VIN_13RF1	Power	1.3V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board	J16, J17, J18
VIN_13RF2	Power	1.3V Analog and RF supply	H16, H17, H18
VIN_18BB	Power	1.8V Analog base band power supply	M16, M17, M18
VIN_18VCO	Power	1.8V RF VCO supply	A12, C11
VSS	Ground	Digital ground	A1, A2, E3, F3, N3, P3, R3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, U1, V1, Y6
VSSA	Ground	Analog ground	A6, A8, A11, A13, A15, A17, A18, B6, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, C6, C7, C8, C12, C13, C14, C16, C17, D16, D17, D18, E16, E17, E18, F16, F17, F18, K16, K17, K18, L16, L17, L18, N16, N17, N18, P16, R16, R17, T17, U17, U18, V17, V18
VOUT_14APLL	O	Internal LDO output	A10
VOUT_14SYNTH	O	Internal LDO output	A9
VOUT_PA	IO	Internal LDO output	G16, G17, G18
Analog Test1 / GPADC1	IO	Analog IO dedicated for ADC service	P18
Analog Test2 / GPADC2	IO	Analog IO dedicated for ADC service	P17
Analog Test3 / GPADC3	IO	Analog IO dedicated for ADC service	R18
Analog Test4 / GPADC4	IO	Analog IO dedicated for ADC service	T18
ANAMUX / GPADC5	IO	Analog IO dedicated for ADC service	C9
VSENSE / GPADC6	IO	Analog IO dedicated for ADC service	C10

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7 Specifications

7.1 Absolute Maximum Ratings

PARAMETERS[1] [2]		MIN	MAX	UNIT
VDDIN	1.2 V digital power supply	–0.5	1.4	V
VIN_SRAM	1.2 V power rail for internal SRAM	–0.5	1.4	V
VNWA	1.2 V power rail for SRAM array back bias	–0.5	1.4	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	–0.5	3.8	V
VIOIN_18	1.8 V supply for CMOS IO	–0.5	2	V
VIN_18CLK	1.8 V supply for clock module	–0.5	2	V
VIOIN_18DIFF	1.8 V supply for LVDS port	–0.5	2	V
VIN_13RF1	1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board.	–0.5	1.45	V
VIN_13RF2				
VIN_13RF1	1-V Internal LDO bypass mode. Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	–0.5	1.4	V
VIN_13RF2				
VIN_18BB	1.8-V Analog baseband power supply	–0.5	2	V
VIN_18VCO supply	1.8-V RF VCO supply	–0.5	2	V
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input		VIOIN + 20% up to 20% of signal period	
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	125	°C
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±1000	V
		Charged-device model (CDM), per AEC Q100-011[2]	±250	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Corner pins are rated as ±750 V

7.3 Power-On Hours (POH)

JUNCTION TEMPERATURE (T_j) (1) (2)	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
–40°C	100% duty cycle	1.2	600 (6%)
75°C			2000 (20%)
95°C			6500 (65%)
125°C			900 (9%)

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) The specified POH are applicable with max Tx output power settings using the default firmware gain tables. The specified POH would not be applicable, if the Tx gain table is overwritten using an API.

7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDDIN	1.2 V digital power supply	1.14	1.2	1.32	V
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	3.15	3.3	3.45	V
		1.71	1.8	1.89	
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.9	V
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9	V
VIOIN_18DIFF	1.8 V supply for LVDS port	1.71	1.8	1.9	V
VIN_13RF1	1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board	1.23	1.3	1.36	V
VIN_13RF2					
VIN_13RF1 (1-V Internal LDO bypass mode)	Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	0.95	1	1.05	V
VIN_13RF2 (1-V Internal LDO bypass mode)					
VIN18BB	1.8-V Analog baseband power supply	1.71	1.8	1.9	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.9	V
V_{IH}	Voltage Input High (1.8 V mode)	1.17			V
	Voltage Input High (3.3 V mode)	2.25			
V_{IL}	Voltage Input Low (1.8 V mode)			0.3*VIOIN	V
	Voltage Input Low (3.3 V mode)			0.62	
V_{OH}	High-level output threshold (I_{OH} = 6 mA)	VIOIN – 450			mV
V_{OL}	Low-level output threshold (I_{OL} = 6 mA)			450	mV
NRESET SOP[2:0]	V_{IL} (1.8V Mode)			0.2	V
	V_{IH} (1.8V Mode)	0.96			
	V_{IL} (3.3V Mode)			0.3	
	V_{IH} (3.3V Mode)	1.57			

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7.5 Power Supply Specifications

表 7-1 describes the four rails from an external power supply block of the AWR1843AOP device.

表 7-1. Power Supply Rails Characteristics

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.3 V (or 1 V in internal LDO bypass mode)(1)	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM

(1) Three simultaneous transmitter operation is supported only in 1-V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin.

表 7-2. Ripple Specifications

FREQUENCY (kHz)	RF RAIL		VCO/IF RAIL
	1.0 V (INTERNAL LDO BYPASS) (μV_{RMS})	1.3 V (μV_{RMS})	1.8 V (μV_{RMS})
137.5	7	648	83
275	5	76	21
550	3	22	11
1100	2	4	6
2200	11	82	13
4400	13	93	19
6600	22	117	29

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7.6 Power Consumption Summary

表 7-3 and summarize the power consumption at the power terminals.

表 7-3. Maximum Current Ratings at Power Terminals

PARAMETER	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
Current consumption	VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			1000	mA
	VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3V or 1.0V rail (2TX, 4 RX simultaneously)(1)			2000	
	VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8V rail			850	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail			50	

(1) 3 Transmitters can simultaneously be deployed only in AWR1843AOP and AWR2243 devices with 1V / LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin. In this case the peak 1V supply current goes up to 2500 mA.

表 7-4. Average Power Consumption at Power Terminals

PARAMETER	CONDITION			DESCRIPTION	MIN	TYP	MAX	UNIT
Average power consumption	1.0-V internal LDO bypass mode	25% Duty Cycle	1TX, 4RX	Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 128 chirps, 128 samples/chirp, 8-µs interchirp time (25% duty cycle), DSP active		1.3		W
			2TX, 4RX			1.38		
		50% Duty Cycle	1TX, 4RX	Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 256 chirps, 128 samples/chirp, 8-µs interchirp time (50% duty cycle), DSP active		1.77		
			2TX, 4RX			1.92		
	1.3-V internal LDO enabled mode	25% Duty Cycle	1TX, 4RX	Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 128 chirps, 128 samples/chirp, 8-µs interchirp time (25% duty cycle), DSP active		1.4		
			2TX, 4RX			1.48		
		50% Duty Cycle	1TX, 4RX	Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 256 chirps, 128 samples/chirp, 8-µs interchirp time (50% duty cycle), DSP active		1.94		
			2TX, 4RX			2.14		

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7.7 RF Specification

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver	Equivalent isotropic noise figure(1)	76 to 77 GHz		10		dB
		77 to 81 GHz		10		
	IF bandwidth(2)				10	MHz
	A2D sampling rate (real)				25	Msps
	A2D sampling rate (complex 1x)				12.5	Msps
	A2D resolution			12		Bits
	Idle Channel Spurs			–90		dBFS
Transmitter	Single transmitter effective isotropic radiated power (EIRP)			16		dBm
Antenna	Antenna 6dB beamwidth			+/–60		deg
Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				100	MHz/µs
	Phase noise at 1-MHz offset	76 to 77 GHz		–95		dBc/Hz
		77 to 81 GHz		–93		

(1) Specification is quoted for complex 1x mode.
(2) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)

HPF1	HPF2
175, 235, 350, 700	350, 700, 1400, 2800

The filtering performed by the digital baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

7.8 CPU Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
DSP Subsystem (C674 Family)	Clock Speed		600		MHz
	L1 Code Memory		32		KB
	L1 Data Memory		32		KB
	L2 Memory		256		KB
Master Controller Subsystem (R4F Family)	Clock Speed		200		MHz
	Tightly Coupled Memory - A (Program)		512		KB
	Tightly Coupled Memory - B (Data)		192		KB
Shared Memory	Shared L3 Memory		1024		KB

7.9 Thermal Resistance Characteristics for FCBGA Package [ALP0180A]

THERMAL METRICS(1) (4)		°C/W(2) (3)
$R_{\Theta JC}$	Junction-to-case	2.6
$R_{\Theta JB}$	Junction-to-board	7.5
$R_{\Theta JA}$	Junction-to-free air	20.3
$R_{\Theta JMA}$	Junction-to-moving air	N/A(4)
Psi_{JT}	Junction-to-package top	0.9

THERMAL METRICS(1) (4)		°C/W(2) (3)
Psi_{JB}	Junction-to-board	7.3

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

A junction temperature of 125°C is assumed.
(4) N/A = not applicable

7.10 Timing and Switching Characteristics

7.10.1 Antenna Radiation Patterns

This section discusses transmitter and receiver antenna radiation patterns in both Azmiuth and Elevaton planes for a specified frequency.

7.10.1.1 Antenna Radiation Patterns for Receiver

图 7-1 shows typical antenna radiation patterns for the four receivers in both Azimuth and Elevation planes.

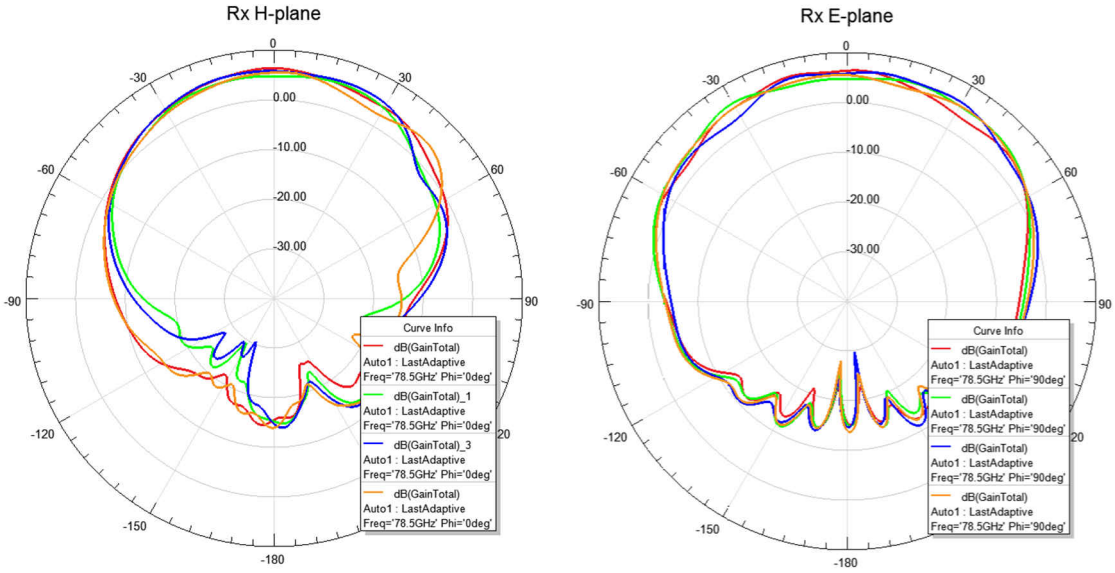

图 7-1. Receiver Antenna Radiation Pattern

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7.10.1.2 Antenna Radiation Patterns for Transmitter

图 7-2 shows typical antenna radiation patterns for the three transmitters in both Azimuth and Elevation planes.

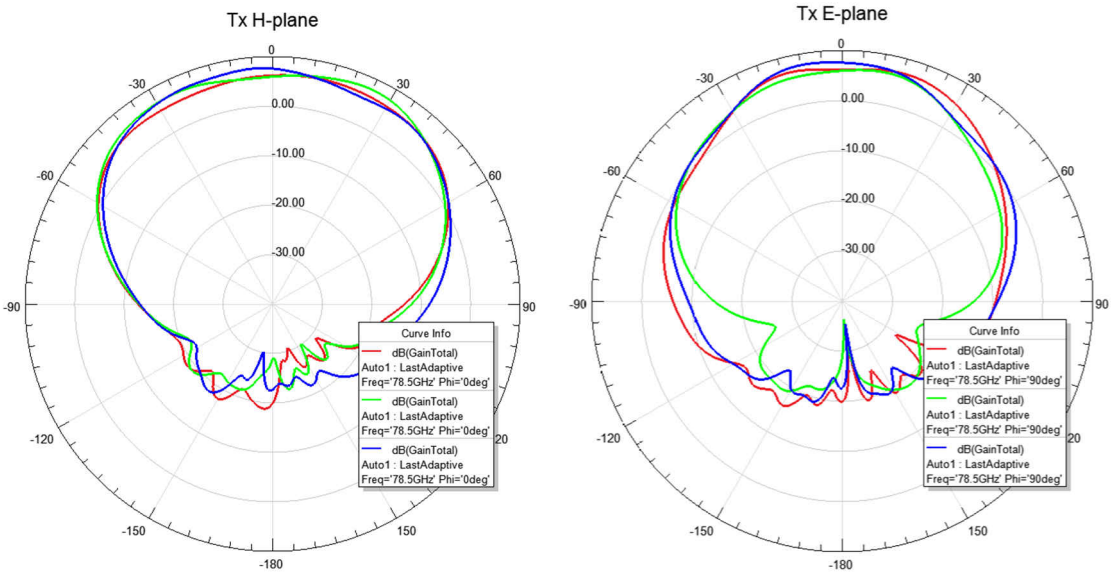


图 7-2. Transmitter Antenna Radiation Pattern

7.10.2 Antenna Positions

图 7-3 shows the placement and relative spacing of the antennas. Lambda corresponds to a frequency of 78.5 GHz.

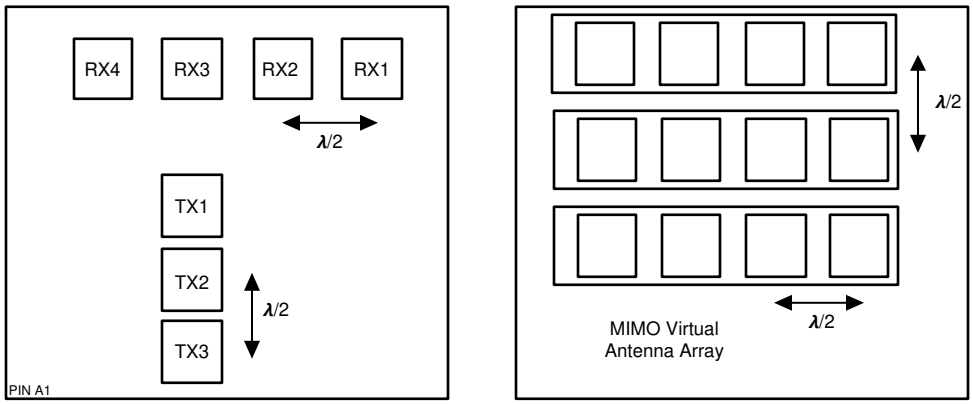
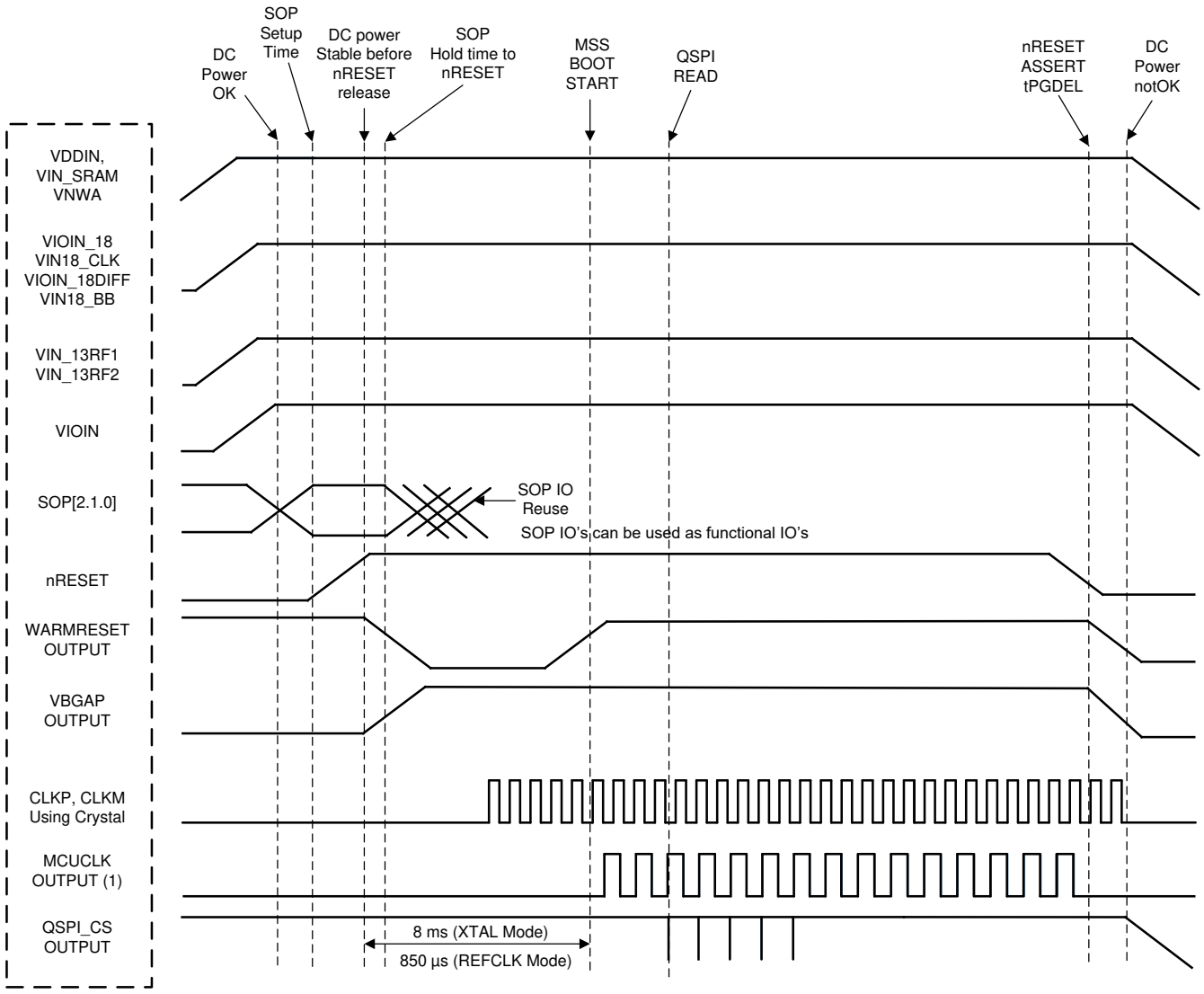


图 7-3. Antenna Positions (Placement and Relative Spacing)

7.10.3 Power Supply Sequencing and Reset Timing

The AWR1843AOP device expects all external voltage rails and SOP lines to be stable before reset is deasserted. 图 7-4 describes the device wake-up sequence.



A. MCU_CLK_OUT in autonomous mode, where AWR1843AOP application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

图 7-4. Device Wake-up Sequence

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7.10.4 Input Clocks and Oscillators

7.10.4.1 Clock Specifications

The AWR1843AOP requires external clock source (that is, a 40-MHz crystal or external clock) for initial boot and as a reference for an internal APLL hosted in the device. An external crystal is connected to the device pins. 图 7-5 shows the crystal implementation.

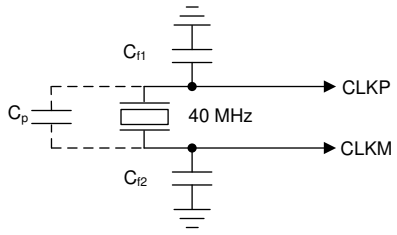

图 7-5. Crystal Implementation

Note

The load capacitors, C_{f1} and C_{f2} in 图 7-5, should be chosen such that 方程式 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

表 7-5 lists the electrical characteristics of the clock crystal.

表 7-5. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		150	°C
Frequency tolerance	Crystal frequency tolerance(1) (2)	–200		200	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

表 7-6. External Clock Mode Specifications

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40 MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	adc patmV (pp)
	Phase Noise at 1 kHz			– 132	dBc/Hz
	Phase Noise at 10 kHz			– 143	dBc/Hz
	Phase Noise at 100 kHz			– 152	dBc/Hz
	Phase Noise at 1 MHz			– 153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	– 50		50	ppm

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7.10.5 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

7.10.5.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Standard SPI and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

7.10.5.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

节 7.10.5.2.2 to SPI Master Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input) assume the operating conditions stated in 节 7.10.5.2.1.

7.10.5.2.1 SPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

7.10.5.2.2 SPI Master Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)

NO.(1) (2) (3)	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)	25		$256t_{c(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 3$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 3$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 10.5$			

NO.(1) (2) (3)	PARAMETER			MIN	TYP	MAX	UNIT
6(5)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	(C2TDELAY+2)* $t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	ns
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	(C2TDELAY+2)* $t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
7(5)	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	
8(4)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
9(4)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
(2) $t_{c(MSS\_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geqslant (PS+1)t_{c(MSS\_VCLK)} \geqslant 25ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS\_VCLK)} \geqslant 25ns$.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

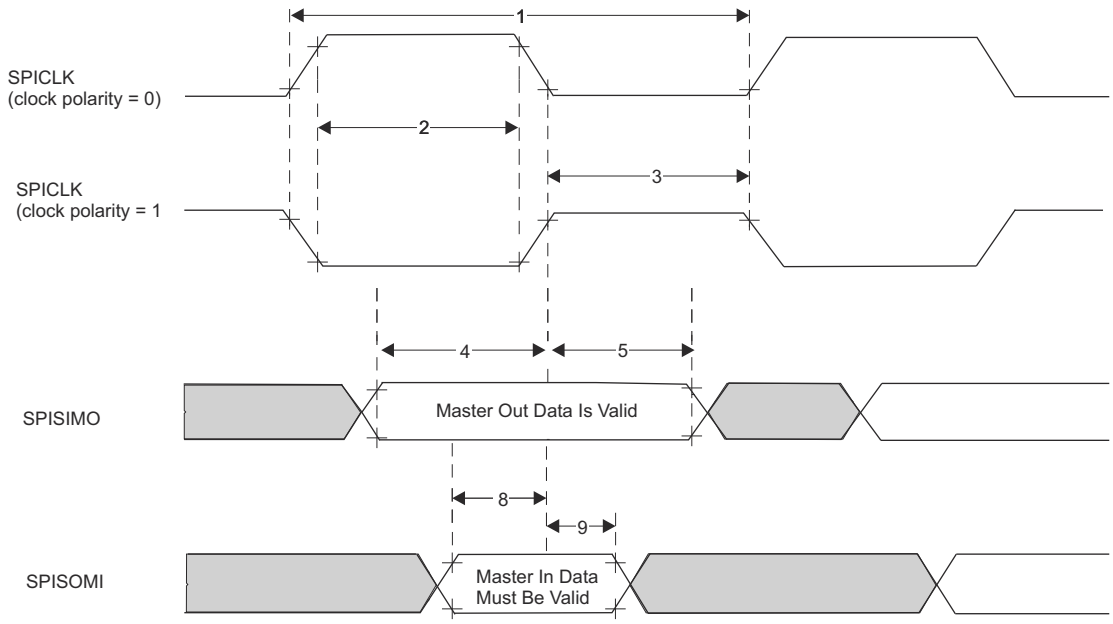

图 7-6. SPI Master Mode External Timing (CLOCK PHASE = 0)

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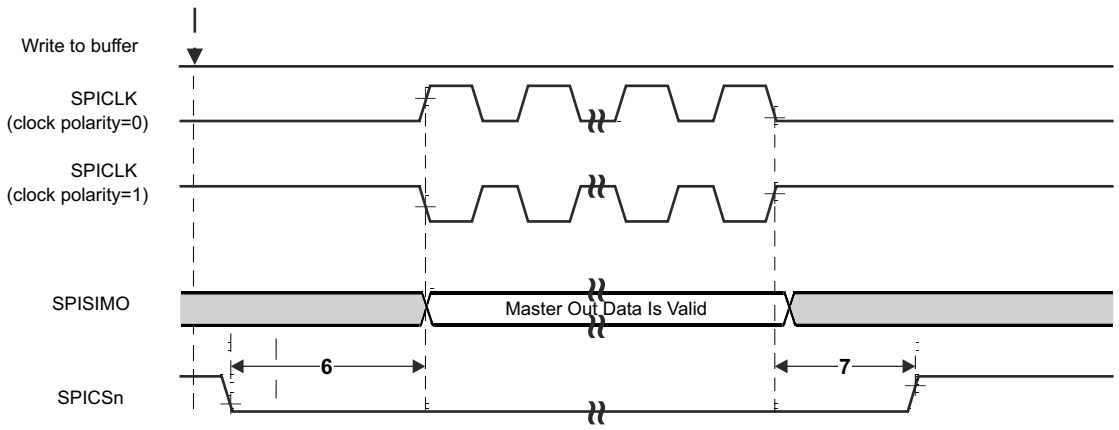

图 7-7. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

7.10.5.2.3 SPI Master Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)

NO.(1) (2) (3)	PARAMETER			MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		25		$256t_{c(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 3$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 3$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 10.5$			
6(5)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} + 7.5$	

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NO.(1) (2) (3)	PARAMETER		MIN	TYP	MAX	UNIT
7(5)	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)	(T2CDELAY + 1) *$t_{c(VCLK)}$ – 7.5		(T2CDELAY + 1) *$t_{c(VCLK)}$ + 7	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)	(T2CDELAY + 1) *$t_{c(VCLK)}$ – 7.5		(T2CDELAY + 1) *$t_{c(VCLK)}$ + 7	
8(4)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	5			
9(4)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
(2) $t_{c(MSS\_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geqslant (PS+1)t_{c(MSS\_VCLK)} \geqslant 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS\_VCLK)} \geqslant 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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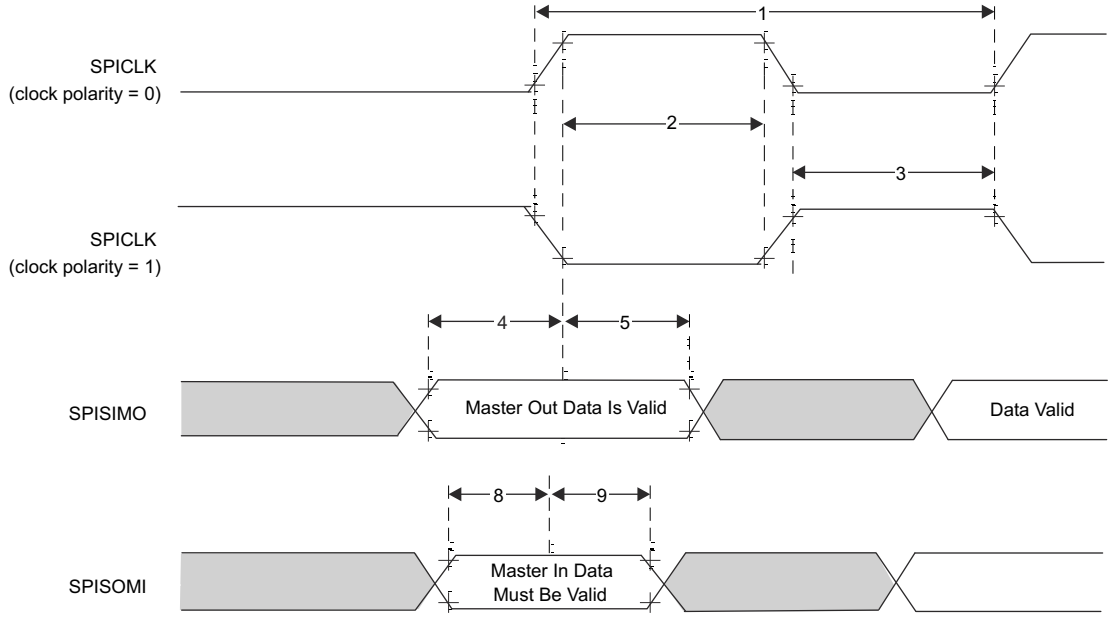

图 7-8. SPI Master Mode External Timing (CLOCK PHASE = 1)

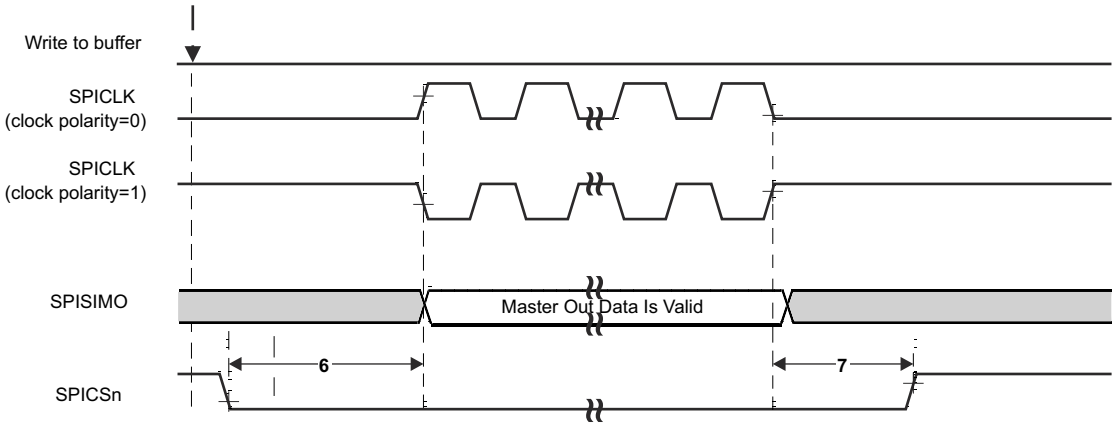

图 7-9. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

7.10.5.3 SPI Slave Mode I/O Timings

7.10.5.3.1 SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)

NO.(1) (2) (3)	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK(4)	25			ns
2(5)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	10			ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	10			
3(5)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	10			ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	10			
4(5)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)			10	
5(5)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	2			
4(5)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)			10	
5(5)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	2			
6(5)	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	3			ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	3			
7(5)	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	1			ns
	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	1			

(1) The MASTER bit (SPIGCRx.0) is cleared (where x = 0 or 1).
(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.
(3) $t_{c(MSS\_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(4) When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)S} \geqslant (PS+1)t_{c(MSS\_VCLK)} \geqslant 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0: $t_{c(SPC)S} = 2t_{c(MSS\_VCLK)} \geqslant 25$ ns.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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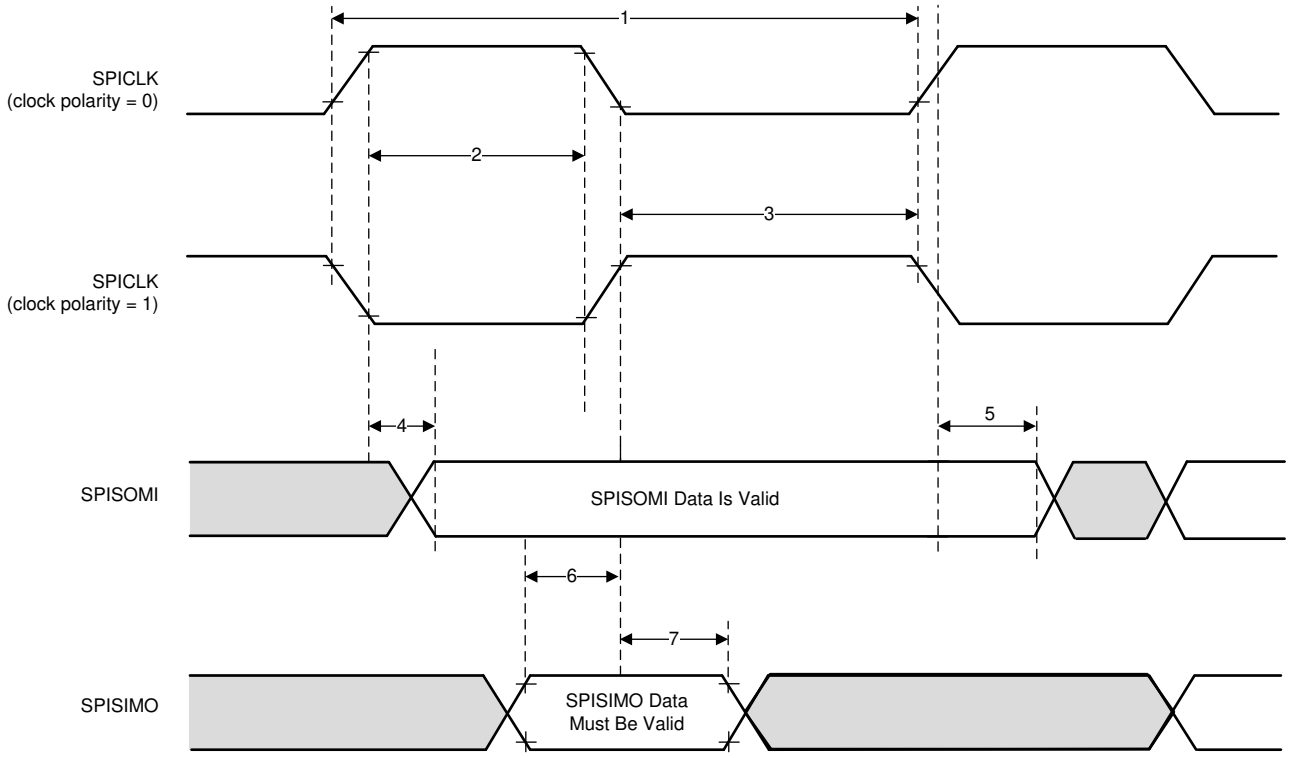

图 7-10. SPI Slave Mode External Timing (CLOCK PHASE = 0)

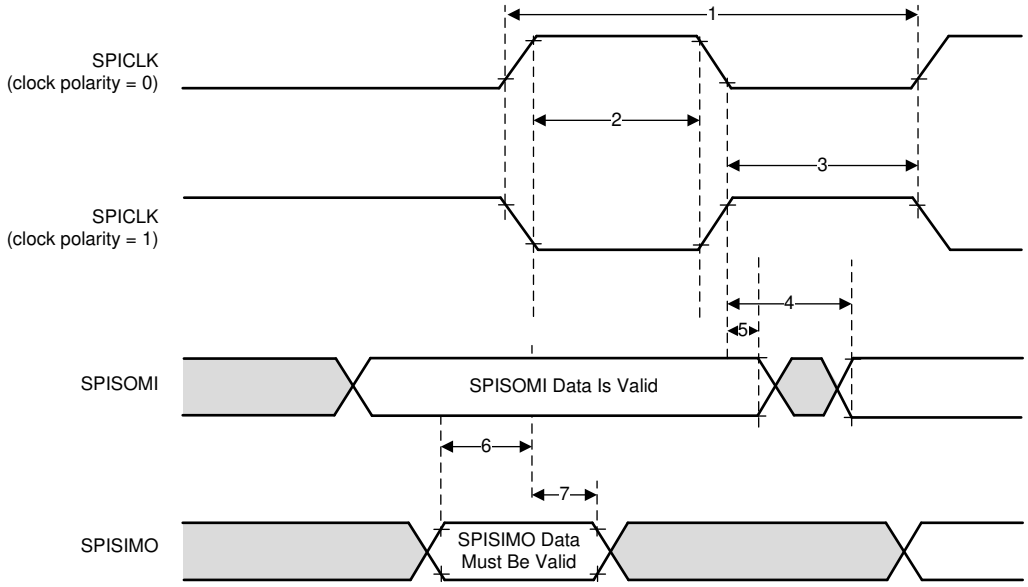

图 7-11. SPI Slave Mode External Timing (CLOCK PHASE = 1)

7.10.5.4 Typical Interface Protocol Diagram (Slave Mode)

1. Host should ensure that there is a delay of two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

图 7-12 shows the SPI communication timing of the typical interface protocol.

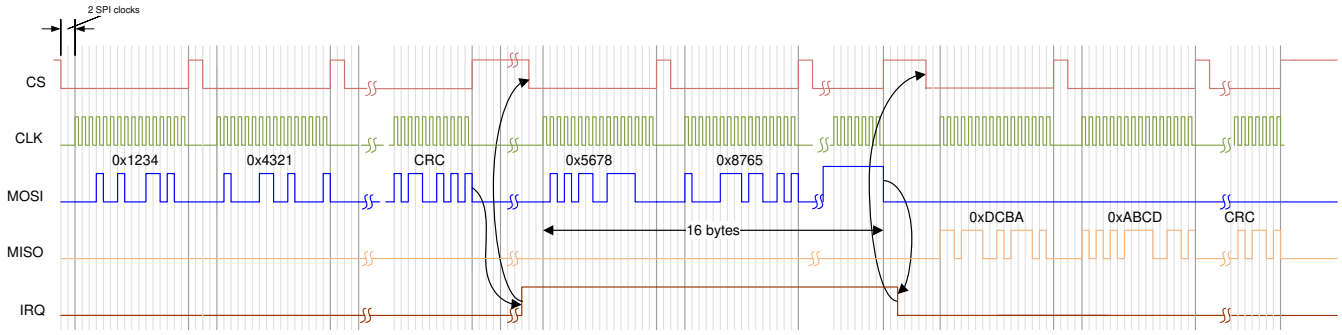

图 7-12. SPI Communication

7.10.6 LVDS Interface Configuration

The supported AWR1843AOP LVDS lane configuration is two Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) and one Frame clock lane (LVDS_FRCLKP/M). The LVDS interface is used for debugging. The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

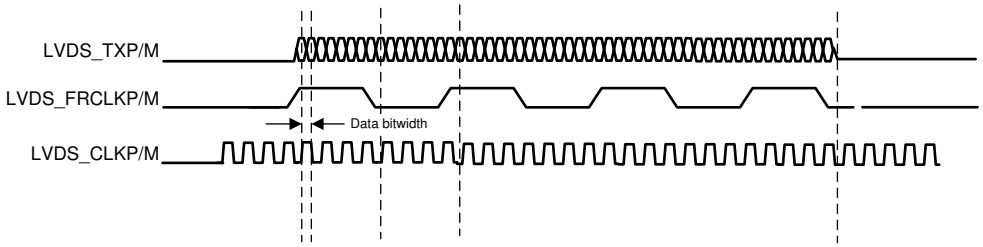

图 7-13. LVDS Interface Lane Configuration And Relative Timings

7.10.6.1 LVDS Interface Timings

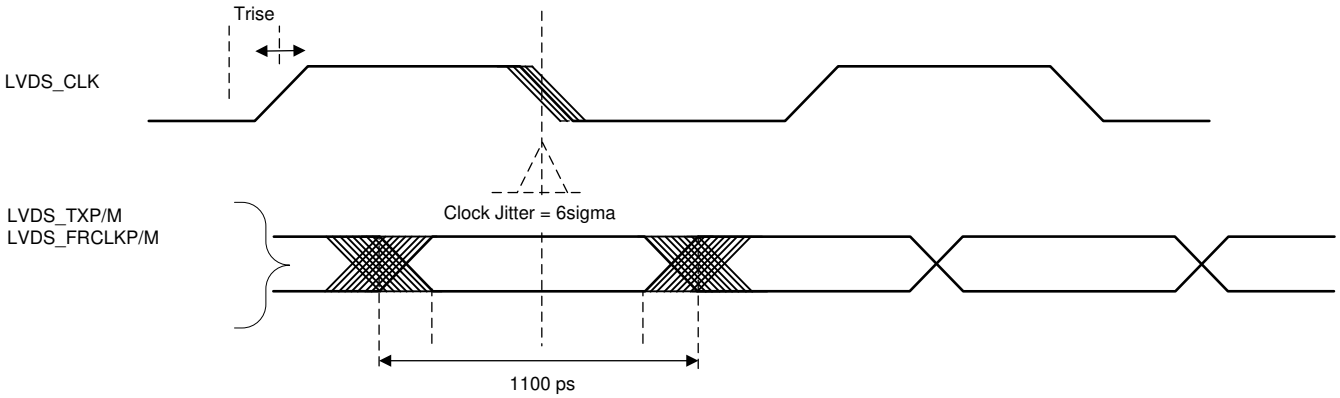

图 7-14. Timing Parameters

表 7-7. LVDS Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 Ω resistive load between differential pairs	250		450	mV
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps		330		ps
Jitter (pk-pk)	900 Mbps		80		ps

7.10.7 General-Purpose Input/Output

节 7.10.7.1 lists the switching characteristics of output timing relative to load capacitance.

7.10.7.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L)[(1) (2)]

PARAMETER		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.8	3.0	ns
			C_L = 50 pF	6.4	6.9	
			C_L = 75 pF	9.4	10.2	
t_f	Max fall time		C_L = 20 pF	2.8	2.8	ns
			C_L = 50 pF	6.4	6.6	
			C_L = 75 pF	9.4	9.8	
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.3	3.3	ns
			C_L = 50 pF	6.7	7.2	
			C_L = 75 pF	9.6	10.5	
t_f	Max fall time		C_L = 20 pF	3.1	3.1	ns
			C_L = 50 pF	6.6	6.6	
			C_L = 75 pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

ADVANCE INFORMATION

7.10.8 Controller Area Network Interface (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments that require reliable serial communication or multiplexed wiring.

The DCAN has the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbps
- Configurable Message objects
- Individual identifier masks for each message object
- Programmable FIFO mode for message objects
- Suspend mode for debug support
- Programmable loop-back modes for self-test operation
- Direct access to Message RAM in test mode
- Supports two interrupt lines - Level 0 and Level 1
- Automatic Message RAM initialization

7.10.8.1 Dynamic Characteristics for the DCANx TX and RX Pins

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CAN\_tx)}$	Delay time, transmit shift register to CAN_tx pin(1)			15	ns
$t_{d(CAN\_rx)}$	Delay time, CAN_rx pin to receive shift register(1)			10	ns

(1) These values do not include rise/fall times of the output buffer.

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7.10.9 Controller Area Network - Flexible Data-rate (CAN-FD)

The CAN-FD module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The CAN-FD has the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1
- Full CAN FD support (up to 64 data bytes per frame)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 11-bit filter elements
- Internal Loopback mode for self-test
- Mask-able interrupts, two interrupt lines
- Two clock domains (CAN clock / Host clock)
- Parity / ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Full Message Memory capacity (4352 words).

7.10.9.1 Dynamic Characteristics for the CANx TX and RX Pins

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CAN\_FD\_tx)}$	Delay time, transmit shift register to CAN_FD_tx pin(1)			15	ns
$t_{d(CAN\_FD\_rx)}$	Delay time, CAN_FD_rx pin to receive shift register(1)			10	ns

(1) These values do not include rise/fall times of the output buffer.

7.10.10 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Two external pins: RS232_RX and RS232_TX

7.10.10.1 SCI Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20 pF		921.6		kHz

7.10.11 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multimaster communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I^{2}C-bus™. This module will support any slave or master I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-master transmitter/ slave receiver mode
  - Multi-master receiver/ slave transmitter mode
  - Combined master transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

Note

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)

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7.10.11.1 I2C Timing Requirements(1)

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		µs
$t_{h(SCLL-SDA)}$	Hold time, SDA valid after SCL low	0	3.45(1)	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b (2) (3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

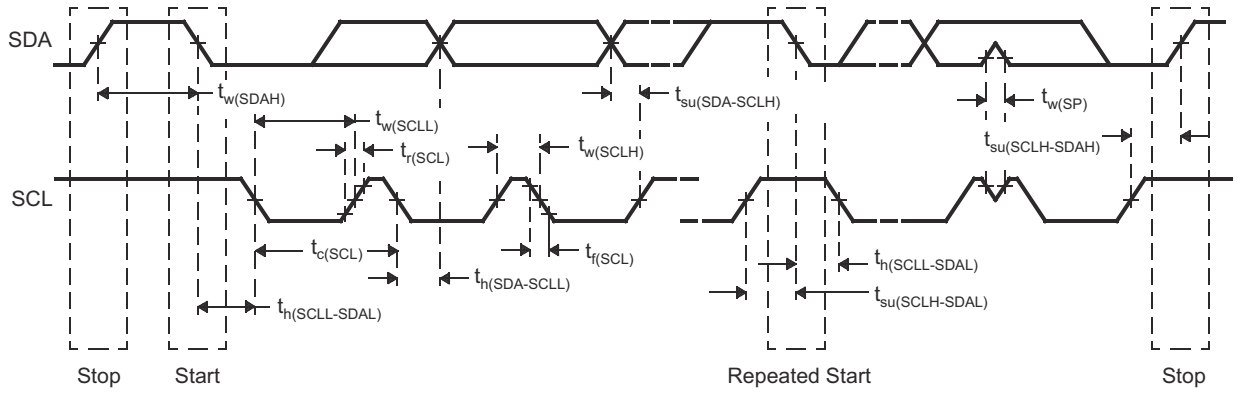

图 7-15. I2C Timing Diagram

Note

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geqslant 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

7.10.12 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI™) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a master only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Support for 3-, 4-, or 6-pin SPI interface
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

节 7.10.12.2 and 节 7.10.12.3 assume the operating conditions stated in 节 7.10.12.1.

7.10.12.1 QSPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

7.10.12.2 Timing Requirements for QSPI Input (Read) Timings[1] [2]

		MIN	TYP	MAX	UNIT
$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge (Q12)	7.3			ns
$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge (Q13)	1.5			ns
$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	7.3 – P[3]			ns
$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1.5 + P[3]			ns

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

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7.10.12.3 QSPI Switching Characteristics

NO.	PARAMETER(1) (2) (3)		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	25			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	0.5*P – 3			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	0.5*P – 3			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	– M*P – 1		– M*P + 2.5	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1		N*P + 2.5	ns
Q6	$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[0] transition	– 3.5		7	ns
Q7	$t_{ena(CS-D1LZ)}$	Enable time, cs active edge to d[0] driven (lo-z)	– P – 4		– P +1	ns
Q8	$t_{dis(CS-D1Z)}$	Disable time, cs active edge to d[0] tri-stated (hi-z)	– P – 4		– P +1	ns
Q9	$t_{d(SCLK-D1)}$	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	– 3.5 – P		7 – P	ns

(1) The Y parameter is defined as follows: If DCLK_DIV is 0 or ODD then, Y equals 0.5. If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1). For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2_H13 output of DPLL_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.
(2) P = SCLK period in ns.
(3) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

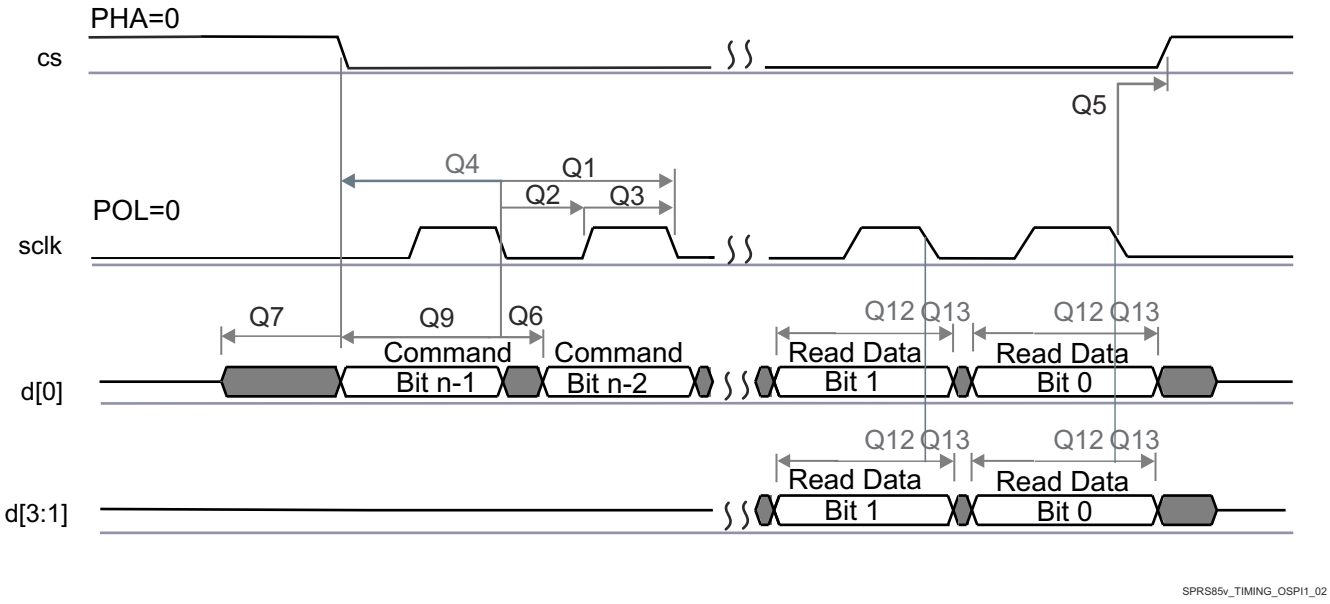

图 7-16. QSPI Read (Clock Mode 0)

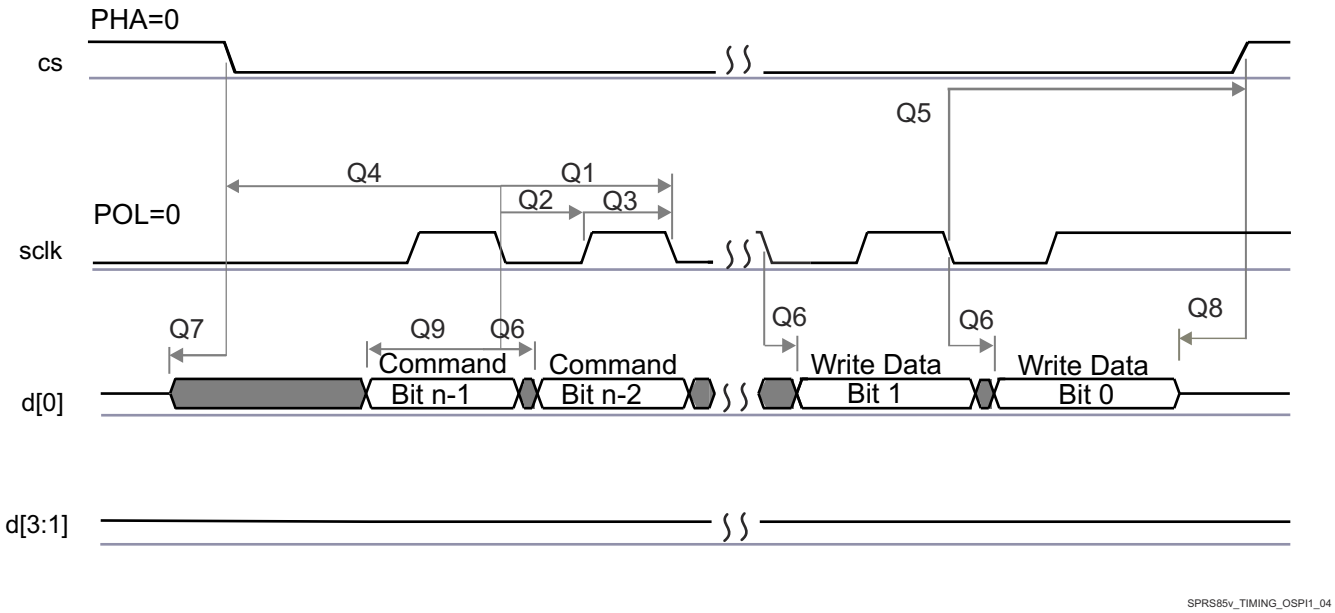

图 7-17. QSPI Write (Clock Mode 0)

7.10.13 ETM Trace Interface

节 7.10.13.2 and List item.referenceTitle assume the recommended operating conditions stated in 节 7.10.13.1.

7.10.13.1 ETMTRACE Timing Conditions

		MIN	TYP	MAX	UNIT
Output Conditions					
C_{LOAD}	Output load capacitance	2		20	pF

7.10.13.2 ETM TRACE Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{cyc(ETM)}$	Cycle time, TRACECLK period	20			ns
2	$t_{h(ETM)}$	Pulse Duration, TRACECLK High	9			ns
3	$t_{l(ETM)}$	Pulse Duration, TRACECLK Low	9			ns
4	$t_{r(ETM)}$	Clock and data rise time			3.3	ns
5	$t_{f(ETM)}$	Clock and data fall time			3.3	ns
6	$t_{d(ETMTRACECLKH-ETMDATAV)}$	Delay time, ETM trace clock high to ETM data valid	1		7	ns
7	$t_{d(ETMTRACECLKl-ETMDATAV)}$	Delay time, ETM trace clock low to ETM data valid	1		7	ns

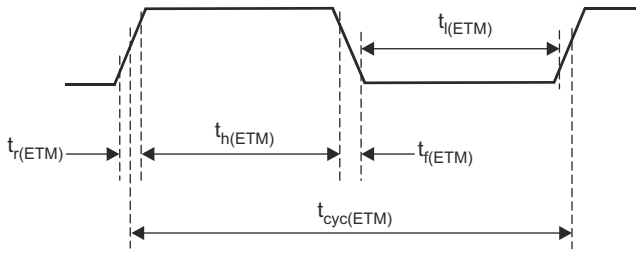

图 7-18. ETMTRACECLKOUT Timing

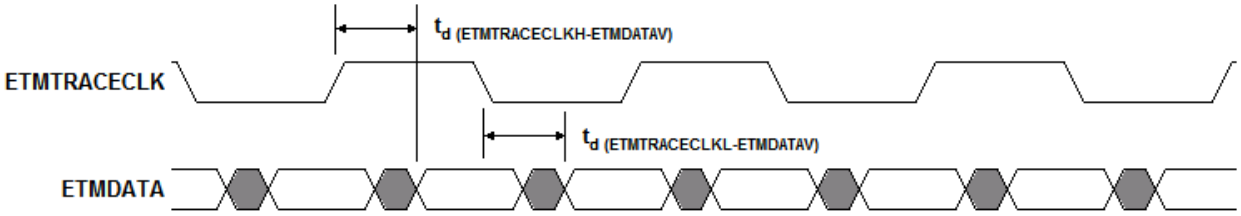

图 7-19. ETMDATA Timing

7.10.14 Data Modification Module (DMM)

A Data Modification Module (DMM) gives the ability to write external data into the device memory.

The DMM has the following features:

- Acts as a bus master, thus enabling direct writes to the 4GB address space without CPU intervention
- Writes to memory locations specified in the received packet (leverages packets defined by trace mode of the RAM trace port [RTP] module)
- Writes received data to consecutive addresses, which are specified by the DMM (leverages packets defined by direct data mode of RTP module)
- Configurable port width (1, 2, 4, 8, 16 pins)
- Up to 65 Mbit/s pin data rate

7.10.14.1 DMM Timing Requirements

		MIN	TYP	MAX	UNIT
$t_{cyc(DMM)}$	Clock period	15.4			ns
t_R	Clock rise time	1		3	ns
t_F	Clock fall time	1		3	ns
$t_{h(DMM)}$	High pulse width	6			ns
$t_{l(DMM)}$	Low pulse width	6			ns
$t_{ssu(DMM)}$	SYNC active to clk falling edge setup time	2			ns
$t_{sh(DMM)}$	DMM clk falling edge to SYNC deactive hold time	3			ns
$t_{dsu(DMM)}$	DATA to DMM clk falling edge setup time	2			ns
$t_{dh(DMM)}$	DMM clk falling edge to DATA hold time	3			ns

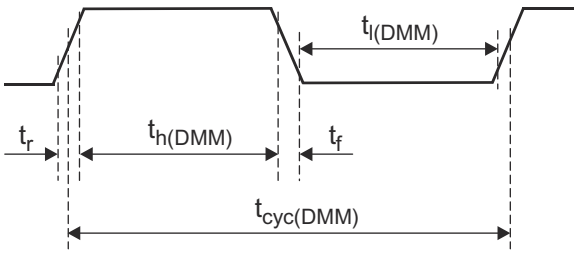

图 7-20. DMMCLK Timing

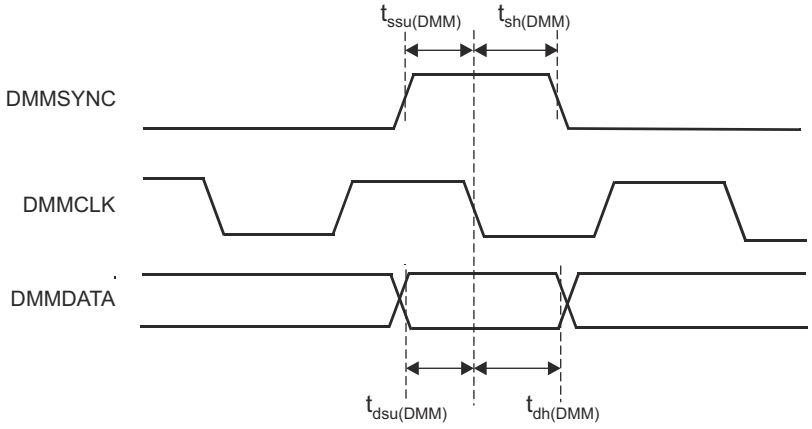

图 7-21. DMMDATA Timing

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7.10.15 JTAG Interface

节 7.10.15.2 and 节 7.10.15.3 assume the operating conditions stated in 节 7.10.15.1.

7.10.15.1 JTAG Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

7.10.15.2 Timing Requirements for IEEE 1149.1 JTAG

NO.			MIN	TYP	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time TCK	66.66			ns
1a	$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	26.67			ns
1b	$t_{w(TCKL)}$	Pulse duration TCK low(40% of tc)	26.67			ns
3	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns
	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
4	$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
	$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

7.10.15.3 Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		25	ns

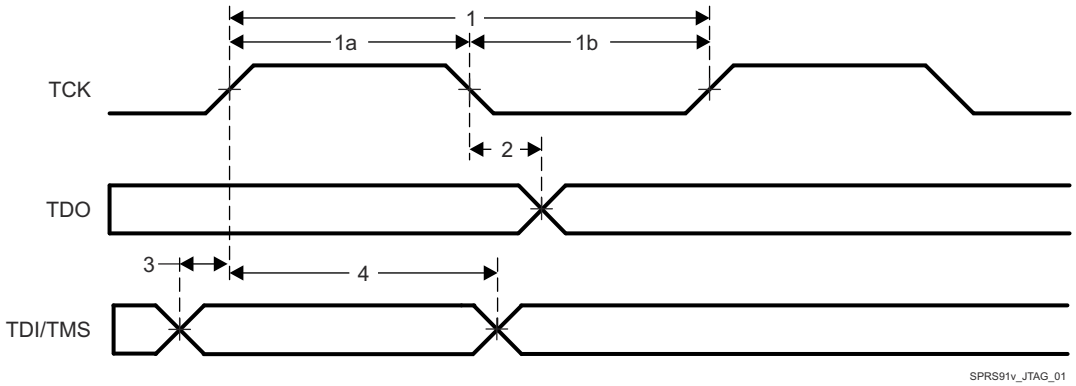


图 7-22. JTAG Timing

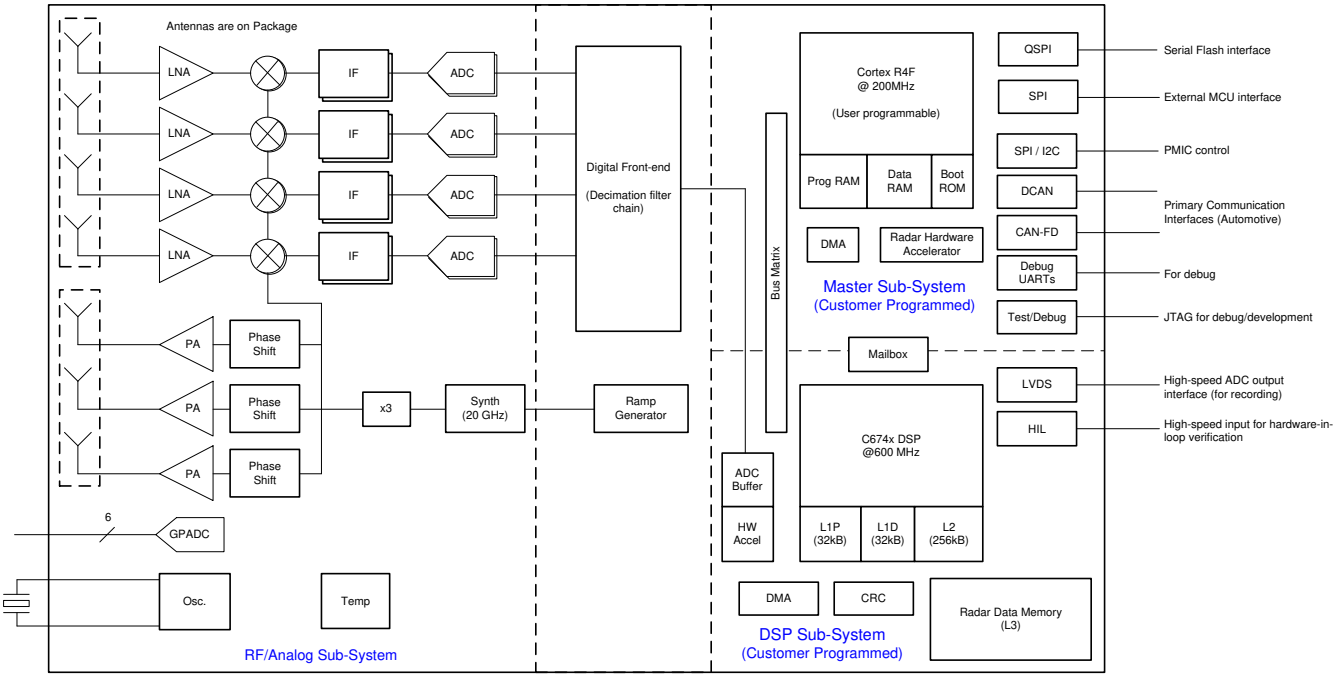
8 Detailed Description

8.1 Overview

The AWR1843AOP is an Antenna-on-Package (AOP) device that includes the entire Millimeter Wave blocks and analog baseband signal chain for two transmitters and four receivers, as well as a customer-programmable MCU. This device is applicable as a radar-on-a-chip in use-cases with modest requirements for memory, processing capacity and application code size. These could be cost-sensitive automotive applications that are evolving from 24 GHz narrowband implementation and some emerging simple ultra-short-range radar applications. Typical application examples for this device include basic Blind Spot Detect, Parking Assist, and so forth.

In terms of scalability, the AWR1843AOP device could be paired with a low-end external MCU, to address more complex applications that might require additional memory for larger application software footprint and faster interfaces.

8.2 Functional Block Diagram



8.3 Subsystems

8.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated up to a maximum of two at a time (simultaneously) for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

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8.3.1.1 Clock Subsystem

The AWR1843AOP clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

图 8-1 describes the clock subsystem.

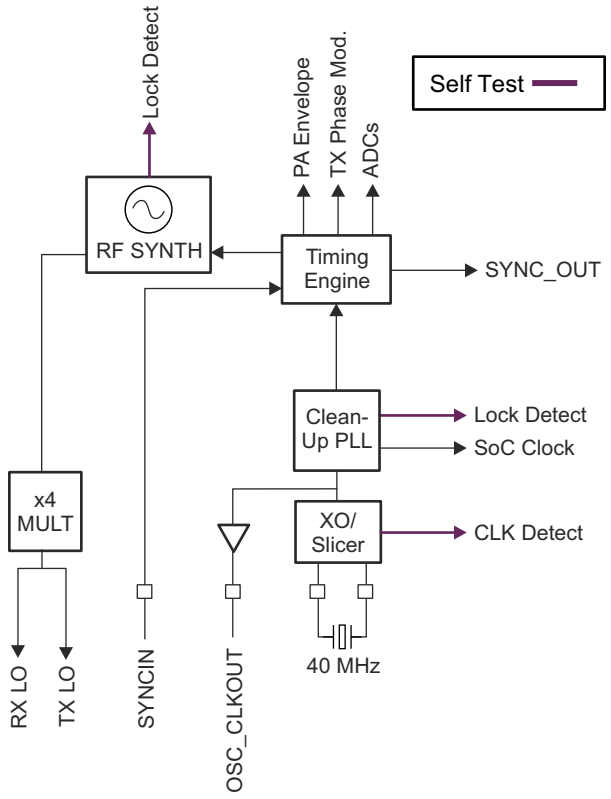

图 8-1. Clock Subsystem

8.3.1.2 Transmit Subsystem

The AWR1843AOP transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. All three transmitters can be used simultaneously. For AWR1843AOP, additional phase shifters are associated with Tx channels, and these can programmed on a per chirp basis.

Each transmit chain can deliver a maximum of 16 dBm. The transmit chains also support programmable backoff for system optimization.

图 8-2 describes the transmit subsystem.

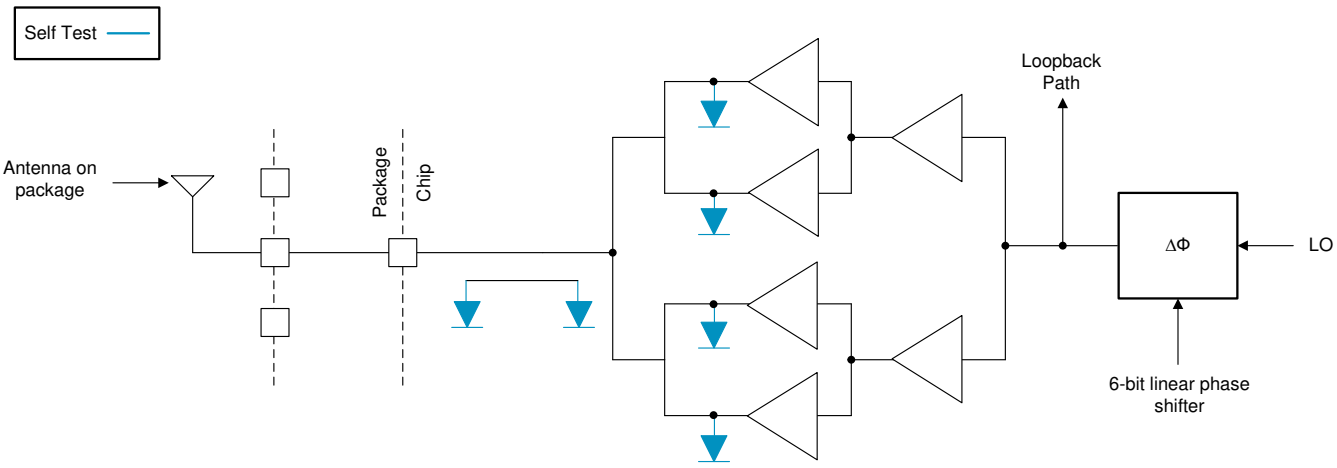

图 8-2. Transmit Subsystem (Per Channel)

8.3.1.3 Receive Subsystem

The AWR1843AOP receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the AWR1843AOP device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The AWR1843AOP is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 10 MHz.

图 8-3 describes the receive subsystem.

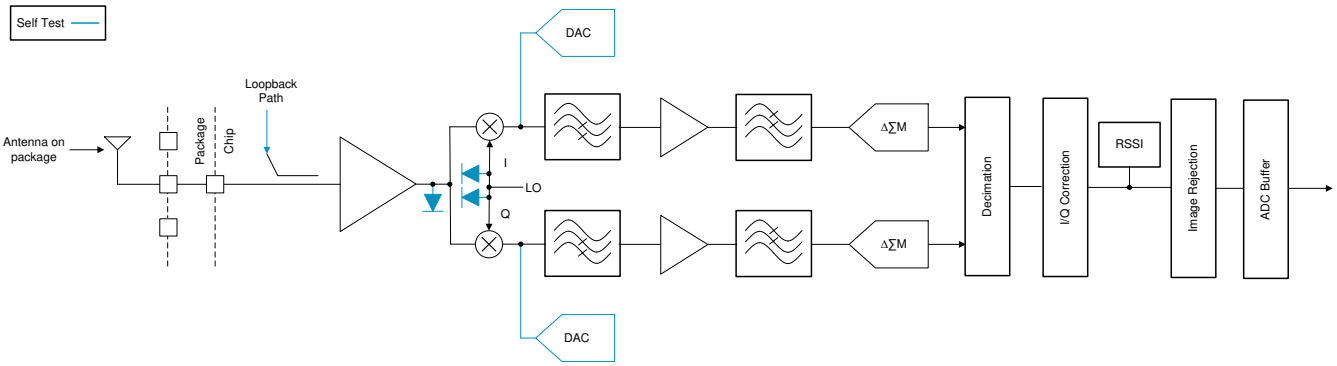

图 8-3. Receive Subsystem (Per Channel)

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8.3.2 Processor Subsystem

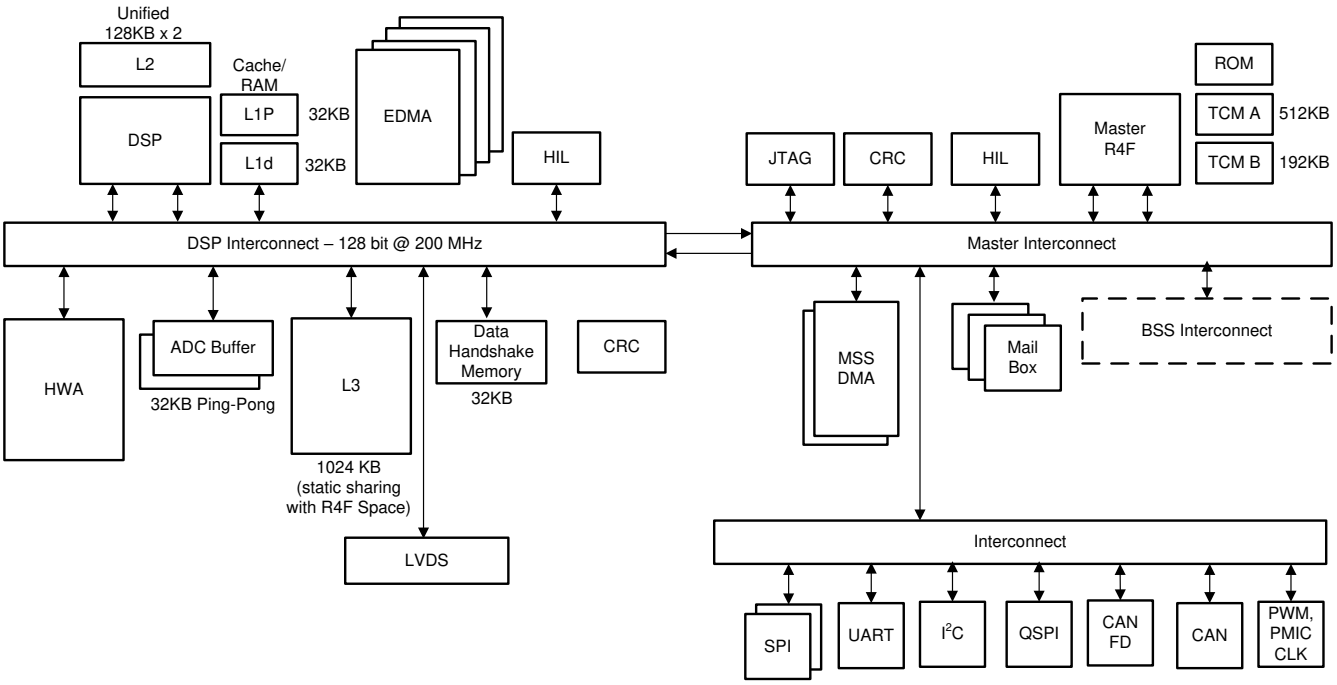

图 8-4. Processor Subsystem

图 8-4 shows the block diagram for customer programmable processor subsystems in the AWR1843AOP device. At a high level there are two customer programmable subsystems. Left hand side shows the DSP Subsystem which contains TI's high-performance C674x DSP, a high-bandwidth interconnect for high performance (128-bit, 200MHz) and associated peripherals – four DMAs for data transfer,

LVDS interface for Measurement data output, L3 Radar data cube memory, ADC buffers, CRC engine, and data handshake memory (additional memory provided on interconnect).

The right side of the diagram shows the Master subsystem. Master subsystem as name suggests is the master of the device and controls all the device peripherals and house-keeping activities of the device. Master subsystem contains Cortex-R4F (Master R4F) processor and associated peripherals and house-keeping components such as DMAs, CRC and Peripherals (I^2C, UART, SPIs, CAN, PMIC clocking module, PWM, and others) connected to Master Interconnect through Peripheral Central Resource (PCR interconnect).

Details of the DSP CPU core can be found at http://www.ti.com/product/TMS320C6748.

HIL module is shown in both the subsystems and can be used to perform the radar operations feeding the captured data from outside into the device without involving the RF subsystem. HIL on master SS is for controlling the configuration and HIL on DSPSS for high speed ADC data input to the device. Both HIL modules uses the same IOs on the device, one additional IO (DMM_MUX_IN) allows selecting either of the two.

8.3.3 Automotive Interface

The AWR1843AOP communicates with the automotive network over the following main interfaces:

- CAN (2 interfaces available, one of them being CAN-FD)

8.3.4 Master Subsystem Cortex-R4F Memory Map

表 8-1 shows the master subsystem, Cortex-R4F memory map.

Note

There are separate Cortex-R4F addresses and DMA MSS addresses for the master subsystem. See the Technical Reference Manual for a complete list.

表 8-1. Master Subsystem, Cortex-R4F Memory Map

NAME	FRAME ADDRESS (HEX)		SIZE	DESCRIPTION
	START	END		
CPU Tightly-Coupled Memories				
TCMA ROM	0x0000_0000	0x0001_FFFF	128 KiB	Program ROM
TCM RAM-A	0x0020_0000	0x0023_FFFF (or 0x0027_FFFF)	512 KiB	
TCM RAM-B	0x0800_0000	0x0802_FFFF	192 KB	Data RAM
S/W Scratch Pad Memory				
SW_ Buffer	0x0C20_0000	0x0C20_1FFF	8 KB	S/W Scratchpad memory
System Peripherals				
Mail Box MSS<->RADARSS	0xF060_1000	0xF060_17FF	2 KB	RADARSS to MSS mailbox memory space
	0xF060_2000	0xF060_27FF		MSS to RADARSS mailbox memory space
	0xF060_8000	0xF060_80FF	188 B	MSS to RADARSS mailbox Configuration registers
	0xF060_8060	0xF060_86FF		RADARSS to MSS mailbox Configuration registers
Mail Box MSS<->DSPSS	0xF060_4000	0xF060_47FF	2 KB	DSPSS to MSS mailbox memory space
	0xF060_5000	0xF060_57FF		MSS to DSPSS mailbox memory space
	0xF060_8400	0xF060_84FF	188 B	MSS to DSPSS mailbox Configuration registers
	0xF060_8300	0xF060_83FF		DSPSS to MSS mailbox Configuration registers
Mail Box RADARSS<->DSPSS	0xF060_6000	0xF060_67FF	2 KB	RADARSS to DSPSS mailbox memory space
	0xF060_7000	0xF060_7FFF		DSPSS to RADARSS mailbox memory space
	0xF060_8200	0xF060_82FF	188 B	RADARSS to DSPSS mailbox Configuration registers
	0xF060_8100	0xF060_81FF		DSPSS to RADARSS mailbox Configuration registers
PRCM and Control Module	0xFFFF_E100	0xFFFF_E2FF	756 B	TOP Level Reset, Clock management registers
	0xFFFF_FF00	0xFFFF_FFFF	256 B	MSS Reset, Clock management registers
	0xFFFF_EA00	0xFFFF_EBFF	512 KB	IO Mux module registers
	0xFFFF_F800	0xFFFF_FBFF	352 B	General-purpose control registers
GIO	0xFFF7_BC00	0xFFF7_BDFF	180 B	GIO module configuration registers
DMA-1	0xFFFF_F000	0xFFFF_F3FF	1 KB	DMA-1 module configuration registers
DMA-2	0xFCFF_F800	0xFCFF_FBFF	1 KB	DMA-2 module configuration registers
DMM-1	0xFCFF_F700	0xFCFF_F7FF	472 B	DMM-1 module configuration registers
DMM-2	0xFCFF_F600	0xFCFF_F6FF	472 B	DMM-2 module configuration registers
VIM	0xFFFF_FD00	0xFFFF_FEFF	512 B	VIM module configuration registers
RTI-A/WD	0xFFFF_FC00	0xFFFF_FCFF	192 B	RTI-A module configuration registers
RTI-B	0xFFFF_EE00	0xFFFF_EEFF	192 B	RTI-B module configuration registers
Serial Interfaces and Connectivity				
QSPI	0xC000_0000	0xC07F_FFFF	8 MB	QSPI – flash memory space
	0xC080_0000	0xC0FF_FFFF	116 B	QSPI module configuration registers
MIBSPI-A	0xFFF7_F400	0xFFF7_F5FF	512 B	MIBSPI-A module configuration registers
MIBSPI-B	0xFFF7_F600	0xFFF7_F7FF	512 B	MIBSPI-B module configuration registers
SCI-A	0xFFF7_E500	0xFFF7_E5FF	148 B	SCI-A module configuration registers
SCI-B	0xFFF7_E700	0xFFF7_E7FF	148 B	SCI-B module configuration registers

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表 8-1. Master Subsystem, Cortex-R4F Memory Map (continued)

NAME	FRAME ADDRESS (HEX)		SIZE	DESCRIPTION
	START	END		
CAN	0xFFF7_DC00	0xFFF7_DDFF	512 B	CAN module configuration registers
CAN_FD(MCAN)	0xFFF7_C800	0xFFF7_CFFF	768 B	CAN-FD module configuration registers
	0xFFF7_A000	0xFFF7_A1FF	452 B	MCAN ECC module registers
I2C	0xFFF7_D400	0xFFF7_D4FF	112 B	I2C module configuration registers
Interconnects				
PCR-1	0xFFF7_8000	0xFFF7_87FF	1 KiB	PCR-1 interconnect configuration port
PCR-2	0xFCFF_1000	0xFCFF_17FF	1 KiB	PCR-2 interconnect configuration port
Safety Modules				
CRC	0xFE00_0000	0xFEFF_FFFF	16 KiB	CRC module configuration registers
PBIST	0xFFFF_E400	0xFFFF_E5FF	464 B	PBIST module configuration registers
STC	0xFFFF_E600	0xFFFF_E7FF	284 B	STC module configuration registers
DCC-A	0xFFFF_EC00	0xFFFF_ECFF	44 B	DCC-A module configuration registers
DCC-B	0xFFFF_F400	0xFFFF_F4FF	44 B	DCC-B module configuration registers
ESM	0xFFFF_F500	0xFFFF_F5FF	156 B	ESM module configuration registers
CCMR4	0xFFFF_F600	0xFFFF_F6FF	136 B	CCMR4 module configuration registers
Security Modules				
Crypto	0xFD00_0000	0XFDFF_FFFF	3 KiB	Crypto module configuration registers
Other Subsystems				
DSS_TPTC0	0x5000 0000	0x5000 0317	792 B	TPTC0 module configuration space
DSS_REG	0x5000 0400	0x5000 075F	864 B	DSPSS control module registers
DSS_TPTC1	0x5000 0800	0x5000 0B17	792 B	TPTC1 module configuration space
DSS_REG2	0x5000 0C00	0x5000 0EA3	676 B	DSPSS control module registers
DSS_TPCC0	0x5001 0000	0x5001 3FFF	16 KB	TPCC0 module configuration space
DSS_RTIA/WDT	0x5002 0000	0x5002 00BF	192 B	DSS_RTIA/WDT configuration space
DSS_SCI	0x5003 0000	0x5003 0093	148 B	SCI memory space
DSS_STC	0x5004 0000	0x5004 011B	284 B	STC module configuration space
DSS_CBUFF	0x5007 0000	0x5007 0233	564 B	Common Buffer module configuration registers
DSS_TPTC2	0x5009 0000	0x5009 0317	792 B	TPTC2 module configuration space
DSS_TPTC3	0x5009 0400	0x5009 0717	792 B	TPTC3 module configuration space
DSS_TPCC1	0x500A 0000	0x500A 3FFF	16 KB	TPCC1 module configuration space
DSS_ESM	0x500D 0000	0x500D 005B	92 B	ESM module configuration registers
DSS_RTIB	0x500F 0000	0x500F 00BF	192 B	RTI-B module configuration registers
DSS_L3RAM Shared memory	0x5100 0000	0x511F FFFF	2 MB(1)	L3 shared memory space
DSS_ADCBUF Buffer	0x5200 0000	0x5200 7FFF	32 KB	ADC buffer memory space
DSS_CBUFF_FIFO	0x5202 0000	0x5202 3FFF	16 KB	Common buffer FIFO space
DSS_HSRAM1	0x5208 0000	0x5208 7FFF	32 KB	Handshake memory space
DSS_DSP_L2_UMAP1	0x577E 0000	0x577F FFFF	128 KB	L2 RAM space
DSS_DSP_L2_UMAP0	0x5780 0000	0x5781 FFFF	128 KB	L2 RAM space
DSS_DSP_L1P	0x57E0 0000	0x57E0 7FFF	32 KB	L1 program memory space
DSS_DSP_L1D	0x57F0 0000	0x57F0 7FFF	32 KB	L1 data memory space
Peripheral Memories (System and Nonsystem)				
CAN RAM	0xFF1E_0000	0xFF1F_FFFF	128 KB	CAN RAM memory space

表 8-1. Master Subsystem, Cortex-R4F Memory Map (continued)

NAME	FRAME ADDRESS (HEX)		SIZE	DESCRIPTION
	START	END		
CAN-FD RAM	0xFF50_0000	0xFF51_FFFF	68 KB	CAN-FD RAM memory space
DMA1 RAM	0xFFF8_0000	0xFFF8_0FFF	4 KB	DMA1 RAM memory space
DMA2 RAM	0xFCF8 1000	0xFCF8_0FFF	4 KB	DMA2 RAM memory space
VIM RAM	0xFFF8_2000	0xFFF8_2FFF	2 KB	VIM RAM memory space
MIBSPIB-TX RAM	0xFF0C_0000	0xFF0C_01FF	0.5 KB	MIBSPIB-TX RAM memory space
MIBSPIB-RX RAM	0xFF0C_0200	0xFF0C_03FF	0.5 KB	MIBSPIB-RX RAM memory space
MIBSPIA-TX RAM	0xFF0E_0000	0xFF0E_01FF	0.5 KB	MIBSPIA-TX RAM memory space
MIBSPIA- RX RAM	0xFF0E_0200	0xFF0E_03FF	0.5 KB	MIBSPIA- RX RAM memory space
Debug Modules				
Debug subsystem	0xFFA0_0000	0xFFAF_FFFF	244 KB	Debug subsystem memory space and registers

(1) 1024 KB memory within 2 MB memory space

8.3.5 DSP Subsystem Memory Map

表 8-2 shows the DSP C674x memory map.

表 8-2. DSP C674x Memory Map

Name	Frame Address (Hex)		Size	Description
	Start	End		
DSP Memories				
DSP_L1D	0x00F0_0000	0x00F0_7FFF	32 KiB	L1 data memory space
DSP_L1P	0x00E0_0000	0x00E0_7FFF	32 KiB	L1 program memory space
DSP_L2_UMAP0	0x0080_0000	0x0081_FFFF	128 KiB	L2 RAM space
DSP_L2_UMAP1	0x007E_0000	0x007F_FFFF	128 KiB	L2 RAM space
EDMA				
TPCC0	0x0201_0000	0x0201_3FFF	16 KiB	TPCC0 module configuration space
TPCC1	0x020A_0000	0x020A_3FFF	16 KiB	TPCC1 module configuration space
TPTC0	0x0200 0000	0x0200 03FF	1 KiB	TPTC0 module configuration space
TPTC1	0x0200 0800	0x0200 0BFF	1 KiB	TPTC1 module configuration space
TPTC2	0x0209_0000	0x0209_03FF	1 KiB	TPTC2 module configuration space
TPTC3	0x0209_0400	0x0209_07FF	1 KiB	TPTC3 module configuration space
Control Registers				
DSS_REG	0x0200_0400	0x0200_07FF	864 B	DSPSS control module registers
DSS_REG2	0x0200_0C00	0x0200_0FFF	624 B	DSPSS control module registers
System Memories				
ADC Buffer	0x2100_0000	0x2100_7FFC	32 KiB	ADC buffer memory space
CBUFF-FIFO	0x2102_0000	0x2102_3FFC	16 KiB	Common buffer FIFO space
L3-Shared memory	0x2000_0000	0x201F_FFFF	2 MB	L3 shared memory space
HS-RAM	0x2108_0000	0x2108_7FFC	32 KiB	Handshake memory space

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表 8-2. DSP C674x Memory Map (continued)

Name	Frame Address (Hex)		Size	Description
	Start	End		
System Peripherals				
RTI-A/WD	0x0202_0000	0x0202_00FF	192 B	RTI-A module configuration registers
RTI-B	0x020F_0000	0x020F_00FF	192 B	RTI-B module configuration registers
CBUFF	0x0207_0000	0x0207_03FF	564 B	Common Buffer module Configuration registers
Mail Box MSS<->RADARSS	0x5060_1000	0x5060_17FF	2 KiB	RADARSS to MSS mailbox memory space
	0x5060_2000	0x5060_27FF		MSS to RADARSS mailbox memory space
	0x0460_8000	0x0460_80FF	188 B	MSS to RADARSS mailbox Configuration registers
	0x0460_8060	0x0460_86FF		RADARSS to MSS mailbox Configuration registers
Mail Box MSS<->DSPSS	0x5060_4000	0x5060_47FF	2 KiB	DSPSS to MSS mailbox memory space
	0x5060_5000	0x5060_57FF		MSS to DSPSS mailbox memory space
	0x0460_8400	0x0460_84FF	188 B	MSS to DSPSS mailbox Configuration registers
	0x0460_8300	0x0460_83FF		DSPSS to MSS mailbox Configuration registers
Mail Box RADARSS<->DSPSS	0x5060_6000	0x5060_67FF	2 KiB	RADARSS to DSPSS mailbox memory space
	0x5060_7000	0x5060_7FFF		DSPSS to RADARSS mailbox memory space
	0x0460_8200	0x0460_82FF	188 B	RADARSS to DSPSS mailbox Configuration registers
	0x0460_8100	0x0460_81FF		DSPSS to RADARSS mailbox Configuration registers
Safety Modules				
ESM	0x020D_0000		92 B	ESM module Configuration registers
CRC	0x2200_0000	0x2200_03FF	1 KiB	CRC module Configuration registers
STC	0x0204_0000	0x0204_01FF	284 B	STC module Configuration registers
Nonsystem Peripherals				
SCI	0x0203_0000	0x0203_00FF	148 B	SCI module Configuration registers

8.4 Other Subsystems

8.4.1 ADC Channels (Service) for User Application

The AWR1843AOP device includes provision for an ADC service for user application, where the

GPADC engine present inside the device can be used to measure up to six external voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, and ADC6 pins are used for this purpose.

- ADC itself is controlled by TI firmware running inside the BIST subsystem and access to it for customer’s external voltage monitoring purpose is via ‘monitoring API’ calls routed to the BIST subsystem. This API could be linked with the user application running on the Master R4.
- BIST subsystem firmware will internally schedule these measurements along with other [1]RF and Analog monitoring operations. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

GPADC Specifications:

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution
- For 5 out of the 6 inputs, an optional internal buffer is available. Without the buffer, the ADC has a switched capacitor input load modeled with 5pF of sampling capacitance and 12pF parasitic capacitance (GPADC channel 6, the internal buffer is not available).

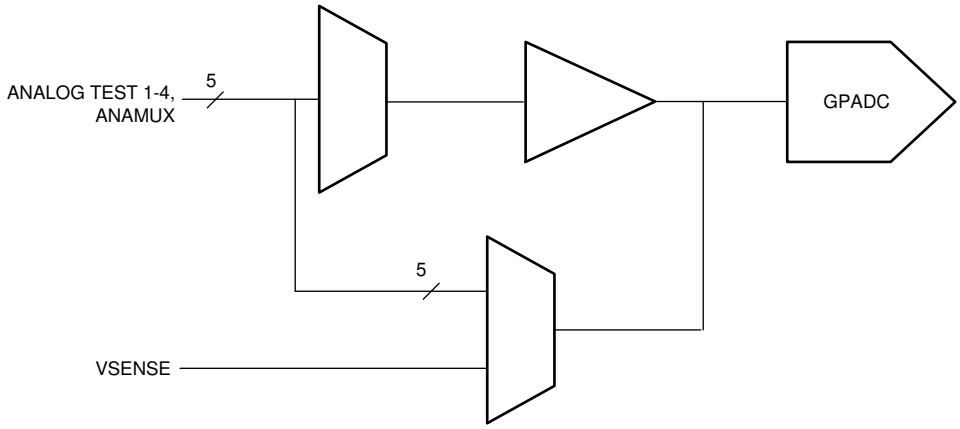

图 8-5. ADC Path

[1] GPADC structures are used for measuring the output of internal temperature sensors. The accuracy of these measurements is ±7°C

9 Monitoring and Diagnostics

9.1 Monitoring and Diagnostic Mechanisms

Below is the list given for the main monitoring and diagnostic mechanisms available in the AWR1843AOP.

表 9-1. Monitoring and Diagnostic Mechanisms for AWR1843AOP

S No	Feature	Description
1	Boot time LBIST For Master R4F Core and associated VIM	AWR1843AOP architecture supports hardware logic BIST (LBIST) engine self-test Controller (STC). This logic is used to provide a very high diagnostic coverage (>90%) on the Master R4F CPU core and Vectored Interrupt Module (VIM) at a transistor level. LBIST for the CPU and VIM need to be triggered by application code before starting the functional safety application. CPU stays there in while loop and does not proceed further if a fault is identified.
2	Boot time PBIST for Master R4F TCM Memories	Master R4F has three Tightly coupled Memories (TCM) memories TCMA, TCMB0 and TCMB1. AWR1843AOP architecture supports a hardware programmable memory BIST (PBIST) engine. This logic is used to provide a very high diagnostic coverage (March-13n) on the implemented Master R4F TCMs at a transistor level. PBIST for TCM memories is triggered by Bootloader at the boot time before starting download of application from Flash or peripheral interface. CPU stays there in while loop and does not proceed further if a fault is identified.
3	End to End ECC for Master R4F TCM Memories	TCMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. An 8-bit code word is used to store the ECC data as calculated over the 64-bit data bus. ECC evaluation is done by the ECC control logic inside the CPU. This scheme provides end-to-end diagnostics on the transmissions between CPU and TCM. CPU can be configured to have predetermined response (Ignore or Abort generation) to single and double bit error conditions.
4	Master R4F TCM bit multiplexing	Logical TCM word and its associated ECC code is split and stored in two physical SRAM banks. This scheme provides an inherent diagnostic mechanism for address decode failures in the physical SRAM banks. Faults in the bank addressing are detected by the CPU as an ECC fault. Further, bit multiplexing scheme implemented such that the bits accessed to generate a logical (CPU) word are not physically adjacent. This scheme helps to reduce the probability of physical multi-bit faults resulting in logical multi-bit faults; rather they manifest as multiple single bit faults. As the SECDED TCM ECC can correct a single bit fault in a logical word, this scheme improves the usefulness of the TCM ECC diagnostic. Both these features are hardware features and cannot be enabled or disabled by application software.
5	Clock Monitor	AWR1843AOP architecture supports Three Digital Clock Comparators (DCCs) and an internal RCOSC. Dual functionality is provided by these modules – Clock detection and Clock Monitoring. DCCint is used to check the availability/range of Reference clock at boot otherwise the device is moved into limp mode (Device still boots but on 10MHz RCOSC clock source. This provides debug capability). DCCint is only used by boot loader during boot time. It is disabled once the APLL is enabled and locked. DCC1 is dedicated for APLL lock detection monitoring, comparing the APLL output divided version with the Reference input clock of the device. Initially (before configuring APLL), DCC1 is used by bootloader to identify the precise frequency of reference input clock against the internal RCOSC clock source. Failure detection for DCC1 would cause the device to go into limp mode. DCC2 module is one which is available for user software . From the list of clock options given in detailed spec, any two clocks can be compared. One example usage is to compare the CPU clock with the Reference or internal RCOSC clock source. Failure detection is indicated to the Master R4F CPU via Error Signaling Module (ESM).
7	RTI/WD for Master R4F	AWR1843AOP architecture supports the use of an internal watchdog that is implemented in the real-time interrupt (RTI) module. The internal watchdog has two modes of operation: digital watchdog (DWD) and digital windowed watchdog (DWWD). The modes of operation are mutually exclusive; the designer can elect to use one mode or the other but not both at the same time. Watchdog can issue either an internal (warm) system reset or a CPU non-mask able interrupt upon detection of a failure. The Watchdog is enabled by the bootloader in DWD mode at boot time to track the boot process. Once the application code takes up the control, Watchdog can be configured again for mode and timings based on specific customer requirements.

表 9-1. Monitoring and Diagnostic Mechanisms for AWR1843AOP (continued)

S No	Feature	Description
8	MPU for Master R4F	Cortex-R4F CPU includes an MPU. The MPU logic can be used to provide spatial separation of software tasks in the device memory. Cortex-R4F MPU supports 12 regions. It is expected that the operating system controls the MPU and changes the MPU settings based on the needs of each task. A violation of a configured memory protection policy results in a CPU abort.
9	PBIST for Peripheral interface SRAMs - SPIs, CANs	AWR1843AOP architecture supports a hardware programmable memory BIST (PBIST) engine for Peripheral SRAMs as well. PBIST for peripheral SRAM memories can be triggered by the application. User can elect to run the PBIST on one SRAM or on groups of SRAMs based on the execution time, which can be allocated to the PBIST diagnostic. The PBIST tests are destructive to memory contents, and as such are typically run only at boot time. However, the user has the freedom to initiate the tests at any time if peripheral communication can be hindered. Any fault detected by the PBIST results in an error indicated in PBIST status registers.
10	ECC for Peripheral interface SRAMs – SPIs, CANs	Peripheral interface SRAMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. When a single or double bit error is detected the Master R4F is notified via ESM (Error Signaling Module). This feature is disabled after reset. Software must configure and enable this feature in the peripheral and ESM module. ECC failure (both single bit corrected and double bit uncorrectable error conditions) is reported to the Master R4F as an interrupt via ESM module.
11	Configuration registers protection for Master SS peripherals	All the Master SS peripherals (SPIs, CANs, I2C, DMAs, RTI/WD, DCCs, IOMUX etc.) are connected to interconnect via Peripheral Central resource (PCR). This provides two diagnostic mechanisms that can limit access to peripherals. Peripherals can be clock gated per peripheral chip select in the PCR. This can be utilized to disable unused features such that they cannot interfere. In addition, each peripheral chip select can be programmed to limit access based on privilege level of transaction. This feature can be used to limit access to entire peripherals to privileged operating system code only. These diagnostic mechanisms are disabled after reset. Software must configure and enable these mechanisms. Protection violation also generates an ‘aerror’ that result in abort to Master R4F or error response to other masters such as DMAs.
12	Cyclic Redundancy Check – Master SS	AWR1843AOP architecture supports hardware CRC engine on Master SS implementing the below polynomials. • CRC16 CCITT – 0x10 • CRC32 Ethernet – 0x04C11DB7 • CRC64 • CRC 32C – CASTAGNOLI – 0x1EDC6F4 • CRC32P4 – E2E Profile4 – 0xF4ACFB1 • CRC-8 – H2F Autosar – 0x2F • CRC-8 – VDA CAN – 0x1D The read operation of the SRAM contents to the CRC can be done by CPU or by DMA. The comparison of results, indication of fault, and fault response are the responsibility of the software managing the test.
13	MPU for DMAs	AWR1843AOP architecture supports MPUs on Master SS DMAs. Failure detection by MPU is reported to the Master R4F CPU core as an interrupt via ESM. DSPSS’s high performance EDMAs also includes MPUs on both read and writes master ports. EDMA MPUs supports 8 regions. Failure detection by MPU is reported to the DSP core as an interrupt via local ESM.
14	Boot time LBIST For BIST R4F Core and associated VIM	AWR1843AOP architecture supports hardware logic BIST (LBIST) even for BIST R4F core and associated VIM module. This logic provides very high diagnostic coverage (>90%) on the BIST R4F CPU core and VIM. This is triggered by Master R4F boot loader at boot time and it does not proceed further if the fault is detected.
15	Boot time PBIST for BIST R4F TCM Memories	AWR1843AOP architecture supports a hardware programmable memory BIST (PBIST) engine for BIST R4F TCMs which provide a very high diagnostic coverage (March-13n) on the BIST R4F TCMs. PBIST is triggered by Master R4F Bootloader at the boot time and it does not proceed further if the fault is detected.

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表 9-1. Monitoring and Diagnostic Mechanisms for AWR1843AOP (continued)

S No	Feature	Description
16	End to End ECC for BIST R4F TCM Memories	BIST R4F TCMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. Single bit error is communicated to the BIST R4FCPU while double bit error is communicated to Master R4F as an interrupt so that application code becomes aware of this and takes appropriate action.
17	BIST R4F TCM bit multiplexing	Logical TCM word and its associated ECC code is split and stored in two physical SRAM banks. This scheme provides an inherent diagnostic mechanism for address decode failures in the physical SRAM banks and helps to reduce the probability of physical multi-bit faults resulting in logical multi-bit faults.
18	RTI/WD for BIST R4F	AWR1843AOP architecture supports an internal watchdog for BIST R4F. Timeout condition is reported via an interrupt to Master R4F and rest is left to application code to either go for SW reset for BIST SS or warm reset for the AWR1843AOP device to come out of faulty condition.
19	Boot time PBIST for L1P, L1D, L2 and L3 Memories	AWR1843AOP architecture supports a hardware programmable memory BIST (PBIST) engine for DSPSS’s L1P, L1D, L2 and L3 memories which provide a very high diagnostic coverage (March-13n). PBIST is triggered by Master R4F Bootloader at the boot time and it does not proceed further if the fault is detected.
20	Parity on L1P	AWR1843AOP architecture supports Parity diagnostic on DSP’s L1P memory. Parity error is reported to the CPU as an interrupt. Note:- L1D memory is not covered by parity or ECC and need to be covered by application level diagnostics.
21	ECC on DSP’s L2 Memory	AWR1843AOP architecture supports both Parity Single error correction double error detection (SECDED) ECC diagnostic on DSP’s L2 memory. L2 Memory is a unified 256KB of memory used to store program and Data sections for the DSP. A 12-bit code word is used to store the ECC data as calculated over the 256-bit data bus (logical instruction fetch size). The ECC logic for the L2 access is located in the DSP and evaluation is done by the ECC control logic inside the DSP. This scheme provides end-to-end diagnostics on the transmissions between DSP and L2. Byte aligned Parity mechanism is also available on L2 to take care of data section.
22	ECC on Radar Data Cube (L3) Memory	L3 memory is used as Radar data section in AWR1843AOP. AWR1843AOP architecture supports Single error correction double error detection (SECDED) ECC diagnostic on L3 memory. An 8-bit code word is used to store the ECC data as calculated over the 64-bit data bus. Failure detection by ECC logic is reported to the Master R4F CPU core as an interrupt via ESM.
23	RTI/WD for DSP Core	AWR1843AOP architecture supports the use of an internal watchdog for BIST R4F that is implemented in the real-time interrupt (RTI) module – replication of same module as used in Master SS. This module supports same features as that of RTI/WD for Master/BIST R4F. This watchdog is enabled by customer application code and Timeout condition is reported via an interrupt to Master R4F and rest is left to application code in Master R4F to either go for SW reset for DSP SS or warm reset for the AWR1843AOP device to come out of faulty condition.
24	CRC for DSP Sub-System	AWR1843AOP architecture supports dedicated hardware CRC on DSPSS implementing the below polynomials. • CRC16 CCITT - 0x10 • CRC32 Ethernet - 0x04C11DB7 • CRC64 The read of SRAM contents to the CRC can be done by DSP CPU or by DMA. The comparison of results, indication of fault, and fault response are the responsibility of the software managing the test.
25	MPU for DSP	AWR1843AOP architecture supports MPUs for DSP memory accesses (L1D, L1P, and L2). L2 memory supports 64 regions and 16 regions for L1P and L1D each. Failure detection by MPU is reported to the DSP core as an abort.
26	Temperature Sensors	AWR1843AOP architecture supports various temperature sensors all across the device (next to power hungry modules such as PAs, DSP etc) which is monitored during the inter-frame period.(1)
27	Tx Power Monitors	AWR1843AOP architecture supports power detectors at the Tx output.(2)

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表 9-1. Monitoring and Diagnostic Mechanisms for AWR1843AOP (continued)

S No	Feature	Description
28	Error Signaling Error Output	When a diagnostic detects a fault, the error must be indicated. The AWR1843AOP architecture provides aggregation of fault indication from internal monitoring/diagnostic mechanisms using a peripheral logic known as the Error Signaling Module (ESM). The ESM provides mechanisms to classify errors by severity and to provide programmable error response. ESM module is configured by customer application code and specific error signals can be enabled or masked to generate an interrupt (Low/High priority) for the Master R4F CPU. AWR1843AOP supports Nerror output signal (IO) which can be monitored externally to identify any kind of high severity faults in the design which could not be handled by the R4F.
29	Synthesizer (Chirp) frequency monitor	Monitors Synthesizer’s frequency ramp by counting (divided-down) clock cycles and comparing to ideal frequency ramp. Excess frequency errors above a certain threshold, if any, are detected and reported.
30	Ball break detection for TX ports (TX Ball break monitor)	AWR1843AOP architecture supports a ball break detection mechanism based on Impedance measurement at the TX output(s) to detect and report any large deviations that can indicate a ball break. Monitoring is done by TIs code running on BIST R4F and failure is reported to the Master R4F via Mailbox. It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4F.
31	RX loopback test	Built-in TX to RX loopback to enable detection of failures in the RX path(s), including Gain/ Noise figure, inter-RX balance, etc.
32	IF loopback test	Built-in IF (square wave) test tone input to monitor IF filter’s frequency response and detect failure.
33	RX saturation detect	Provision to detect ADC saturation due to excessive incoming signal level and/or interference.
34	Boot time LBIST for DSP core	AWR1843AOP device supports boot time LBIST for the DSP Core. LBIST can be triggered by the Master R4F application code during boot time.

(1) Monitoring is done by the TI's code running on BIST R4F. There are two modes in which it could be configured to report the temperature sensed via API by customer application.

a. Report the temperature sensed after every N frames

b. Report the condition once the temperature crosses programmed threshold.

It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4Fvia Mailbox.

(2) Monitoring is done by the TI's code running on BIST R4F.
There are two modes in which it could be configured to report the detected output power via API by customer application.

a. Report the power detected after every N frames

b. Report the condition once the output power degrades by more than configured threshold from the configured.

It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4F.

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9.1.1 Error Signaling Module

When a diagnostic detects a fault, the error must be indicated. AWR1843AOP architecture provides aggregation of fault indication from internal diagnostic mechanisms using a peripheral logic known as the error signaling module (ESM). The ESM provides mechanisms to classify faults by severity and allows programmable error response. Below is the high level block diagram for ESM module.

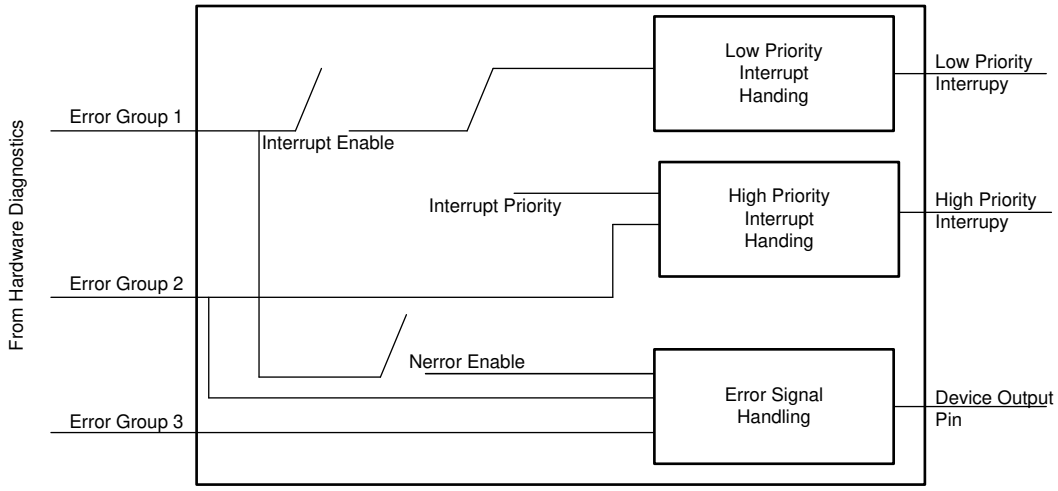

图 9-1. ESM Module Diagram

10 Applications, Implementation, and Layout

Note

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Application information can be found on AWR Application web page.

10.2 Reference Schematic

The reference schematic and power supply information can be found in the AWR1843AOP EVM Documentation.

Listed for convenience are: Design Files, Schematics, Layouts, and Stack up for PCB.

- Altium AWR1843AOP EVM Design Files
- AWR1843AOP EVM Schematic Drawing, Assembly Drawing, and Bill of Materials

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AWR1843AOP*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ALP0180A), the temperature range (for example, blank is the default commercial temperature range). 图 11-1 provides a legend for reading the complete device name for any *AWR1843AOP* device.

For orderable part numbers of *AWR1843AOP* devices in the ALP0180 package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *AWR1843AOP Device Errata*.

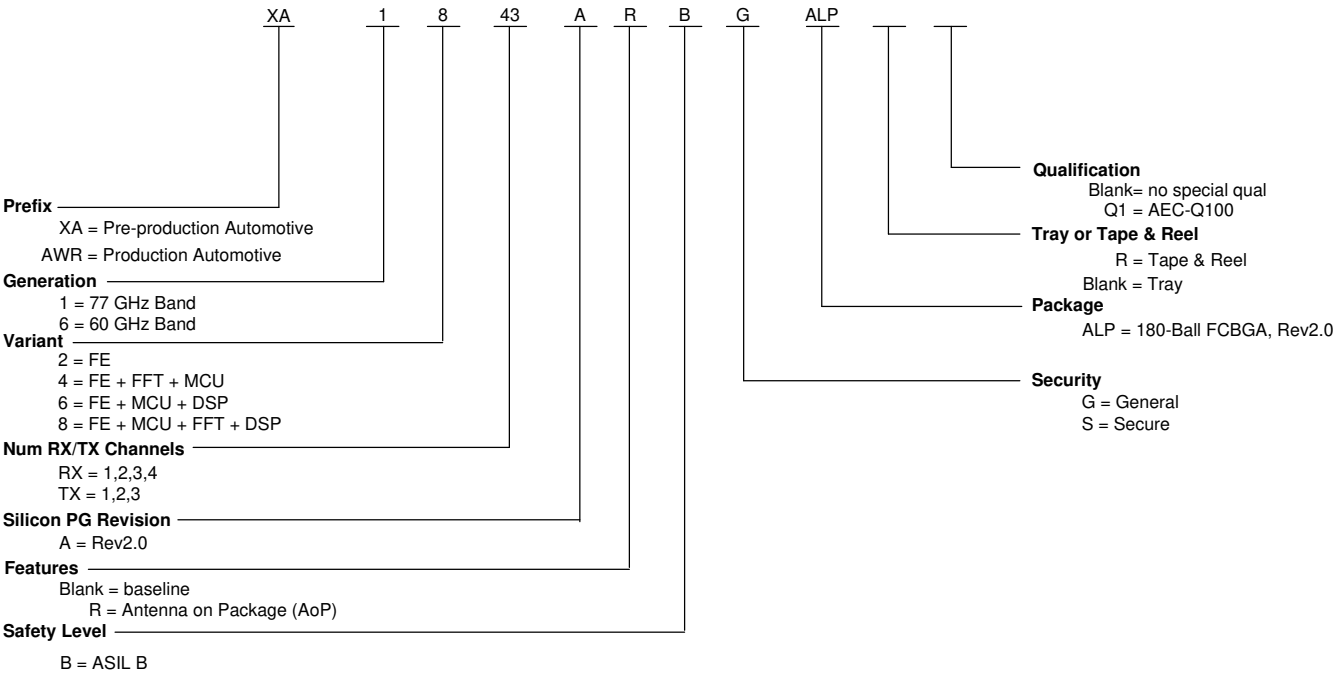

图 11-1. Device Nomenclature

11.2 Tools and Software

Models

AWR1843AOP IBIS model IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

11.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

Errata

AWR1843AOP device errata Describes known advisories, limitations, and cautions on silicon and provides workarounds.

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.5 Trademarks

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Arm® and Cortex® are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
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11.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

12.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

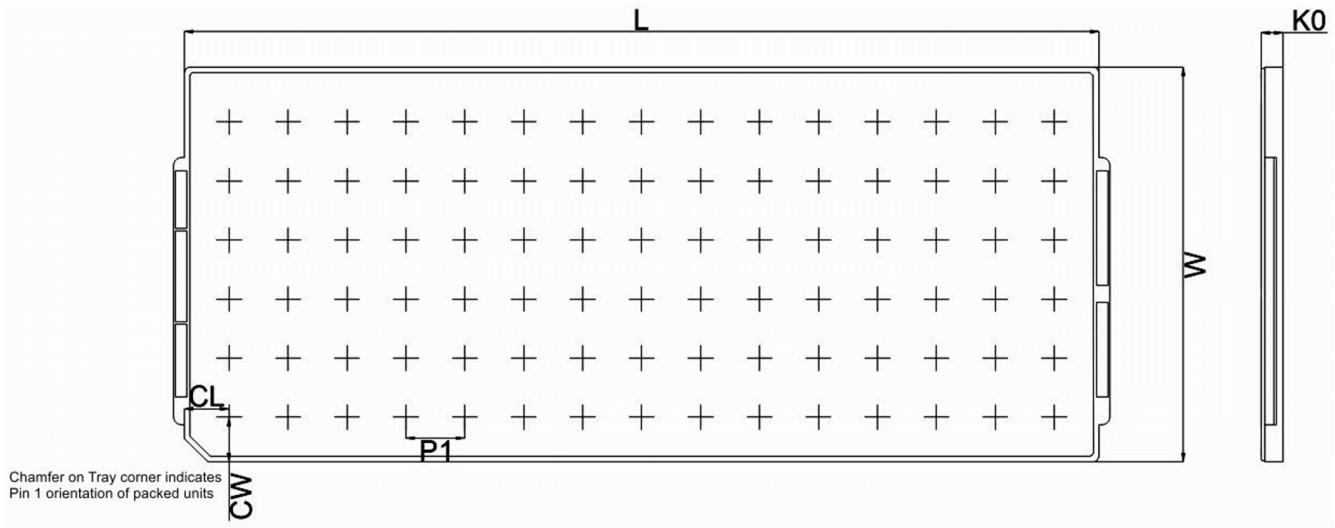
CAUTION

The following package information is subject to change without notice.

Note

Variability in the color (or appearance) of Texas Instrument’s (TI’s) Antenna-on-Package (AoP) product is normal and expected. This variation is not indicative of any degradation or variability to the performance specifications of the AoP products.

12.2 Tray Information for ALP, 15 × 15 mm



Device	Package Type	Package Name	Pins	SPQ	Unit Array Matrix	Max Temp. (°C)	L (mm)	W (mm)	K0 (mm)	P1 (mm)	CL (mm)	CW (mm)
XA1843ARBGALP	FCBGA	ALP	180	TBD	TBD	150	TBD	TBD	TBD	TBD	TBD	TBD

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XA1843ARBGALP	ACTIVE	FCBGA	ALP	180	1	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

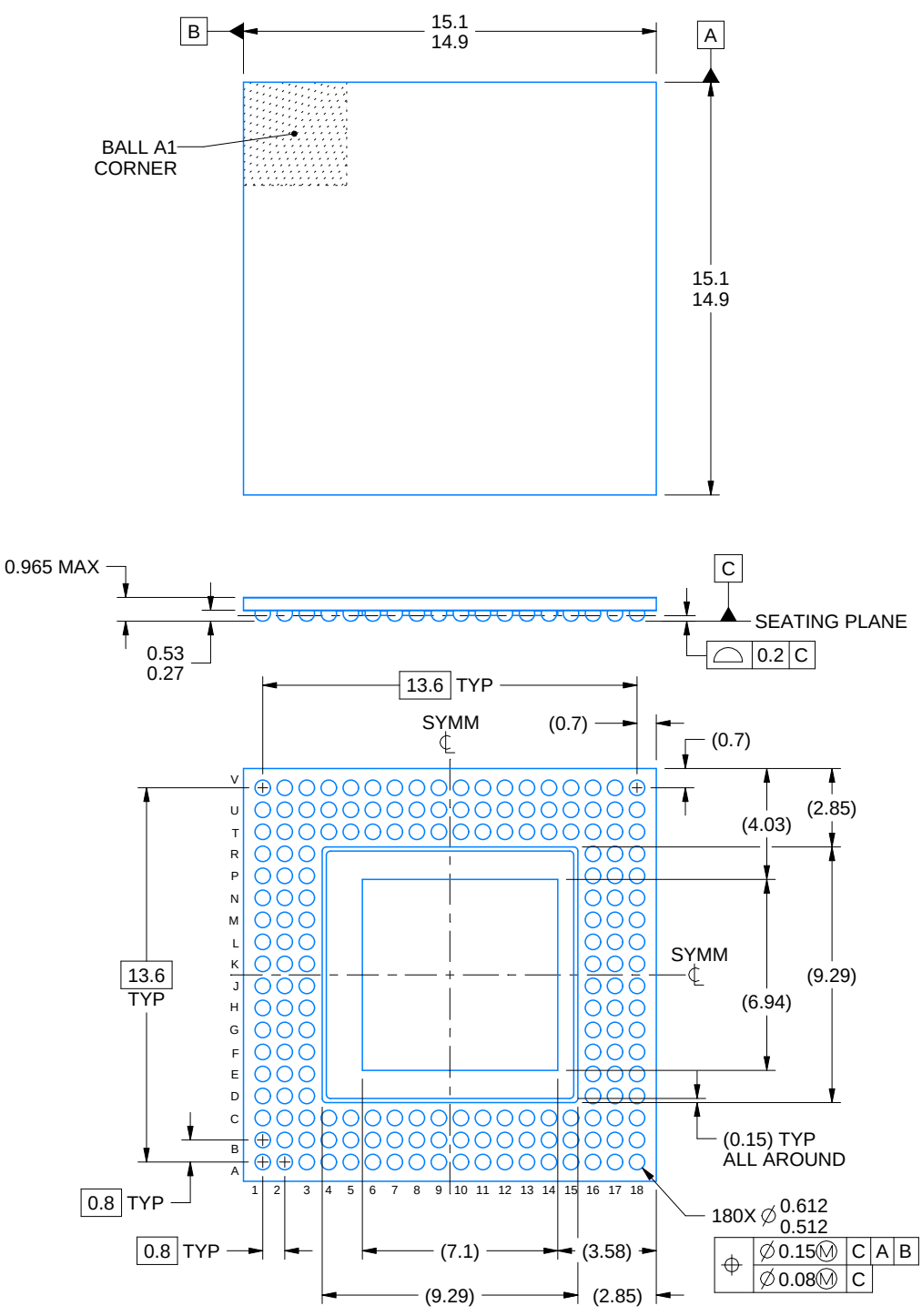
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

ALP0180A

FCBGA - 0.965 mm max height

PLASTIC BALL GRID ARRAY



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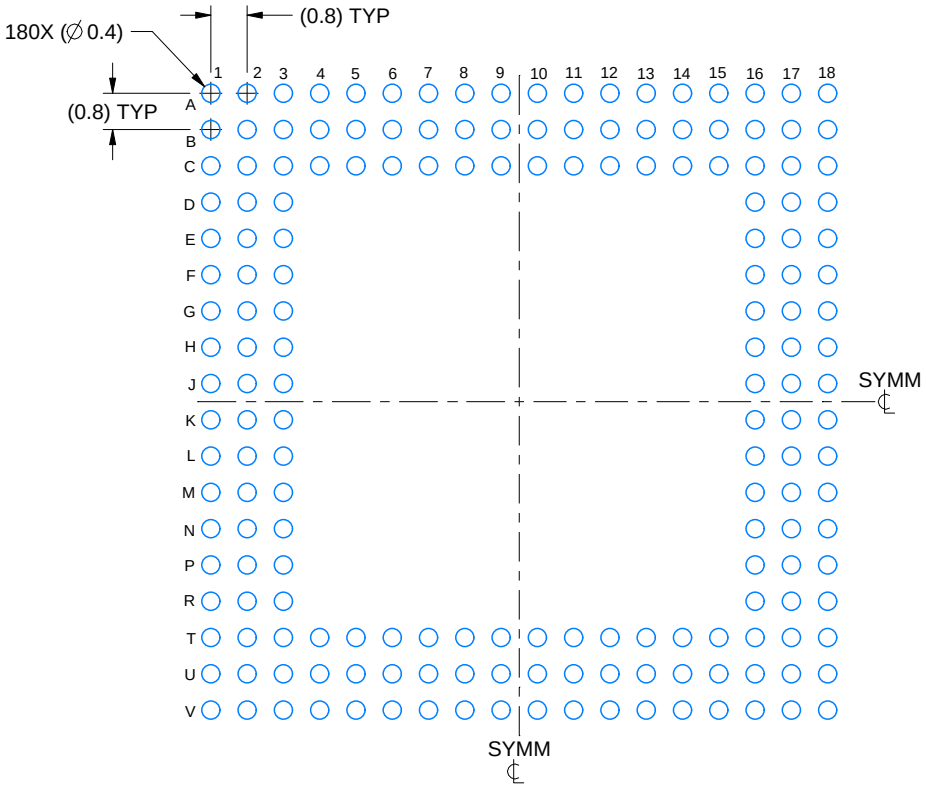
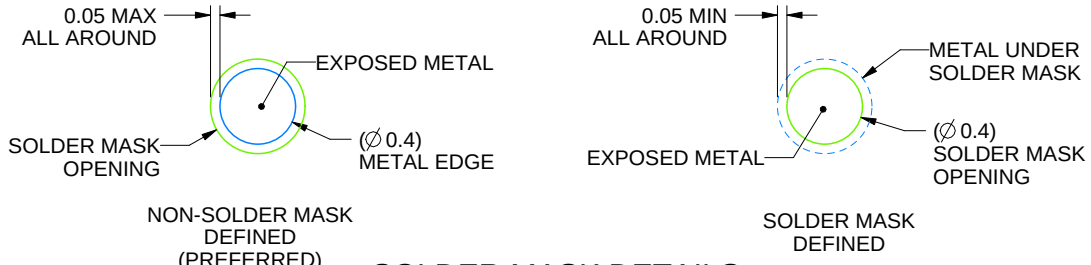
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X



SOLDER MASK DETAILS
NOT TO SCALE

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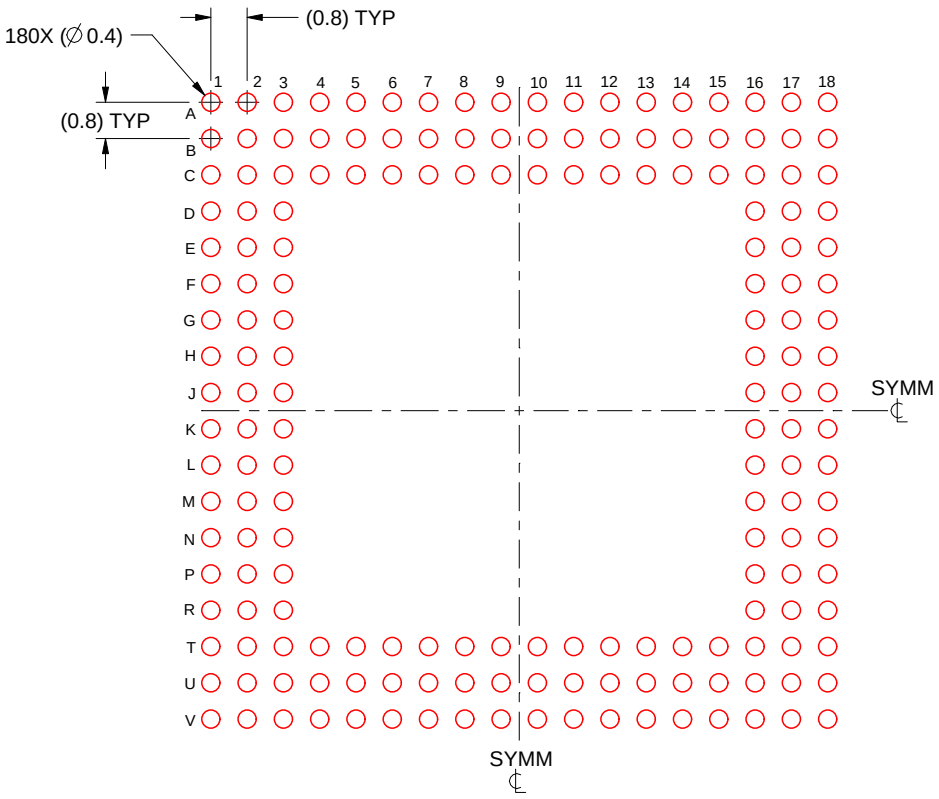
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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