

bq25071 带有 50mA 低压降稳压器 (LDO) 的 1A、单输入、单节 LiFePO₄ 线性电池充电器

1 特性

- 单节 LiFePO₄ 充电算法
- 30V 额定输入电压, 具有 10.5V 过压保护 (OVP)
- 50mA 集成低压降稳压器 (LDO)
- 可编程的充电电流 (通过 ISET 和 EN 端子)
- 充电电流调节精度为 7%
- 热调节和保护
- 软启动特性可降低浪涌电流
- 电池负温度系数 (NTC) 监视
- 充电状态指示

2 应用范围

- 智能电话
- 移动电话
- 便携式媒体播放器
- 低功耗手持设备

3 说明

bq25071 是一款高度集成的 LiFePO₄ 线性电池充电器, 面向空间受限的便携式应用。它由 USB 端口或交流适配器供电, 并为单节 LiFePO₄ 电池提供高达 1A 的充电电流。带 10.5V 输入过压保护的 30V 额定输入电压支持低成本、未稳压的适配器。

bq25071 具有一个电源输出, 可在对电池充电的同时为系统供电。输入电流既可通过 ISET 输入编程设定在 100mA 至 1A 范围内, 也可以在 USB500 模式下配置。另外, IC 中还集成了一个 4.9V ±10% 50mA LDO, 用于为低功耗外部电路供电。

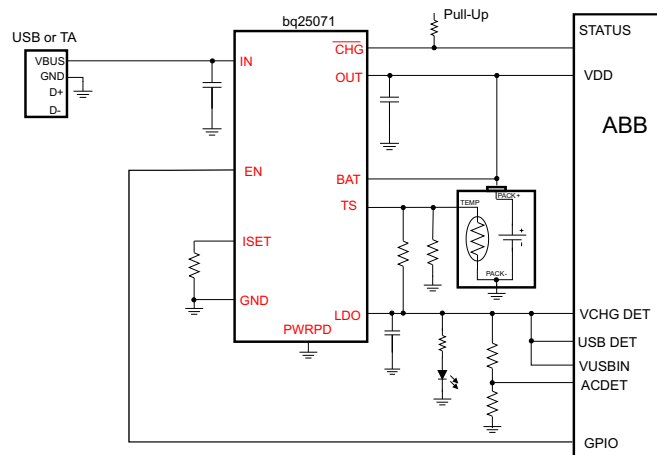
LiFePO₄ 充电算法可消除锂电池充电周期中所用的恒压模式控制下常见的电流逐渐减小过程, 可大幅缩短充电时间。在这种情况下, 电池将快速充电至过充电电压, 然后降至较低的浮充电压阈值。该充电器集成了具有充电电流和电压感应功能的功率级, 可在电流和电压调节环路中获得高级别的精度。内部控制环路可在整个充电周期内监视 IC 结温, 并在温度超过内部温度阈值时减小充电电流。

器件信息⁽¹⁾

部件号	封装	封装尺寸 (标称值)
bq25071	超薄小外形尺寸无引线封装 (WSO) (10)	2.00mm x 3.00mm

(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。

4 应用电路原理图



目录

1	特性	1	9.1	Overview	8
2	应用范围	1	9.2	Functional Block Diagram	9
3	说明	1	9.3	Feature Description	10
4	应用电路原理图	1	9.4	Device Functional Modes	12
5	修订历史记录	2	10	Application and Implementation	14
6	Device Comparison Table	3	10.1	Application Information	14
7	Pin Configuration and Functions	3	10.2	Typical Application	14
8	Specifications	4	11	Power Supply Recommendations	17
8.1	Absolute Maximum Ratings	4	12	Layout	17
8.2	Handling Ratings	4	12.1	Layout Guidelines	17
8.3	Recommended Operating Conditions	4	12.2	Layout Example	17
8.4	Thermal Information	4	13	器件和文档支持	19
8.5	Electrical Characteristics	5	13.1	Trademarks	19
8.6	Timing Requirements	6	13.2	Electrostatic Discharge Caution	19
8.7	Typical Characteristics	7	13.3	术语表	19
9	Detailed Description	8	14	机械封装和可订购信息	19

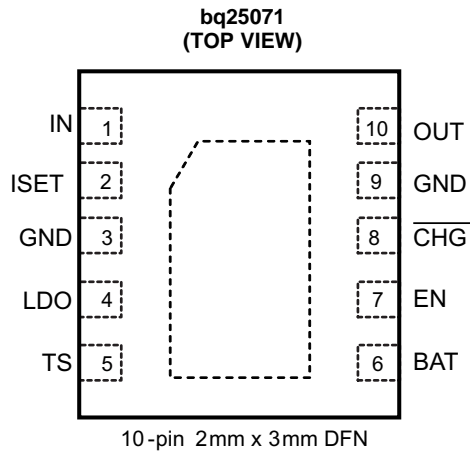
5 修订历史记录

日期	修订版本	注释
2014 年 7 月	*	最初发布。

6 Device Comparison Table

PART NUMBER	$V_{BAT(OVCH)}$	$V_{BAT(FLOAT)}$	$V_{(OVP)}$	$V_{(LDO)}$
bq25071DQCR	3.7 V	3.5 V	10.5 V	4.9 V
bq25071DQCT	3.7 V	3.5 V	10.5 V	4.9 V

7 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	Input power supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to GND with at least a 0.1 μ F ceramic capacitor.
ISET	2	O	Input current programming bias pin. Connect a resistor from ISET to GND to program the input current limit when the user programmable mode is selected by grounding the EN pin. The resistor range is between 1 k Ω and 10 k Ω to set the current between 100 mA and 1 A.
GND	3, 9	–	Ground pin. Connect to the thermal pad and the ground plane of the circuit.
LDO	4	O	LDO output. LDO is regulated to 4.9V and drives up to 50 mA. Bypass LDO to GND with a 0.1 μ F ceramic capacitor. LDO is enabled when $V_{(UVLO)} < V_{IN} < V_{(OVP)}$.
TS	5	I	Battery pack NTC monitoring input. Connect a resistor divider from LDO to GND with TS connected to the center tap to set the charge temperature window. The battery pack NTC is connected in parallel with the bottom resistor of the divider. See the Detailed Design Procedure section for details on the selecting the proper component values.
BAT	6	I	BAT is the sense input for the battery voltage. Connect BAT and OUT to the battery.
EN	7	I	Enable input. Drive EN high to disable the IC. Connect EN to GND to place the bq25071 in the user programmable mode using the ISET input where the input current is programmed. Leave EN floating to place the bq25071 in USB500 mode. See the Input Current Limit Control (EN) section for details on using the EN interface.
\overline{CHG}	8	O	Charge status indicator open-drain output. \overline{CHG} is pulled low while the device is charging the battery. \overline{CHG} goes high impedance when the battery is fully charged.
OUT	10	O	System output connection. Bypass the OUT to GND with a 1 μ F ceramic capacitor. Connect OUT and BAT together.
Thermal Pad	Pad	–	There is an internal electrical connection between the exposed thermal pad and the GND pin of the device. The thermal pad must be connected to the same potential as the GND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. GND pin must be connected to ground at all times.

8 Specifications

8.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage	IN (with respect to GND)	−0.3	30	V
	EN, TS (with respect to GND)	−0.3	7	V
Output Voltage	BAT, OUT, LDO, $\overline{\text{CHG}}$, ISET (with respect to GND)	−0.3	7	V
Input Current (Continuous)	IN		1.2	A
Output Current (Continuous)	BAT		1.2	A
Output Current (Continuous)	LDO		100	mA
Output Sink Current	$\overline{\text{CHG}}$		5	mA
Junction temperature, T _J		−40	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground pin unless otherwise noted.

8.2 Handling Ratings

		MIN	MAX	UNIT
T _{STG}	Storage temperature	−65	150	°C
V _{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	MAX	UNITS
V _{IN}	IN voltage	3.75 ⁽¹⁾	28	V
	IN operating voltage	3.75 ⁽¹⁾	10.2	
I _{IN}	Input current, IN		1	A
I _{OUT}	Output Current in charge mode, OUT		1	A
T _J	Junction Temperature	0	125	°C

- (1) Charge current may be limited at low input voltages due to the dropout of the device.

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾		bq25071	UNIT
		DQC (10 PINS)	
R _{θJA}	Junction-to-ambient thermal resistance	61.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	65.5	
R _{θJB}	Junction-to-board thermal resistance	22.8	
Ψ _{JT}	Junction-to-top characterization parameter	1.5	
Ψ _{JB}	Junction-to-board characterization parameter	22.7	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	5.5	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

8.5 Electrical Characteristics

Over junction temperature range $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V _(UVLO)	Under-voltage lock-out	V _{IN} : 0 V → 4 V	3.15	3.30	3.55	V
V _{HYS(UVLO)}	Hysteresis on V _(UVLO)	V _{IN} : 4 V → 0 V		250		mV
V _{IN(SLP)}	Valid input source threshold V _{IN(SLP)} above V _{BAT}	Input power good if V _{IN} > V _{BAT} + V _{IN(SLP)} V _(BAT) = 3.6 V, V _{IN} : 3.5 V → 4 V	30	75	150	mV
V _{HYS(INSLP)}	Hysteresis on V _{IN(SLP)}	V _(BAT) = 3.6 V, V _{IN} : 4 V → 3.5 V	18	32	54	mV
t _{DGL(NO-IN)}	Delay time, input power loss to charger turn-off	Time measured from V _{IN} : 5 V → 2.5 V 1 μs fall-time		32		ms
V _{OVP}	Input over-voltage protection threshold	V _{IN} : 5 V → 11 V	10.2	10.5	10.8	V
V _{HYS(OVP)}	Hysteresis on OVP	V _{IN} : 11 V → 5 V		100		mV
QUIESCENT CURRENT						
I _{BAT(PDWN)}	Battery current into BAT, No input connected	V _{IN} = 0 V ⁽¹⁾ , V _(CHG) = Low, T _J = 85°C			6	μA
I _{IN(STDBY)}	Standby current into IN pin	EN = HI, V _{IN} = 5.5V			0.25	mA
		EN = HI, V _{IN} ≤ V _(OVP)			0.5	
		EN = HI, V _{IN} > V _(OVP)			2	
BATTERY CHARGER FAST-CHARGE						
V _{BAT(REG)}	Battery charge regulation voltage	T _A = 0°C to 125°C, I _{OUT} = 50 mA	3.455	3.5	3.545	V
		T _A = 25°C	3.455	3.5	3.539	
V _{BAT(OVCH)}	Battery overcharge voltage threshold		3.62	3.7	3.78	V
I _{IN(RANGE)}	User programmable input current limit range	R _(ISET) = 1 kΩ to 10kΩ, EN = V _{SS}	100		1000	mA
I _{IN(LIM)}	Input current limit, or fast-charge current	EN = FLOAT	435	467	500	mA
		EN = V _{SS}	K _{ISET} /R _{ISET}			
K _{ISET}	Fast charge current factor	R _(ISET) = 1 kΩ to 10 kΩ, EN = V _{SS}	900	1000	1100	AΩ
V _{DO(IN-OUT)}	V _{IN} – V _{OUT}	V _{IN} = 3.55 V, I _{OUT} = 0.75 A		500	900	mV
ISET SHORT CIRCUIT PROTECTION						
R _{ISET(MAX)}	Highest resistor value considered a short fault	R _(ISET) : 900 Ω → 300 Ω, I _{OUT} latches off, Cycle power to reset, Fault range > 1.10 A	430		700	Ω
I _{OUT(CL)}	Maximum OUT current limit regulation (Clamp)		1.07		2	A
PRE-CHARGE AND CHARGE DONE						
V _(LOWV)	Pre-charge to fast-charge transition threshold		0.5	0.7	0.9	V
I _(PRECHARGE)	Precharge current to BAT during precharge mode	V _(BAT) = 0 V to 0.7 V	41.5	45	48.5	mA
RECHARGE OR REFRESH						
V _(RCH)	Recharge detection threshold	V _(BAT) falling	3.1	3.3	3.5	V
LDO						
V _(LDO)	LDO Output Voltage	V _{IN} = 5 V to 10.5 V, I _(LDO) = 0 mA to 50 mA	4.7	4.9	5.1	V
I _(LDO)	Maximum LDO Output Current		60			mA
V _(DO)	Dropout Voltage	V _{IN} = 4.5V, I _(LDO) = 50 mA		200	350	mV

(1) Force $V_{(CHG)}$

Electrical Characteristics (continued)

Over junction temperature range $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS ON EN						
V_{IL}	Logic low input voltage				0.4	V
V_{IH}	Logic high input voltage		1.4			V
$V_{(FLT)}$	Logic FLOAT input voltage		600	850	1100	mV
$I_{(FLT)ikg}$	Maximum leakage sink or source current to keep in FLOAT				1	μA
$I_{EN(DRIVE)}$	Minimal drive current from an external device for Low or High		8			μA
BATTERY-PACK NTC MONITOR (TS)						
$V_{(COLD)}$	TS Cold Threshold	$V_{(TS)}$ Rising	24.5	25	25.5	% V_{LDO}
$V_{(CUTOFF)}$	TS Cold Cutoff Threshold	$V_{(TS)}$ Falling		1		% V_{LDO}
$V_{(HOT)}$	TS Hot Threshold	$V_{(TS)}$ Falling	12	12.5	13	% V_{LDO}
$V_{(HOT)(HYS)}$	TS Hot Cutoff Threshold	$V_{(TS)}$ Rising		1		% V_{LDO}
CHG OUTPUT						
V_{OL}	Output LOW voltage	$I_{(SINK)} = 1\text{ mA}$			0.45	V
I_{IH}	Leakage current	CHG = 5 V			1	μA
THERMAL REGULATION						
$T_{J(REG)}$	Temperature Regulation Limit	T_J rising		125		$^{\circ}\text{C}$
$T_{J(OFF)}$	Thermal shutdown temperature	T_J rising		155		$^{\circ}\text{C}$
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis	T_J falling		20		$^{\circ}\text{C}$

8.6 Timing Requirements

			MIN	TYP	MAX	UNIT
INPUT						
$t_{BLK(OVP)}$	Input overvoltage blanking time			100		μs
$t_{REC(OVP)}$	Input overvoltage recovery time	Time measured from $V_{IN}: 11\text{ V} \rightarrow 5\text{ V}$ 1 μs fall-time to LDO = HI, $V_{(BAT)} = 3.5\text{ V}$		100		μs
ISSET SHORT CIRCUIT PROTECTION						
$t_{DGL(SHORT)}$	Deglintch time transition from $I_{(SET)}$ short to I_{OUT} disable	Clear fault by cycling $V_{(BUS)}$ or EN		1.5		ms
PRE-CHARGE AND CHARGE DONE						
$t_{DGL1(LOWV)}$	Deglintch time on pre-charge to fast-charge transition			25		ms
$t_{DGL2(LOWV)}$	Deglintch time on fast-charge to pre-charge transition			25		ms
RECHARGE OR REFRESH						
$t_{DGL(RCH)}$	Deglintch time, recharge threshold detected	$V_{(BAT)}$ falling to New Charge Cycle		25		ms
BATTERY-PACK NTC MONITOR (TS)						
$t_{dgl(TS)}$	Deglintch for TS Fault	Fault detected on TS to stop charge		25		ms

8.7 Typical Characteristics

$V_{IN} = 5\text{ V}$, $V_{BAT} = 3.2\text{ V}$, $I_{(CHG)} = 280\text{ mA}$, Typical Application Circuit

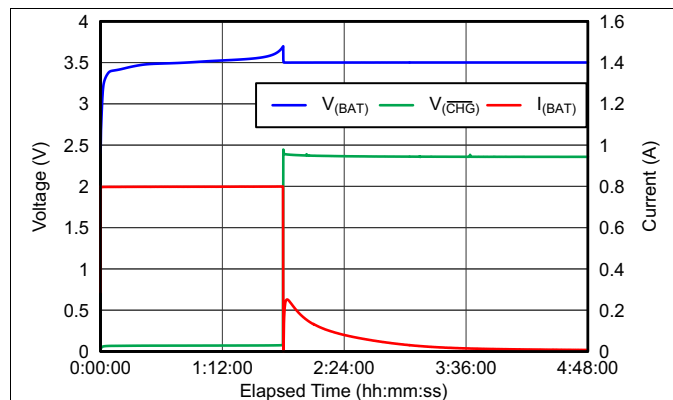


Figure 1. Voltage and Current vs Elapsed Time

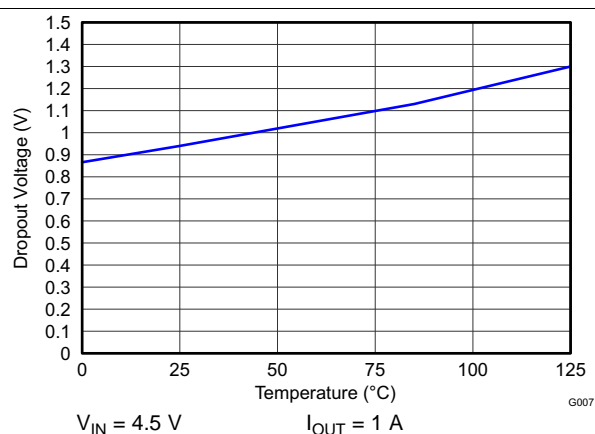


Figure 2. Dropout Voltage vs Temperature

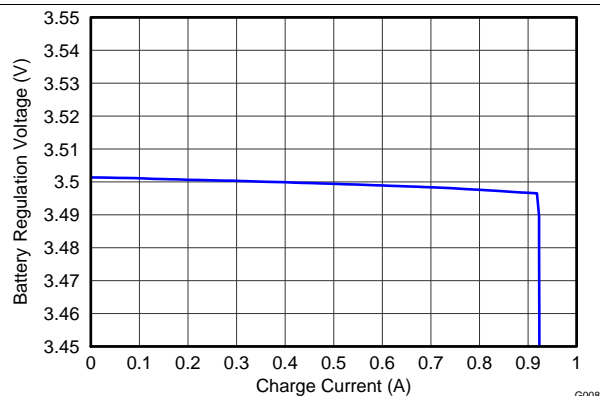


Figure 3. Battery Regulation Voltage vs Charge Current

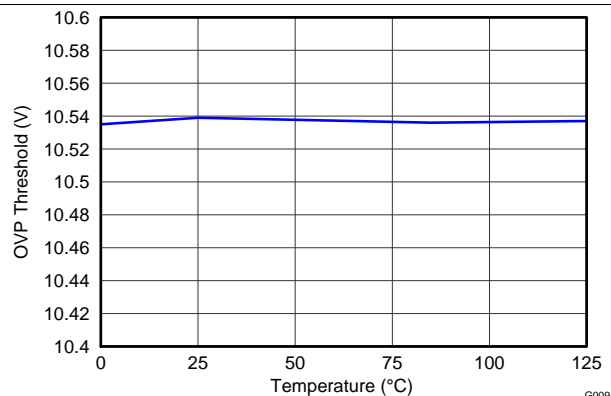


Figure 4. OVP Threshold vs Temperature

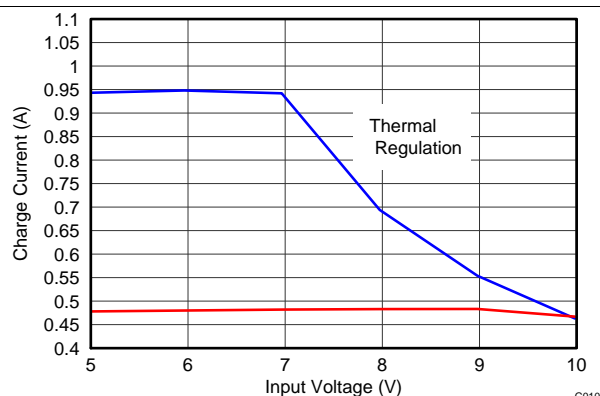


Figure 5. Charge Current vs Input Voltage

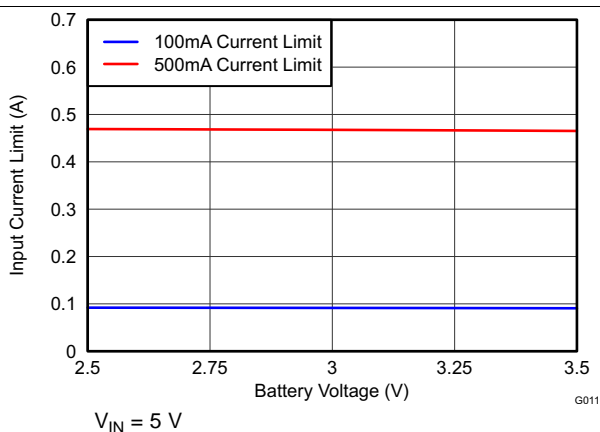


Figure 6. Input Current Limit vs Battery Voltage

9 Detailed Description

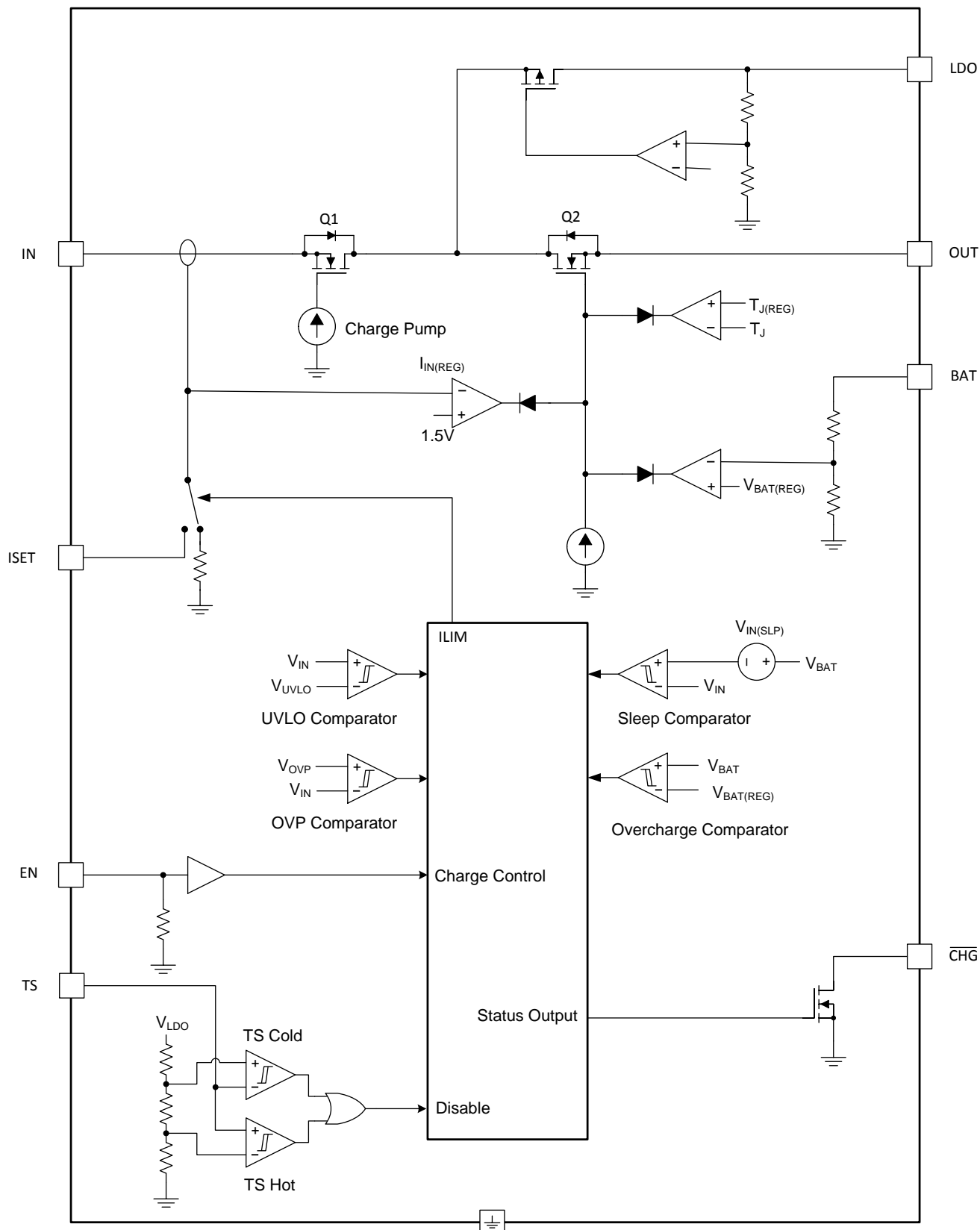
9.1 Overview

The bq25071 is a highly integrated, linear, LiFePO_4 battery charger targeted at space-limited portable applications. It accepts power from either a USB port or AC adapter and charges a single-cell LiFePO_4 battery with up to 1 A of charge current. The 30 V input rating with 10.5 V input overvoltage protection supports low-cost unregulated adapters.

The bq25071 has a single power output that simultaneously charges the battery and powers the system. The input current is programmable from 100 mA up to 1 A using the ISET input or configurable for USB500. There is also a 4.9 V $\pm 10\%$ 50 mA LDO is integrated into the IC for supplying low power external circuitry.

The LiFePO_4 charging algorithm removes the constant voltage mode control typically used in Li-Ion battery charge cycles which reduces charge time significantly. Instead, the battery is fast charged to the overcharge voltage and then allowed to relax to a lower float charge voltage threshold. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, and charge status display. During the charge cycle, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Input Overvoltage Protection

The bq25071 contains an input overvoltage protection circuit that disables the LDO output and charging when the input voltage rises above $V_{(OVP)}$. This prevents damage from faulty adapters. The OVP circuitry contains an 100 μ s blanking period that prevents ringing on the input from line transients from tripping the OVP circuitry falsely. If an adapter with an output greater than $V_{(OVP)}$ is plugged in, the IC completes soft-start power up and then shuts down if the voltage remains above $V_{(OVP)}$ after 100 μ s. The LDO remains off and charging remains disabled until the input voltage falls below $V_{(OVP)}$.

9.3.2 Undervoltage Lockout (UVLO)

The bq25071 remains in power down mode when the input voltage is below the undervoltage lockout threshold ($V_{(UVLO)}$). During this mode, the control input (EN) is ignored. The LDO, the charge FET connected between IN and OUT are off and the status output (CHG) is high impedance. Once the input voltage rises above $V_{(UVLO)}$, the internal circuitry is turned on and the normal operating procedures are followed.

9.3.3 External NTC Monitoring (TS)

The bq25071 features a flexible, voltage based external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging, the voltage at TS is continuously monitored. If the voltage at the TS pin is outside of the operating range ($V_{(HOT)}$ to $V_{(COLD)}$) for longer than the built in 25 ms deglitch time, charging is suspended. When the voltage measured at TS returns to within the operation window, charging resumes. When a battery pack temperature fault occurs charging is suspended, but the CHG output remains low and continues to indicate charging.

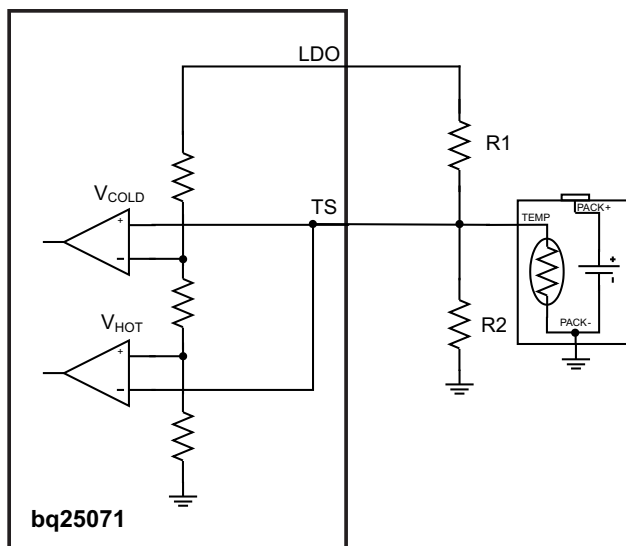
The temperature thresholds are programmed using a resistor divider from LDO to GND with the NTC thermistor connected to the center tap from TS to GND. See [Figure 7](#) for the circuit example. The value of R1 and R2 are calculated using the following equations:

$$R1 = \frac{-R2 \times RHOT \times (0.125 - 1)}{0.125 \times (R2 + RHOT)} \quad (1)$$

$$R2 = \frac{-RHOT \times RCOLD \times (0.125 - 0.250)}{RHOT \times 0.250 \times (0.125 - 1) + RCOLD \times 0.125 \times (1 - 0.250)} \quad (2)$$

RHOT is the expected thermistor resistance at the programmed hot threshold; RCOLD is the expected thermistor resistance at the programmed cold threshold.

Feature Description (continued)



For applications that do not require the TS monitoring function, set $R1 = 490\text{ k}\Omega$ and $R2 = 100\text{ k}\Omega$ to set the TS voltage at a valid level and maintain charging.

Figure 7. NTC Monitoring Function

9.3.4 50 mA LDO (LDO)

The LDO output of the bq25071 is a low dropout linear regulator (LDO) that supplies up to 50 mA while regulating to $V_{(LDO)}$. The LDO is active whenever the input voltage is above $V_{(UVLO)}$ and below $V_{(OVP)}$. It is not affected by the EN input. The LDO output is used to power and protect circuitry such as USB transceivers from transients on the input supply.

9.3.5 Charge Status Indicator ($\overline{\text{CHG}}$)

The bq25071 contains an open drain $\overline{\text{CHG}}$ output that indicates charging state and faults. When charging a battery in precharge or fastcharge mode, the CHG output is pulled to GND. Once the BAT output reaches the overcharge voltage threshold, CHG goes high impedance to signal the battery is fully charged. When the battery voltage drops below the recharge voltage threshold the CHG output is pulled low to signal the host of a new charge cycle. Connect $\overline{\text{CHG}}$ to the required logic level voltage through a 1 k Ω to 100 k Ω resistor to use the signal with a microprocessor. $I_{(\overline{\text{CHG}})}$ must be below 5 mA.

The IC monitors the CHG pin when no input is connected to verify if the system circuitry is active. If the voltage at CHG is logic being drive low when no input is connected, the TS circuit is turned off for a low quiescent current state. Once the voltage at CHG increases above logic high, the TS circuit is turned on.

9.3.6 Input Current Limit Control (EN)

The bq25071 contains a 3-state that controls the input current limit. Drive EN low to program the input current limit to the user defined value programmed using ISET. Drive EN high to place the bq25071 in USB suspend mode. In USB suspend mode, the input current into bq25071 is reduced. Leaving EN unconnected or connected to a high impedance source programs the USB500 input current limit.

Table 1. EN Input Definition

EN	MODE
Low	ISET
Hi-Z	USB500
Hi	USB Suspend

9.4 Device Functional Modes

9.4.1 Charging Operation

The bq25071 uses a charge algorithm that is unique to LiFePO₄ chemistry cells. The current taper typically seen as part of the constant voltage mode control usually present in Li-Ion battery charge cycles is replaced with a floating regulation voltage with minimal charging current. This dramatically decreases the charge time. When the bq25071 is enabled by EN, the battery voltage is monitored to verify which stage of charging must be used. When $V_{(BAT)} < V_{(LOWV)}$, the bq25071 charges in precharge mode; when $V_{(BAT)} > V_{(LOWV)}$, the normal charge cycle is used.

9.4.1.1 Charger Operation with Minimum System Voltage Mode Enabled

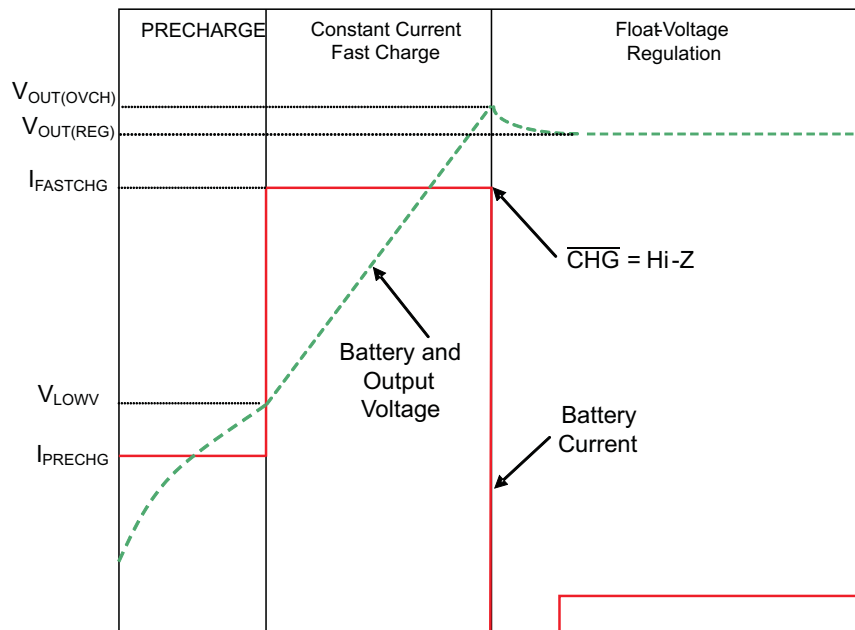


Figure 8. Typical Charging Cycle with Minimum System Voltage Enabled

9.4.1.2 Precharge Mode ($V_{(BAT)} \leq V_{(LOWV)}$)

The bq25071 enters precharge mode when $V_{BAT} \leq V_{(LOWV)}$. Upon entering precharge mode, the battery is charged with a 47.5 mA current and \overline{CHG} goes low.

9.4.1.3 Fast Charge Mode

Once $V_{(BAT)} > V_{(LOWV)}$, the bq25071 enters constant current (CC) mode where charge current is regulated using the internal MOSFETs between IN and OUT. The total current is shared between the output load and the battery. Once the battery voltage charges up to $V_{BAT(OVCH)}$, the \overline{CHG} output goes high indicating the charge cycle is complete and the bq25071 switches the battery regulation voltage to $V_{BAT(REG)}$. The battery voltage is allowed to relax down to $V_{BAT(REG)}$. The charger remains enabled and regulates the output to $V_{BAT(REG)}$. If at any time the battery falls below $V_{(RCH)}$, the charge cycle restarts.

Device Functional Modes (continued)

9.4.2 Programmable Input Current Limit (ISET)

When the charger is enabled, and the user programmable current limit is selected by the EN input, internal circuits generate a current proportional to the input current at the ISET input. The current out of ISET is 1/1000 ($\pm 10\%$) of the charge current. This current, when applied to the external charge current programming resistor, R1 (Figure 9), generates an analog voltage that is regulated to program the fast charge current. Connect a resistor from ISET to GND to program the input current limit using the following equation:

$$I_{(IN_LIM)} = \frac{K_{(ISET)}}{R_{(ISET)}} = \frac{1000A \times \Omega}{R_{(ISET)}} \quad (3)$$

$I_{(IN_LIM)}$ is programmable from 100 mA to 1 A. The voltage at ISET can be monitored by an external host to calculate the charging current to the battery. The input current is related to the ISET voltage using the following equation:

$$I_{IN} = V_{(ISET)} \times \frac{1000}{R_{(ISET)}} \quad (4)$$

Monitoring the ISET voltage allows for the host to calculate the actual charging current and therefore perform more accurate termination. The input current to the system must be monitored and subtracted from the current into the bq25071 which is show by $V_{(ISET)}$.

9.4.3 Thermal Regulation and Thermal Shutdown

The bq25071 contains a thermal regulation loop that monitors the die temperature continuously. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high V_{IN} conditions. If the die temperature increases to $T_{J(OFF)}$, the IC is turned off. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the device turns on and returns to thermal regulation. Continuous overtemperature conditions result in the pulsing of the load current. If the junction temperature of the device exceeds $T_{J(OFF)}$, the charge FET is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

Note that these features monitor the die temperature of the bq25071. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm.

10 Application and Implementation

10.1 Application Information

The typical application circuit uses a single output which charges the battery and powers the system. Additionally a 50-mA LDO can supply a low power external circuit.

The bq25071EVM-658 evaluation module (EVM) is a complete charger module for evaluating the bq25071. Refer to [SLUUB49](#).

10.2 Typical Application

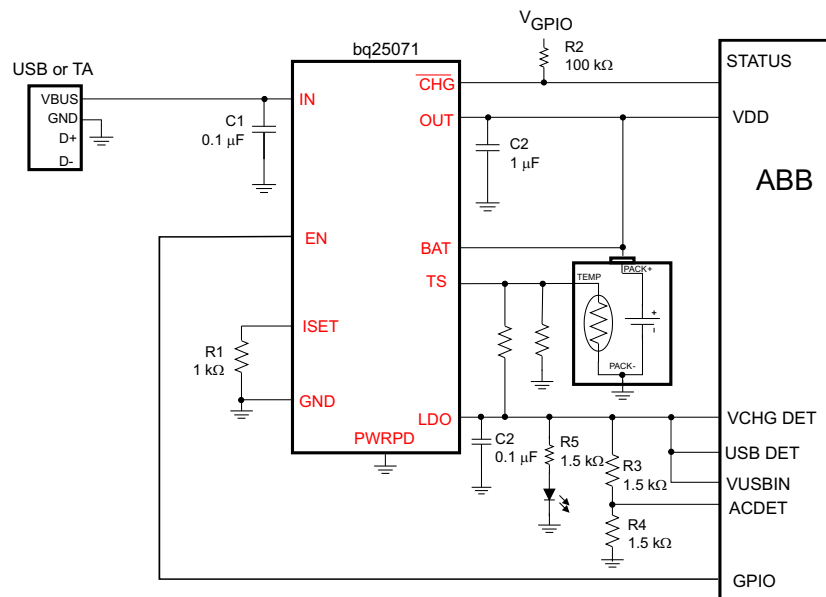


Figure 9. bq25071 Typical Application Circuit

10.2.1 Design Requirements

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Input supply range	5 V $\pm 5\%$
Output voltage range	3.5 V
Output current rating	1000 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Selection of Input and Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. For normal charging applications, a 0.1 μF ceramic capacitor, placed in close proximity to the IN pin and GND pad works best. In some applications, depending on the power supply characteristics and cable length, it may be necessary to increase the input filter capacitor to avoid exceeding the OVP voltage threshold during adapter hot plug events where the ringing exceeds the deglitch time.

The charger in the bq25071 requires a capacitor from OUT to GND for loop stability. Connect a 1 μF ceramic capacitor from OUT to GND close to the pins for best results. More output capacitance may be required to minimize the output drop during large load transients.

The LDO also requires an output capacitor for loop stability. Connect a 0.1 μF ceramic capacitor from LDO to GND close to the pins. For improved transient response, this capacitor may be increased.

10.2.2.2 Thermal Considerations

The bq25071 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* ([SLUA271](#)).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

Where:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \quad (5)$$

T_J = chip junction temperature

T_A = ambient temperature

P_D = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P_D , is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Due to the charge profile of LiFePO_4 batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See the charging profile, [Figure 8](#). If the board thermal design is not adequate the programmed fast charge rate current may not be achieved under maximum input voltage and minimum battery voltage, as the thermal loop can be active, effectively reducing the charge current to avoid excessive IC junction temperature.

10.2.3 Application Curves

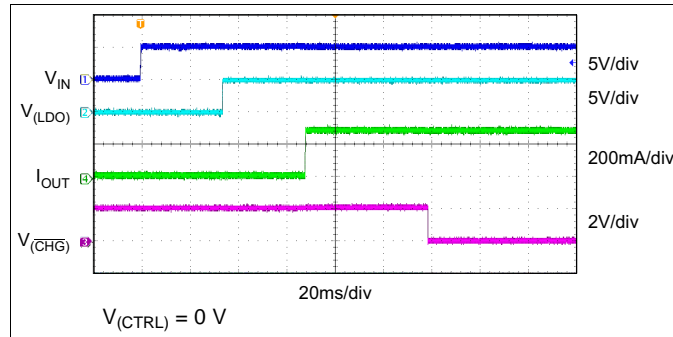


Figure 10. Adapter Plug-In With Battery Connected

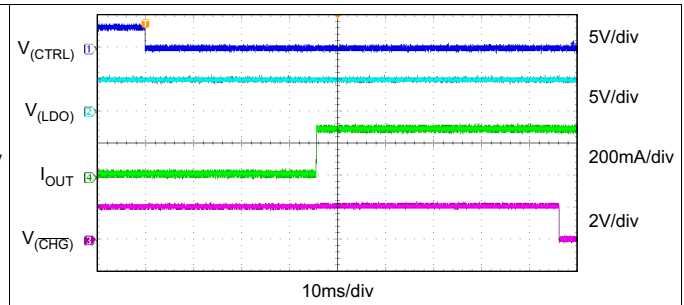


Figure 11. Charger Enable Using EN

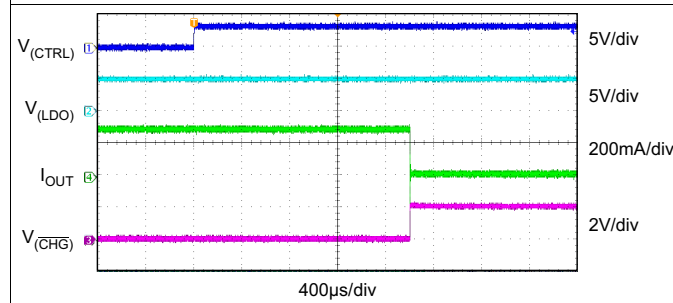


Figure 12. Charger Disable Using EN

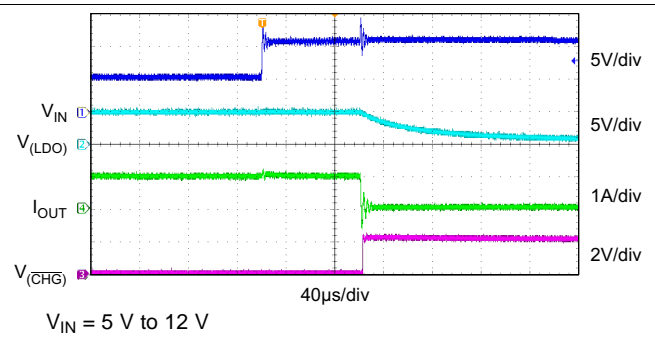


Figure 13. OVP Fault

11 Power Supply Recommendations

In a typical application, the system is powered by a USB port or USB wall adapter.

The wide input voltage range supports low cost and unregulated adapters.

The minimum input voltage - where the charging process starts with a reduced charging current - could be 3.75 V. The maximum supported input voltage is up to 10 V; the overvoltage protection kicks in at 10.5 V and the maximum input voltage rating is 30 V Input Rating.

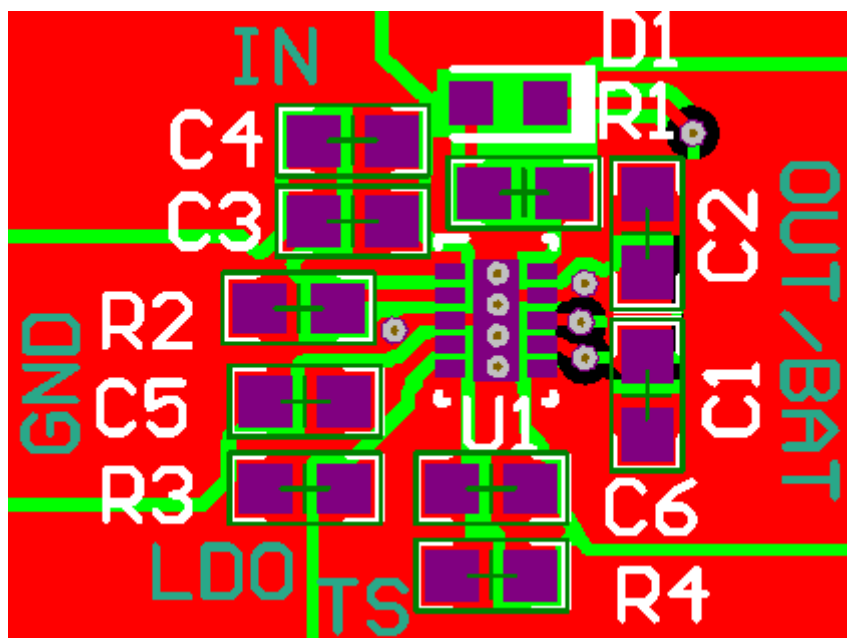
12 Layout

12.1 Layout Guidelines

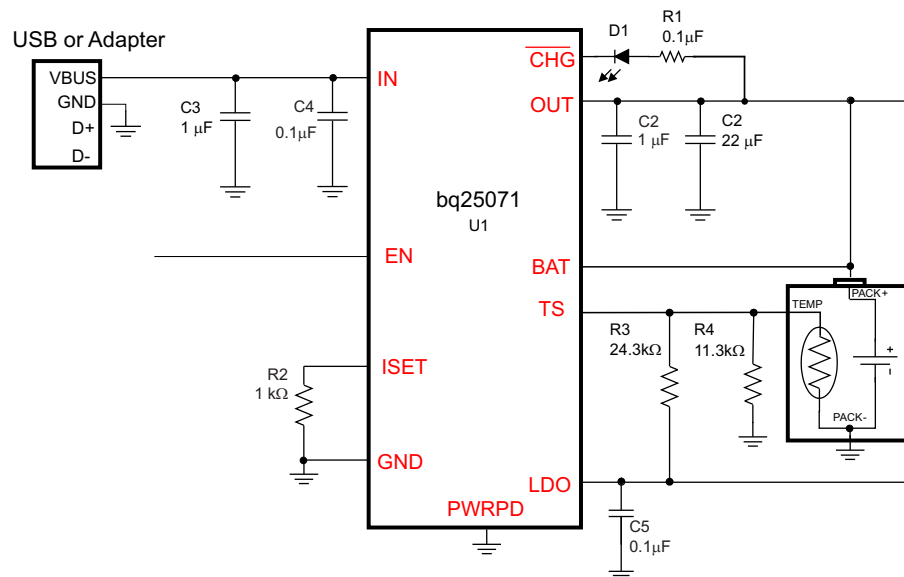
It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq25071, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq25071 is packaged in a thermally enhanced SON package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* ([SLUA271](#)).

12.2 Layout Example



The bottom plane is a ground plane that is connected to the top through vias.

Layout Example (continued)

Figure 14. Schematic

13 器件和文档支持

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 术语表

[SLYZ022](#) — *TI* 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25071DQCR	ACTIVE	WSO	DQC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25071	Samples
BQ25071DQCT	ACTIVE	WSO	DQC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25071	Samples

(1) The marketing status values are defined as follows:

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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

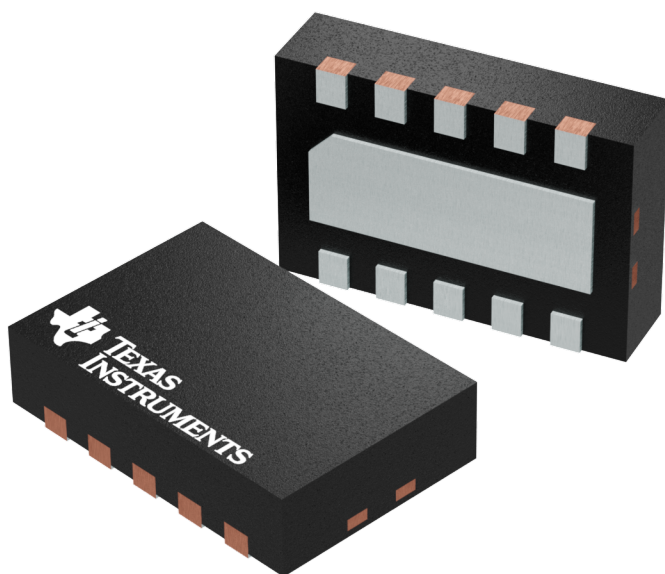
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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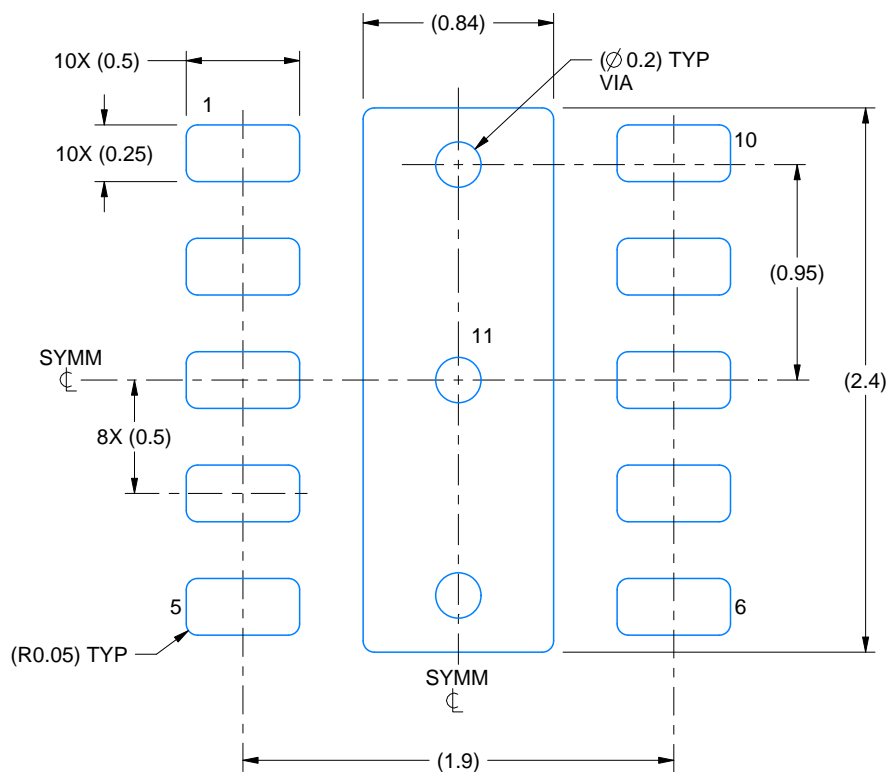
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

EXAMPLE BOARD LAYOUT

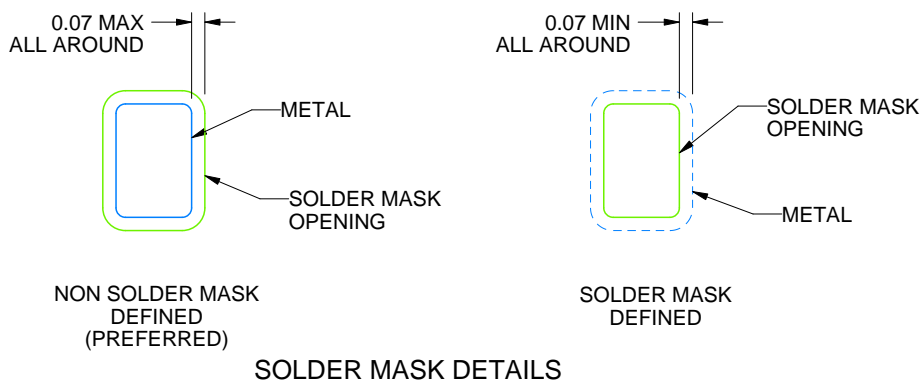
DQC0010A

WSN - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 30X



SOLDER MASK DETAILS

4218281/B 11/2016

NOTES: (continued)

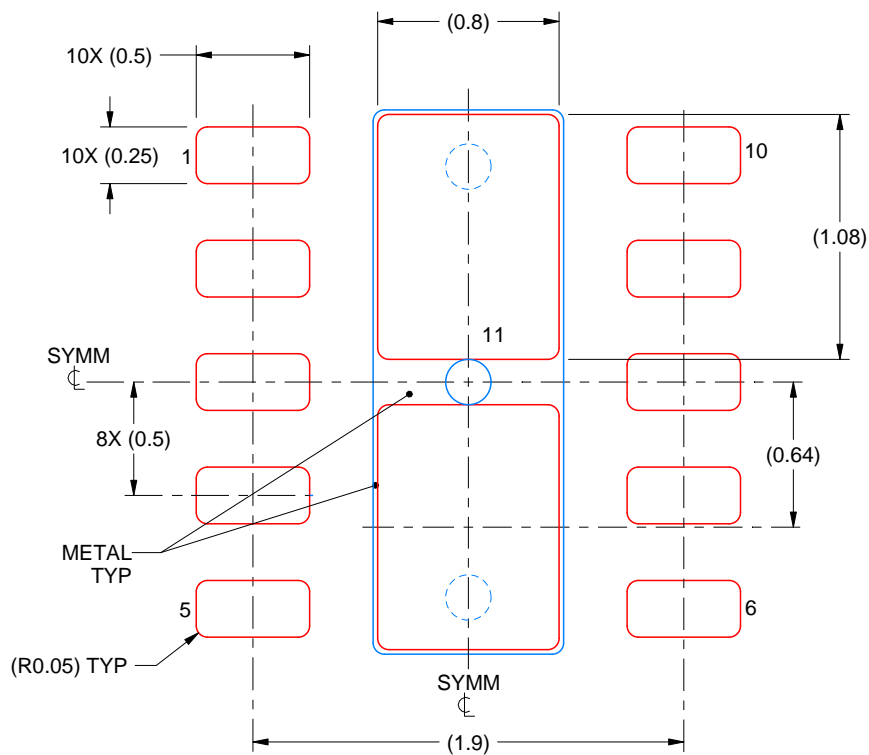
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DQC0010A

WSN - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 30X

4218281/B 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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