具有单线制 HDQ 接口和温度传感器的 4Kb EEPROM

查询样品: **bq2028**

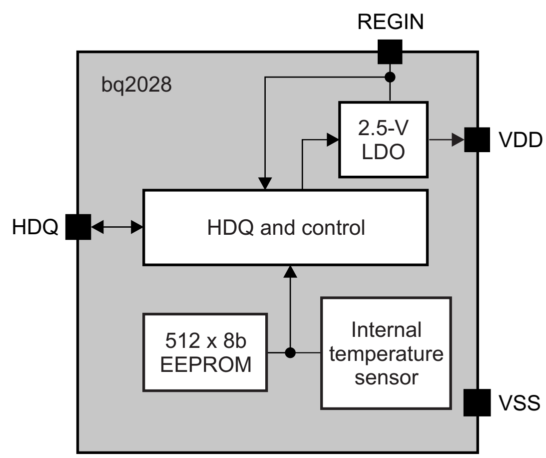
特性

- 串行非易失性存储器 **(NVM)**
  - **512** 字节 **(4Kb) EEPROM**
  - 提供用于 **bq27505-E1** 电量计的电池组非易失性存储器 **(NVM)** 存储：
    - 制造数据
    - 操作历史记录
    - 电阻值表
    - 健康信息状态
- 单线制 **HDQ** 通信端口
- 集成型 **2.5V** 低压降 **(LDO)** 线性稳压器
  - 借助自动超时和**/**或者主机命令的超低功耗**“**关断**”**模式（典型值**1μA**）
  - 通过 **HDQ** 中断从关断中唤醒
- 内部芯片温度传感器
  - **±5°C** 范围 **= -40°C** 至 **85°C**
  - 主机固件执行的原始 **AD** 到温度转换
- 封装
  - **12** 引脚，**1490μm x 2350μm (YZG)**，最大厚度 **0.625mm**，焊球间距 **0.5mm**

说明

德州仪器 (TI) 生产的具有集成温度传感器和 LDO 线性稳压器的 bq2028 串联 4Kb 非易失性存储器 (EEPROM) 可提供针对诸如 bq27505-E1 单节系统侧电池电量计解决方案的电池组存储器存储和温度监视。

bq2028 使用一个软件开销最小而又确保无错数据传输的协议，通过一个单线制 HDQ 接口与 bq 27505-E1 电量计进行通信。



English Data Sheet: SLUSB22

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

AVAILABLE OPTIONS

PRODUCTION PART #	PACKAGE	T_A	TAPE and REEL QUANTITY
bq2028YZGR	12-pin WCSP	–40°C to 85°C	3000
bq2028YZGT			250

PIN ASSIGNMENT

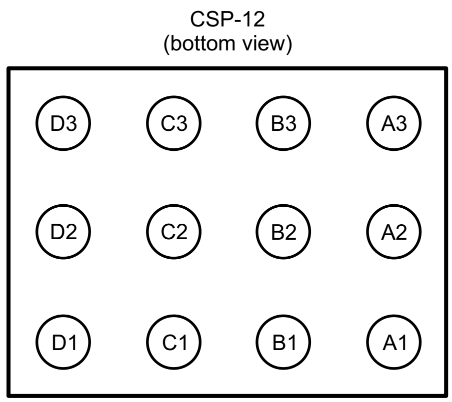


Figure 1. bq2028 Pin Assignment (Bottom View)

PIN DESCRIPTIONS

PIN NAME	CSP-12 PIN	I/O	DESCRIPTION
TEST3	C3	I/O	Reserved for factory test. Connect to VSS in application circuit.
REGIN	D3	P	Regulator input. Typically connected to battery CELL+.
VDD	D2	P	Regulator 2.5V output. Decouple with a 0.47μF cap to VSS.
VSS	A1, B1, D1, B2, C2	P	Ground pin.
HDQ	A2	I/O	HDQ Data pin. Open-drain I/O. Requires external pull-up for proper operation.
TEST1	C1	I/O	Reserved for factory test. Connect to VSS in application circuit.
TEST0	B3	I/O	Reserved for factory test. Connect to VSS in application circuit.
TEST2	A3	I/O	Reserved for factory test. Connect to VSS in application circuit.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		VALUE		UNIT
		MIN	MAX	
V_{REGIN}	Supply voltage range	–0.3	5.5	V
HDQ	Open-drain I/O pin	–0.3	5.5	V
V_I	Input voltage range to all other pins (TEST0-3)	–0.3	V_{REG25} + 0.3	V
ESD	HBM for pins other than TEST1, TEST2, TEST3		2	kV
T_A	Operating free-air temperature range	–40	85	°C
T_F	Functional temperature	–40	100	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating condition" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

T_A = 25°C, C_{LDO25} = 0.47 µF, V_{REGIN} = 3.6V (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{REGIN}	Supply Voltage		2.45		4.5	V
R_{PUEXT}	HDQ external pull-up	To system-side 2.5V LDO output. Recommend using 10kΩ, 5% resistor.		10	22	kΩ
C_{HDQ}	HDQ capacitive loading	Total external bus capacitance		50	250	pF
C_{REGIN}	External input capacitor for internal LDO between REGIN and VSS	Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{LDO25}	External output capacitor for internal LDO between VDD and VSS			0.47		µF

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, C_{LDO25} = 0.47 µF, V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{CC}	Supply Current (1)	SHUTDOWN Mode (LDO = off)		1	2	µA
		SLEEP Mode (LFO = on; HFO = off)		20	50	
		IDLE Mode (LFO, HFO = on; CONV= 0)		55	110	
		TEMP Read (LFO, HFO = on; CONV = 1)		110	200	
		EEPROM Read (LFO, HFO = on)		300	600	
		EEPROM Write (LFO, HFO = on)		2300	5000	
2.5V LDO REGULATOR						
V_{REG25}	Regulator output voltage	2.7 V ≤ V_{REGIN} ≤ 4.5 V, I_{OUT} ≤ 10 mA	2.4	2.5	2.6	V
		2.45 V ≤ V_{REGIN} < 2.7 V (low battery), I_{OUT} ≤ 3 mA	2.4			
OTHER ANALOG: POWER ON RESET, TEMPERATURE SENSOR, INTERNAL VOLTAGE REFERENCE						
V_{POR+}	POR Threshold	Positive-going input at VDD, T_A = 25°C	2.05	2.20	2.31	V
V_{HYSPOR}	POR Hysteresis	TA=25°C	45	115	185	mV
V_{WU+}	HDQ Wakeup threshold	Positive-going input at HDQ, T_A = 25°C	1.2	1.4		V
V_{HYSWU}	HDQ Wakeup hysteresis	T_A = 25°C		505		mV
V_{ASD}	Auto shutdown threshold		2.05	2.20	2.31	V
V_{HYSASD}	Auto shutdown hysteresis		45	115	185	V
$V_{(TEMP)}$	Temperature sensor			–1.986		mV/°C
HDQ INTERFACE						
V_{IH}	Input voltage high		1.8			V
V_{IL}	Input voltage low				0.6	V
V_{OH}	Output voltage high	Open drain, external pull up to VDD	V_{DD}–0.5			V
V_{OL}	Output voltage low	Open-drain IOL = 1mA			0.4	V
C_I	Input capacitance			10		pF
I_{itot}	HDQ input total current	Includes leakage plus internal pull-down			2	µA
I_{OL}	Output low sink current	VOL = 0.4V			1	mA
R_{PDINT}	HDQ internal pull-down	For auto-shutdown	1.25	2.5	5	MΩ

(1) An EEPROM write operation is required for proper device initialization following exit from SHUTDOWN, SLEEP, or POWER-ON RESET.

AC ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, C_{LDO25} = 0.47 µF, V_{REGIN} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
EEPROM						
	Array Size	128 words x 32 bits = 4Kbits		512		Bytes
	Write Cycle Endurance		1000			K cycles
	HDQ Data Access	Via 32 bit BUFFER		8		Bits
	Program time	Per word (internal timing only)		6	20	mS
	Read time	Per word (internal timing only)		300	2000	nS
HDQ INTERFACE AND MISCELLANEOUS (Refer to Figure 6 and Figure 7)						
t_B	Break time		190			µs
t_{BR}	Break recovery time		40			µs
t_{SLWU}	SLEEP wakeup	Host drives HDQ Break. Timed from rising edge of first wakeup break pulse to falling edge of next break pulse with first data.	200			µs
t_{SHWU}	SHUTDOWN wakeup		20			ms
t_{SHUTDN}	SHUTDOWN time	Time delay after V_{ASD} threshold is met before SHUTDOWN mode is entered.		2	10	S
t_{ASHWU}	AUTOSHUTDOWN wakeup	Time delay after V_{ASD} threshold is met or 2 second timeout is met before Host can drive HDQ break for wakeup.		2	10	S
t_{PORWU}	POR wakeup	Power on reset wakeup time before device is ready to receive first HDQ message	35			ms
$t_{REGINHDQ}$	REGIN to HDQ	REGIN valid to 1st rising edge of HDQ to POR device. (Figure 3)	15			ms
t_{POR}	POR	VDD ramp to POR release.(Figure 3)			11	ms
t_{GRST}	Global reset	POR release to GRST release. (Figure 3)		4		ms
t_{HW1}	Host Write 1 time	Host drives HDQ	5		50	µs
t_{HW0}	Host Write 0 time	Host drives HDQ	86		145	µs
t_{CYCH}	Host cycle time	Host drives HDQ	190			µs
t_{DW1}	Device Write 1 time	bq2028 drives HDQ	39	41	43	µs
t_{DW0}	Device Write 0 time	bq2028 drives HDQ	106	111	116	µs
t_{CYCD}	Device cycle time	bq2028 drives HDQ	197	207	217	µs
t_{RSPS}	Device response time	bq2028 drives HDQ	211	222	233	µs
$t_{HDQSTDET}$	HDQ Start detect	bq2028 filters out very short HDQ pulses	0		1.98	µs
A/D CONVERTER						
$f_{(SAMPLE)}$	Sampling frequency	Delta Sigma modulator frequency		65.5		kHz
$t_{(CONV)}$	Conversion time	SPEED[1:0] = 00		125		ms
		SPEED[1:0] = 01		62.50		
		SPEED[1:0] = 10		31.25		
		SPEED[1:0] = 11		7.8125		
$V_{(ADC\_IN)}$	Input voltage range	Internal Vref, T_A = 25°C, VTEMP internal channel only	–0.2		1	V
HIGH FREQUENCY OSCILLATOR (HFO)						
HF_{OSC}	Operating frequency			8.389		MHz
HF_{ERR}	Frequency error	T_A = –40°C to 85°C	–8.0%		8.0%	
HF_{START}	Start-up time			14	200	µs
LOW FREQUENCY OSCILLATOR (LFO)						
LF_{OSC}	Operating frequency			32.768		kHz
LF_{ERR}	Frequency error	T_A = –40°C to 85°C	–8.0%		8.0%	
LF_{START}	Start-up time			100	500	µs

BLOCK DIAGRAM

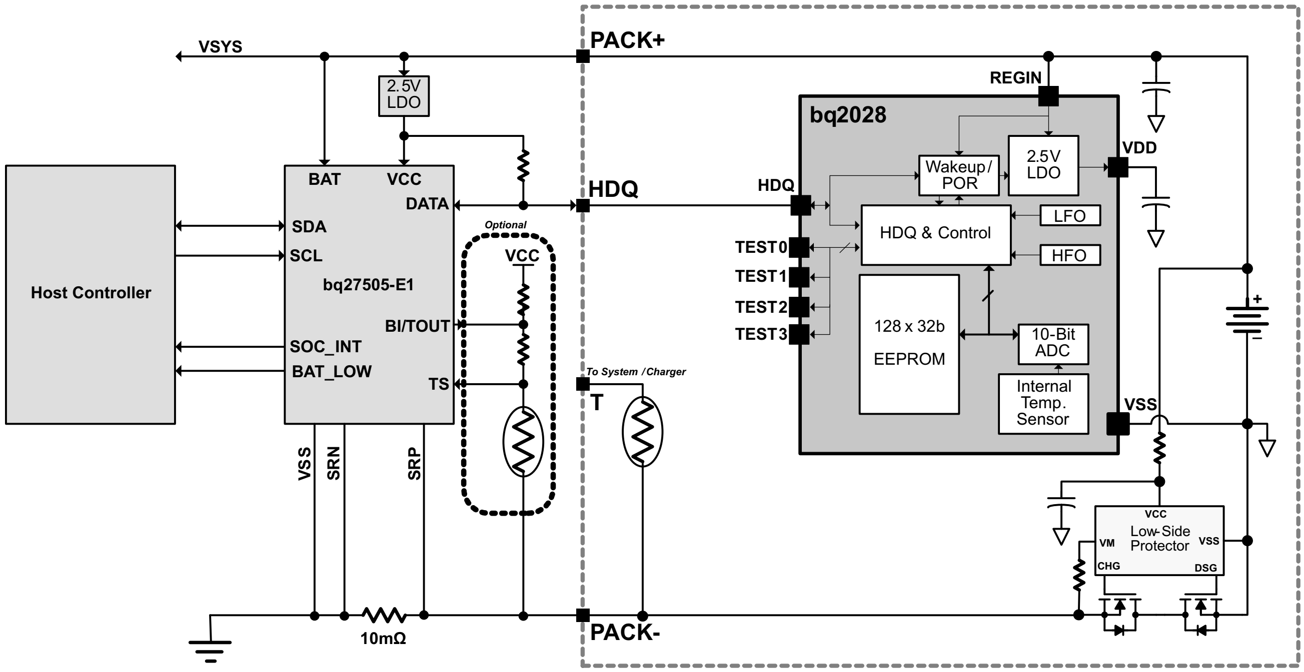


Figure 2. bq2028 Block Diagram

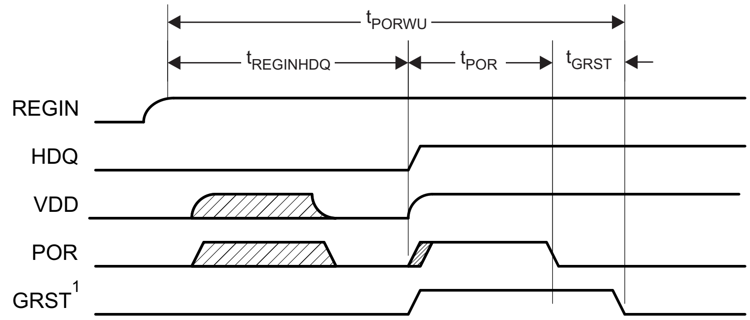
Power Modes

The bq2028 has multiple operational modes for reduced power consumption. defines which circuits are enabled in each of these operational modes.

Table 1. Power Mode Table(1)

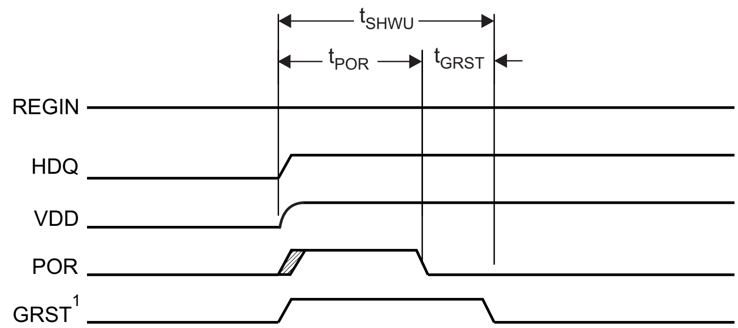
CIRCUIT	SHUT-DOWN	SLEEP	IDLE	HDQ READ/WRITE	TEMP READ	EEPROM READ	EEPROM WRITE
Wakeup/POR	√	√	√	√	√	√	√
LDO Regulator	–	√	√	√	√	√	√
32kHz LFO	–	√	√	√	√	√	√
8MHz HFO	–	–	√	√	√	√	√
HDQ Interface	–	–	–	√	√	√	√
ADC	–	–	–	–	√	–	–
EEPROM Read	–	–	–	–	–	√	–
EEPROM Write	–	–	–	–	–	–	√

(1) √: Active –: Not in use



(1) Internal digital core reset, held for 4 ms after analog POR deasserted

Figure 3. Power Up Sequence



(1) Internal digital core reset, held for 4 ms after analog POR deasserted

Figure 4. Shutdown Wake Up Sequence

HDQ Interface

The bq2028 supports a single-wire, open-drain communication interface that supports the HDQ protocol as shown in Figure 5. The HDQ protocol is based on the Texas Instruments HDQ standard as discussed in the TI application report (SLUA408A) (http://focus.ti.com.cn/cn/lit/an/slua408a/slua408a.pdf).

The communication protocol is asynchronous return-to-one referenced to Vss. A passive pullup resistance is required to pull the HDQ line to a high state when neither the host nor the slave is pulling the line low during two-way communication over the single wire interface. The interface uses a command-based protocol, where the host sends a command byte to the HDQ slave device. The command directs the slave to either receive or transmit the next byte of data. The last transmitted bit of the command byte determines the direction of the data (read or write) as shown in Figure 7.

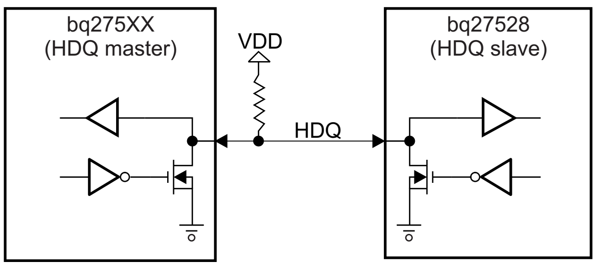


Figure 5. HDQ Interface Connections (single wire configuration)

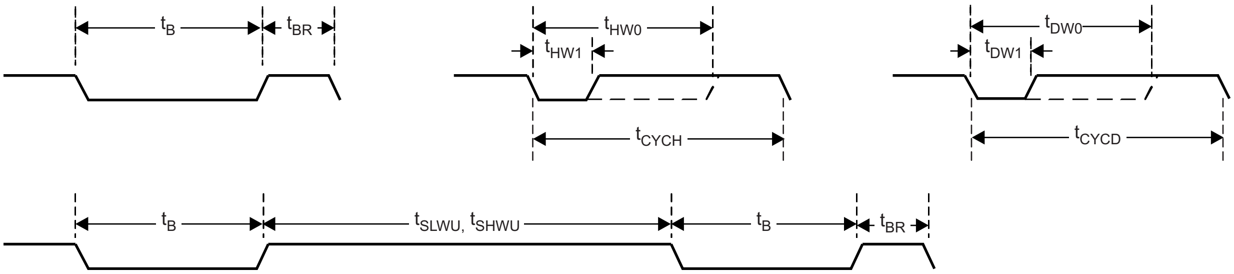


Figure 6. HDQ Detailed Timing Waveform

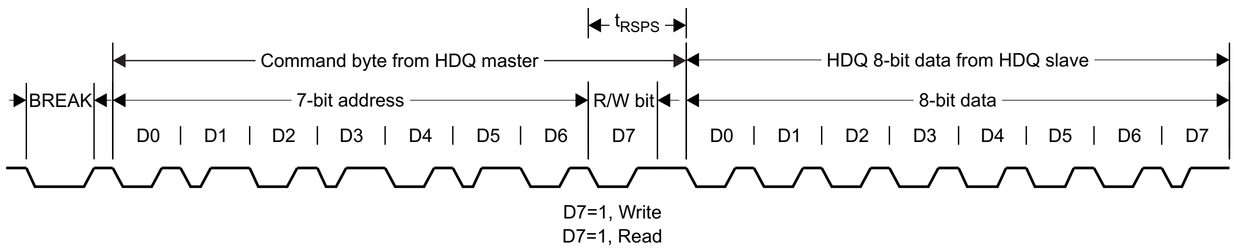


Figure 7. HDQ 8-bit Mode Read Cycle

Device Control

Using a register address access method, the HDQ command byte limits addressing to 7 bits so a mapping scheme is necessary to differentiate device control and status registers from EEPROM data. This register and paged EEPROM access scheme is shown in Figure 8.

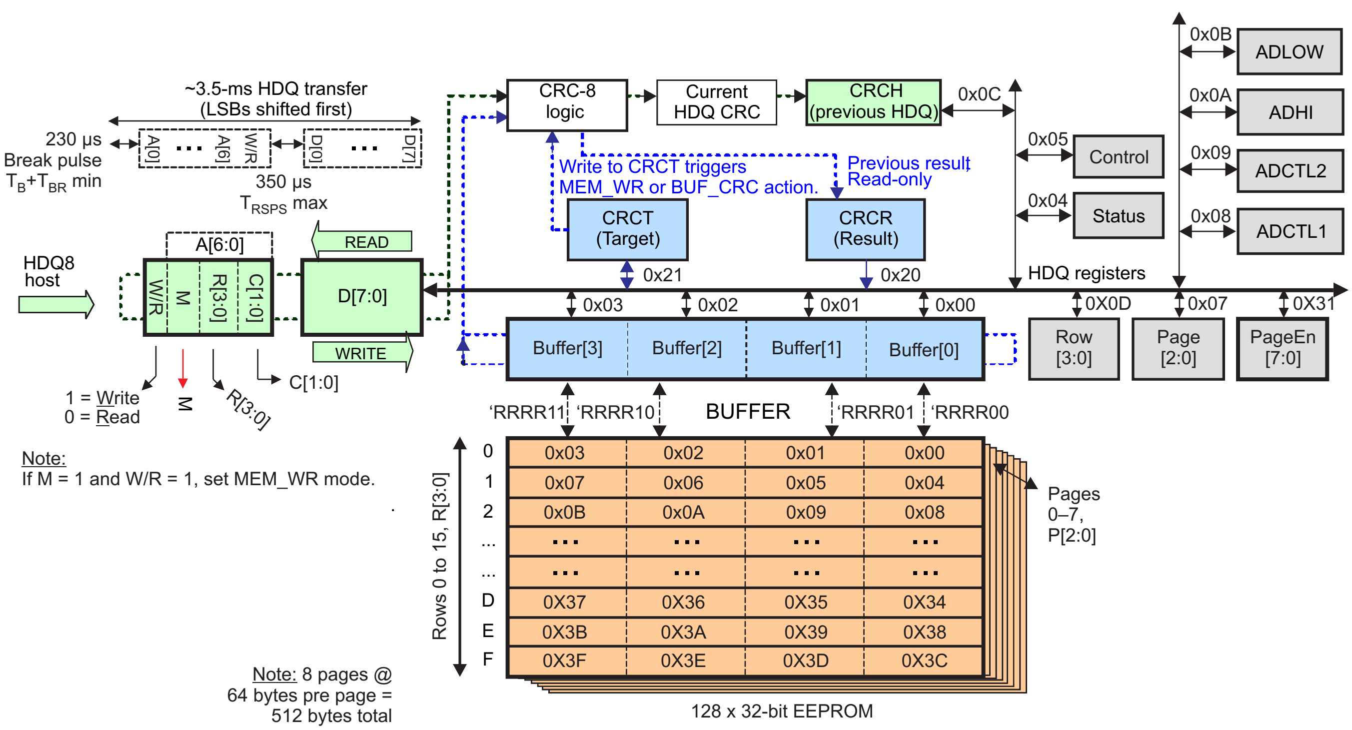


Figure 8. Register and EEPROM Access Scheme

Access to device control and data registers use the “Un-Mapped” address space with the “M” (Map bit) set to ‘0’. Access to the EEPROM space uses a Memory Mapped scheme with the “M” bit set to ‘1’. Refer to Figure 9 for details.

Memory Mapped Registers

		R[3:0]				C[1:0]	
W/R	1	R3	R2	R1	R0	C1	C0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 = W/R: Read/Write command (1 = Write, 0 = Read)
Bit 6 = Map Bit, M = 1
Bits 5:2 = Row index: R[3:0]
Bits 1:0 = Column/Buffer index: C[1:0]

Unmapped Registers

		A[5:0]					
W/R	0	A5	A4	A3	A2	A1	A0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 = W/R: Read/Write command (1 = Write, 0 = Read)
Bits 6:5 = Map Bit, M = 0
Bits 4:0 = HDQ register: A[5:0] Range = 0x00 to 0x3F

Figure 9. HDQ Command Byte Decode

7 HDQ Access Method

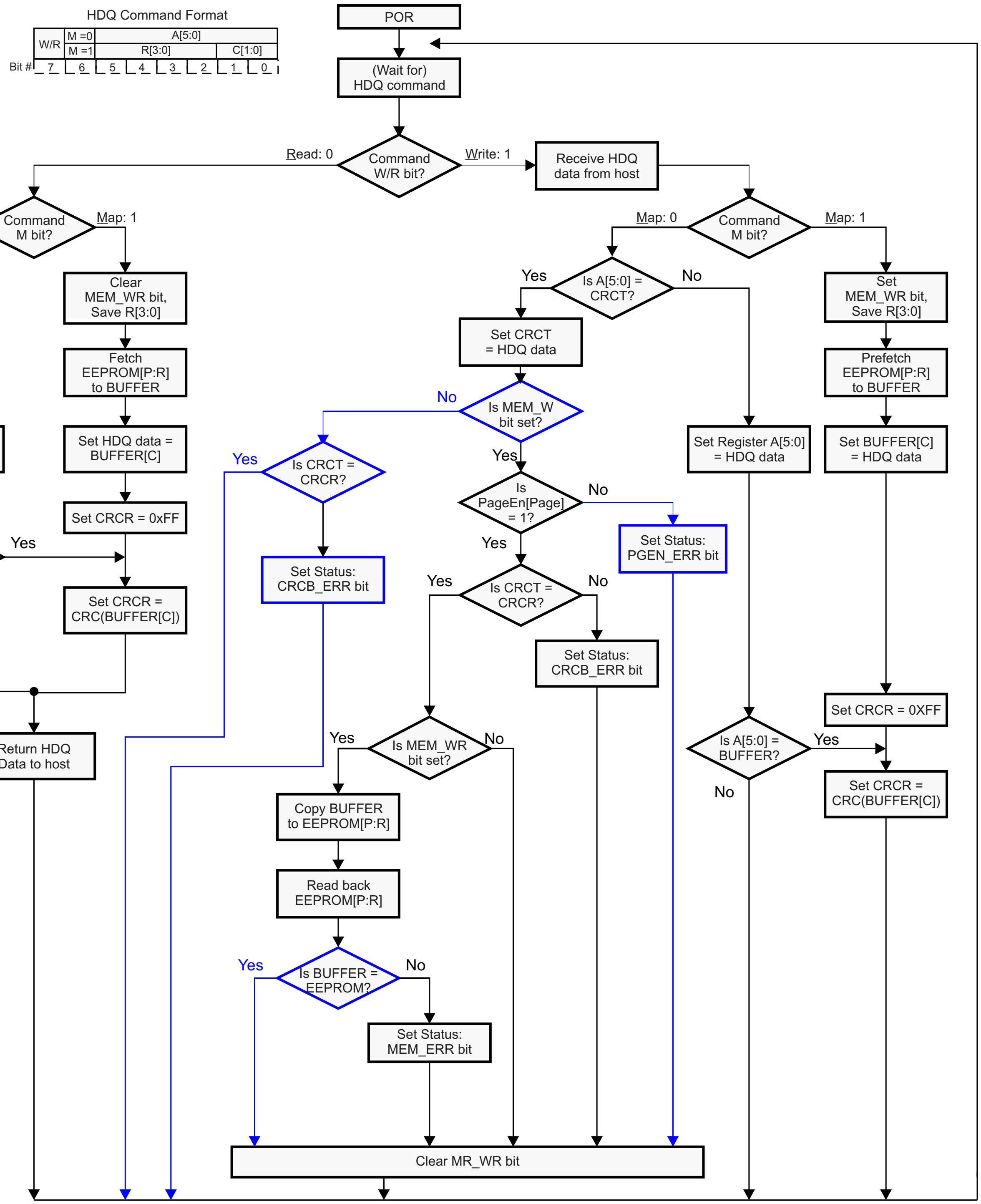


Figure 10. HDQ Access Flow Chart

EEPROM Access

The bq2028 provides 512 bytes of EEPROM non-volatile memory storage organized as 128 words x 32 bits. Due to the address limitations of the HDQ interface protocol, the EEPROM is accessed in 8 pages, with 16 rows of 4 bytes each. For IC manufacturing and analog trim data, 16 bytes or 4 words are reserved in last page of data. The access model terminology is listed below:

EEPROM	=	128x32-bit (512 bytes) non-volatile memory with paged access
BUFFER	=	32-bit long word in 4x8b volatile Buffer
C	=	2-bit byte **C**olumn index for Buffer: C[1:0]
Buffer[C]	=	8-bit access to BUFFER at index C. MSB is at byte indexed by C='11'.
P	=	3-bit **P**age index for EEPROM: P[2:0] (8 pages/EEPROM)
PAGE[P]	=	16x32-bit rows (64 bytes) from EEPROM indexed by [P]
R	=	4-bit **R**ow index for EEPROM: R[3:0] (16 rows/page)
ROW[P,R]	=	32-bit long word from EEPROM indexed by [P,R]
Pre-Fetch	=	Automatic copy of an ROW[P,R] to BUFFER before read/write operation
M	=	**M**apping operations to access BUFFER and EEPROM: M[1:0]

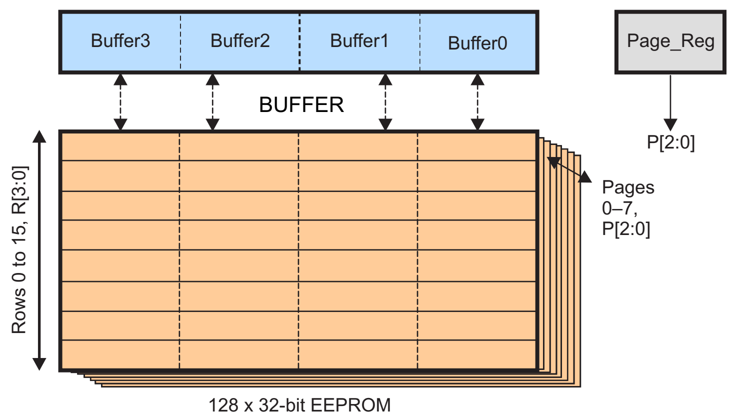


Figure 11. Memory Map

HDQ Registers

A summary of the Un-Mapped HDQ Registers is provided by Table 2.

Table 2. HDQ Un-Mapped Register Summary(1)(2)

A[5:0]	R/W	Register	B	A[5:0]	R/W	Register	B	A[5:0]	R/W	Register	B	A[5:0]	R/W	Register
0x00	R/W	Buffer0	–	0x10	–	(Reserved)	–	0x20	R	CRCR	–	0x30	R/W	(Reserved)
0x01	R/W	Buffer1	–	0x11	–	(Reserved)	–	0x21	R/W	CRCT	–	0x31	R/W	PageEn
0x02	R/W	Buffer2	–	0x12	–	(Reserved)	–	0x22	–	(spare)	–	0x32	R/W	(Trim)
0x03	R/W	Buffer3	–	0x13	–	(Reserved)	–	0x23	–	(spare)	–	0x33	R/W	(Trim)
0x04	R	Status	–	0x14	–	(Reserved)	–	0x24	–	(Reserved)	–	0x34	R/W	(Trim)
0x05	R/W	Control	–	0x15	–	(Reserved)	–	0x25	–	(Reserved)	–	0x35	R/W	(Trim)
0x06	-	(spare)	–	0x16	–	(Reserved)	–	0x26	–	(Reserved)	–	0x36	R/W	(Trim)
0x07	R/W	Page	–	0x17	–	(Reserved)	–	0x27	–	(Reserved)	–	0x37	–	(Reserved)
0x08	R/W	ADCTL1	–	0x18	–	(spare)	–	0x28	–	(Reserved)	–	0x38	–	(Reserved)
0x09	R/W	ADCTL2	–	0x19	–	(spare)	–	0x29	–	(spare)	–	0x39	–	(Reserved)
0x0A	R	ADHI	–	0x1A	–	(spare)	–	0x2A	–	(spare)	–	0x3A	–	(Reserved)
0x0B	R	ADLOW	–	0x1B	–	(spare)	–	0x2B	–	(spare)	–	0x3B	–	(Reserved)
0x0C	R	CRCH	–	0x1C	–	(spare)	–	0x2C	–	(Reserved)	–	0x3C	–	(Reserved)
0x0D	R	Row	–	0x1D	–	(spare)	–	0x2D	–	(Reserved)	–	0x3D	–	(Reserved)
0x0E	R	DeviceRev	–	0x1E	–	(spare)	–	0x2E	–	(spare)	–	0x3E	–	(Reserved)
0x0F	R	DeviceID	–	0x1F	–	(spare)	–	0x2F	–	(spare)	–	0x3F	–	(Reserved)

(1) B = Defaults "**B**acked Up" in EEPROM Page[0] and auto-loaded at Power On Reset
(2) Page[0] EEPROM Addresses 0x38 to 0x3F contain the TI Die ID but these are not mapped to HDQ registers.

32-bit BUFFER Access (addresses 0x00 through 0x03)

Access to the 32-bit words in the EEPROM is provided by a 32-bit BUFFER that is available as 8-bit HDQ registers: Buffer0 [LSB], Buffer1, Buffer2, Buffer[MSB].

32-BIT BUFFER			
MS-Byte			LS-Byte
Buffer3	Buffer2	Buffer1	Buffer0

	7(MSB)	6	5	4	3	2	1	0
Name	Buffer0[7:0] (address 0x00) – Least Significant Byte							
Name	Buffer1[7:0] (address 0x01)							
Name	Buffer2[7:0] (address 0x02)							
Name	Buffer3[7:0] (address 0x03) – Most Significant Byte							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	Undefined							

Status Register (address 0x04):

	7(MSB)	6	5	4	3	2	1	0
Name	BUSY	ADC_DRDY	PGEN_ERR	MEM_WR	RSVD	RSTBIT	MEM_ERR	CRCB_ERR
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

BUSY (bit 7): Busy flag. This bit is normally ‘0’ and is set to ‘1’ when the device is performing an extended duration function such as device initialization, an ADC measurement or EEPROM write. Upon completion of the function, the BUSY bit will automatically clear to ‘0’.

ADC_DRDY (bit 6): ADC Data ready flag. This bit indicates that conversion data is ready in the ADC Data Registers (ADHI and ADLOW). This bit is cleared by setting the CONV bit in the Control register.

1 – ADC data is ready
0 – ADC data is not ready.

PGEN_ERR (bit 5): Page Enable Error flag. This indicates that an EEPROM write was attempted to a page that was not enabled for write-access.

MEM_WR (bit 4): Memory Write flag. This bit is set during the EEPROM memory access scheme when the Map bit is set with an HDQ write command. This bit is cleared if the Map bit is set with an HDQ read command or upon completion of an EEPROM program cycle. Refer to Figure 10.

RSTBIT (bit 2): This bit is set to ‘1’ when the device has reset due to a Power On Reset (POR) event or a soft reset initiated by the Control:Reset bit. The RSTBIT will remain set to ‘1’ until the Control:RSTCLR bit is set to ‘1’.

MEM_ERR (bit 1): This bit is set to ‘1’ when the device detects an EEPROM memory error. Refer to Figure 10. This bit, along with CRCB_ERR, is cleared using the Control:ERRCLR bit.

CRCB_ERR (bit 0): This bit is set to ‘1’ when the device detects a BUFFER memory error after computing a CRC check. Refer to Figure 10. This bit, along with MEM_ERR, is cleared using the Control:ERRCLR bit.

Control Register (address 0x05):

	7(MSB)	6	5	4	3	2	1	0
Name	CONV	RSVD	RSVD	ERRCLR	SLEEP	RSTCLR	RESET	SHUTDOWN
Access	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CONV (bit 7): Convert command bit. This bit is used to start an ADC conversion when set to ‘1’ and is automatically cleared at the end of data conversion cycle in order to minimize HDQ traffic. At the start of data conversion, the device sets the Status:BUSY flag and automatically clears the Status:ADC_DRDY flag to indicate data conversion is in progress. When data conversion is complete, both the CONV bit and BUSY flag are cleared and the ADC_DRDY flag is set. To abort an ADC conversion in process, the host can clear the CONV bit to ‘0’.

ERRCLR (bit 4): A ‘1’ written to this bit will clear both the Status:MEM_ERR and CRCB_ERR bits. This bit auto-clears itself so a readback always reads ‘0’.

SLEEP (bit 3): A ‘1’ written to this bit enables a lower-power mode with the HFO disabled. This bit is automatically cleared upon detection of HDQ communication activity. Therefore a readback of this bit over HDQ will always be ‘0’.
Note: If SLEEP mode is commanded, the host should wake up the bq2028 by issuing an HDQ break pulse with no associated data, followed by a wait period of at least 200 us (tSLWU), then send a second HDQ break pulse with the first command.

RSTCLR (bit 2): A ‘1’ written to this bit will clear the Status:RSTBIT flag and auto-clear itself so a readback always reads ‘0’.

RESET (bit 1): A ‘1’ written to this bit will initiate a full device initialization. The device will auto-clear the RESET bit and set the Status:RSTBIT and Status:BUSY flags at the start of initialization. After initialization is complete the device will clear the BUSY flag.

SHUTDOWN (bit 0): A ‘1’ written to this bit will initiate a full device Shutdown. This bit is automatically cleared upon a POR and must be cleared for correct HDQ activity. Therefore a readback of this bit over HDQ will always be ‘0’.
Note: If SHUTDOWN mode is commanded, the host should wake up the bq2028 by issuing an HDQ break pulse with no associated data, followed by a wait period of at least 15ms (t_{SHWU}), then send a second HDQ break pulse with the first command.

Page Register (address 0x07): EEPROM Page Register

	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	RSVD	Page[2:0]		
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Page[2:0]: This contains the current 3-bit Page pointer for EEPROM access.

ADCTL1 (address 0x08): ADC Control Register 1

	7(MSB)	6	5	4	3	2	1	0
Final Product	RSVD	VRVDD	SPEED[1]	SPEED[0]	RSVD	CHAN[2]	CHAN[1]	CHAN[0]
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RSVD (bit 7) Do not use.

VRVDD (bit 6): Voltage reference selection bit. This bit selects which voltage reference (either V_{DD} or internal V_{REF}) is used by the ADC.

1 – Selects VDD as the ADC reference voltage for ratio metric conversions
0 – Selects the internal V_{REF} as the ADC reference voltage

SPEED[1:0] (bits 5-4):
Conversion speed selection bits.

SPEED[1:0]	FILTER LENGTH	CONVERSION TIME
00	8192	125ms
01	4096	62.5ms
10	2048	31.25ms
11	512	7.8125ms

RSVD (bit 3) Do not use.

CHAN[2:0] (bits 2–0): ADC Channel selection bits. Set to VTEMP (‘101’) to measure the internal die temperature sensor or set to VSS (‘111’) for measuring ADC offset.

CHAN[2:0]	ADC INPUT CHANNEL (Product Datasheet)
000	RSVD
001	RSVD
010	RSVD
011	RSVD
100	RSVD
101	VTEMP
110	RSVD
111	VSS

ADCTL2 (address 0x09): ADC Control Register 2

	7(MSB)	6	5	4	3	2	1	0
Final Product	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

RSVD (bits 7:0): Do not use.

ADHI (address 0x0A): ADC High Byte Data Register

This register provides the high byte ADC conversion data in 2's complement format. A full scale (max value) for this register is 7FFFh. A zero scale (min value) for this register is 8000h.

	7(MSB)	6	5	4	3	2	1	0
Name	ADC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	1	0	0	0	0	0	0	0

ADC[15:8] (bits 7:0): ADC high byte conversion data.

ADLOW (address 0x0B): ADC Low Byte Data Register

	7(MSB)	6	5	4	3	2	1	0
Name	ADC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	1	0	0	0	0	0	0	0

ADC[7:0] (bits 7:0): ADC low byte conversion data.

CRCH Register (address 0x0C): HDQ CRC Register

The register contains the CRC-8 result of the previous HDQ command + data sequence and is useful for data integrity checks for single HDQ packet transfers.

	7(MSB)	6	5	4	3	2	1	0
Name	CHRH[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

CHCH[7:0]: CRC-8 data from the previous HDQ packet. Data is computed using the full 16-bit HDQ package sequence included W/R bit, 7-bit command and 8-bit data.

Row Register (address 0x0D): EEPROM Row Register

	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	Row[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Row[3:0]: This contains the current 4-bit Row pointer for a particular page. The value is automatically updated by Mapped access to the EEPROM.

DeviceRev Register (address 0x0E): Device Revision Register

	7(MSB)	6	5	4	3	2	1	0
Name	DeviceRev[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	DeviceRev[7:0]							

DeviceRev[7:0]: The read-only register returns the hardware device revision value The initial revision is 0x01 and increments by 1 for each design revision.

DeviceID Register (address 0x0F): Device ID Register

	7(MSB)	6	5	4	3	2	1	0
Name	DeviceID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	DeviceID[7:0] = 0x28							

DeviceRev[7:0]: This read-only register returns the unique device identification value which provides a method for the host to distinguish the bq2028 from other HDQ devices. The DeviceID for the bq2028 = 0x28.

CRCR Register (address 0x20): BUFFER CRC Result Register

	7(MSB)	6	5	4	3	2	1	0
Name	CRCR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	Undefined							

CRCR[7:0]: This register contains the last BUFFER CRC computation result.

CRCT Register (address 0x21): BUFFER CRC Target Register

	7(MSB)	6	5	4	3	2	1	0
Name	CRCT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CRCT[7:0]: This register contains the CRC computation target for verifying the BUFFER contents prior to writing the data to EEPROM. This method is used to prevent EEPROM data corruption due to interrupted HDQ transfers or communication errors. An HDQ write to this register triggers the comparison of the CRC previously calculated as BUFFER data is loaded from the HDQ interface. If the MEM_WR flag is set and the CRCT target register matches the CRCR result register, the device will write the BUFFER to the EEPROM using the current ROW and PAGE register values. Then a read-back of the EEPROM will be re-checked to confirm the integrity of the memory write. Refer to flow chart in Figure 10 for CRC initialization and computations. An HDQ read of this register returns the previously written target value.

CONTROL2 (address 0x25): CONTROL2 Register

	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	MANWREN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RSVD (bits 7:1): Do not use.

MANWREN (Bit 0): A ‘1’ enables write access to the Page 0 Manufacturer’s area registers and associated EEPROM locations 0x30 through 0x3F. Users of the bq2028 may only change the PageEn register (0x031) without adversely changing manufacturing trim data.

PageEn Register (address 0x31): Page Enable Register

	7(MSB)	6	5	4	3	2	1	0
Name	PageEn[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	EEPROM Page[0], Address 0x31							

PageEn[X]: Each bit maps to the associated EEPROM page and enables write access. An attempt to write to Page[X] with PageEn[X]=0 will cause the PGEN_ERR bit to be set in the Status Register. This register has a hardware write protection feature. To write to this register, the MANWREN bit must be set in the Control 2 Register. This register is automatically loaded at reset with data stored in the EEPROM memory (page 0, byte address 0x31)

1 – Page[X] is writable

0 – Page[X] is read-only

CRC FUNCTIONS FOR DATA INTEGRITY

For data integrity checks, the bq2028 provides a CRC-8 computation block with the polynomial function of (X^8+X^5+X^4+ 1). The following Python code indicates the parallel computation method where the 8-bit variable ‘c’ is the new data for calculating the CRC and the 8-bit variable ‘prev’ is the previous result if calculating the CRC on multiple data items. To start a new sequence, the ‘prev’ variable is initialized with the value 0xFF. Note: The initialization value of 0xFF is new in spec version 1.5. Previous versions used an initialization value of 0x00.

```
c ^= prev
for I in range(8):
    if (c & 0x80):
        c = ((c << 1 & 0xff)) ^ 0x31
    else:
        c = (c << 1) & 0xff
return c
```

Refer to the table below for example data sequences and the expected CRC:

EXAMPLE DATA SEQUENCE (Byte order left to right)	CRC
0x00	0xAC
0xAA	0x8B
0xFF	0x00
0x00 0xAA	0xA6
0xAA 0x55	0x1B
0xFF 0x01 0x55	0x7F
0x00 0x01 0x55 0xAA	0xF1

The CRC-8 function is typically used for verification of EEPROM data integrity via the BUFFER. To prevent EEPROM memory corruption, BUFFER data will not be written to EEPROM without passing a CRC verification check. Refer to the Figure 10 flow-char for the HDQ Access Method related to CRC computation and verification. The additional complexity of this CRC-8 computation method is provided to minimize HDQ overhead traffic when performing data integrity checks on variable length data elements.

The CRC-8 function is initiated on every HDQ data transfer with the result of the previous CRC-8 stored in the CRCH register. The CRCH register is typically used for single HDQ data packet integrity checks. Since the HDQ protocol shifts data with the LSB arriving first, the CRC is computed in this order:

A0:A6, R/W, D0-D7.

Note: This is the opposite bit ordering from the BUFFER CRC-8 computations.

Memory Access HDQ host pseudo-code examples

```
8-bit EEPROM Write (Example is <Byte1>):
Crc8 = FnCRC8(Byte1)       // Pre-Compute CRC-8 for 8-bit data
WRITE '1RRRR01', Byte1     // Pre-fetch EEPROM ROW 'RRRR', Poke Buffer[1], Set MEM_WR
WRITE '0100001', Crc8      // Poke Crc8 to CRCT trigger MEM write and re-check
READ  '0000100', Status    // Peek Status Register.
IF (Status && 0x03) THEN CALL bq2028_Error   // B0 = CRCB_ERR, B1 = MEM_ERR

8-bit EEPROM Read  (Example is <Byte2>):
READ  '1RRRR10', Byte2     // Fetch ROW 'RRRR' to BUFFER, Peek Buffer[2], Clear MEM_WR
Crc8 = FnCRC8(Byte2)    // Compute CRC-8 on 1 byte read
WRITE '0100001', Crc8     // Poke Crc8 to CRCT trigger MEM write and re-check
READ  '0000100', Status    // Peek Status Register.
IF (Status && 0x03) THEN CALL bq2028_Error   // B0 = CRCB_ERR, B1 = MEM_ERR

16-bit EEPROM Write (Lower 2-Bytes)
Crc8 = FnCRC8(Byte0, Byte1)   // Pre-Compute CRC-8 for 16-bit data
WRITE '1RRRR00', Byte0    // Pre-fetch EEPROM ROW 'RRRR', Poke Buffer[0], Set MEM_WR
WRITE '0000001', Byte1    // Poke Buffer[1]
WRITE '0100001', Crc8     // Poke Crc8 to CRCT trigger MEM write and re-check
READ  '0000100', Status    // Peek Status Register.
IF (Status && 0x03) THEN CALL bq2028_Error   // B0 = CRCB_ERR, B1 = MEM_ERR

16-bit EEPROM Read (Lower 2-Bytes)
READ  '1RRRR00', Byte0    // Fetch ROW 'RRRR' to BUFFER, Peek Buffer[0], Clear MEM_WR
READ  '0000001', Byte1    // Peek Buffer[1]
Crc8 = FnCRC8(Byte0, Byte1)   // Compute CRC-8 on 2 bytes read
WRITE '0100001', Crc8     // Poke Crc8 to CRCT trigger MEM write and re-check
READ  '0000100', Status    // Peek Status Register.
IF (Status && 0x03) THEN CALL bq2028_Error   // B0 = CRCB_ERR, B1 = MEM_ERR
```

```
24-bit EEPROM Write (Lower 3-Bytes)
Crc8 = FnCRC8(Byte0, Byte2, Byte3)   // Pre-Compute CRC-8 for 24-bit data
WRITE '1RRRR00', Byte0    // Pre-fetch EEPROM ROW 'RRRR', Poke Buffer[0], Set MEM_WR
WRITE '0000001', Byte1    // Poke Buffer[1]
WRITE '0000010', Byte2    // Poke Buffer[2]
WRITE '0100001', Crc8     // Poke Crc8 to CRCT trigger MEM write and re-check
READ  '0000100', Status    // Peek Status Register.
IF (Status && 0x03) THEN CALL bq2028_Error   // B0 = CRCB_ERR, B1 = MEM_ERR

24-bit EEPROM Read (Lower 3-Bytes)
READ  '1RRRR00', Byte0    // Fetch ROW 'RRRR' to BUFFER, Peek Buffer[0], Clear MEM_WR
READ  '0000001', Byte1    // Peek Buffer[1]
READ  '0000010', Byte2    // Peek Buffer[2]
Crc8 = FnCRC8(Byte0, Byte2, Byte3)   // Compute CRC-8 on 3 bytes read
WRITE '0100001', Crc8     // Poke Crc8 to CRCT trigger MEM write and re-check
READ  '0000100', Status    // Peek Status Register.
IF (Status && 0x03) THEN CALL bq2028_Error   // B0 = CRCB_ERR, B1 = MEM_ERR

32-bit EEPROM Write (Full 4-Bytes)
Crc8 = FnCRC8(Byte0, Byte1, Byte2, Byte3)   // Pre-Compute CRC-8 for 32-bit data
WRITE '1RRRR00', Byte0    // Pre-fetch EEPROM ROW 'RRRR', Poke Buffer[0], Set MEM_WR
WRITE '0000001', Byte1    // Poke Buffer[1]
WRITE '0000010', Byte2    // Poke Buffer[2]
WRITE '0000011', Byte3    // Poke Buffer[3]
WRITE '0100001', Crc8     // Poke Crc8 to CRCT trigger MEM write and re-check
READ  '0000100', Status    // Peek Status Register.
IF (Status && 0x03) THEN CALL bq2028_Error   // B0 = CRCB_ERR, B1 = MEM_ERR

32-bit EEPROM Read (Full 4-Bytes)
READ  '1RRRR00', Byte0    // Fetch ROW 'RRRR' to BUFFER, Peek Buffer[0], Clear MEM_WR
READ  '0000001', Byte1    // Peek Buffer[1]
READ  '0000010', Byte2    // Peek Buffer[2]
READ  '0000011', Byte3    // Peek Buffer[3]
Crc8 = FnCRC8(Byte0, Byte1, Byte2, Byte3)   // Compute CRC-8 on 3 bytes read
WRITE '0100001', Crc8     // Poke Crc8 to CRCT trigger MEM write and re-check
READ  '0000100', Status    // Peek Status Register.
IF (Status && 0x03) THEN CALL bq2028_Error   // B0 = CRCB_ERR, B1 = MEM_ERR
```

INTERNAL TEMPERATURE SENSOR

An internal die temperature sensor is available on the bq2028 to reduce the cost, power, and size of the external components necessary to measure temperature. Temperature sensing uses the V_{BE} method to present a voltage to a delta-sigma ADC converter. The host reads the ADC data over the HDQ interface and uses firmware to convert the data to Kelvin temperature units.

ADC data is formatted to 16-bits even though the data conversion performance may be limited to 10 effective bits. An ADC conversion starts when the Control:CONV bit is set to ‘1’ and is automatically cleared at the end of the data conversion cycle . At the start of data conversion, the device sets the Status:BUSY flag and automatically clears the Status:ADC_DRDY flag to indicate data conversion is in progress. When data conversion is complete, both the CONV bit and BUSY flag are cleared and the ADC_DRDY flag is set. To abort an ADC conversion in process, the host can clear the CONV bit to ‘0’.

The data in the ADC Data Registers is stored in 2s complement format. Full scale (7FFFh) is referred to the reference voltage (Vref), typically 1.225 V. A hardware protection circuit will not allow the converter to rollover from a full scale value (7FFFh) to a min scale value (8000h).

CLOCK GENERATOR CIRCUITS

The clock generator circuits are used to generate the internal clocks for the bq2028. The primary internal clocks are derived from the low frequency oscillator (32.768kHz), and the high frequency oscillator (8.389 MHz). The analog oscillator circuits are trimmed for accuracy, and then divided down for use throughout the device in both the analog and digital circuits. The bq2028 makes extensive use of clock gating to dynamically shutdown clocks to modules and interfaces not in use for low power operation. The low frequency oscillator (LFO) is required to run continuously during operation of the device with exception to a shutdown condition. The high frequency oscillator (HFO) is dynamically enabled and disabled as needed.

Low Frequency Oscillator Operation

The 32.768 kHz low frequency oscillator clock is generated from a fully integrated oscillator circuit with no requirements for external components. This circuit is trimmed for accuracy during factory production. The LFO trim value is stored in EEPROM memory Page 0. The LFO trim value is automatically read from EEPROM and written to the LFO trim register shortly after the device comes out of reset. The LFO output is divided down for various interfaces and modules in the device, as shown in Table 3.

Table 3. LFO Clocked Interfaces

INTERFACE OR MODULE	REQUIRED WHEN:	Frequency	DIVIDE
HFO Trim Circuit	HFO is enabled	32.768 kHz	LFO
Reset Timer	Power up of device (4ms)	32.768 kHz	LFO
HDQ low timeout	HDQ line is pulled low for 2sec	128 Hz	LFO/256

High Frequency Oscillator Operation

The 8.389 MHz high frequency oscillator clock is generated from a fully integrated oscillator circuit with no requirements for external components. The bq2028 trims the 8.389MHz high frequency clock output internally by using an automatic high frequency trim circuit. Using the more accurate 32.768kHz clock as a reference, the high frequency clock is adjusted until it is determined to be within the desired operating frequency. The trim circuit continues to monitor and adjust the 8.389MHz clock as needed. Due to the nature of the trim algorithm, some small changes may be noticed in the 8.389MHz clock as it is adjusted based upon operating conditions and the 32.768kHz reference clock. The HFO output is divided down for various modules in the device.

Table 4. HFO Clocked Interfaces

INTERFACE OR MODULE	REQUIRED WHEN:	FREQUENCY	DIVIDE
HFO Trim Circuit	HFO is enabled	8.389 MHz	HFO
HDQ Communication	HDQ interface is enabled	1.049 MHz	HFO/8
HDQ Register Access	Writing or reading unmapped HDQ registers	1.049 MHz	HFO/8
EEPROM Access	Reading or programming EEPROM memory	1.049 MHz	HFO/8
ADC	ADC conversion enabled	65.536 kHz	HFO/128

REVISION HISTORY

Changes from Original (October 2012) to Revision A	Page
• Deleted footnote "Assured by design. Not production tested" from DC Electrical Characteristics table.	4
• Deleted footnote "Assured by design. Not production tested" from AC Electrical Characteristics table.	5

Changes from Revision A (October 2012) to Revision B	Page
• Added Note 1 to I_{CC} Supply Current	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2028YZGR	ACTIVE	DSBGA	YZG	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ2028	Samples
BQ2028YZGT	ACTIVE	DSBGA	YZG	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ2028	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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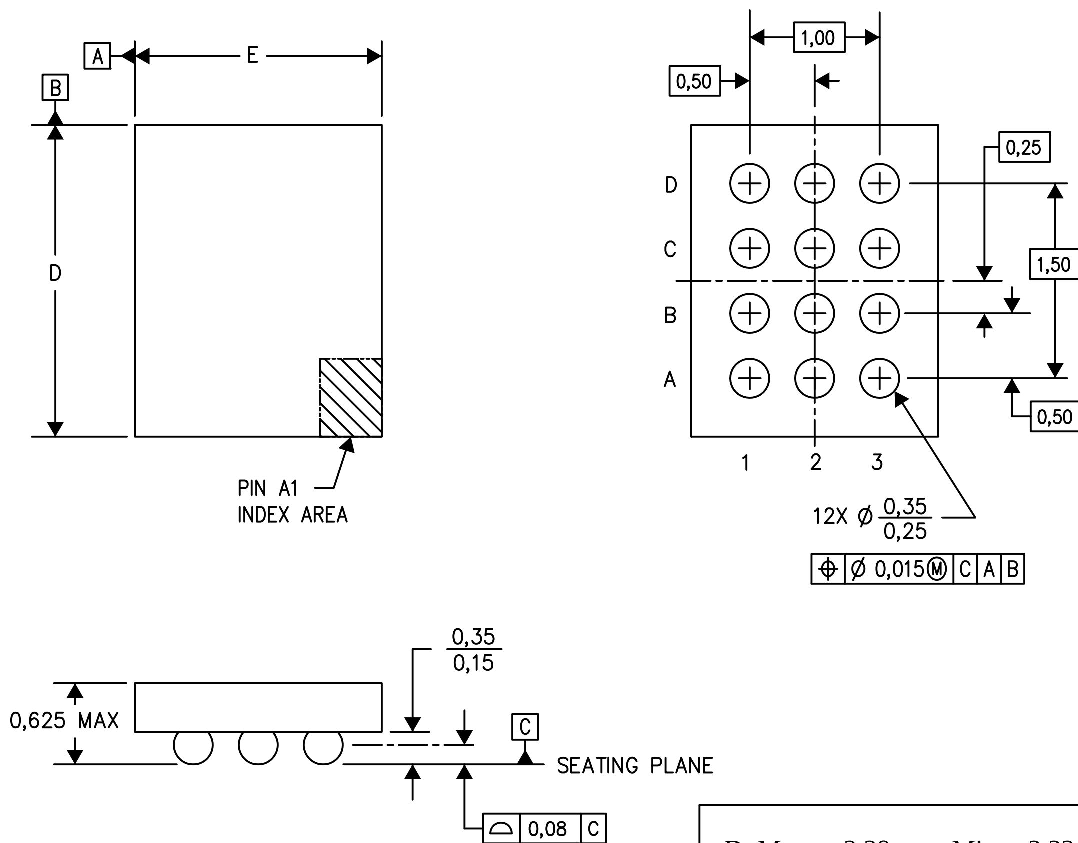
YZG (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



D: Max = 2.38 mm, Min = 2.32 mm

E: Max = 1.52 mm, Min = 1.46 mm

4205059/E 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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