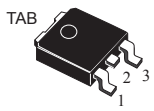
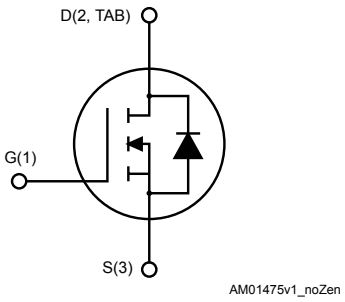
Datasheet

N-channel 200 V, 290 mΩ typ., 7 A, STripFET™ Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD7NS20T4	200 V	400 mΩ	7 A

- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Gate charge minimized

Applications

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

STPOWER

Product status link
STD7NS20T4

Product summary	
Order code	STD7NS20T4
Marking	D7NS20
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-source voltage (V_{GS} = 0 V)	200	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	7	A
	Drain current (continuous) at T_C = 100 °C	4.4	A
I_{DM}(1)	Drain current (pulsed)	28	A
P_{TOT}	Total power dissipation at T_C = 25 °C	86	W
E_{AS}(2)	Single pulse avalanche energy	110	mJ
dv/dt(3)	Drain-body diode dynamic dv/dt ruggedness	5.8	V/ns
T_{stg}	Storage temperature range	-65 to 175	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *Starting T_J = 25 °C, I_D = 4.5 A*
3. *I_{SD} = 7 A, di/dt = 520 A/µs, V_{DD} = 50 V, T_J < T_{Jmax}*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.74	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50	°C/W

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board.*

2 Electrical characteristics

T_{CASE} = 25 °C unless otherwise specified

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0 V	200			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V, V_{GS} = 0 V			1	µA
		V_{DS} = 200 V, V_{GS} = 0 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3.5 A		290	400	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	370	-	pF
C_{oss}	Output capacitance		-	77	-	pF
C_{rss}	Reverse transfer capacitance		-	14	-	pF
Q_g	Total gate charge	V_{DD} = 160 V, I_D = 7 A V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	11.6	-	nC
Q_{gs}	Gate-source charge		-	2.2	-	nC
Q_{gd}	Gate-drain charge		-	5.4	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V, I_D = 4.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	5.6	-	ns
t_r	Rise time		-	2.6	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 7 A, di/dt = 100 A/µs, V_{DD} = 50 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	118.5		ns
Q_{rr}	Reverse recovery charge		-	393		nC
I_{RRM}	Reverse recovery current		-	6.6		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

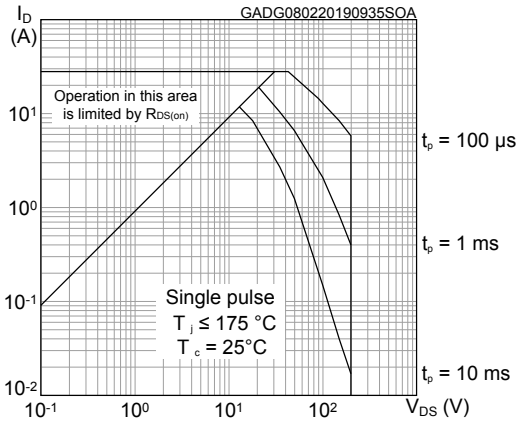


Figure 2. Thermal impedance

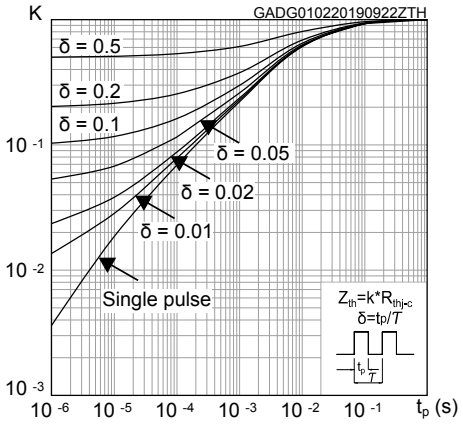


Figure 3. Output characteristics

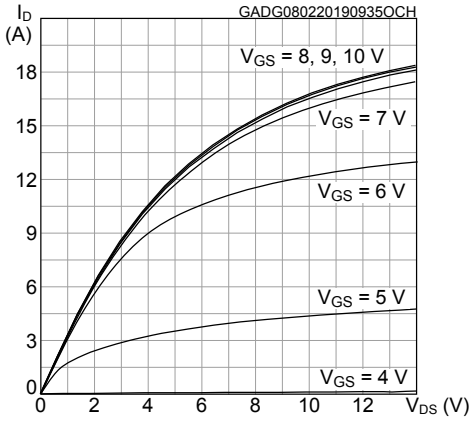


Figure 4. Transfer characteristics

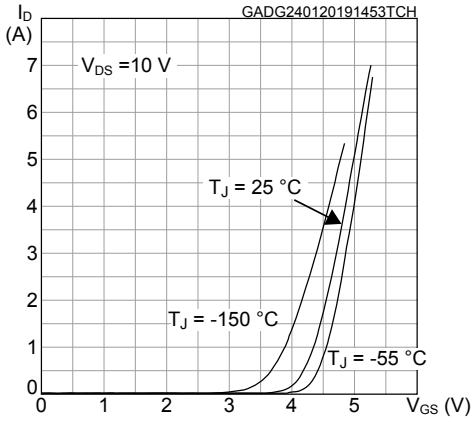


Figure 5. Gate charge vs gate-source voltage

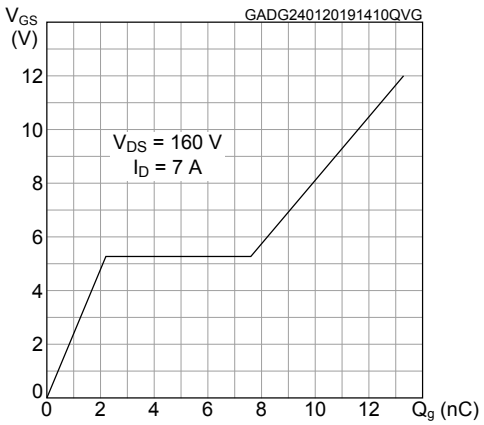


Figure 6. Static drain-source on-resistance

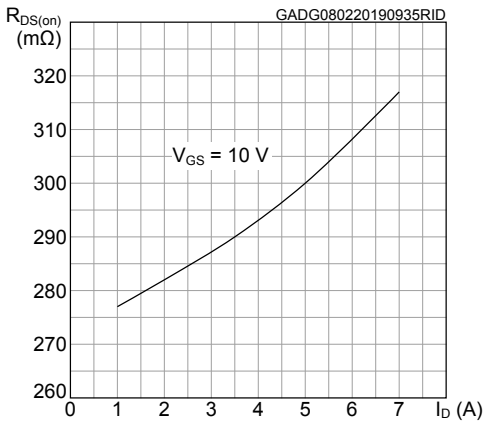


Figure 7. Capacitance variations

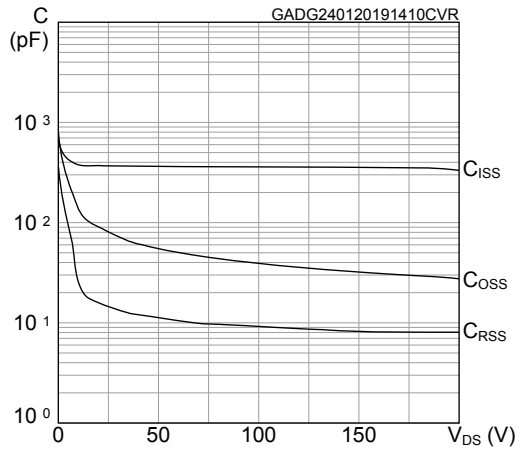


Figure 8. Normalized gate threshold voltage vs temperature

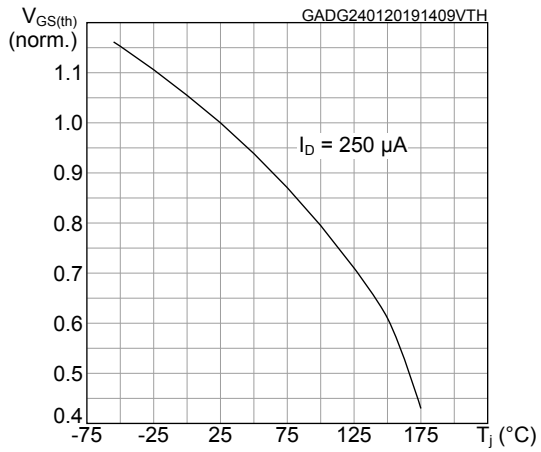


Figure 9. Normalized on-resistance vs temperature

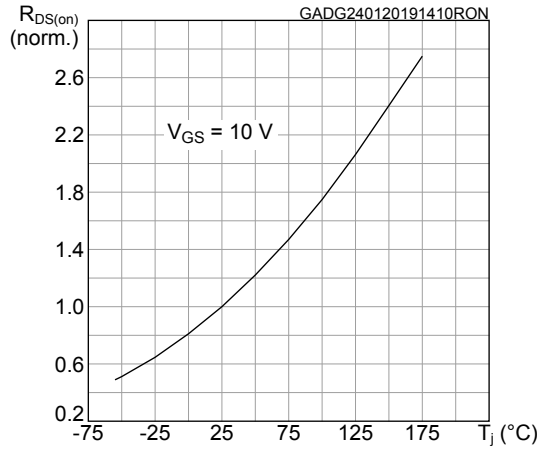


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

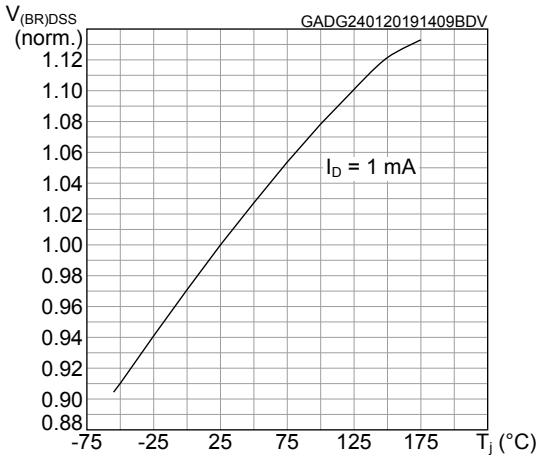
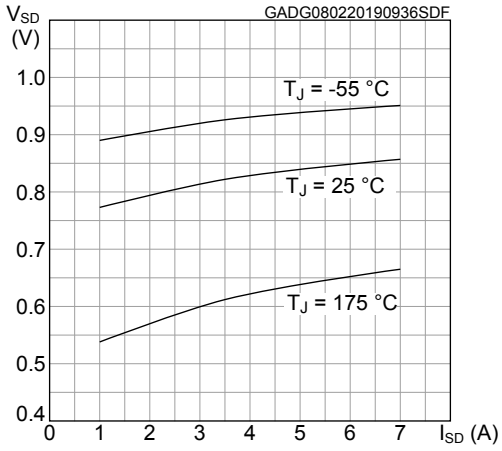


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

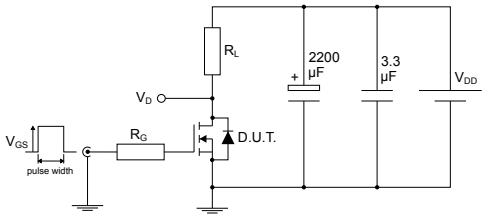


Figure 13. Test circuit for gate charge behavior

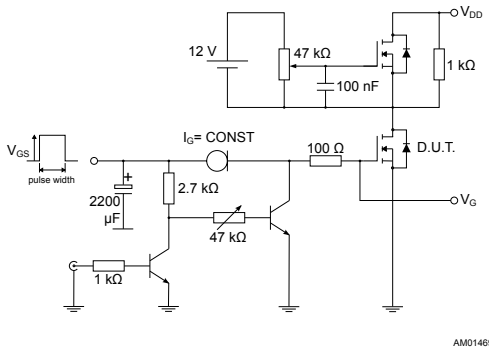


Figure 14. Test circuit for inductive load switching and diode recovery times

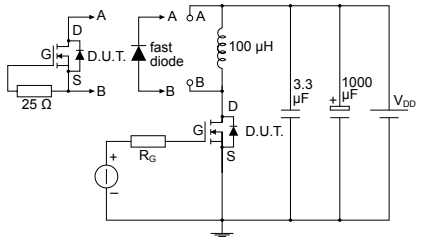


Figure 15. Unclamped inductive load test circuit

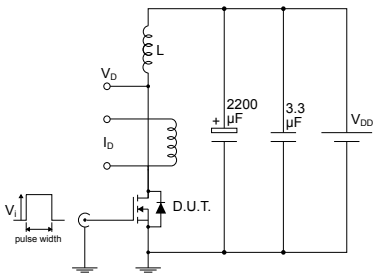


Figure 16. Unclamped inductive waveform

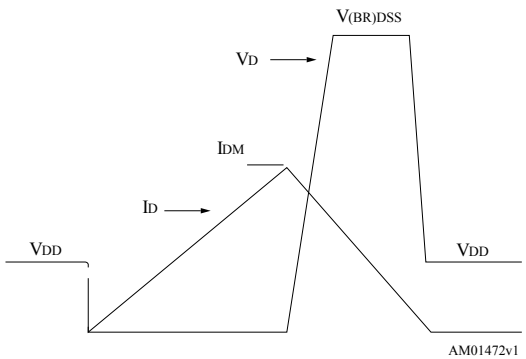
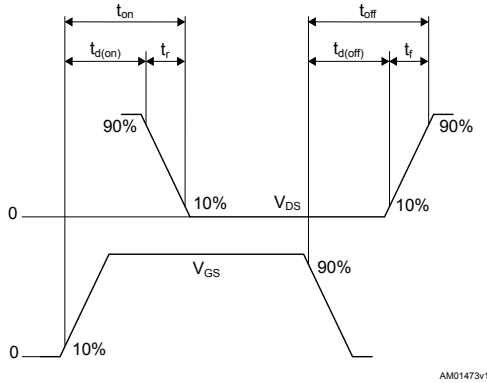


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 18. **DPAK (TO-252) type A package outline**

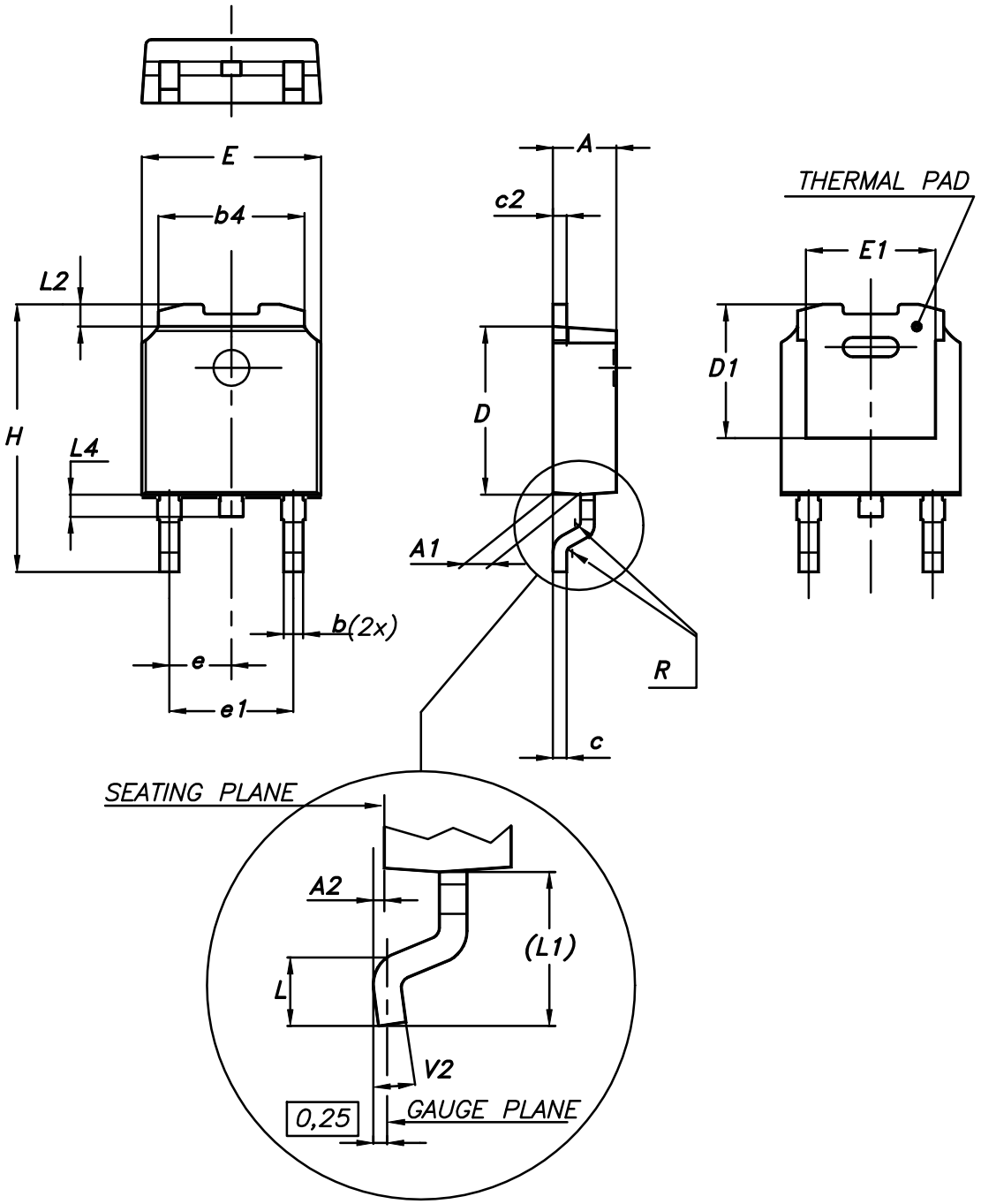
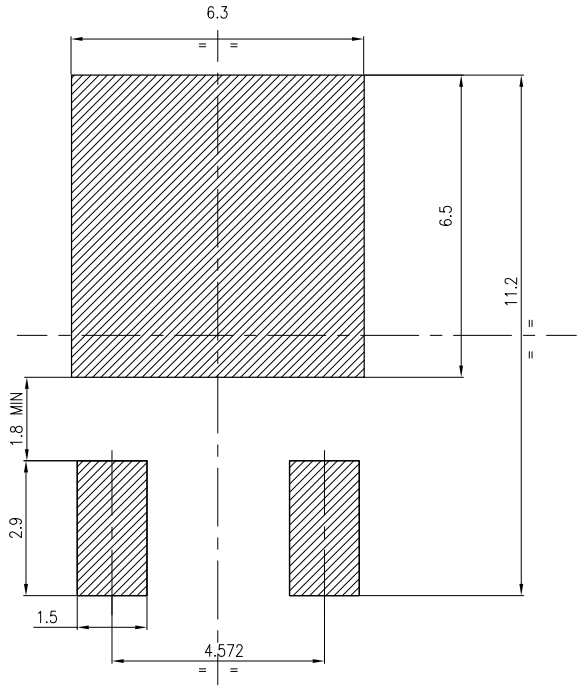


Table 7. **DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 19. DPAK (TO-252) type A recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 20. **DPAK (TO-252) tape outline**

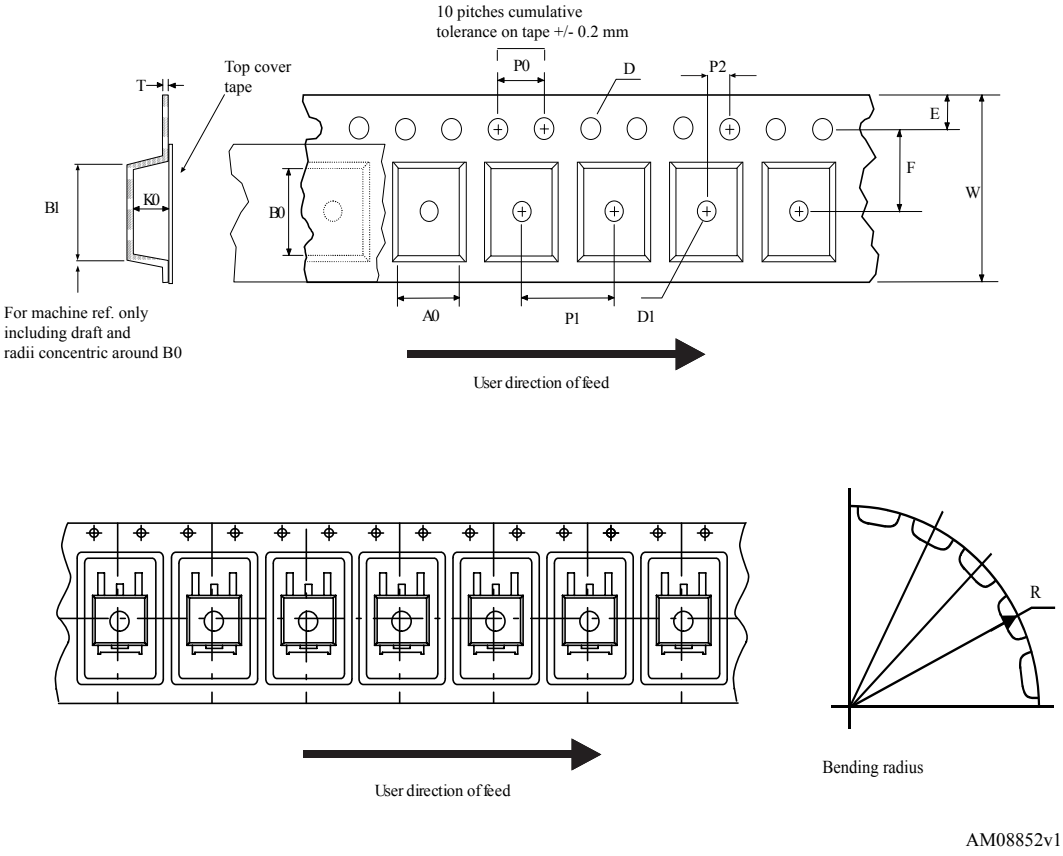


Figure 21. **DPAK (TO-252) reel outline**

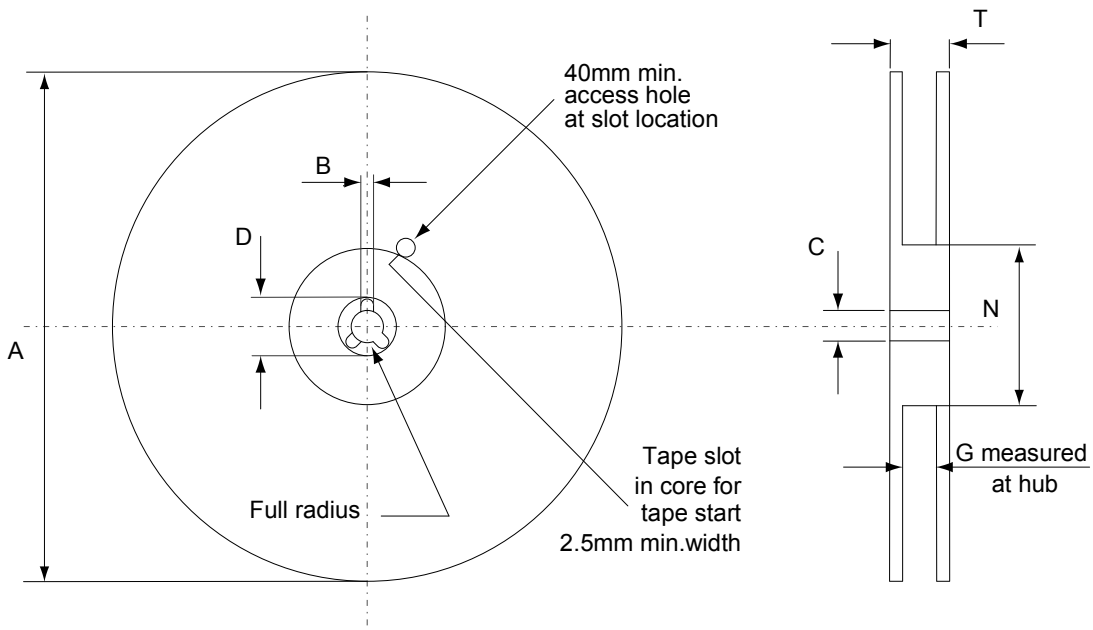


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Table 8. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 9. **Document revision history**

Date	Version	Changes
11-Feb-2019	1	First release.

Contents