STP260N4F7

N-channel 40 V, 1.8 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - production data

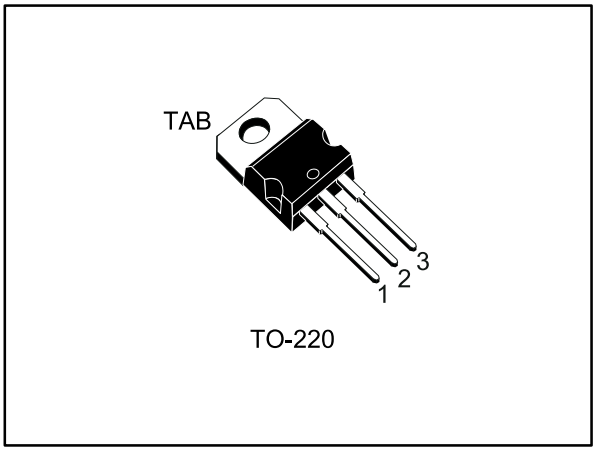
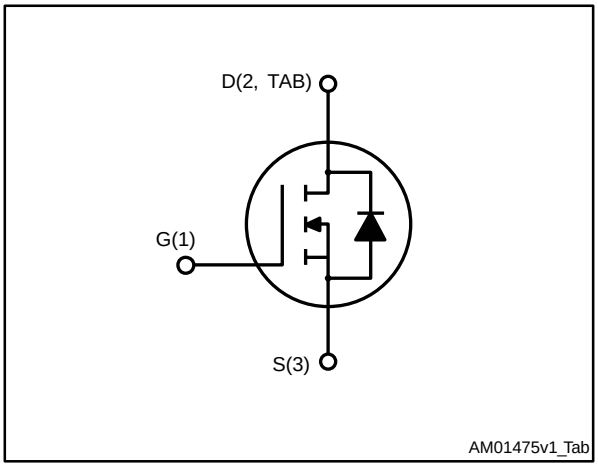


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)max}$	I_D	P_{TOT}
STP260N4F7	40 V	2.2 mΩ	120 A	235 W

Features

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP260N4F7	260N4F7	TO-220	Tube

Contents

1 Electrical ratings 3
2 Electrical characteristics 4
2.1 Electrical characteristics (curves) 6
3 Test circuits 8
4 Package information data 9
4.1 TO-220 type A package information 10
5 Revision history 12

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate source voltage	±20	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	120	A
I_D(1)	Drain current (continuous) at T_C = 100 °C	120	A
I_{DM}(2)	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at T_C = 25 °C	235	W
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

Notes:

(1)Current limited by package.

(2)Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.64	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D= 250 µA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS}= 0 V, V_{DS}= 40 V			1	µA
		V_{GS}= 0 V, V_{DS}= 40 V, T_C= 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 60 A		1.8	2.2	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS}= 25 V, f = 1 MHz	-	5600	-	pF
C_{oss}	Output capacitance		-	2400	-	pF
C_{rss}	Reverse transfer capacitance		-	35	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 120 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	67	-	nC
Q_{gs}	Gate-source charge		-	31	-	nC
Q_{gd}	Gate-drain charge		-	9	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20V, I_D = 60 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	30	-	ns
t_r	Rise time		-	21	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
t_f	Fall time		-	13	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	V_{GS} = 0 V, I_{SD}= 120 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs	-	68		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 32 V, T_J= 150 °C	-	98		nC
I_{RRM}	Reverse recovery current	(see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	2.9		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

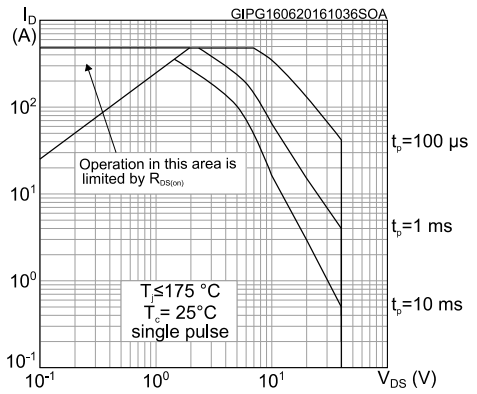


Figure 3: Thermal impedance

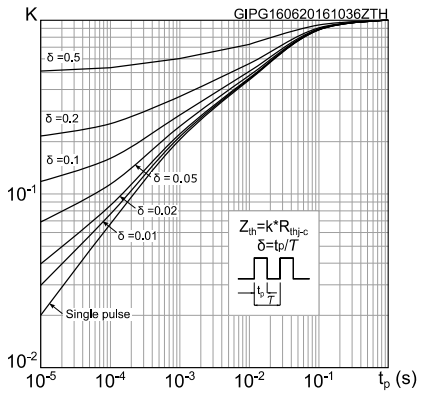


Figure 4: Output characteristics

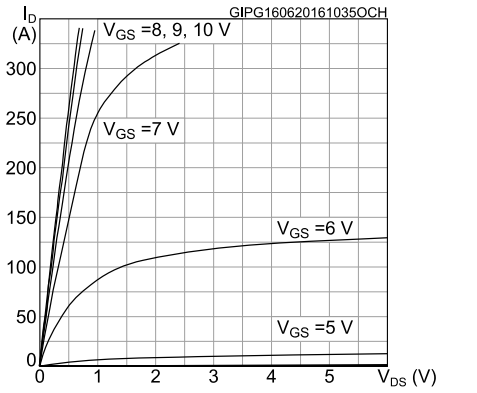


Figure 5: Transfer characteristics

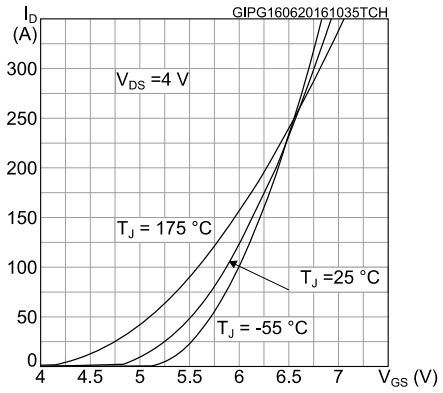


Figure 6: Gate charge vs gate-source voltage

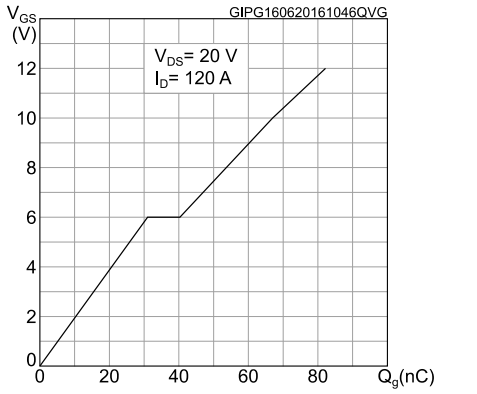


Figure 7: Static drain-source on-resistance

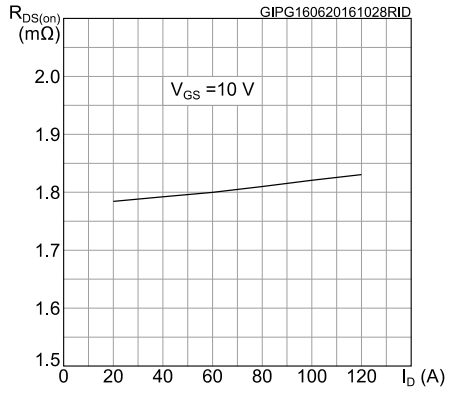


Figure 8: Capacitance variations

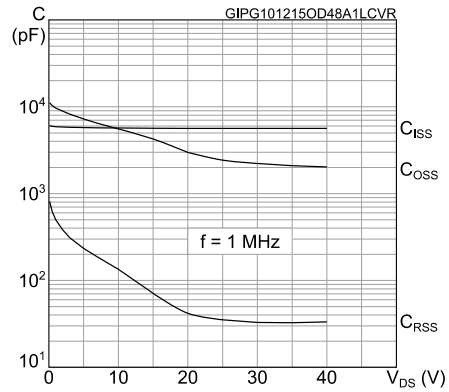


Figure 9: Normalized on-resistance vs temperature

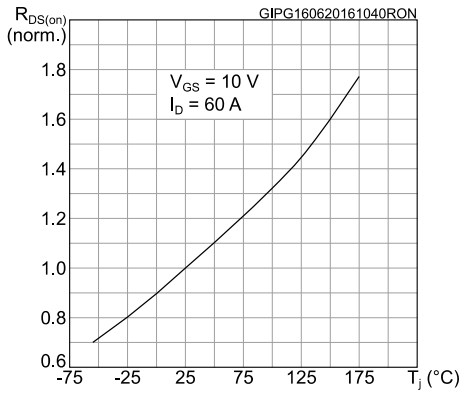


Figure 10: Normalized $V_{(BR)DSS}$ vs temperature

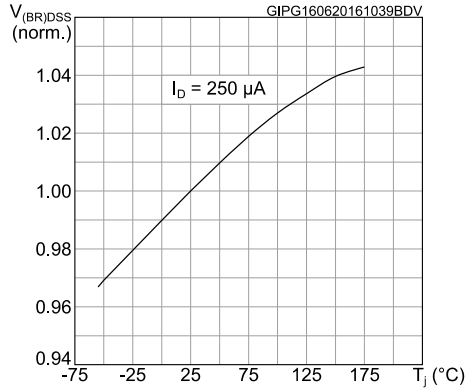


Figure 11: Normalized gate threshold voltage vs temperature

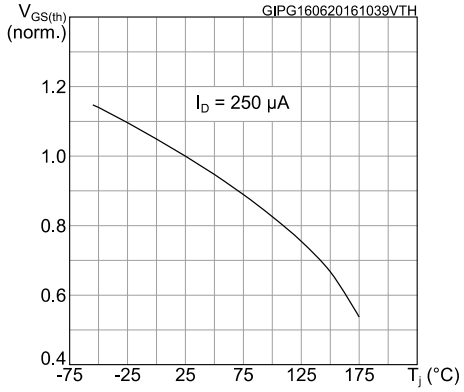
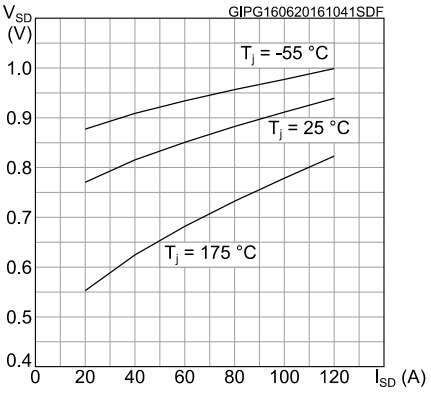


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

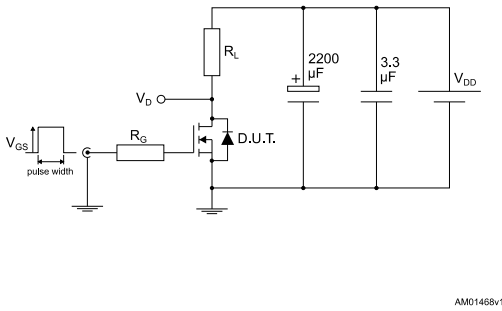


Figure 14: Test circuit for gate charge behavior

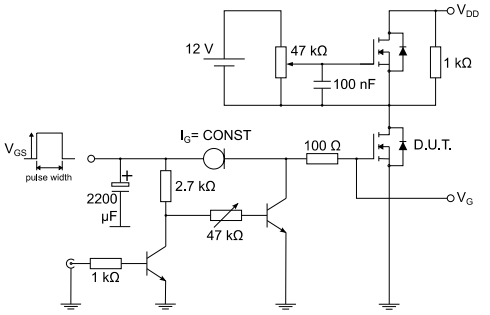


Figure 15: Test circuit for inductive load switching and diode recovery times

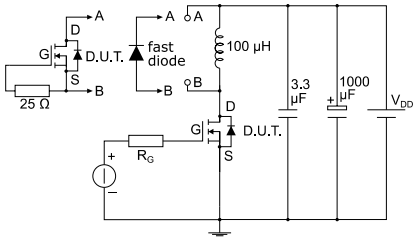


Figure 16: Unclamped inductive load test circuit

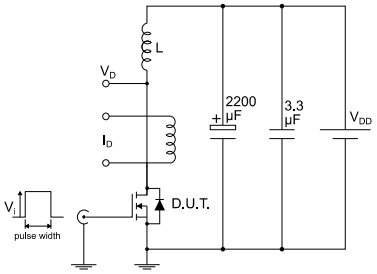


Figure 17: Unclamped inductive waveform

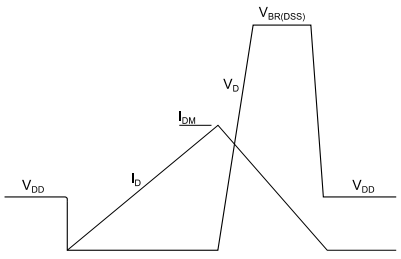
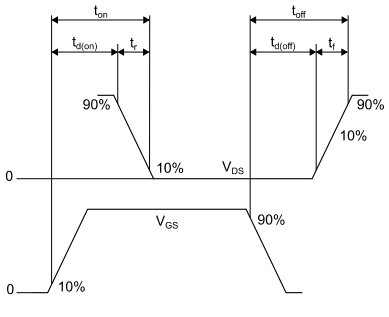


Figure 18: Switching time waveform



4 Package information data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 19: TO-220 type A package outline

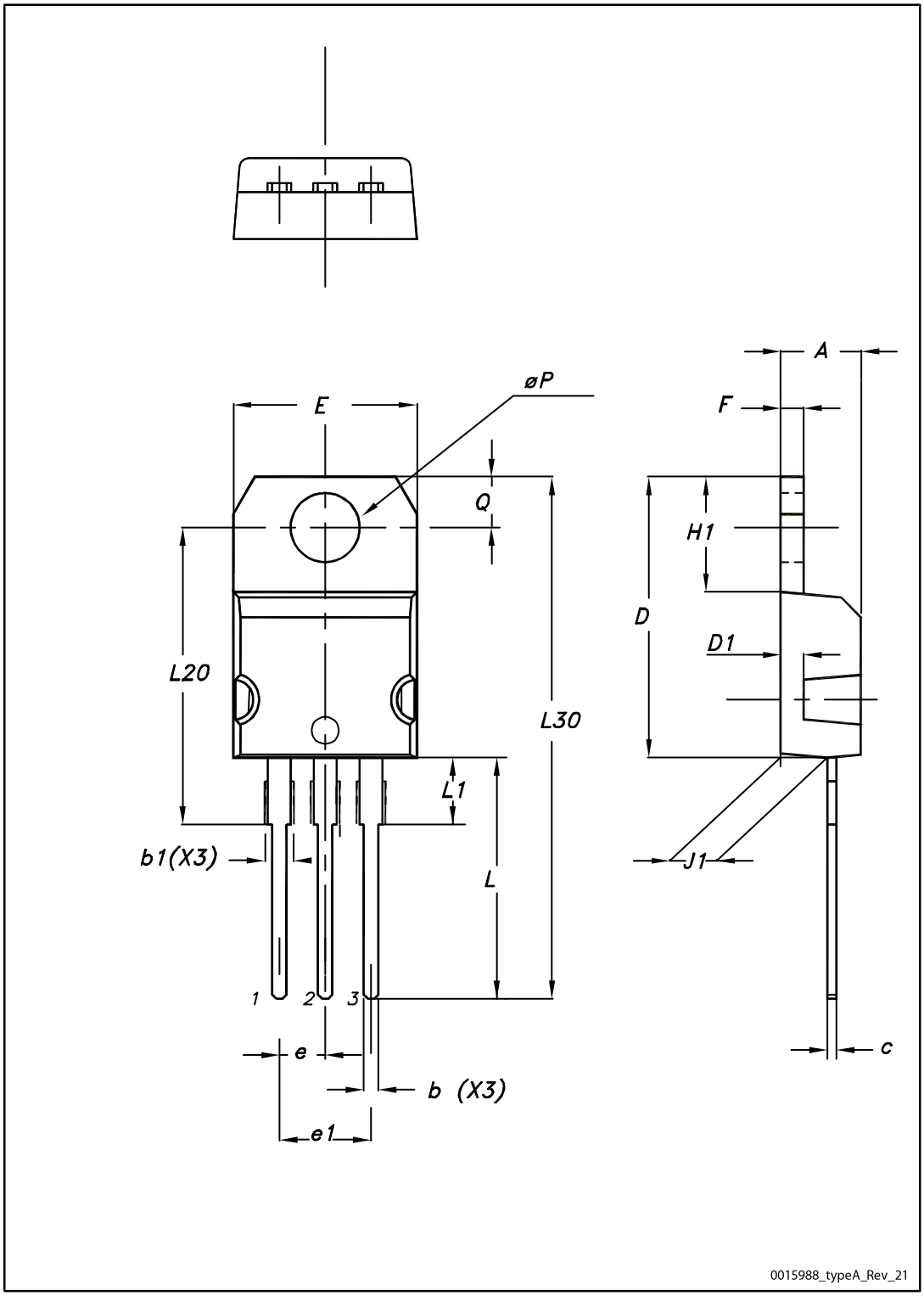


Table 8: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
21-Sep-2015	1	First release.
16-Jun-2016	2	Modified: title anf features in cover page Modified: *Table 2: "Absolute maximum ratings"*, *Table 3: "Thermal data"*, *Table 4: "On /off states"*, *Table 5: "Dynamic"*, *Table 6: "Switching times"* and *Table 7: "Source-drain diode"* Added: *Section 5.1: "Electrical characteristics (curves)"* Minortext changes

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.