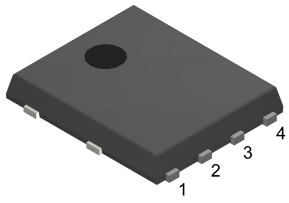
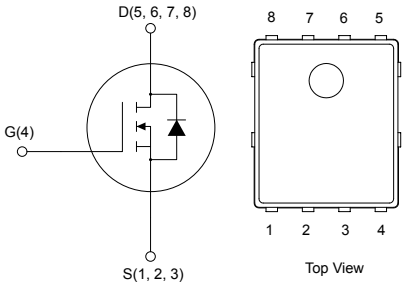
N-channel 40 V, 1.3 mΩ typ., 120 A STripFET F7 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL210N4F7	40 V	1.6 mΩ	120 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status link
STL210N4F7

Product summary	
Order code	STL210N4F7
Marking	210N4
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	120	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	120	A
I_{DM} (2) (1)	Drain current (pulsed)	480	A
P_{TOT}	Total power dissipation at T_C = 25 °C	150	W
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	40	A
E_{AS}	Single pulse avalanche energy (T_j = 25 °C, I_D = I_{AV}, V_{DD} = 25 V)	300	mJ
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. *Drain current is limited by package, the current capability of the silicon is 229 A at 25 °C.*
2. *Pulse width limited by safe operating area*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max.	31.3	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	1.0	°C/W

1. *When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D= 250 µA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS}= 40 V			1	µA
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 16 A		1.3	1.6	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS}= 0 V	-	3600	-	pF
C_{oss}	Output capacitance		-	1240	-	pF
C_{rss}	Reverse transfer capacitance		-	88	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 40 A, V_{GS} = 10 V (see Figure 13. Test circuit for gate charge behavior)	-	43	-	nC
Q_{gs}	Gate-source charge		-	19	-	nC
Q_{gd}	Gate-drain charge		-	13	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	34	-	ns
t_f	Fall time		-	12	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 40 A, V_{GS} = 0 V	-		1.2	V
t_{rr}	Reverse recovery time	(see)Figure 14. Test circuit for inductive load switching and diode recovery times I_D = 40 A, di/dt = 100 A/µs V_{DD} = 32 V	-	53		ns
Q_{rr}	Reverse recovery charge		-	71		nC
I_{RRM}	Reverse recovery current		-	2.7		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

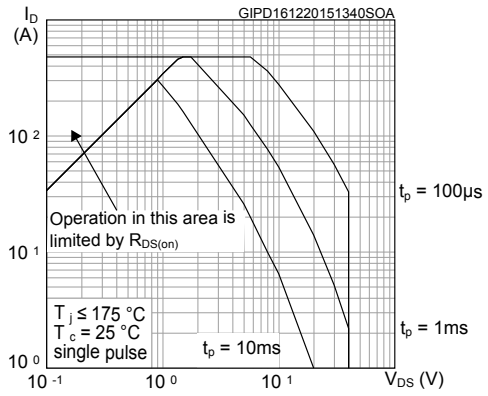


Figure 2. Thermal impedance

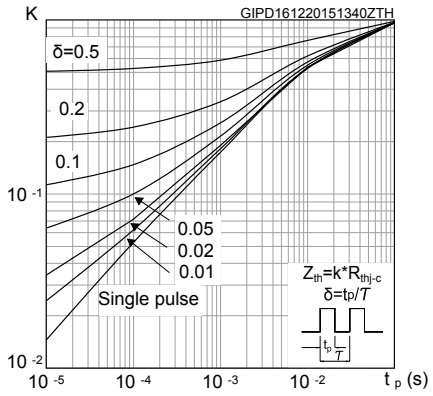


Figure 3. Output characteristics

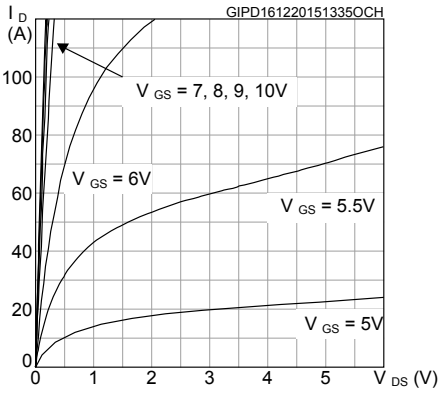


Figure 4. Transfer characteristics

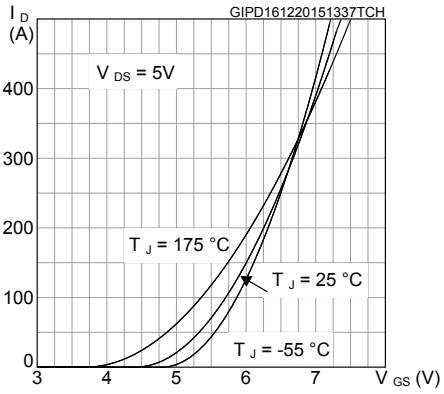


Figure 5. Gate charge vs gate-source voltage

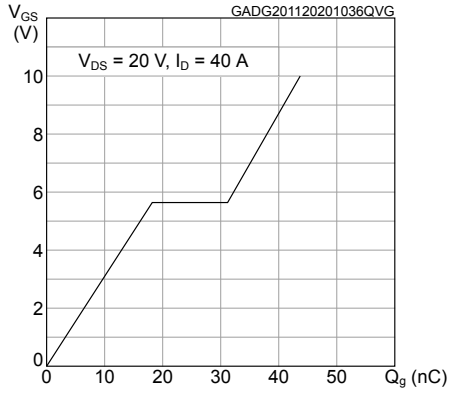


Figure 6. Static drain-source on-resistance

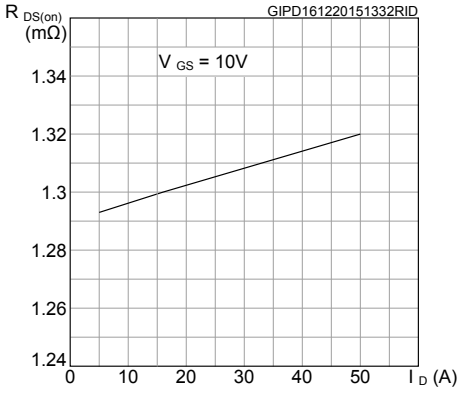


Figure 7. Capacitance variations

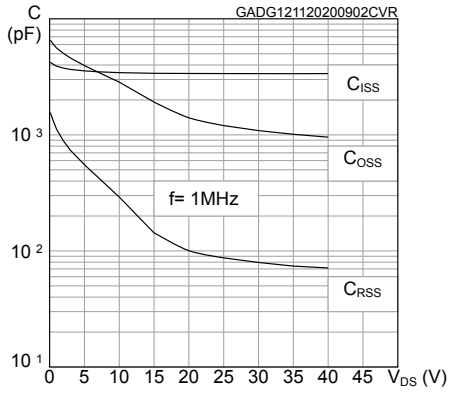


Figure 8. Normalized on-resistance vs temperature

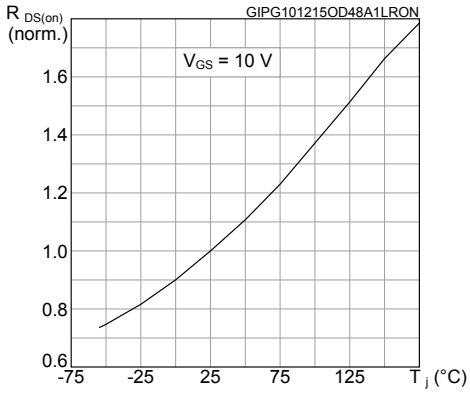


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

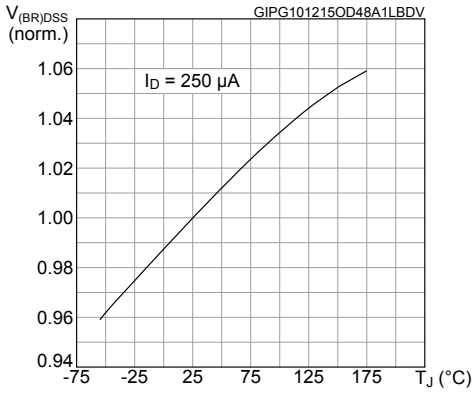


Figure 10. Normalized gate threshold voltage vs temperature

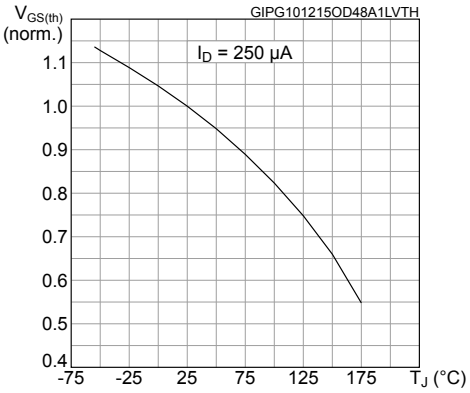
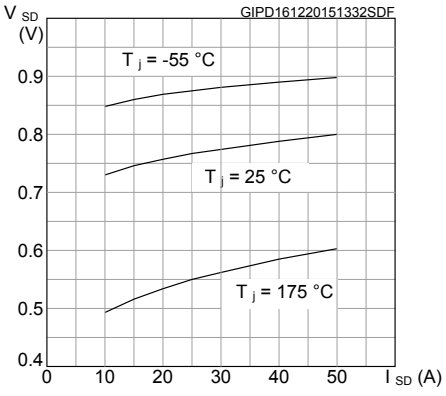


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

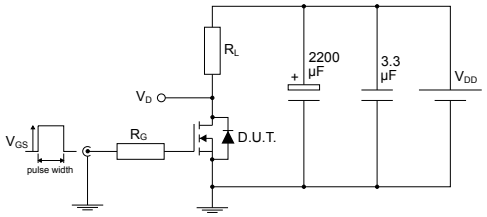


Figure 13. Test circuit for gate charge behavior

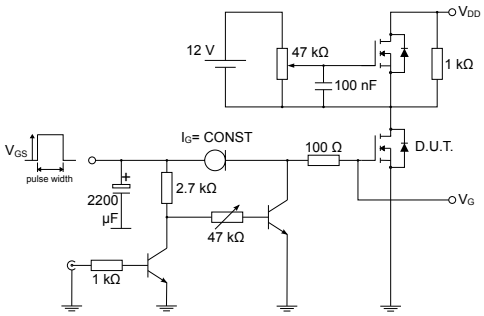


Figure 14. Test circuit for inductive load switching and diode recovery times

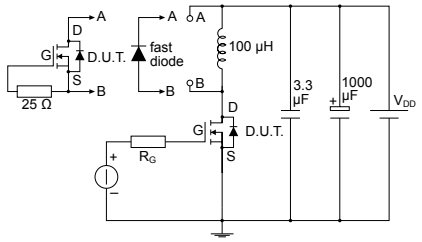


Figure 15. Unclamped inductive load test circuit

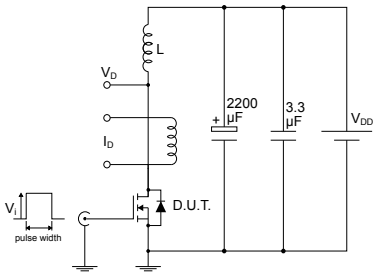


Figure 16. Unclamped inductive waveform

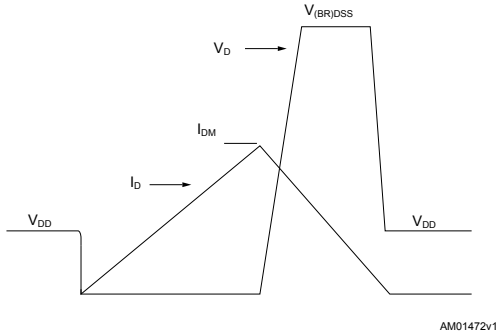
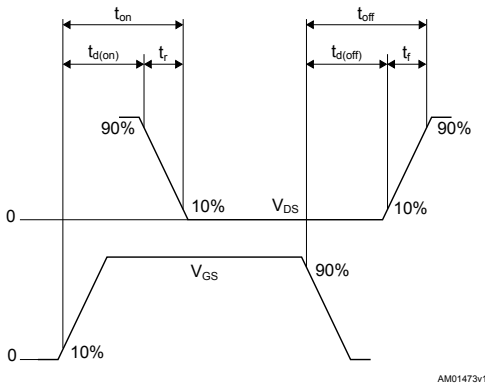


Figure 17. Switching time waveform

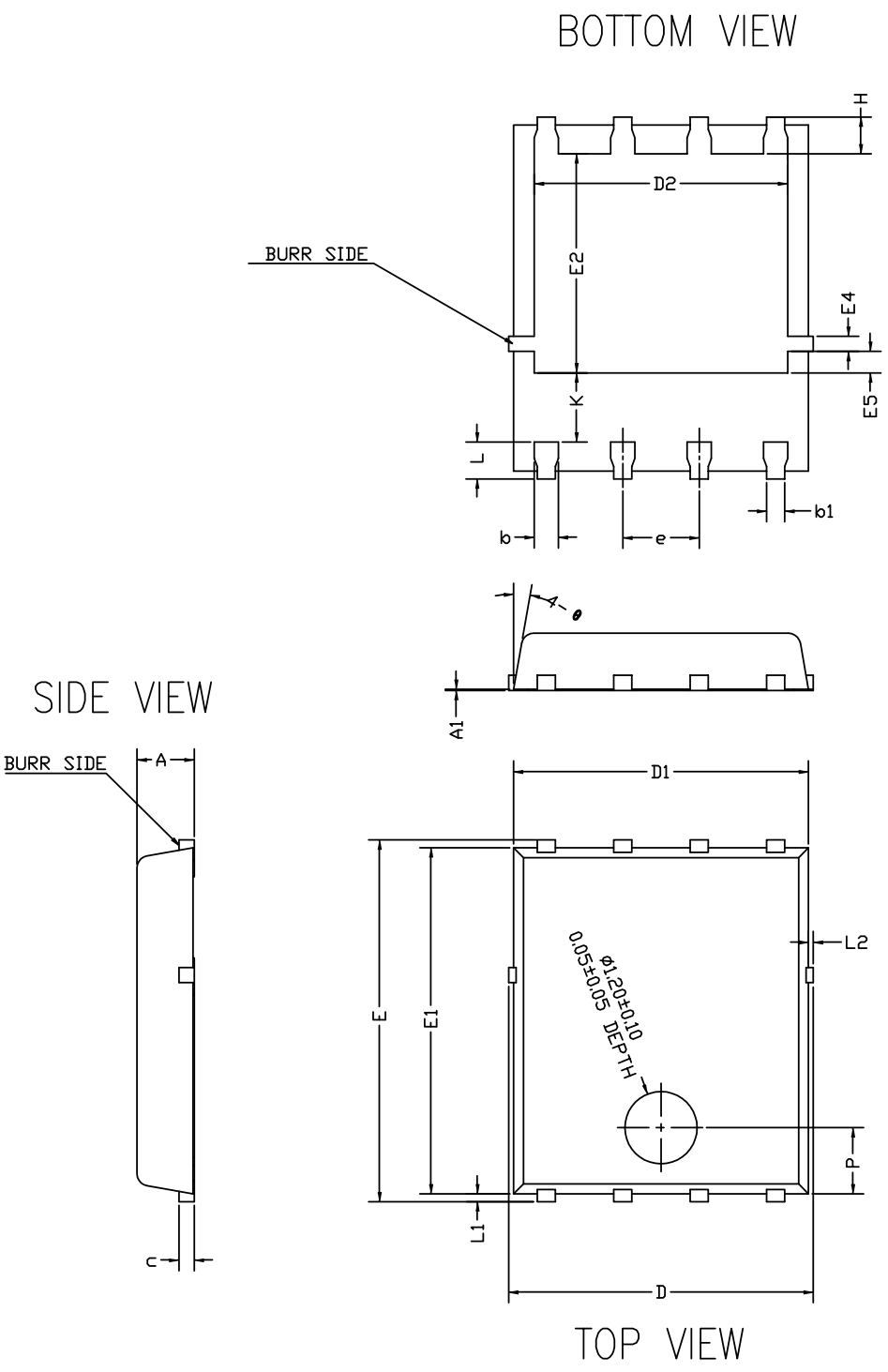


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 type SUBCON package information

Figure 18. **PowerFLAT 5x6 type SUBCON package outline**

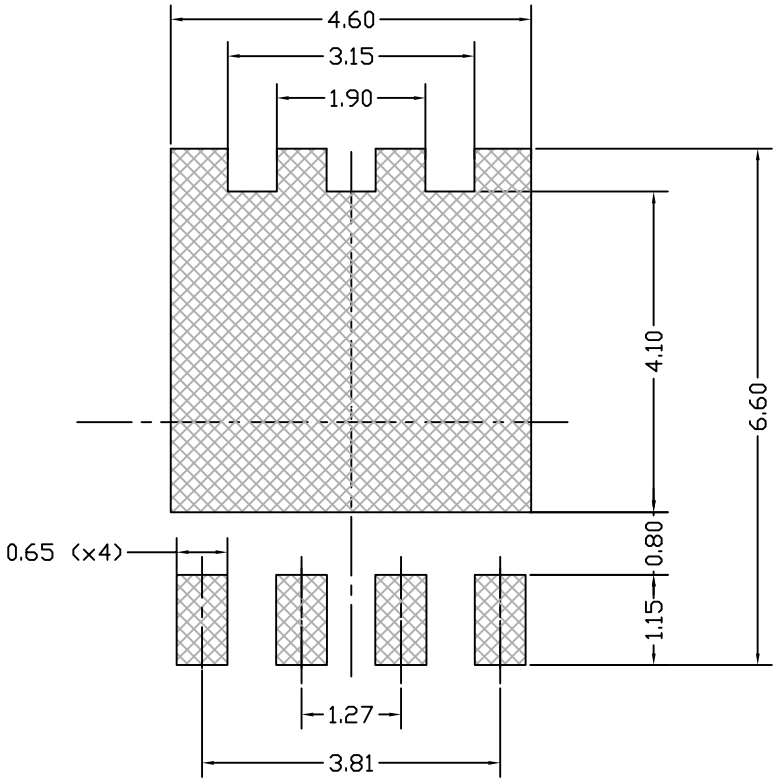


8231817_SUBCON_REV4

Table 7. PowerFLAT 5x6 type SUBCON package mechanical data

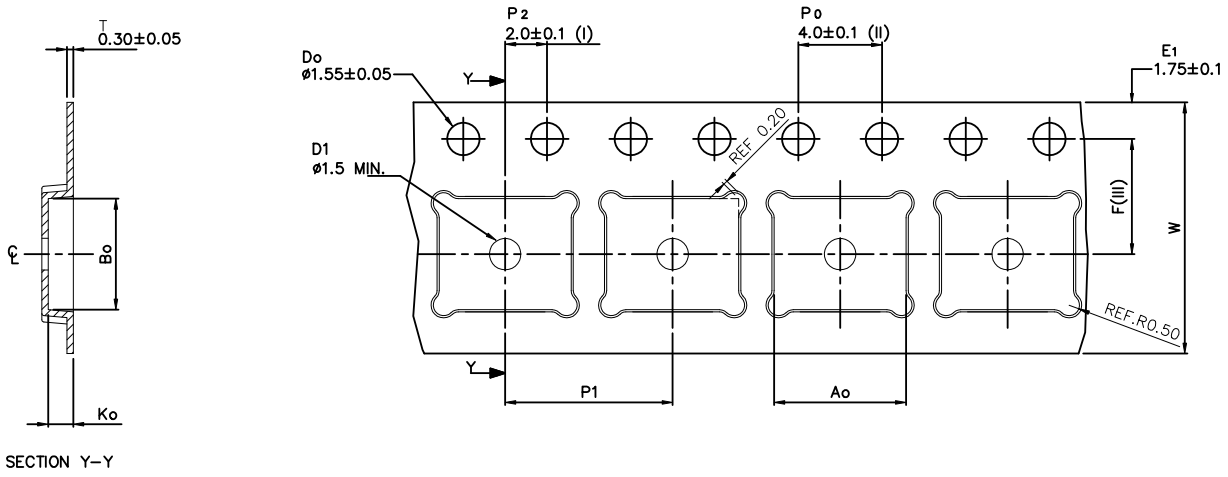
Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D	4.80		5.10
D1	4.80	4.90	5.00
D2	4.01	4.21	4.31
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.54	3.64	3.74
E4	0.15	0.25	0.35
E5	0.26	0.36	0.46
H	0.51	0.61	0.71
K	0.95		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

Figure 19. **PowerFLAT 5x6 recommended footprint (dimensions are in mm)**



4.2 PowerFLAT 5x6 packing information

Figure 20. PowerFLAT 5x6 tape (dimensions are in mm)



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 21. PowerFLAT 5x6 package orientation in carrier tape

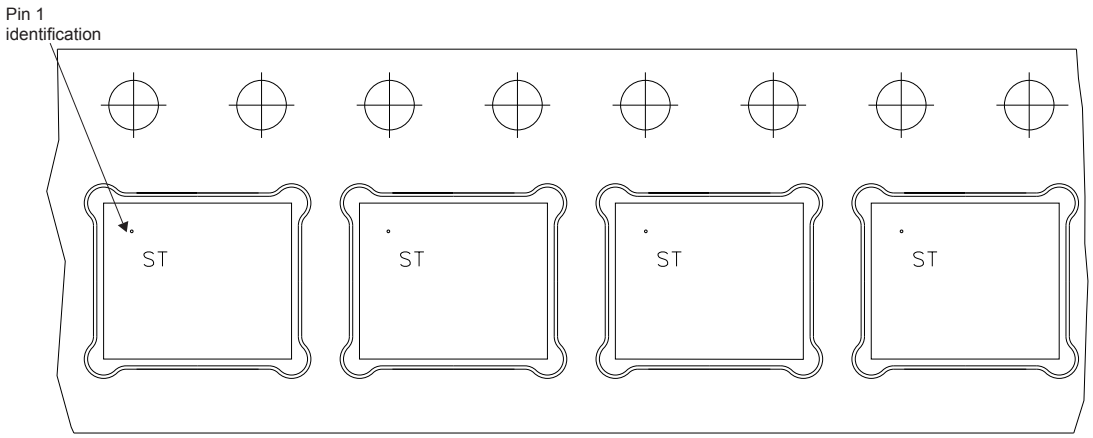
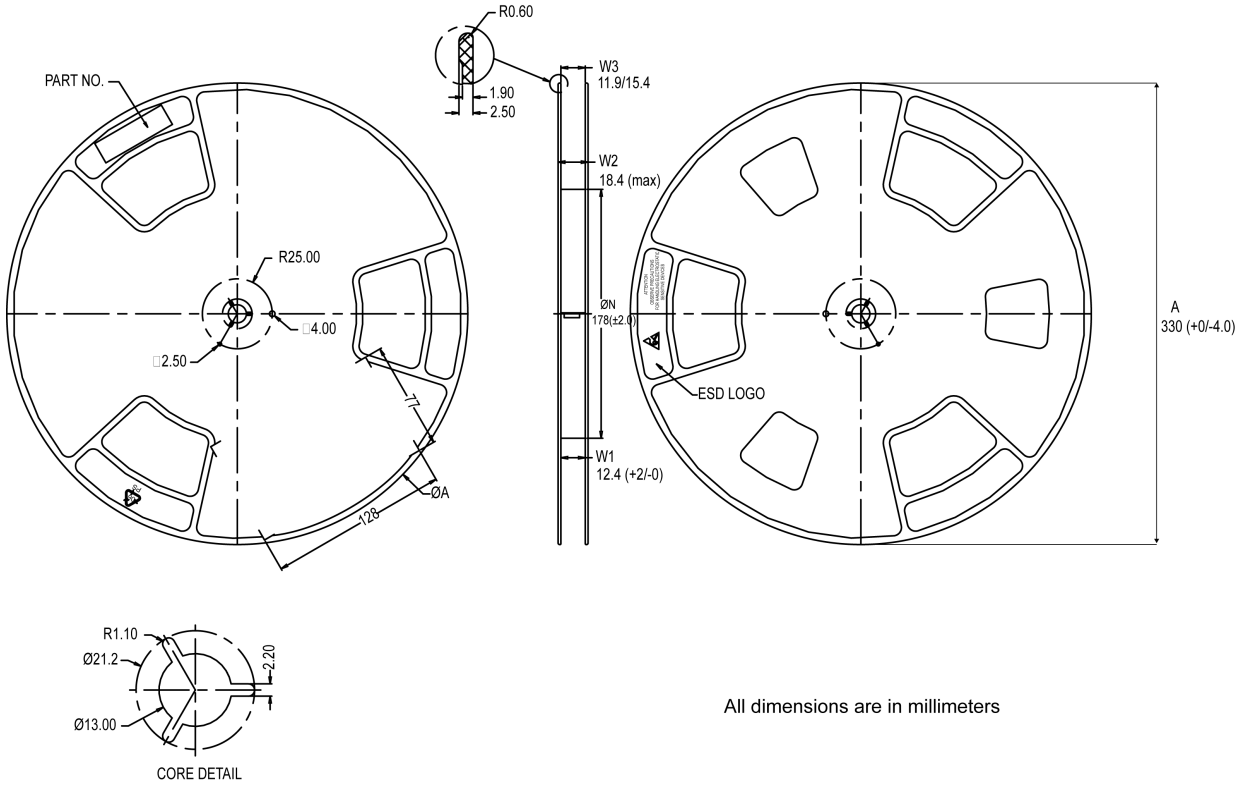


Figure 22. **PowerFLAT 5x6 reel**

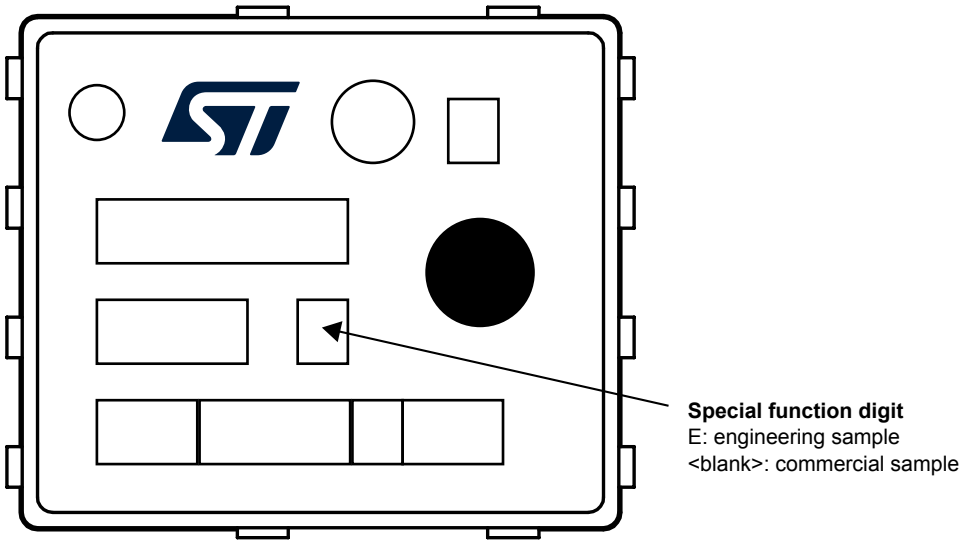


All dimensions are in millimeters

8234350_Reel_rev_C

4.3 PowerFLAT 5x6 marking information

Figure 23. **PowerFLAT 5x6 marking information**



Note: Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

Revision history

Table 8. **Document revision history**

Date	Version	Changes
13-Oct-2020	1	Initial release.
20-Nov-2020	2	Updated Section 2 Electrical characteristics, Figure 7. Capacitance variations and Figure 5. Gate charge vs gate-source voltage.

Contents