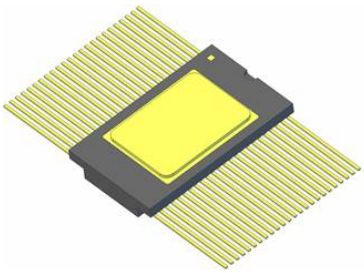
RHFLVDS218

Datasheet

Rad-hard LVDS deserializer

Ceramic Flat-48



The upper metallic lid is connected to pin 17

Product status link
RHFLVDS218

Features

- 15 to 75 MHz shift clock support
- 50 % duty cycle on receiver output clock
- -4 V to 5 V common-mode range
- Cold sparing all pins
- Fail-safe function
- Narrow bus reduces cable size and cost
- Up to 1.575 Gbps throughput
- Up to 197 Mbytes/s bandwidth
- 325 mV (typ) LVDS swing
- PLL requires no external components
- Rising edge strobe
- Operational environment: total dose irradiation testing to MIL-STD-883 method 1019
  - Total-dose: 300 krad (Si)
  - Latchup immune (LET > 120 MeV-cm2/mg)
- Compatible with TIA/EIA-644 LVDS standard

Description

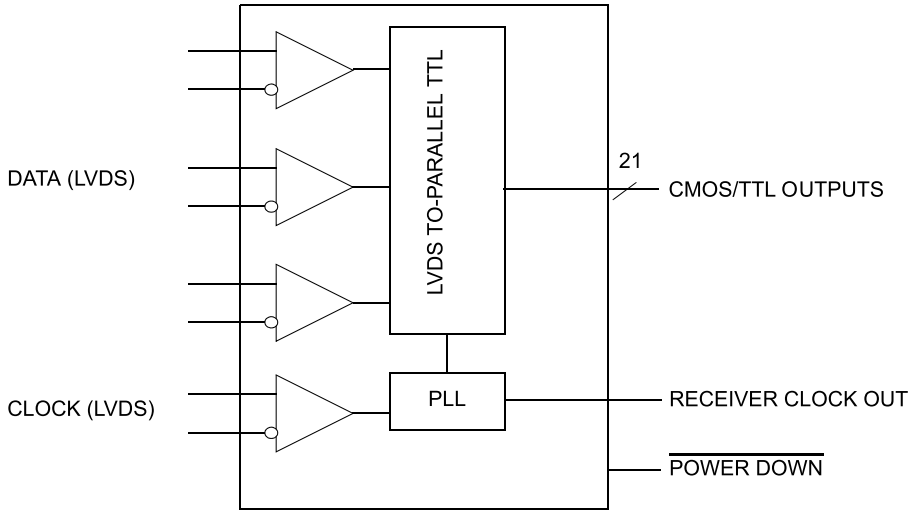
The RHFLVDS218 deserializer converts the three LVDS data streams back into 21 bits of CMOS/TTL data. At a transmitter clock frequency of 75 MHz, 21 bits of TTL data are transmitted at a rate of 525 Mbps per LVDS data channel. Using a 75 MHz clock, the data throughput is 1.575 Gbit/s (197 Mbytes/s).

The RHFLVDS218 deserializer allows the use of wide, high speed TTL interfaces while reducing overall EMI and cable size.

All pins have cold spare buffers. These buffers are high impedance when V_{CC} is tied to 0 V.

1 Functional description

Figure 2. **RHFLVDS218 deserializer functional block diagram**



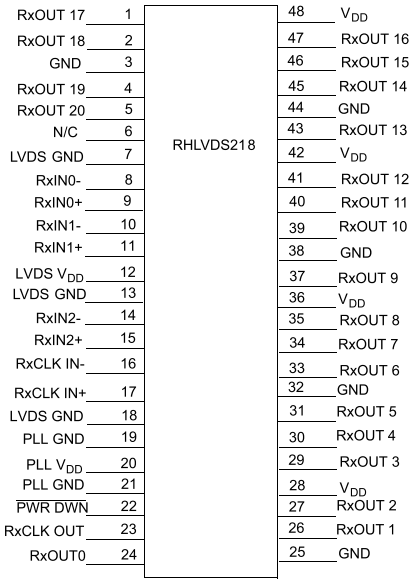
2 Pin configuration

Table 1. Pin description

Pin name	I/O	N	Description
RxIN+	I	3	Positive LVDS differential data inputs (1)
RxIN-	I	3	Negative LVDS differential data output (1)
RxOUT	O	21	TTL level data outputs
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN-	I	1	Negative LVDS differential clock input
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low
V_{CC}	I	4	Power supply pins for TTL outputs and logic
GND	I	5	Ground pins for TTL outputs and logic
PLL V_{CC}	I	1	Power supply pins for PLL
PLL GND	I	2	Ground pins for PPL
LVDS V_{CC}	I	1	Power supply pin for LVDS pins
LVDS GND	I	3	Ground pins for LVDS inputs

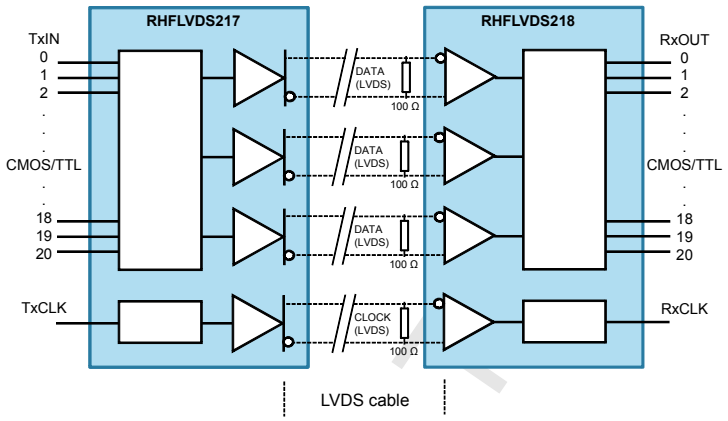
1. *These receivers have input fail-safe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs are in a HIGH state. If a clock signal is present, data outputs are all be HIGH. If the clock input is also floating/terminated outputs remain in the last valid state. A floating/terminated clock input results in a LOW clock output.*

Figure 3. RHFLVDS218 pinout



3 Typical application

Figure 4. **RHFLVDS218 typical application**



4 Absolute maximum ratings and operating conditions

Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond the limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

Table 2. Absolute maximum ratings (references to GND)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		4.8	V
V_i	TTL inputs (operating or cold-spare)		-0.3 to 4.8	
V_{CM}	LVDS common-mode (operating or cold-spare)		-5 to 6	
T_{stg}	Storage temperature range		-65 to 150	°C
T_j	Maximun junction temperature		150	
R_{thjc}	Thermal resistance junction to case (2)		10	°C/W
ESD	HBM: human body model	All pins except LVDS outputs	2	kV
		LVDS inputs vs. GND	8	
	CDM: charge device model		500	V

1. *All voltages, except the differential I/O bus voltage, are with respect to the network ground terminal.*
2. *Test per MIL-STD-883, method 1012. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.*

Table 3. Recommended operating conditions (referenced to GND)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CM}	Static common-mode on the receiver	-4		5	
T_A	Ambient temperature range	-55		125	°C
C_L	Output capacitive load	3			pF

5 Electrical characteristics

In Table 4. DC electrical characteristics, V_{CC} = 3 V to 3.6 V, - 55 °C < T_A < 125 °C, unless otherwise specified, T_A is per the temperature noted. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.

Table 4. DC electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
CMOS/TTL DC specifications ($\overline{\text{PWR DWN}}$, RXOUT)						
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.8	
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.25	
V_{OH}	High-level output voltage	I_{OL} = -0.4 mA	2.7			
I_{IH}	High-level input current	V_{IN} = 3.6 V, V_{CC} = 3.6 V	-10		10	µA
I_{IL}	Low-level input current	V_{IN} = 0 V, V_{CC} = 3.6 V	-10		10	
V_{CL}	Input clamp voltage	I_{CL} = -18 mA			-1.5	V
I_{CS}	Cold spare leakage current	V_{IN} = 3.6 V, V_{CC} = GND	-10		10	µA
I_{OS} (1)	Output short-circuit current	V_{OUT} = 0 V	-30		-90	mA
I_{OFF}	TTL/CMOS and clock output leakage current in power-down	PWR DWN low, V_{out} = 0 V and PWR DWN low, V_{out} = V_{CC}	-10		10	µA
Z_{OUT}	Output impedance			100		Ω
LVDS receiver DC specifications (IN+, IN-)						
V_{TL}	Differential input low threshold	V_{CM} = 1.2 V	-100			mV
		-4 V < V_{CM} < 5 V	-130			
V_{TH} (2)	Differential input high threshold	V_{CM} = 1.2 V			100	
		-4 V < V_{CM} < 5 V			130	
V_{CMR} (3)	Common-mode voltage range	V_{ID} = 200 mVp-p	- 4		5	V
V_{CMREJ}	Common-mode rejection	F = 10 MHz			300	mVp-p
I_{ID}	Differential Input current	V_{ID} = 400 mVp-p	-10		10	µA
I_{ICM}	Common mode Input current	V_{IC} = - 4 V to 5 V	-70		70	
I_{CSIN}	Clod spare leakage current	V_{IN} = 3.6 V, V_{CC} = GND	-60		60	
C_{IN}	Input capacitance	On each LVDS input vs. GND			3	pF
Supply current						
I_{CCL}	Active supply current	C_L = 8 pF			65	mA
I_{CCPD}	Power-down supply current	$\overline{\text{PWR DWN}}$ = low, LVDS inputs = logic low, V_{CC} = 3.6 V			2	mA

1. *Output short current is specified as magnitude only. A minus sign indicates direction only. Only one output should be shorted at a time for a maximum duration of one second.*
2. *Guaranteed by design*
3. *Functionally tested*

In Table 5. Receiver switching characteristics, V_{CC} = 3 V to 3.6 V, T_A = - 55 °C to 125 °C, and unless otherwise specified, T_A is per the temperature noted. The receiver skew margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window). This margin allows for an LVDS interconnect skew, an inter-symbol interference (both dependent on type/length of cable), and a source clock jitter less than 250 ps which is calculated from T_{POS} - R_{POS} (see Figure 12. RHFLVDS218 receiver skew margin).

Table 5. Receiver switching characteristics

Symbol	Parameter	Min.	Max.	Unit
CLHT (1)	CMOS/TTL low-to-high transition time (Figure 6. RHFLVDS218 output load and transition times)		3.5	ns
CHLT (1)	CMOS/TTL high-to-low transition time (Figure 6. RHFLVDS218 output load and transition times)		3.5	
RSPos0 (1)	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 50 MHz	1.17	2.15	
	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	0.87	1.65	
RSPos1 (1)	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 50 MHz	4.03	5.01	
	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	2.77	3.55	
RSPos2 (1)	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 50 MHz	6.88	7.86	
	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	4.68	5.46	
RSPos3 (1)	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 50 MHz	9.74	10.72	
	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	6.58	7.36	
RSPos4 (1)	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 50 MHz	12.60	13.58	
	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	8.49	9.27	
RSPos5 (1)	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 50 MHz	15.46	16.44	
	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	10.39	11.17	
RSPos6 (1)	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 50 MHz	18.31	19.29	
	Receiver input strobe position for bit 0 (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	12.30	13.08	
RCOP (1)	RxCLK OUT period (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	13.3	66.7	
RCOH (1)	RxCLK OUT high time (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	3.6		
RCOL (1)	RxCLK OUT low time (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	3.6		
RSRC (1)	RxOUT setup to RxCLK OUT (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	3.5		
RHRC (1)	RxOUT hold to RxCLK OUT (Figure 11. RHFLVDS218 receiver input strobe position), f = 75 MHz	3.5		
RCCD (2)	RxCLK IN to RxCLK OUT delay (Figure 8. RHFLVDS218 clock-to-clock out delay), f = 75 MHz		8.3	
RPLLS (3)	Receiver phase lock loop set (Figure 9. RHFLVDS218 phase-lock-loop set time), f = 75 MHz		10	ms
RPDD	Receiver power-down delay (Figure 10. RHFLVDS218 receiver power-down delay)		2	µs

1. *Guaranteed by characterization.*
2. *Total latency for the channel link chip-set is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for LVDS217 serializer and the LVDS218 deserializer is (T + TCCD) + 2*T + RCCD), where T = clock period.*
3. *Functionally tested.*

Note: In Table 5. Receiver switching characteristics, receiver skew margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min. and max.) and the receiver input setup and hold time (internal data sampling window). This margin also allows LVDS interconnect skew, inter-symbol interface (both dependent on type/length of cable), and source clock jitter less than 250 ps (calculated from T_{POS} to R_{POS}).

Note: In power-down, all CMOS/TTL and clock outputs are in high impedance.

Cold sparing

The RHFLVDS218 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (VCC = GND) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and VCC. ESD protection is ensured through a non-conventional dedicated structure.

Fail-safe

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of an LVDS input short-circuit or floating inputs, the TTL outputs remain in a stable logic-high state.

6 Radiations

Total dose (MIL-STD-883 TM 1019)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFLVDS218 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in Table 4. DC electrical characteristics apply to both pre- and post-irradiation, as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy-ions

The behavior of the product when submitted to heavy-ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 6. Radiation

Type	Characteristics	Value	Unit
TID(1)	High-dose rate (50 - 300 rad/sec) up to:	300	krad
Heavy-ions	SEL (2) immune up to: (with a particle angle of 60 ° at 125 °C and a fluence of 1e+7 cm^{-2})	120	MeV.cm²/mg
	SEL (2) immune up to: (with a particle angle of 0 ° at 125 °C and a fluence of 1e+7 cm^{-2})	60	

1. *A total ionizing dose (TID) of 300 krad(Si) is equivalent to 3000 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latch-up.*

7 Test circuit and AC timing diagrams

Figure 5. **Test pattern**

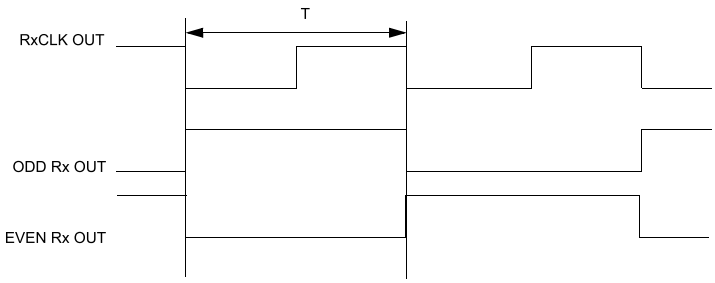


Figure 6. **RHFLVDS218 output load and transition times**

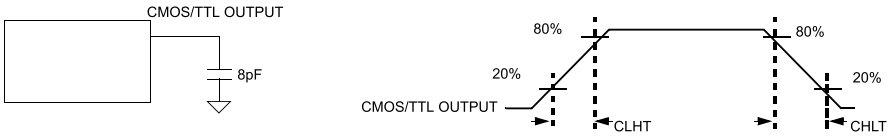


Figure 7. **RHFLVDS218 setup/hold and high/low times**

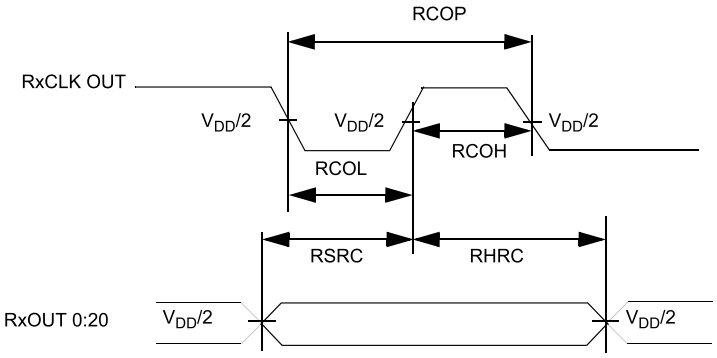


Figure 8. **RHFLVDS218 clock-to-clock out delay**

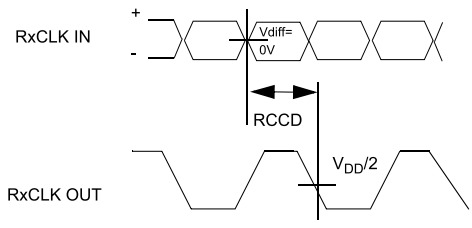


Figure 9. **RHFLVDS218 phase-lock-loop set time**

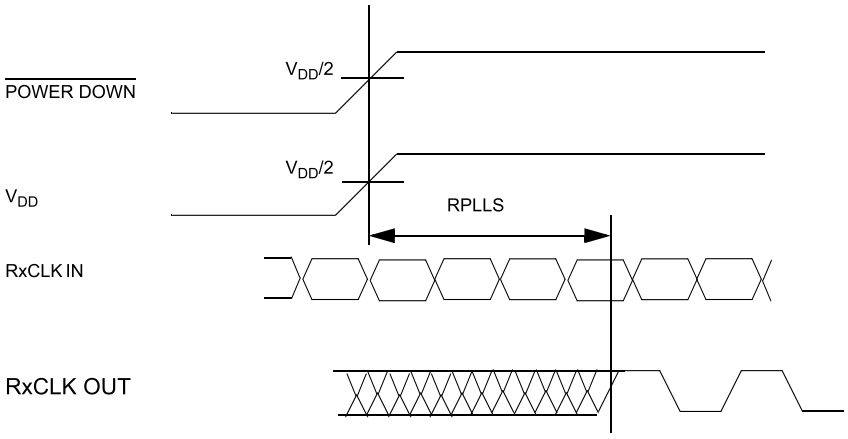


Figure 10. **RHFLVDS218 receiver power-down delay**

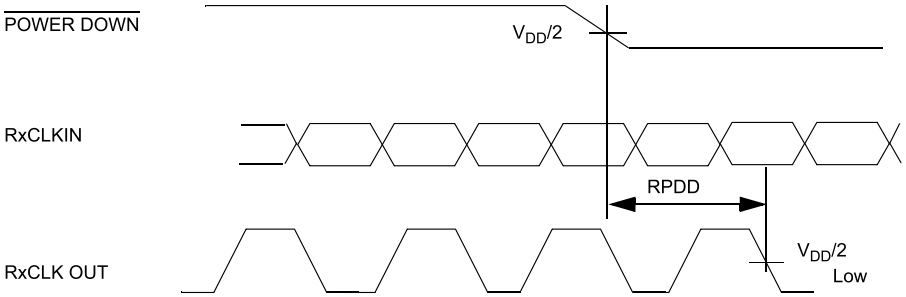


Figure 11. RHFLVDS218 receiver input strobe position

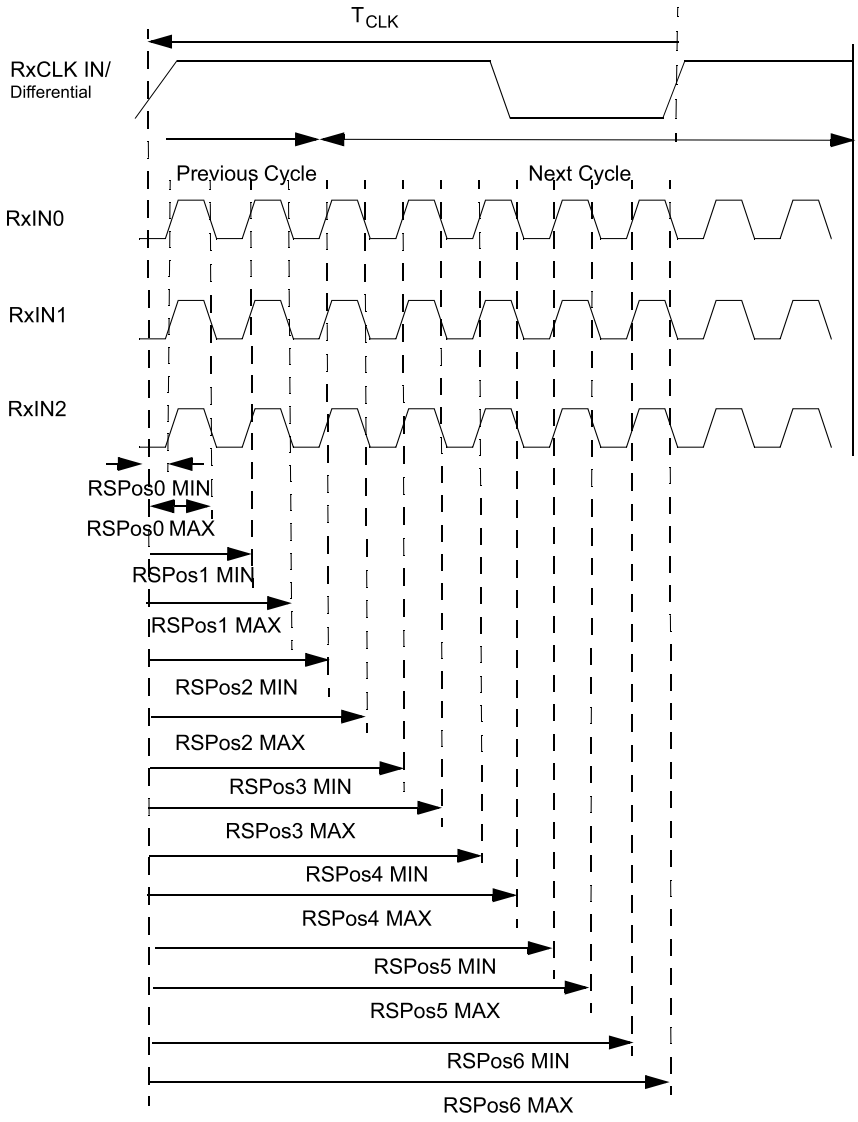
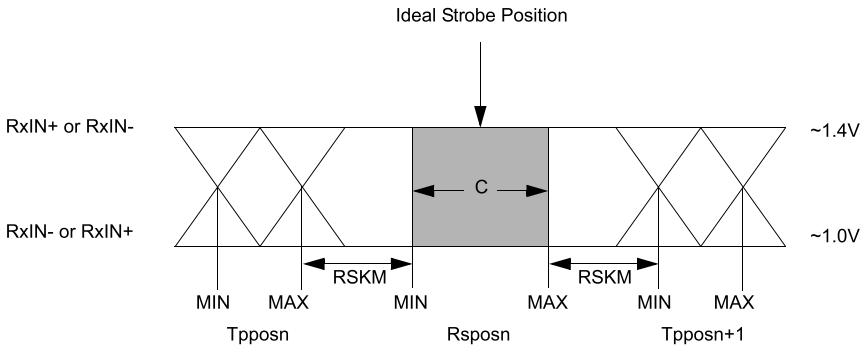


Figure 12. RHFLVDS218 receiver skew margin



$$RSKM(Side) > \frac{\text{Cable Skew}}{2} + \frac{\text{Source Clock Jitter}}{2} + \frac{\text{ISI}}{2}$$

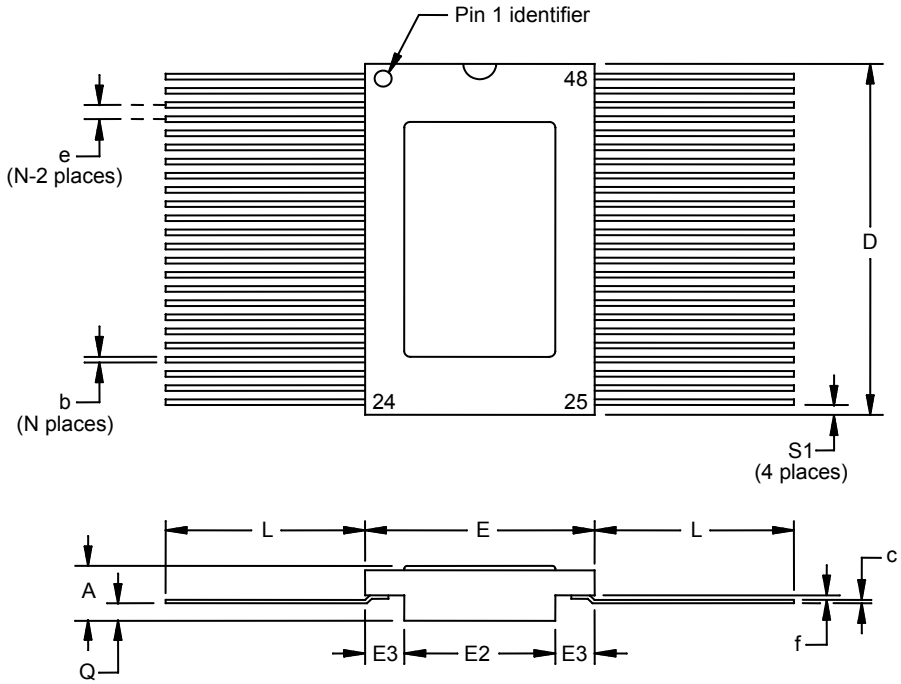
1. C: setup and hold time (internal data sampling window) defined by RSPosN (receiver input strobe position min and max TPPosN (transmitter output pulse position min. and max.).
2. Cable skew: based on type and length, typically 10 ps - 40 ps per foot, media dependent
3. Source clock jitter: cycle-to-cycle jitter is less than 250 ps at 75 MHz
4. ISI: inter-symbol interference, dependent on interconnect length, may be zero

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 Ceramic Flat-48 package information

Figure 13. Ceramic Flat-48 package outline



1. The upper metallic lid is connected to pin 17.

Table 7. Ceramic Flat-48 mechanical data

Dim.	mm			Inches		
	Typ	Min.	Max.	Typ.	Min.	Max.
A	2.47	2.18	2.72	0.097	0.086	0.107
b	0.254	0.20	0.30	0.010	0.008	0.012
c	0.15	0.12	0.18	0.006	0.005	0.007
D	15.75	15.57	15.92	0.620	0.613	0.627
E	9.65	9.52	9.78	0.380	0.375	0.385
E2	6.35	6.22	6.48	0.250	0.245	0.255
E3	1.65	1.52	1.78	0.065	0.060	0.070
e	0.635			0.025		
f	0.20			0.008		
L	8.38	6.85	9.40	0.330	0.270	0.370
Q	0.79	0.66	0.92	0.031	0.026	0.036
S1	0.43	0.25	0.61	0.017	0.010	0.024

9 Ordering information

Table 8. Order code

Order code	SMD[1]	Quality level	Temp. range	Mass	Package	Lead finish	Marking[2]	Packing
RHFLVDS218K1	-	Engineering model	-55 to +125 °C	1.22 g	Flat-48	Gold	RHFLVDS218K1	Conductive strip pack
RHFLVDS218K01V	5962F01535	QML-V flight					5962F0153503VYC	

1. *Standard microcircuit drawing.*
2. *Specific marking only. Complete marking includes the following:*
   - *ST logo*
   - *Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)*
   - *Country of origin (FR = France)*

Note: Contact your ST sales office for information about the specific conditions for products in die form.

Other information

Date code:

The date code is structured as engineering model: EM xyywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 9. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including : Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to TN1181 on engineering models ST Rennes assembly lot ID

Quality level	Item
QML-V Flight	Certificate of Conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
08-Apr-2016	1	Initial release
25-Oct-2016	2	Status of datasheet changed from "preliminary data" to "production data". Added order code RHFLVDS218K01V to Table 1: "Device summary" Table 3: "Absolute maximum ratings (references to GND)": updated Rthjc value from 22 °C/W to 10 °C/W and updated footnote 2. Table 5: "DC electrical characteristics": updated VOL, VOH, IOS, IOFF, VTL, and VTH values; added footnote 1, 2 and 3. Table 6: "Receiver switching characteristics": removed footnote 2 (guaranteed by design), variables previously related to this footnote are now related to footnote 1 (guaranteed by characterization). Parameters related to Figure 6 are now related to Figure 10. Added note below Table 6: "Receiver switching characteristics" regarding "receiver skew margin". Added order code RHFLVDS218K01V to Table 9: "Order codes"
03-Jul-2018	3	Updated Section 5 Electrical characteristics, Section 6 Radiations and Section 9 Ordering information.

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