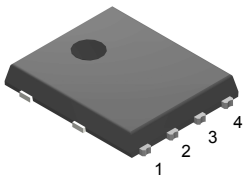
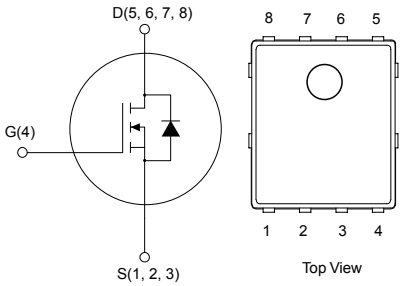
STL64N4F7AG

Datasheet

Automotive-grade 40 V, 7.0 mΩ typ., 64 A, STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package



PowerFLAT™ 5x6



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL64N4F7AG	40 V	8.5 mΩ	64 A

- AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status link
STL64N4F7AG

Product summary	
Order code	STL64N4F7AG
Marking	64N4F7
Package	PowerFLAT™ 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	64	A
	Drain current (continuous) at T_C = 100 °C	40.3	A
I_{DM}(1)	Drain current (pulsed)	256	A
P_{TOT}	Total dissipation at T_C = 25 °C	65	W
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	32	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.3	°C/W

1. *When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D= 1 mA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS}= 40 V			1	µA
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 32 A		7.0	8.5	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS}= 0 V	-	637	-	pF
C_{oss}	Output capacitance		-	240	-	pF
C_{rss}	Reverse transfer capacitance		-	26	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 64 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	9.8	-	nC
Q_{gs}	Gate-source charge		-	3.8	-	nC
Q_{gd}	Gate-drain charge		-	3.1	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 32 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	18.8	-	ns
t_r	Rise time		-	102.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	21.4	-	ns
t_f	Fall time		-	13.3	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 64 A, V_{GS} = 0 V	-		1.3	V
t_{rr}	Reverse recovery time	I_D = 64 A, di/dt = 100 A/µs	-	27.5		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 32 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	17.3		nC
I_{RRM}	Reverse recovery current		-	1.4		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

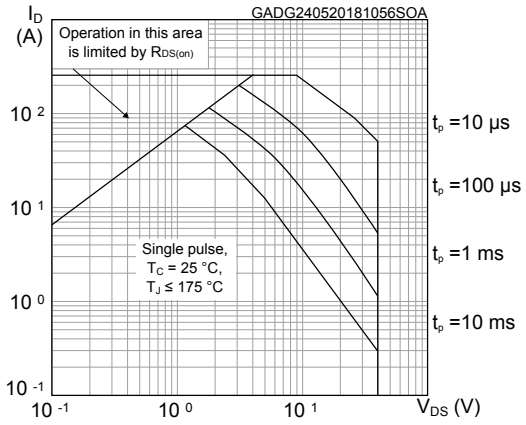


Figure 2. Thermal impedance

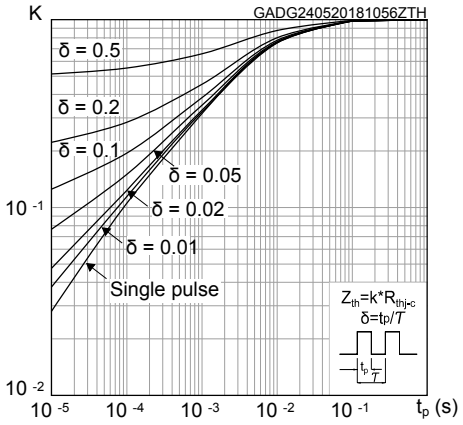


Figure 3. Output characteristics

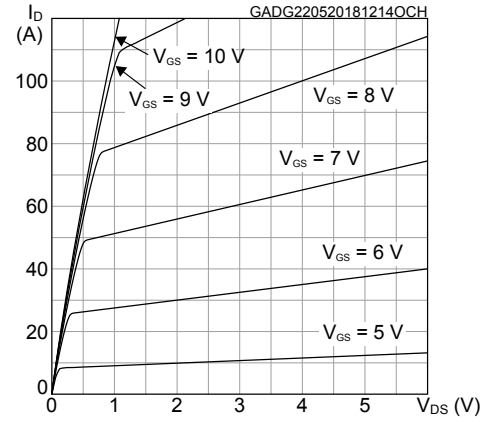


Figure 4. Transfer characteristics

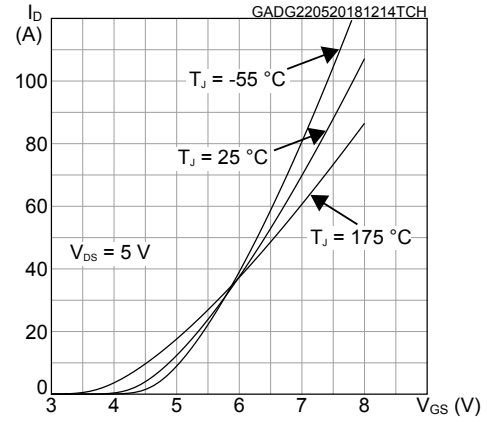


Figure 5. Gate charge vs gate-source voltage

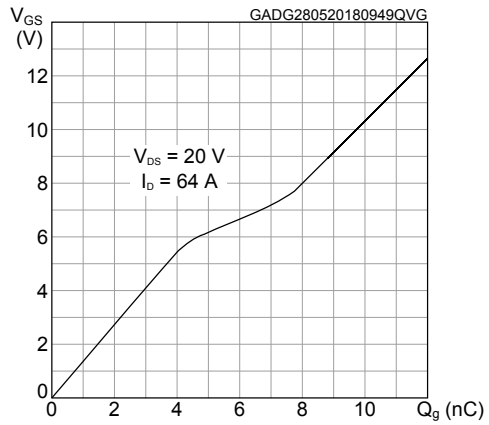


Figure 6. Static drain-source on-resistance

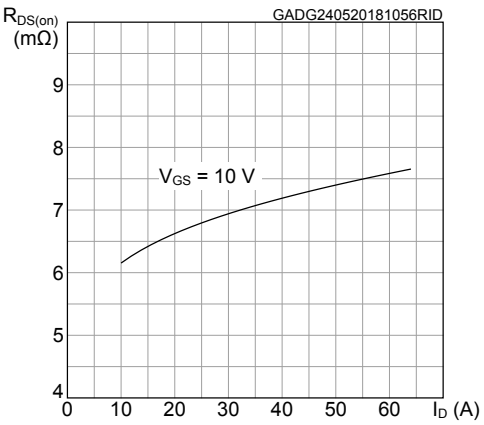


Figure 7. Capacitance variations

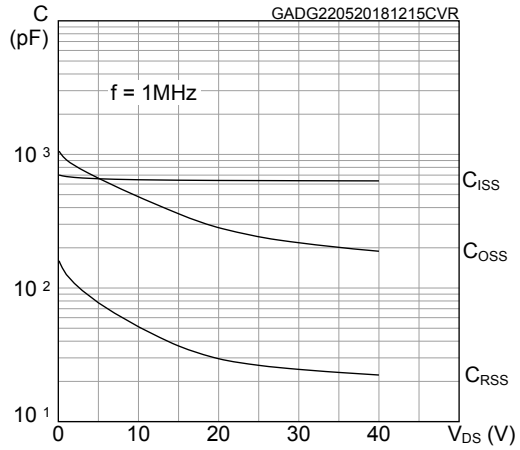


Figure 8. Normalized on-resistance vs temperature

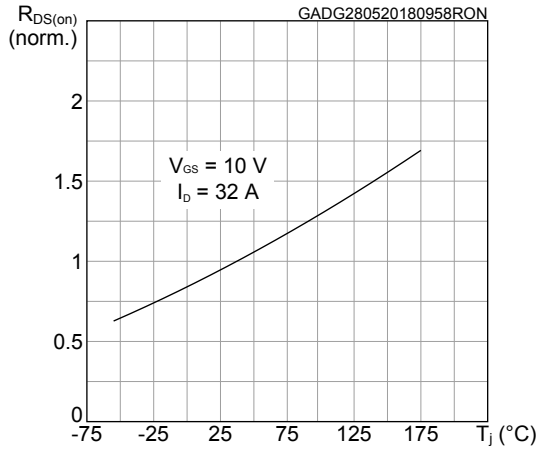


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

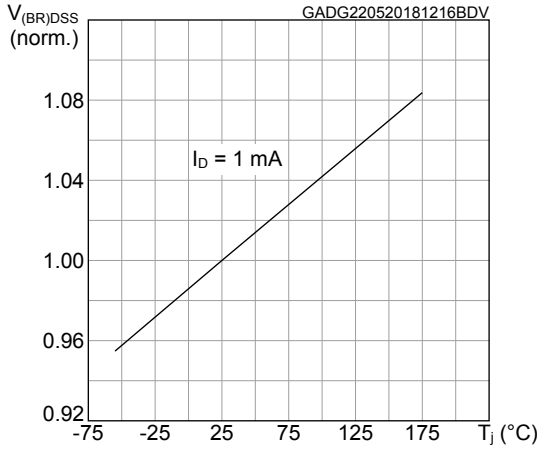


Figure 10. Normalized gate-threshold voltage vs temperature

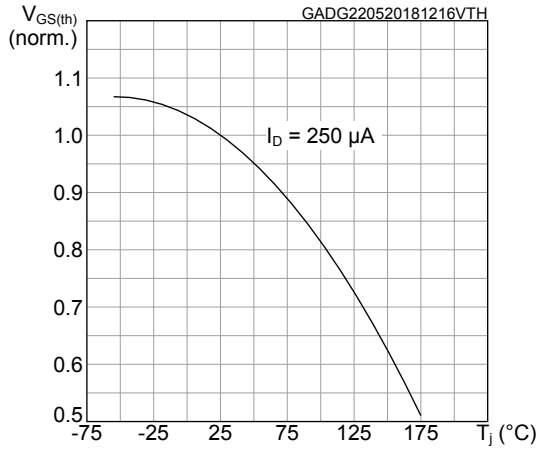
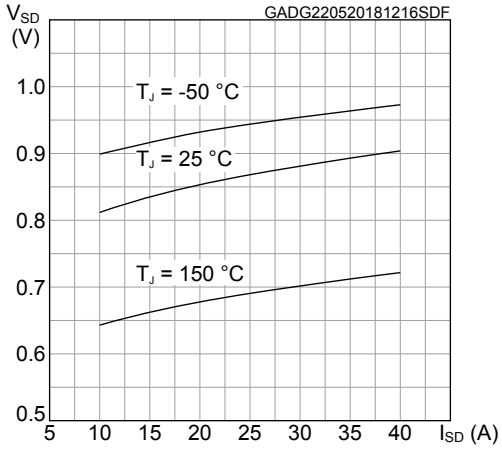


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

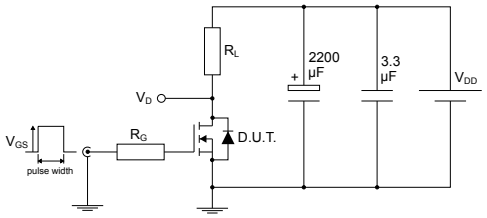


Figure 13. Test circuit for gate charge behavior

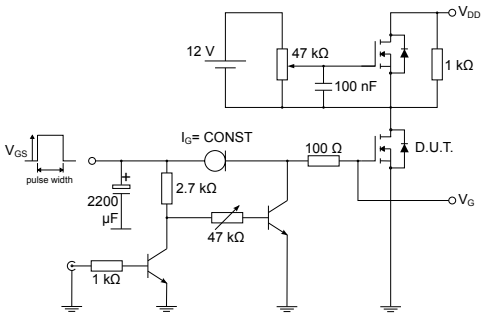


Figure 14. Test circuit for inductive load switching and diode recovery times

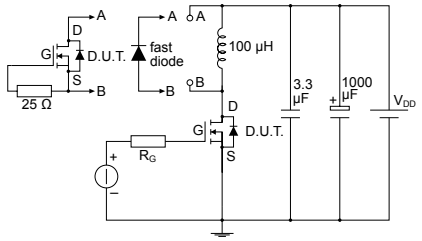


Figure 15. Unclamped inductive load test circuit

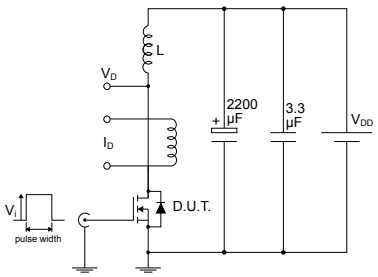


Figure 16. Unclamped inductive waveform

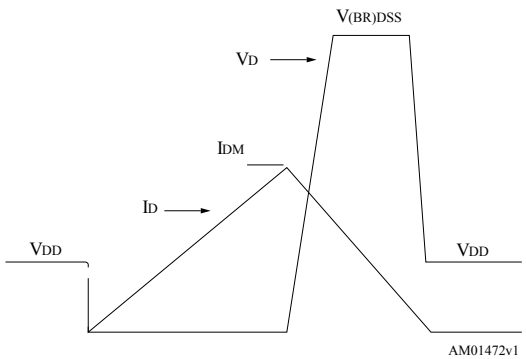
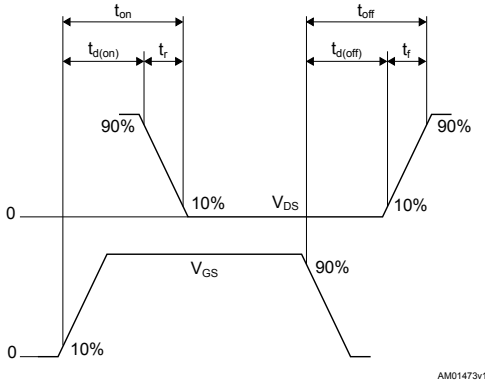


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type C package information

Figure 18. **PowerFLAT™ 5x6 WF type C package outline**

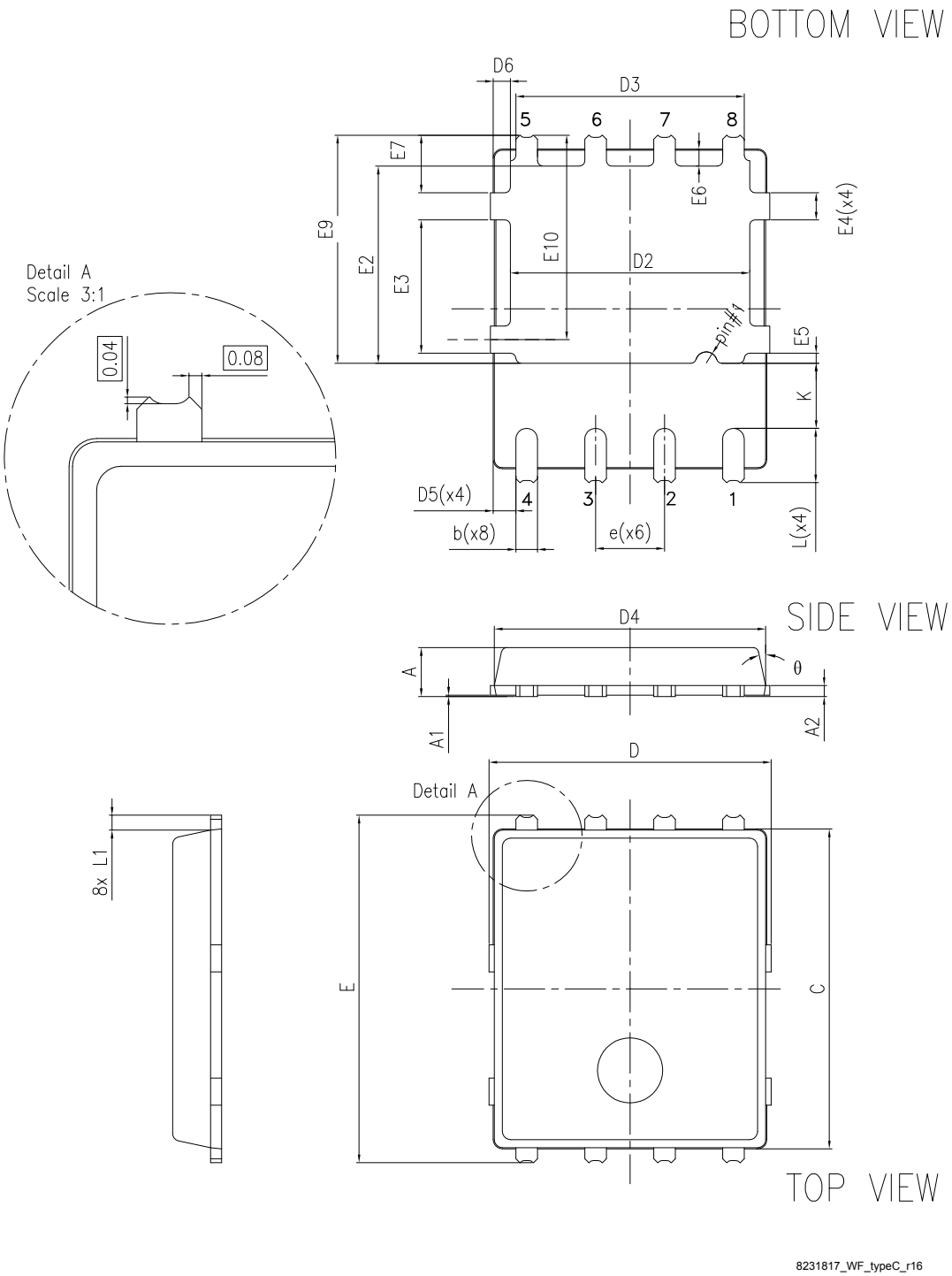
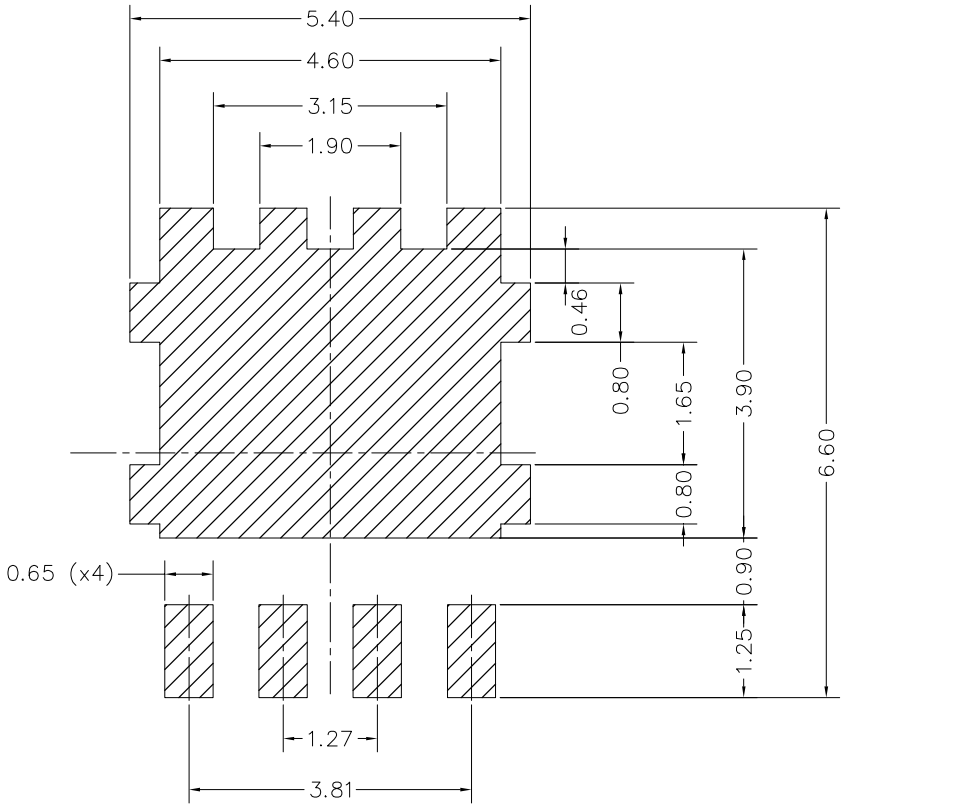


Table 7. **PowerFLAT™ 5x6 WF type C mechanical data**

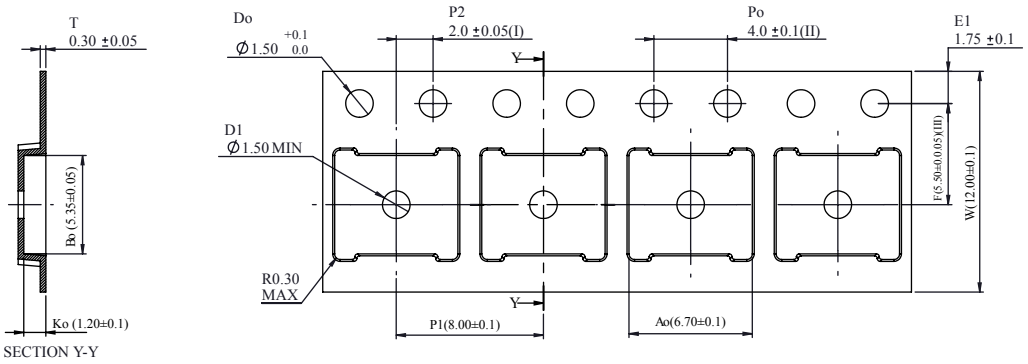
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 19. **PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)**



4.2 PowerFLAT™ 5x6 WF packing information

Figure 20. PowerFLAT™ 5x6 WF tape (dimensions are in mm)



(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs

8234350_TapeWF_rev_C

Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape

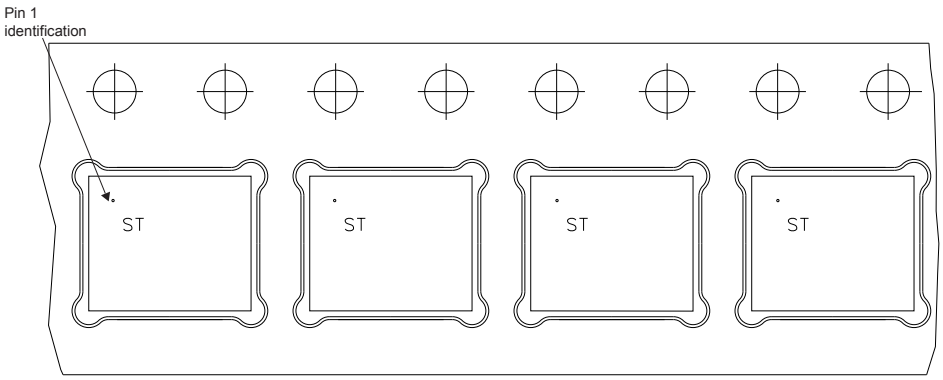
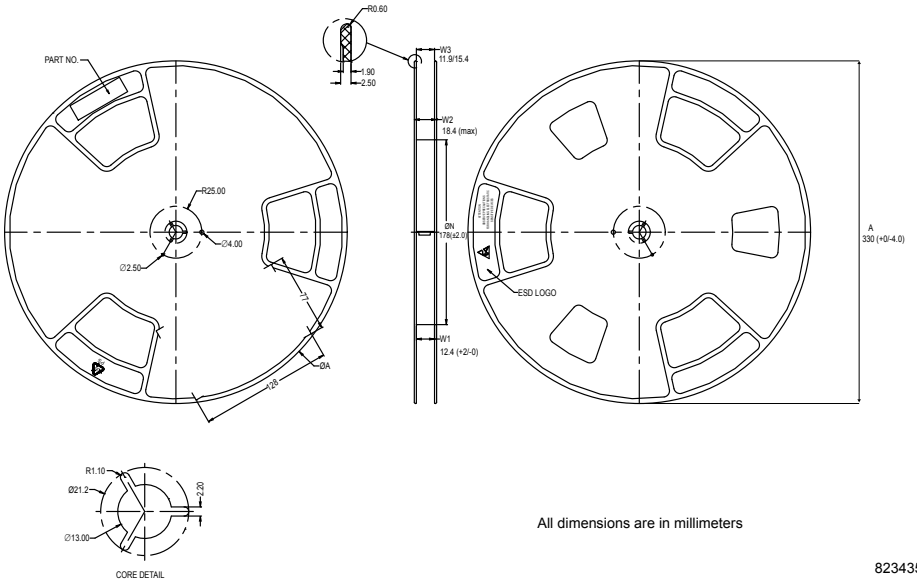


Figure 22. PowerFLAT™ 5x6 reel (dimensions are in mm)



All dimensions are in millimeters

8234350_Reel_rev_C

Revision history

Table 8. **Document revision history**

Date	Version	Changes
30-May-2018	1	Initial release
27-Jun-2018	2	Updated title and features in cover page.

Contents