

Automotive IPD 1ch Low Side Switch

BV1LB025EFJ-C

Features

- Built-in Dual TSD^{*1}
- AEC-Q100 Qualified^{*2}
- Built-in Over Current Protection Function(OCP)
- Built-in Active Clamp Function
- Direct Control Enabled from CMOS Logic IC, etc.
- On Resistance R_{DS(ON)} = 25 mΩ (Typ) (when V_{IN} = 5 V, I_{OUT} = 2.4 A, Tj = 25 °C)
- Monolithic Power Management IC with the Control Block (CMOS) and Power MOS FET Mounted on a Single Chip
- *1 This IC has thermal shutdown (Junction temperature detect) and Δ Tj Protection (Power-MOS steep temperature rising detect).
- *2 Grade1

General Description

The BV1LB025EFJ-C is an automotive 1ch low side switch IC, which has built-in Dual TSD, OCP and active clamp function.

Application

Driving Resistive, Inductive and Capacitive Load

Block Diagram

Key Specifications

On-state Resistance (Tj = 25 °C, Typ)	25 mΩ
Over Current Limitation Level (Tj = 25 °C, Typ)	50 A
Output Clamp Voltage (Min)	42 V
Active Clamp Energy $(Tj_{(START)} = 25 °C)$	220 mJ

Package

HTSOP-J8

W (Typ) x D (Typ) x H (Max) 4.9 mm x 6.0 mm x 1.0 mm



OUT



 \odot Product structure : Silicon integrated circuit \odot This product has no designed protection against radioactive rays.

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Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	IN	Input pin, with internal pull-down resistor.
2	N.C.	No connected to internal circuit. Open or connected to GND or connected IN.
3	N.C.	No connected to internal circuit. Open or connected to GND or connected IN.
4	N.C.	No connected to internal circuit. Open or connected to GND or connected IN.
5	GND	GND pin
6	GND	GND pin
7	GND	GND pin
8	GND	GND pin
EXP-PAD	OUT	Output pin. When output pin shorted to battery, output current is limited to protect IC.

Definition



Absolute Maximum Ratings (Tj = 25°C)

Parameter	Symbol	Ratings	Unit
Output Voltage	V _{OUT}	-0.3 to +42	V
Input Voltage	V _{IN}	-0.3 to +7	V
Output Current	I _{OUT}	35 (inside limited) ^{*1}	А
Active Clamp Energy (Single Pulse) Tj _(START) = 25 °C, $I_{OUT(START)}$ = 4 A	E _{AS(25 °C)}	220	
Active Clamp Energy (Single Pulse) Tj _(START) = 150 °C, $I_{OUT(START)}$ = 4 A ^{*2}	E _{AS(150 °C)}	140	mJ
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

*1 Internally limited by over current protection function.

*2 Not 100 % tested.

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Caution 3: When IC turns off with an inductive load, reverse energy has to be dissipated in the BV1LB025EFJ-C. This energy can be calculated by the following equation:

$$E_L = \frac{1}{2} L I_{OUT(START)}^2 \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CL)}} \right)$$

Where:

L is the inductance of the inductive load. $I_{OUT(START)}$ is the output current at the time of turning off. $V_{OUT(CL)}$ is the output clamp voltage.

The IC integrates the active clamp function to internally absorb the reverse energy E_L which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy E_L is active clamp tolerance E_{AS} (refer to Figure 1.) or under when inductive load is used.



Figure 1. Active Clamp Energy (Single Pulse) vs Output Current (Start)

Recommended Operating Conditions

Parameter	Symbol	Min	Тур	Max	Unit
Input Voltage	V_{IN}	3.5	5.0	5.5	V
Operating Temperature	Tj	-40	+25	+150	°C

Thermal Resistance^{*1}

Parameter	Symbol	Тур	Unit	Condition	
HTSOP-J8					
		121.7	°C/W	1s	*2
Between Junction and Surroundings Temperature Thermal Resistance	θ _{JA}	34.0	°C/W	2s	*3
		23.3	°C/W	2s2p	*4

*1 The thermal impedance is based on JESD51-2A (Still-Air) standard. It is used the chip of BV1LB025EFJ-C.

(Top copper foil: ROHM recommended Footprint + wiring to measure, 2 oz. copper.)

- Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm,
 - copper (top & reverse side) 2 oz.)

*4 JESD51-5, 7 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 4-layers (2s2p) (Top copper foil: ROHM recommended Footprint + wiring to measure/ 2 inner layers and copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm, copper (top & reverse side/inner layers) 2 oz./1 oz.)

■ PCB Layout 1 layer (1s)



Dimension	Value
Board Finish Thickness	1.57 mm ± 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top Layer)	0.070 mm (Cu:2 oz)
Copper Foil Area Dimension	Footprint / 100 mm ² / 600 mm ² / 1200 mm ²

^{*2} JESD51-3 standard FR4 114.3 mm x 76.2 mm x 1.57 mm 1-layer (1s)

^{*3} JESD51-5 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 2-layers (2s) (Top copper foil: ROHM recommended Footprint + wiring to measure/

Thermal Resistance – continued

■ PCB Layout 2 layers (2s)



Cross Section

Dimension	Value
Board Finish Thickness	1.60 mm ± 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top/Bottom Layers)	0.070 mm (Cu + Plating)
Thermal Vias Separation/Diameter	1.2 mm / 0.3 mm

Thermal Resistance – continued

■ PCB Layout 4 layers (2s2p)



Dimension	Value
Board Finish Thickness	1.60 mm \pm 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top/Bottom Layers)	0.070 mm (Cu + Plating)
Thermal Vias Separation/Diameter	1.2 mm / 0.3 mm

Thermal Resistance – continued

■ Transient Thermal Resistance (Single Pulse)



■ Thermal Resistance (θ_{JA} vs Copper foil area (1s))



Electrical Characteristics (Unless otherwise specified, $-40 \text{ }^{\circ}\text{C} \le \text{Tj} \le +150 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Limit		Unit	Conditions		
Farameter	Symbol	Min	Тур	Max	Unit	Conditions	
Input (IN)							
Input Threshold Voltage	V _{IN(TH)}	1.1	-	3.5	V	$R_L = 4.7 \ \Omega$, $V_{BAT} = 12 \ V$	
High Level Input Current 1 (in Normal Operation)	$I_{IN(H1)}$	-	85	170	μA	$V_{IN} = 5 V$	
High Level Input Current 2 (in Abnormal Operation) ^{*1}	$I_{\text{IN}(\text{H2})}$	-	-	1000	μA	$V_{IN} = 5 V$	
Low Level Input Current	$I_{\text{IN}(L)}$	-10	0	+10	μA	$V_{IN} = 0 V$	
Power MOS Output							
On-state Resistance	R _{DS(ON)}	-	25.0	32.5	mΩ	$V_{IN} = 5 \text{ V, } I_{OUT} = 2.4 \text{ A,}$ $Tj = 25 \text{ °C}$	
	R _{DS(ON)}	-	44.0	62.5	mΩ	$V_{IN} = 5 \text{ V}, I_{OUT} = 2.4 \text{ A},$ Tj = 150 °C	
Leak Current	$I_{\text{OUT}(L)}$	-	0.0	0.5	μA	$ V_{IN} = 0 \ V, \ V_{OUT} = 18 \ V, $	
	$I_{OUT(L)}$	-	2.5	50.0	μA	$\label{eq:VIN} \begin{array}{l} V_{IN} = 0 \ V, \ V_{OUT} = 18 \ V, \\ Tj = 150 \ ^{\circ}C \end{array}$	
Output Clamp Voltage	V _{OUT(CL)}	42	48	54	V	$V_{\rm IN}$ = 0 V, $I_{\rm OUT}$ = 1 mA	
Turn-ON Time	t _{on}	-	50	100	μs		
Turn-OFF Time	t _{OFF}	-	60	120	μs	$\label{eq:VIN} \begin{array}{l} V_{IN} = 5 \; V \; \text{to} \; 0 \; V \text{,} \; R_{L} = 4.7 \; \Omega \text{,} \\ V_{BAT} = 12 \; V \text{,} \; Tj = 25 \; ^{\circ}C \end{array}$	
Slew Rate On	SR _{ON}	-	0.3	0.6	V/µs		
Slew Rate Off	SROFF	-	0.3	0.6	V/µs		
Protection Function							
Over Current Limitation Level	$I_{\text{OUT(LIM)}}$	35	50	65	А	V _{IN} = 5 V, Tj = 25 °C	
Thermal Shutdown Detected Temperature ^{*2}	T_{TSDD}	150	180	-	°C	$V_{IN} = 5 V$	
Thermal Shutdown Released Temperature ^{*2}	T_{TSDR}	135	160	-	°C	$V_{IN} = 5 V$	
Thermal Shutdown Hysteresis Temperature ^{*2}	T _{TSDHYS}	-	20	-	°C	$V_{IN} = 5 V$	
ΔTj Protection Detected Temperature ^{*2}	T _{DTJD}	-	75	-	°C	$V_{IN} = 5 V$	
ΔTj Protection Released Temperature ^{*2}	T _{DTJR}	-	45	-	°C	$V_{IN} = 5 V$	
ΔTj Protection Hysteresis Temperature ^{*2}	T _{DTJHYS}	-	30	-	°C	$V_{IN} = 5 V$	

*1 When thermal shutdown function or over current protection function is ON.

*2 Not 100 % tested.

Typical Performance Curves (Unless otherwise specified, Tj = 25 °C, $V_{IN} = 5 \text{ V}$)





Typical Performance Curves – continued (Unless otherwise specified, $Tj = 25 \text{ °C}, V_{IN} = 5 \text{ V}$)







Typical Performance Curves – continued (Unless otherwise specified, Tj = 25 °C, V_{IN} = 5 V)







Typical Performance Curves – continued (Unless otherwise specified, Tj = 25 °C, V_{IN} = 5 V)



Figure 15. Slew Rate On vs Junction Temperature

Figure 16. Slew Rate Off vs Junction Temperature

Typical Performance Curves – continued (Unless otherwise specified, Tj = 25 °C, V_{IN} = 5 V)



Measurement Circuit for Typical Performance Curves





Measurement Circuit for Figure 5 and Figure 6









Measurement Circuit for Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15 and Figure 16

Measurement Circuit for Typical Performance Curves – continued



I/O Pin Truth Table

Priority	IN Pin Voltage	Operating Status	OUT Pin
1	Low	Standby	OFF
2	High	Dual TSD Detection	OFF
3	High	Over Current Limitation	Current Limitation
4	High	Normal	ON

Timing Chart



Figure 18. Definition of Turn-ON Time, Turn-OFF Time, and Slew Rate





Function Description

Over Current Protection Function and Dual TSD Function
This IC has OCP function and Dual TSD function. Following shows the behavior when the OUT pin short circuit.



Figure 20. The Behavior when the OUT Pin Short Circuit

- ① I_{OUT} is limited at Over Current Limitation Level ($I_{OUT(LIM)}$) = 50 A (Typ) when over current is occurred.
- ② The temperature of Power MOS FET part and the control part in this IC is each $T_{POWER-MOS}$, T_{AMB} . When the temperature difference becomes 75 °C (Typ) or more, the output turns OFF. This temperature defines as ΔTj Protection Detected Temperature (T_{DTJD}).
- 3 When the temperature difference of $T_{POWER-MOS}$ and T_{AMB} becomes 45 °C (Typ) or less, the output turns automatically ON. This temperature defines as ΔTj Protection Released Temperature (T_{DTJR}).
- ④ The output is turned off when the temperature of the IC reaches Thermal Shutdown Detected Temperature $(T_{TSDD}) = 180 \text{ °C} (Typ)$ or more.
- (5) The output returns to its normal state when the temperature of the IC becomes Thermal Shutdown Released Temperature $(T_{TSDR}) = 160 \text{ °C} (Typ)$ or less.

Operational Notes

1. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

2. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

3. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

4. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

5. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

6. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

7. Thermal Shutdown Function (TSD)

This IC has a built-in thermal shutdown function that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD function that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD function operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD function be used in a set design or for any purpose other than protecting the IC from heat damage.

8. Over Current Protection Function (OCP)

This IC incorporates an integrated overcurrent protection function that is activated when the load is shorted. This protection function is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection function.

9. Active Clamp Operation

The IC integrates the active clamp function to internally absorb the reverse energy E_L which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy E_L is active clamp tolerance E_{AS} (refer to Figure 1.) or under when inductive load is used.

Operational Notes – continued

10. Negative Current of Output

When the OUT pin (DRAIN) becomes lower than the GND pin (SOURCE), a current flow from the in pin (the IN pin) to the OUT pin (DRAIN) through a parasitic transistor. As shown in Figure 21 when the input pin is High, a current flow from a power supply of the connection (MCU, and so on) of the input pin to the OUT pin (DRAIN). As shown in Figure 22 when the input pin is Low, a current flow from the GND of parts (MCU, and so on) that connected to the input pin to the OUT pin (DRAIN).

Therefore, set the OUT pin (DRAIN) is -0.3 V or higher. When the OUT pin becomes lower than -0.3V, add a restriction resistance 330 Ω or higher to the IN pin. However, set the value of restriction resistance in consideration of the voltage descent caused by power supply pin and input pins currents.







Figure 22. Negative Current Path (when the input pins are Low)

Ordering Information



Marking Diagram



Datasheet



Revision History

Revision mis	luiy	
Date	Revision	Changes
20.Nov.2020	001	New Release

Notice

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JAPAN	USA	EU	CHINA
CLASSI	CLASSⅢ	CLASS II b	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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