TPS63900 1.8V 至 5.5V、400mA、200nA 静态电流降压/升压转换器

1 特性

- 输入电压范围：1.8V 至 5.5V
- 输出电压范围：1.8V 至 5V（100mV 阶跃）
  - 可使用外部电阻器进行编程
  - SEL 引脚用于在两个输出电压预设之间切换
- V_I ≥ 1.8V、V_O = 3.3V 时，输出电流 > 400mA（峰值开关电流限制典型值 1.9A）
- 负载电流为 10µA 时，效率 > 90%
  - 200nA 工作静态电流
  - 60nA 关断电流
- 单模式运行
  - 无需在降压、降压/升压和升压模式之间转换
  - 低输出波纹
  - 出色的瞬态性能
- 安全、可靠运行 特性
  - 集成软启动
  - 可编程输入电流限制，具有八个设置（1mA 至 100mA 和无限制）
  - 输出短路和过热保护
- 微型解决方案尺寸
  - 小型 2.2µH 电感器，单个 22µF 输出电容器
  - 10 引脚、2.5mm × 2.5mm、0.5mm 间距 WSON 封装

2 应用

- 智能仪表和传感器节点
- 电子智能锁
- 医疗传感器贴片和患者监护仪
- 可穿戴电子产品
- 资产跟踪
- 工业物联网（智能传感器）/窄带物联网

3 说明

TPS63900 器件是一款具有超低静态电流（典型值为 200nA）的高效同步降压/升压转换器。该器件具有 32 个用户可编程的输出电压设置，范围为 1.8V 至 5V。

通过动态电压调节功能，可在 应用 运行期间更改输出电压；例如，在待机运行期间可通过降低系统电源电压来降低功耗。

凭借其宽电源电压范围和可编程的输入电流限制（1mA 至 10mA 和无限制），该器件非常适合与 3 节碱性电池、1 节锂二氧化锰 (Li-MnO_2) 或 1 节锂亚硫酰氯 (Li-$SOCl_2$) 等各种一次电池以及二次电池搭配使用。

高输出电流功能支持低于 1GHz、BLE、LoRa、wM-Bus 和 NB-IoT 等常用射频标准。

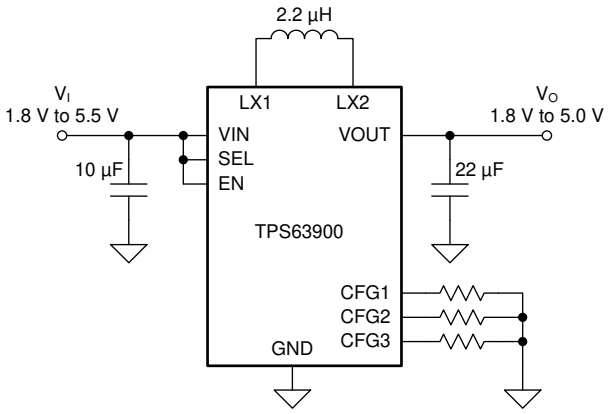
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS63900	WSON (10)	2.5mm × 2.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

ADVANCE INFORMATION

简化原理图



目录

ADVANCE INFORMATION

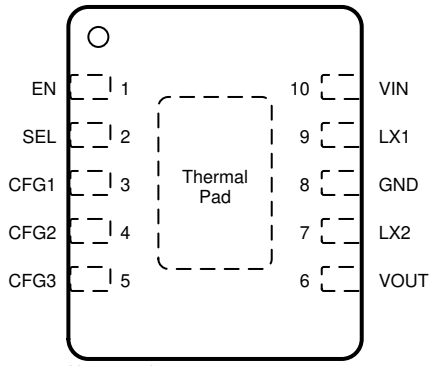
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (March 2020) to Revision A	Page
• 首次公开发布	1

5 Pin Configuration and Functions

DSK Package
10-Pin WSON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	EN	I	Device enable. A high level applied to this pin enables the device and a low level disables it. It must not be left open.
2	SEL	I	Output voltage select. Selects $V_{O(2)}$ when a high level is applied to this pin. Selects $V_{O(1)}$ when a low level is applied to this pin. It must not be left open.
3	CFG1	I	Configuration pin 1. Connect a resistor between this pin and ground to set $V_{O(2)}$ and input current limit, must not be left open.
4	CFG2	I	Configuration pin 2. Connect a resistor between this pin and ground to set $V_{O(2)}$ and input current limit. Must not be left open.
5	CFG3	I	Configuration pin 3. Connect a resistor between this pin and ground to set $V_{O(1)}$. Must not be left open.
6	VOUT	—	Output voltage
7	LX2	—	Switching node of the boost stage
8	GND	—	Ground
9	LX1	—	Switching node of the buck stage
10	VIN	—	Supply voltage
—	Thermal Pad	—	Connect this pin to ground for correct operation.

ADVANCE INFORMATION

6 Specifications

CAUTION

The pre-production samples with XPS63900DSKT orderable part number (top marking: X639) have a silicon issue which causes leakage of around 300 µA in normal operation. This leads to a reduced efficiency at light loads. Quiescent current into V_{IN} measurements on the pre-production silicon parts show 200 nA typical, if V_O is forced to 5 V.

The root cause of this leakage is understood and will be fixed for production units.

All other functions of the converter can be evaluated.

Production unit samples will be available in 3Q20.

For detailed information, contact bcs_request_fs@list.ti.com.

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage (VIN, LX1, LX2, VOUT, EN, CFG1, CFG2, CFG3, SEL)(2)	–0.3	5.9	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		1.8		5.5	V
V_O	Output voltage		1.8		5.0	V
I_O	Output current (V_I ≥ 1.8 V, V_O = 3.6 V)				0.4	A
C_I	Input capacitance (V_I = 2.5 V to 5 V, V_O = 3.3 V, I_O = 0.4 A)(1)		5			µF
C_O	Output capacitance (V_I = 2.5 V to 5 V, V_O = 3.3 V, I_O = 0.4 A)(1)		10			µF
$C_{(CFG)}$	Capacitance (CFG1, CFG2, CFG3)				10	pF
L	Inductance			2.2		µH
I_{SAT}	Inductor saturation current rating	Unlimited current setting	2			A
		≤100-mA current settings	1			
T_A	Operating ambient temperature		–40		85	°C
T_J	Operating junction temperature		–40		125	°C

(1) Effective capacitance after DC bias effects have been considered.

ADVANCE INFORMATION

6.4 Thermal Information

THERMAL METRIC(1)		TPS63900 DSK Package (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.0 V, V_O = 2.5 V and T_J = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY								
	Quiescent current into VIN		$V_{(EN)}$ = 3 V, no load, not switching, "unlimited" current setting			0.2	1	µA
	Shutdown current into VIN		$V_{(EN)}$ = 0 V			60		nA
$V_{IT+(UVLO)}$	Positive-going UVLO threshold voltage				1.73	1.75	1.77	V
$V_{hys(UVLO)}$	UVLO threshold voltage hysteresis				90	100	110	mV
I/O SIGNALS								
V_{IH}	High-level input voltage (EN, SEL)						1.2	V
V_{IL}	Low-level input voltage (EN, SEL)				0.4			V
	Input current (EN, SEL)		$V_{(EN)}$, $V_{(SEL)}$ = 1.8 V or 0 V. T_J = 25°C			±1	±10	nA
POWER SWITCH								
$r_{DS(on)}$	On-state resistance	Q1	V_I = 3 V, V_O = 3.6 V, test current = 1 A			110		mΩ
		Q2				105		
		Q3				105		
		Q4				110		
CURRENT LIMIT								
	Peak current limit during Startup (Q1)		V_I = 3.6 V, unlimited current limit setting		0.48		0.83	A
	Peak current limit (Q1)		V_I = 1.8 V, V_O = 3.6 V, unlimited current limit setting		1.33	2.1	2.47	A
			V_I = 3.6 V, V_O = 3.3 V, 100-mA current limit setting		0.15	0.4	0.51	
	Average input current limit		T_J = –40°C to 85°C	1-mA setting		1		mA
				2.5-mA setting		2.5		
				5-mA setting		5		
				10-mA settting		10		
				25-mA setting		25		
				50-mA setting		50		
				100-mA setting		100		
OUTPUT								
	Output voltage DC accuracy		I_O = 1 mA, $C_{O(eff)}$ = 4 µF, $L_{(eff)}$ = 2.2 µH				±1.8	%
CONTROL								
	Internal reference resistor					33		kΩ

ADVANCE INFORMATION

Electrical Characteristics (continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.0 V, V_O = 2.5 V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{CFG}	R2D setting #0			0	0.1	kΩ
	R2D setting #1		–3%	0.511	+3%	
	R2D setting #2		–3%	1.15	+3%	
	R2D setting #3		–3%	1.87	+3%	
	R2D setting #4		–3%	2.74	+3%	
	R2D setting #5		–3%	3.83	+3%	
	R2D setting #6		–3%	5.11	+3%	
	R2D setting #7		–3%	6.49	+3%	
	R2D setting #8		–3%	8.25	+3%	
	R2D setting #9		–3%	10.5	+3%	
	R2D setting #10		–3%	13.3	+3%	
	R2D setting #11		–3%	16.2	+3%	
	R2D setting #12		–3%	20.5	+3%	
	R2D setting #13		–3%	24.9	+3%	
	R2D setting #14		–3%	30.1	+3%	
	R2D setting #15		–3%	36.5	+3%	
PROTECTION FEATURES						
	Thermal shutdown threshold temperature		140	150	160	°C
	Thermal shutdown hysteresis		15	20	25	°C
TIMING PARAMETERS						
$t_{d(POR)}$	POR signal delay after reaching POR threshold			3.8		ms
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of the output voltage ramp	Supply voltage stable before EN pin goes high			1.5	ms
$t_{w(SS)}$	Soft-start step duration		100	125	150	µs
$t_{d(SEL)}$	Delay between a change in the state of the SEL pin and the first step change in the output voltage			30	40	µs
$t_{w(DVS)}$	Dynamic voltage scaling step duration		100	125	150	µs
	Overcurrent protection timeout	R_L = 10 Ω	0.8	1	1.2	ms
$t_{d(RESTART)}$	Restart delay after protection			10	11	ms

6.6 Typical Characteristics

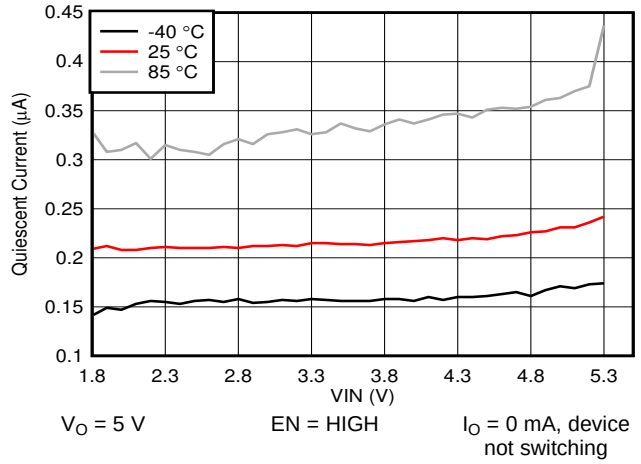


图 1. Quiescent Current versus Input Voltage

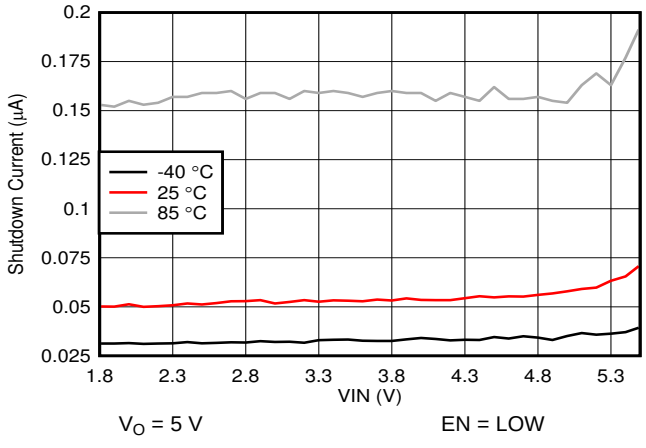


图 2. Shutdown Current versus Input Voltage

ADVANCE INFORMATION

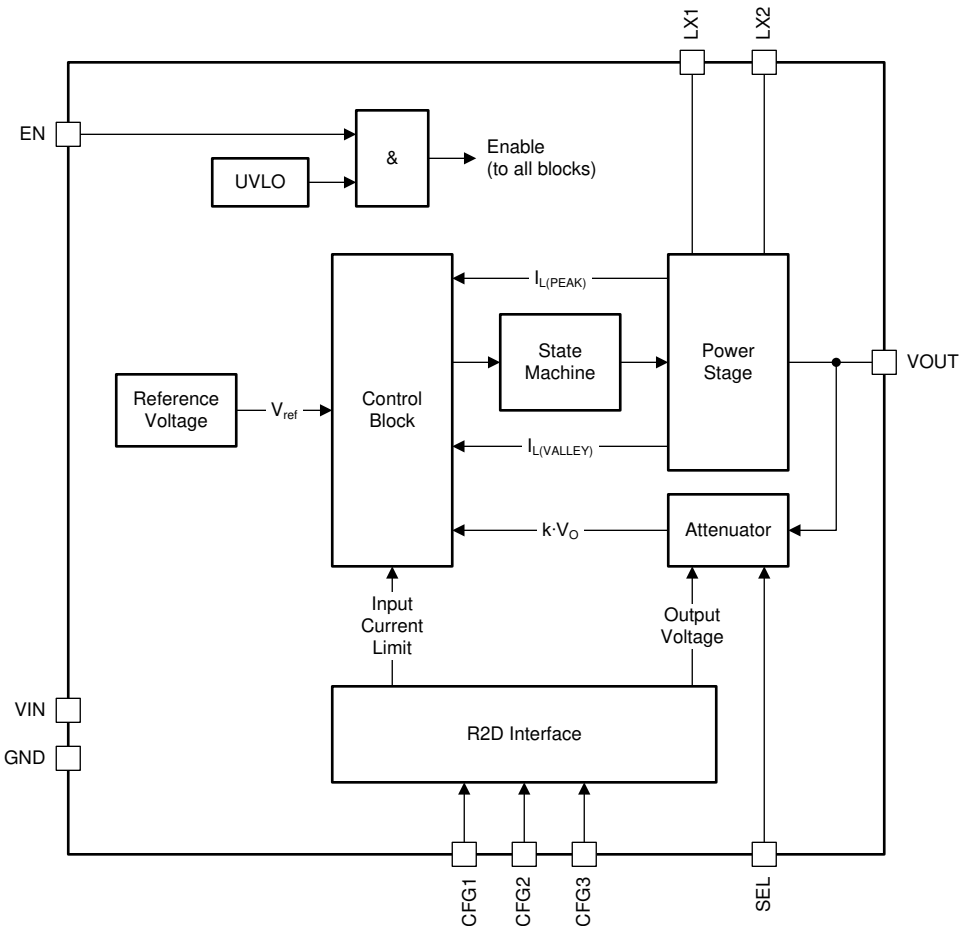
7 Detailed Description

7.1 Overview

The TPS63900 device is a four-switch synchronous buck-boost converter with a maximum output current of 400 mA. It has a single-mode operation that allows the device to regulate the output voltage to a level above, below, or equal to the input voltage without displaying the mode-switching transients and unpredictable inductor current ripple from which many other buck-boost devices suffer.

The switching frequency of the TPS63900 device varies with the operating conditions: it is lowest when I_O is low and increases smoothly as I_O increases.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Trapezoidal Current Control

图 3 shows a simplified block diagram of the power stage of the device. Inductor current is sensed in series with Q1 (the peak current) and Q4 (the valley current).

ADVANCE INFORMATION

Feature Description (接下页)

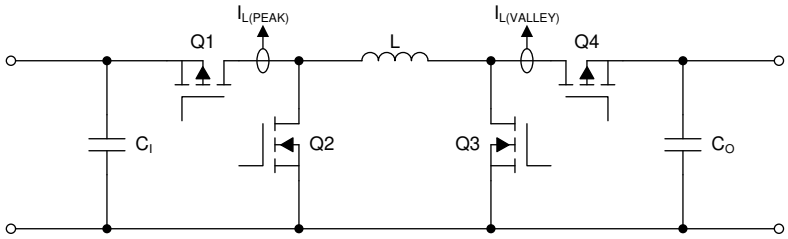


图 3. Power Stage Simplified Block Diagram

The device uses a trapezoidal inductor current to regulate its output under all operating conditions. Thus, the device only has one operating mode and does not display any of the mode-change transients or unpredictable switching displayed by many other buck-boost devices.

There are four phases of operation:

- Phase A – Q1 and Q3 are on and Q2 and Q4 are off
- Phase B – Q1 and Q4 are on and Q2 and Q3 are off
- Phase C – Q2 and Q4 are on and Q1 and Q3 are off
- Phase D – Q2 and Q3 are on and Q1 and Q4 are off

图 4 shows the inductor current waveform when $V_I > V_O$, 图 5 shows the current waveform when $V_I = V_O$, and 图 6 shows the current waveform when $V_I < V_O$.

图 4 through 图 6 show the typical waveforms during continuous conduction mode (CCM) switching for three operating conditions. During discontinuous conduction mode (DCM), the typical inductor current waveforms look similar to CCM with Phase D at 0 A inductor current. In deep boost mode, where $V_I << V_O$, Phase C length gradually decreases to zero until the switching waveform becomes triangular.

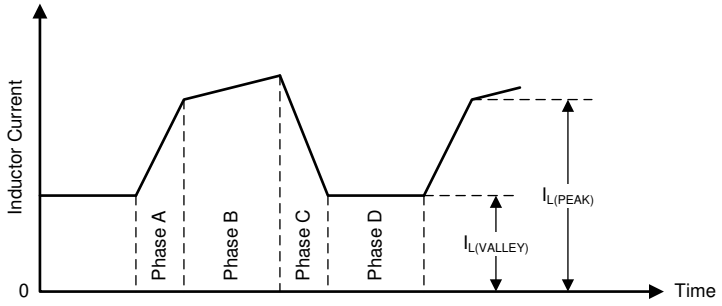


图 4. Inductor Current Waveform when $V_I > V_O$ (CCM)

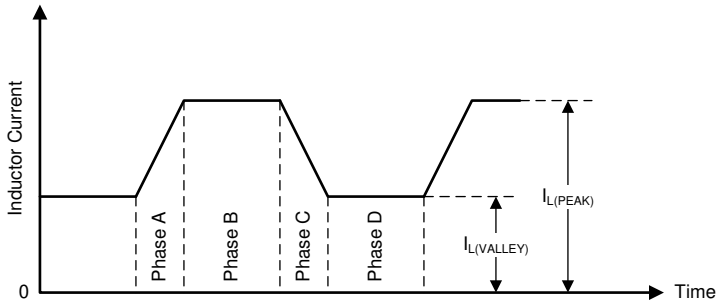


图 5. Inductor Current Waveform when $V_I = V_O$ (CCM)

ADVANCE INFORMATION

Feature Description (接下页)

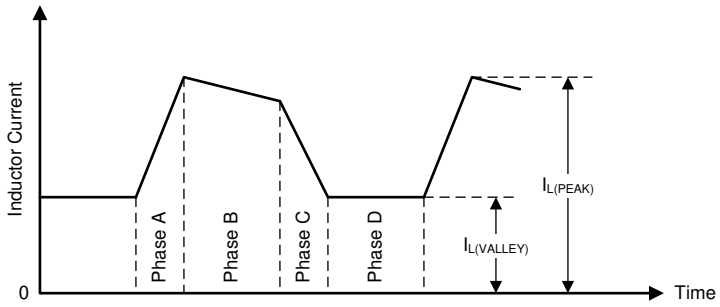


图 6. Inductor Current Waveform when $V_I < V_O$ (CCM)

The ideal relationship between V_I and V_O (that is, assuming no losses) is

$$V_O = V_I \left(\frac{t_{w(A)} + t_{w(B)}}{t_{w(B)} + t_{w(C)}} \right) \quad (1)$$

where

- V_I is the input voltage
- V_O is the output voltage
- $t_{w(A)}$ is the duration of phase A
- $t_{w(B)}$ is the duration of phase B
- $t_{w(C)}$ is the duration of phase C

By varying relative duration of each phase, the device can regulate V_O to be less than, equal to, or greater than V_I.

7.3.2 Device Enable / Disable

The device turns on when *all* the following conditions are true:

- The supply voltage is greater than the positive-going undervoltage lockout (UVLO) threshold.
- The EN pin is high.

The device turns off when *at least one* of the following conditions is true:

- The supply voltage is less than the negative-going UVLO threshold.
- The EN pin is low.

A complete state diagram is shown in 图 16.

After the device turns on, the internal reference system starts, then the trimming information and the CFG pins are read out. The device ignores any further changes to the CFG pins during device operation.

图 7 shows the internal start-up sequence.

ADVANCE INFORMATION

Feature Description (接下页)

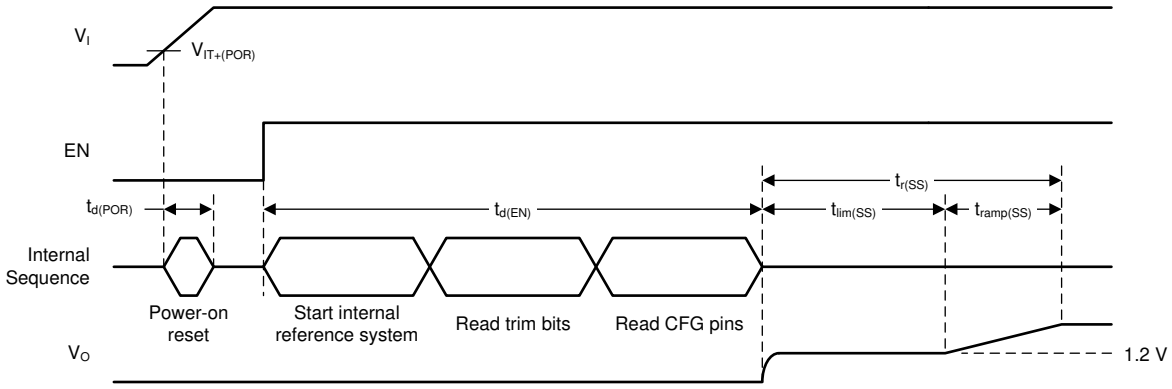


图 7. Internal Start-Up Sequence

7.3.3 Soft Start

注

The pre-production samples with XPS63900DSKT orderable part number show a different start up behavior below V_O = 1.8 V (see Soft Start - Pre-production material for details).

The device has a soft-start feature that starts the device typically with 500-mA peak current limit until V_O = 1.8 V and 500 µs elapsed when the input current limit is set to unlimited (see the *Input Current Limit* section). Afterwards, the output voltage ramps in a series of discrete steps (see 图 8).

- When $V_O \leq 1.8$ V, peak current is limited to 500 mA typical for 500 µs.
- When $V_O > 1.8$ V, each step is 100 mV high and has a duration of 125 µs.

The total start-up time can be calculated with 公式 2.

$$t_{r(SS)} = V_O \times 1.25 \left[{}^{ms}/_{V} \right] - 1.75[ms] \quad (2)$$

where

- $t_{r(SS)}$ is the rise time of the output voltage in milliseconds
- V_O is the output voltage in volts

图 8 shows a typical start-up case.

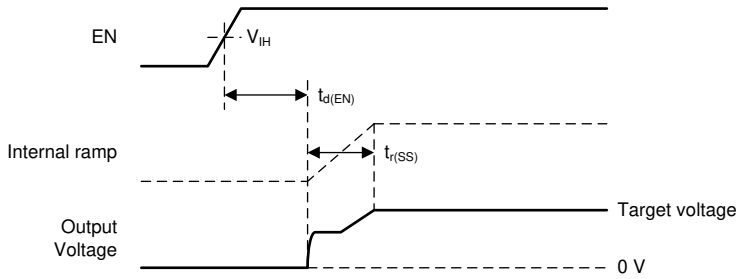


图 8. Start-Up Behavior

图 9 illustrates the start-up step size behavior.

ADVANCE INFORMATION

Feature Description (接下页)

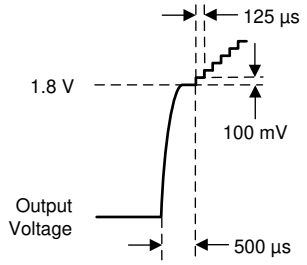


图 9. Typical Soft-Start Ramp Step Size

表 1 shows the typical start-up time for a number of standard output voltages.

表 1. Typical Start-Up Times

OUTPUT VOLTAGE	START-UP TIME
1.8 V	0.5 ms
2.5 V	1.375 ms
3.3 V	2.375 ms
5 V	4.5 ms

If the output is prebiased – that is, the initial output voltage is not zero – the start-up behavior is as follows:

- If the prebias voltage is *lower* than the target voltage, the device does not start switching until the ramping output voltage is greater than the prebias voltage (see 图 10).
- If the prebias voltage is *higher* than the target voltage, the device does not start to switch until the output voltage has decreased to the target voltage (see 图 11). The device cannot actively discharge the output to the target voltage and relies on the load current to discharge the output capacitor and decrease the output voltage to the target value.

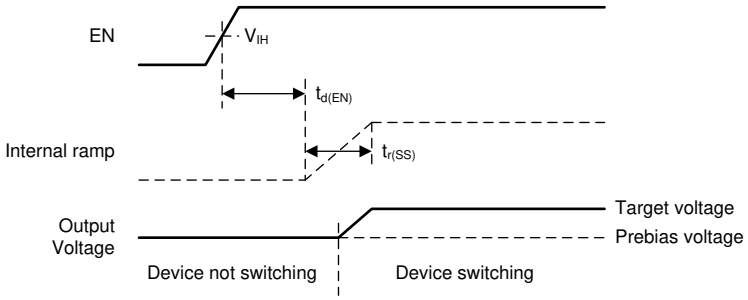


图 10. Start-Up Behavior into Prebiased (Low) Output

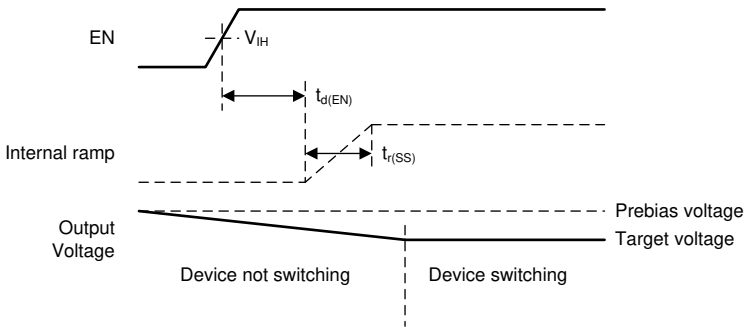


图 11. Start-Up Behavior into Prebiased (High) Output

ADVANCE INFORMATION

7.3.4 Soft Start - Pre-production material

注

This section only applies to pre-production samples with XPS63900DSKT orderable part number.

The device has a soft-start feature that starts the device typically with 500-mA peak current limit until V_O = 1.2 V and 750 µs elapsed. Afterwards, the output voltage ramps in a series of discrete steps (see 图 8).

- When $V_O \leq 1.2$ V, peak current is limited to 500 mA typical for 750 µs.
- When $V_O \leq 1.8$ V, each step is 200 mV high and has a duration of 125 µs.
- When $V_O > 1.8$ V, each step is 100 mV high and has a duration of 125 µs.

The total start-up time can be calculated with 公式 3.

$$t_{r(SS)} = V_O \times 1.25 \left[{}^{ms}/_{V} \right] - 1.125[ms] \quad (3)$$

where

- $t_{r(SS)}$ is the rise time of the output voltage in milliseconds
- V_O is the output voltage in volts

图 12 illustrates the start-up step size behavior.

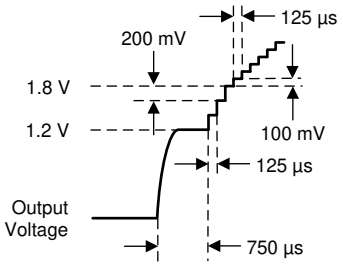


图 12. Typical Soft-Start Ramp Step Size

表 2 shows the typical start-up time for a number of standard output voltages.

表 2. Typical Start-Up Times

OUTPUT VOLTAGE	START-UP TIME
1.8 V	1.125 ms
2.5 V	2 ms
3.3 V	3 ms
5 V	5.125 ms

7.3.5 Input Current Limit

The device can limit the current drawn from its supply, so that it can be used with batteries that do not support high peak currents. The input current limit is active during normal operation and at start-up to avoid high inrush current. The device has eight current limit settings:

- 1 mA
- 2.5 mA
- 5 mA
- 10 mA
- 25 mA
- 50 mA
- 100 mA
- Unlimited

ADVANCE INFORMATION

CFG1 and CFG2 pins select which setting is active (see the *Device Configuration (Resistor-to-Digital Interface)* section).

7.3.6 Dynamic Voltage Scaling

The device has a dynamic voltage scaling function to switch between the two output voltage settings. When the SEL pin changes state, the output voltage ramps to the new value in 100-mV steps. The duration of each step is 125 µs (see 图 13).

The device does not actively discharge the output capacitor, when the output voltage ramps to a lower level. This leads to a longer output voltage settling time when light load is applied (see 图 14). The settling time can be calculated with 公式 4.

$$t_{settle} = C_O \times \frac{V_{O(HIGH)} - V_{O(LOW)}}{I_O} \quad (4)$$

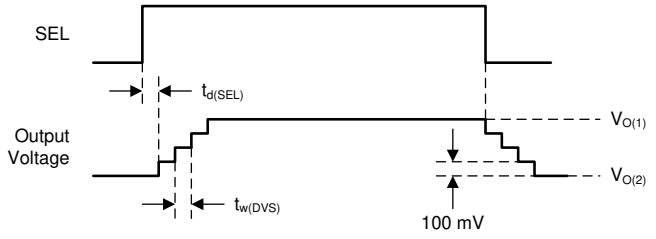


图 13. Dynamic Voltage Scaling with High Load

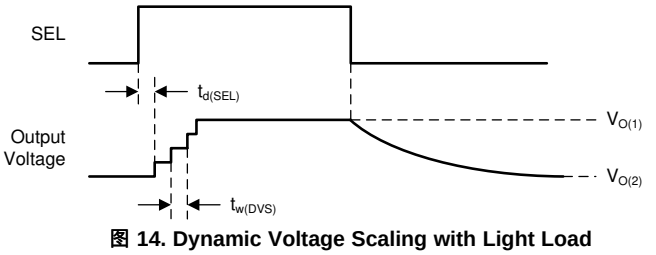


图 14. Dynamic Voltage Scaling with Light Load

7.3.7 Device Configuration (Resistor-to-Digital Interface)

The device has three configuration pins (CFG1, CFG2, and CFG3) that control its operation. When the device starts up, a resistor-to-digital (R2D) interface reads the values of the configuration resistors on the CFG pins and transfers the setting to an internal configuration register (see 图 15).

- CFG1 and CFG2 set $V_{O(2)}$ level and the input current limit.
- CFG3 sets $V_{O(1)}$ level.

To reduce power consumption, the device reads the value of the resistors connected to the configuration pins during start-up and then disables these pins. Once the device has started to operate, changes to the configuration pins have no effect.

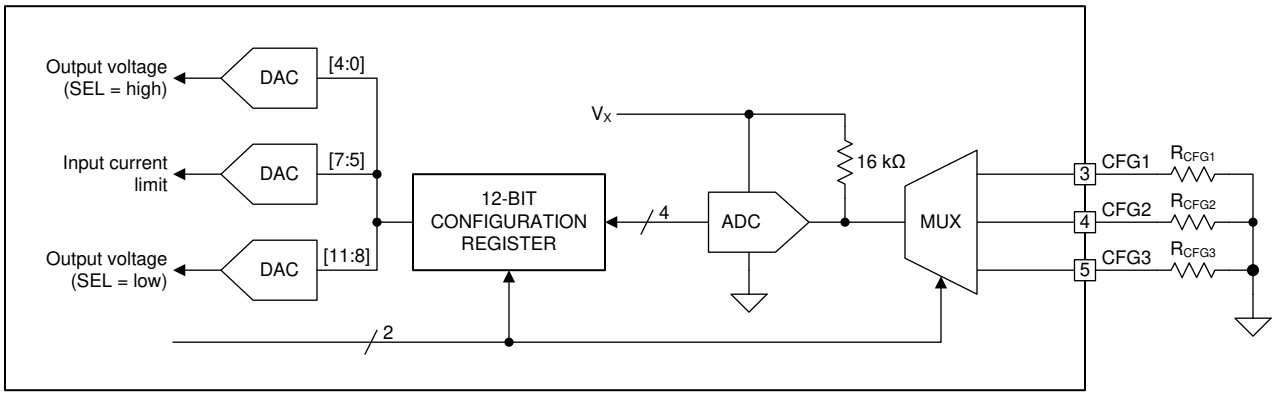


图 15. Resistor-to-Digital Interface Block Diagram

表 3 summarizes the resistor values needed to configure the device for different input current limit and output voltage (SEL = high) settings. For correct operation, use resistors with a tolerance of ±1% or better and a temperature coefficient of ±200 ppm or better.

ADVANCE INFORMATION

注

For correct operation, TI recommends that the total RMS error of the configuration resistors—including initial tolerance, temperature drift, and ageing—is less than ±3%.

表 3. Input Current Limit and Output Voltage (SEL = High) Settings

OUTPUT VOLTAGE - $V_{O(2)}$ (SEL = HIGH)		INPUT CURRENT LIMIT							
		Unlimited	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
1.8 V	R_{CFG1}	0 Ω							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
1.9 V	R_{CFG1}	511 Ω							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.0 V	R_{CFG1}	1.15 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.1 V	R_{CFG1}	1.87 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.2 V	R_{CFG1}	2.74 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.3 V	R_{CFG1}	3.83 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.4 V	R_{CFG1}	5.11 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.5 V	R_{CFG1}	6.49 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.6 V	R_{CFG1}	8.25 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.7 V	R_{CFG1}	10.5 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.8 V	R_{CFG1}	13.3 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.9 V	R_{CFG1}	16.2 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.0 V	R_{CFG1}	20.5 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.1 V	R_{CFG1}	24.9 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.2 V	R_{CFG1}	30.1 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.3 V	R_{CFG1}	36.5 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.4 V	R_{CFG1}	0 Ω							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.5 V	R_{CFG1}	511 Ω							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.6 V	R_{CFG1}	1.15 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.7 V	R_{CFG1}	1.87 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ

ADVANCE INFORMATION

表 3. Input Current Limit and Output Voltage (SEL = High) Settings (接下页)

OUTPUT VOLTAGE - $V_{O(2)}$ (SEL = HIGH)		INPUT CURRENT LIMIT							
		Unlimited	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
3.8 V	R_{CFG1}	2.74 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.9 V	R_{CFG1}	3.83 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.0 V	R_{CFG1}	5.11 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.1 V	R_{CFG1}	6.49 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.2 V	R_{CFG1}	8.25 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.3 V	R_{CFG1}	10.5 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.4 V	R_{CFG1}	13.3 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.5 V	R_{CFG1}	16.2 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.6 V	R_{CFG1}	20.5 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.7 V	R_{CFG1}	24.9 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.8 V	R_{CFG1}	30.1 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
5.0 V	R_{CFG1}	36.5 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ

表 4 summarizes the resistor values needed to configure the device for different output voltage (SEL = low) settings. For correct operation, use resistors with a tolerance of ±1% or better and a temperature coefficient of better than ±200 ppm.

表 4. Output Voltage (SEL Pin = Low) Settings

OUTPUT VOLTAGE - $V_{O(1)}$ (SEL = LOW)	R_{CFG3}
1.8 V	0 Ω
2.0 V	511 Ω
2.1 V	1.15 kΩ
2.2 V	1.87 kΩ
2.3 V	2.74 kΩ
2.4 V	3.83 kΩ
2.5 V	5.11 kΩ
2.6 V	6.49 kΩ
2.7 V	8.25 kΩ
2.8 V	10.5 kΩ
3.0 V	13.3 kΩ
3.3 V	16.2 kΩ
3.6 V	20.5 kΩ
4.0 V	24.9 kΩ
4.5 V	30.1 kΩ

ADVANCE INFORMATION

表 4. Output Voltage (SEL Pin = Low) Settings (接下页)

OUTPUT VOLTAGE - $V_{O(1)}$ (SEL = LOW)	R_{CFG3}
5.0 V	36.5 kΩ

7.3.8 SEL Pin

The SEL pin selects which configuration bits control the output voltage.

- When SEL = high, the output voltage $V_{O(2)}$ is set.
- When SEL = low, the output voltage $V_{O(1)}$ is set.

7.3.9 Short-Circuit Protection

7.3.9.1 Current Limit Setting = 'Unlimited'

The device has a function to limit the current through Q1. When the peak current is limited for longer than 1 ms, the device detects a short-circuit condition and turns off the output. The device automatically restarts operation after a delay of $t_{d(RESTART)}$.

7.3.9.2 Current Limit Setting = 1 mA to 100 mA

The input current limiting function automatically limits current during a short-circuit condition. The device regulates the average input current for as long as the short-circuit condition exists and does not turn off the output.

7.3.10 Thermal Shutdown

The device has a thermal shutdown function that disables the device if it gets too hot for correct operation. When the device cools down, it automatically restarts operation after a typical delay of $t_{d(RESTART)}$ = 10 ms. The device starts with the soft-start feature (see the *Soft Start* section) and keeps the previously read CFG pin setting.

7.4 Device Functional Modes

The device has two functional modes: on and off. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

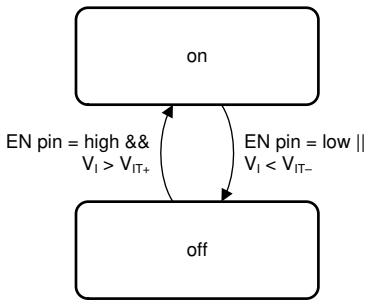


图 16. Device Functional Modes

ADVANCE INFORMATION

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS63900 is a high efficiency, non-inverting buck-boost converter with an extremely low quiescent current, suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage. The input current limit and output voltage are set through resistors connected to the three CFGx pins.

8.2 Typical Application

注

The pre-production samples with XPS63900DSKT orderable part number need to be operated with 10 µF output capacitor (0603). For the production material the minimum output capacitor is 22 µF (0603).

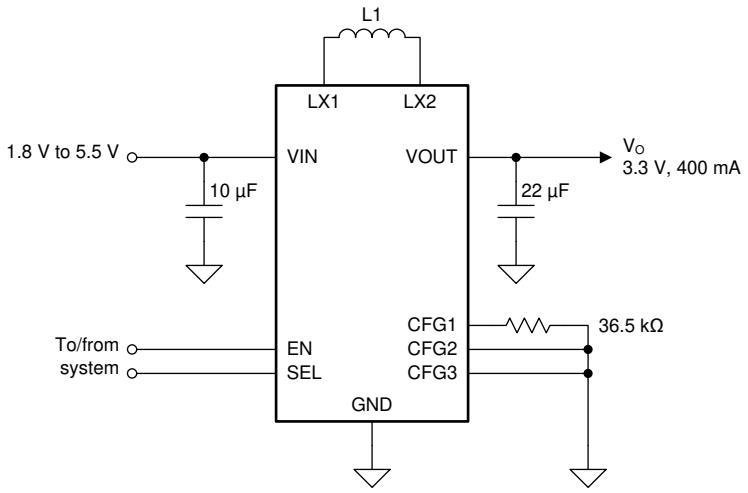


图 17. 3.3 V_{OUT} Typical Application

8.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the *Recommended Operating Conditions*.

表 5. Matrix of Output Capacitor and Inductor Combinations

Nominal Inductor Value [µH](1)	Nominal Output Capacitor Value [µF](2)				
	22	47	66	100	≥ 300
2.2	+ (3)	+	+	+	+(4)

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and DC bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application. Other check marks indicate possible filter combinations.
(4) Only with input current limit active.

ADVANCE INFORMATION

8.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, the *Recommended Operating Conditions* outlines minimum and maximum values for inductance and capacitance. Tolerance and derating must be taken into account when selecting nominal inductance and capacitance.

8.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS63900 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint or cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.2.2 Inductor Selection

The inductor selection is affected by several parameters such as inductor ripple current, output voltage ripple, transition point into Power Save Mode, and efficiency. See 表 6 for typical inductors.

For high efficiencies, the inductor must have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the core and conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using 公式 6. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{5}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{6}$$

where:

- D = Duty Cycle in Boost mode
- f = Converter switching frequency
- L = Inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption)

注

The calculation must be done for the minimum input voltage in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated using 公式 6. Possible inductors are listed in 表 6.

ADVANCE INFORMATION

表 6. List of Recommended Inductors (1)

Inductor Value [µH]	Saturation Current [A]	DCR [mΩ]	Part Number	Manufacturer	Size (LxWxH mm)
2.2	3.5	21	XFL4020-222ME	Coilcraft	4 x 4 x 2
2.2	1.9	40	1231AS-H-2R2M	Murata	3.7 x 3.5 x 1.8
2.2	1.7	72	SRN3015TA-2R2M	Bourns	3 x 3 x 1.5
2.2	3.1	97	DFE252010F-2R2M	Murata	2.5 x 2 x 1

(1) See *Third-party Products Disclaimer*

8.2.2.3 Output Capacitor Selection

For the output capacitor, use of small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC is recommended. The recommended nominal output capacitor value is a single 22 µF. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor must be placed as close as possible to the VOUT and GND pins of the IC.

It is important that the effective capacitance is given according to the recommended value in the *Recommended Operating Conditions*. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a tradeoff between size and transient behavior as higher capacitance reduces transient response overshoot and undershoot and increases transient response time. Possible output capacitors are listed in 表 7.

There is no upper limit for the output capacitance value.

表 7. List of Recommended Capacitors(1)

Capacitor Value [µF]	Voltage Rating [V]	Part Number	Manufacturer	Size (Metric)
22	6.3	GRM187R60J226ME15	Murata	0603 (1608)
22	6.3	GRM219R60J476ME44	Murata	0805 (3210)
47	6.3	GRM188R60J476ME15	Murata	0603 (1608)

(1) See *Third-party Products Disclaimer*

8.2.2.4 Input Capacitor Selection

A 10-µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS63900 converter additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

表 8. List of Recommended Capacitors(1)

Capacitor Value [µF]	Voltage Rating [V]	Part Number	Manufacturer	Size (Metric)
10	6.3	GRM188R60J106ME47	Murata	0603 (1608)
10	10	GRM188R61A106ME69	Murata	0603 (1608)
22	6.3	GRM187R60J226ME15	Murata	0603 (1608)

(1) See *Third-party Products Disclaimer*

8.2.2.5 Setting The Output Voltage

The output voltage is set with CFGx pins (see the *Device Configuration (Resistor-to-Digital Interface)* section).

ADVANCE INFORMATION

8.2.3 Application Curves

注

The pre-production samples with XPS63900DSKT orderable part number need to be operated with 10 µF output capacitor (0603). For the production material the minimum output capacitor is 22 µF (0603).

表 9. Components for Application Characteristic Curves for V_{OUT} = 3.3 V(1)(2)

Reference	Description	Part Number	Manufacturer
U1	400-mA ultra low Iq Buck-Boost Converter (2.5 mm x 2.5 mm QFN)	TPS63900DSK	Texas Instruments
L1	2.2 µH, 4 mm x 4 mm x 2 mm, 3.5 A, 10 mΩ	XFL4020-222ME	Coilcraft
C1	10 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J106ME47	Murata
C2	22 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM187R60J226ME15	Murata
CFG1	36.5 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard
CFG2	0 Ω, 0603 Resistor, 1%, 100 mW	Standard	Standard
CFG3	0 Ω, 0603 Resistor, 1%, 100 mW	Standard	Standard

(1) See *Third-Party Products Discalimer*
(2) For other output voltages, refer to 表 5 for resistor values.

表 10. Typical Characteristics Curves

PARAMETER	CONDITIONS	FIGURE
Output Current Capability		
Typical Output Current Capability versus Input Voltage	V_O = 1.8 V to 5.0 V	图 18
Typical Burst Switching Frequency versus Output Current	V_O = 1.8 V to 3.6 V	图 19
Efficiency		
Efficiency versus Output Current	V_I = 2.5 V to 5.5 V, V_O = 3.3 V	图 20
Efficiency versus Input Voltage	I_O = 10 mA to 500 mA, V_O = 3.3 V	图 21
Switching Waveforms		
Switching Waveforms, Boost Operation	V_I = 1.8 V, V_O = 3.3 V	图 22
Switching Waveforms, Boost Operation	V_I = 2.8 V, V_O = 3.3 V	图 23
Switching Waveforms, Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V	图 24
Switching Waveforms, Buck Operation	V_I = 4.0 V, V_O = 3.3 V	图 25
DVS (Digital Voltage Scaling)		
DVS Behavior at Light Load	V_I = 3.3 V, $V_{O(1)}$ = 2.2 V, $V_{O(2)}$ = 3.6 V, Load = 1 kΩ	图 26
DVS Behavior at High Load	V_I = 3.3 V, $V_{O(1)}$ = 2.2 V, $V_{O(2)}$ = 3.6 V, Load = 30 Ω	图 27

ADVANCE INFORMATION

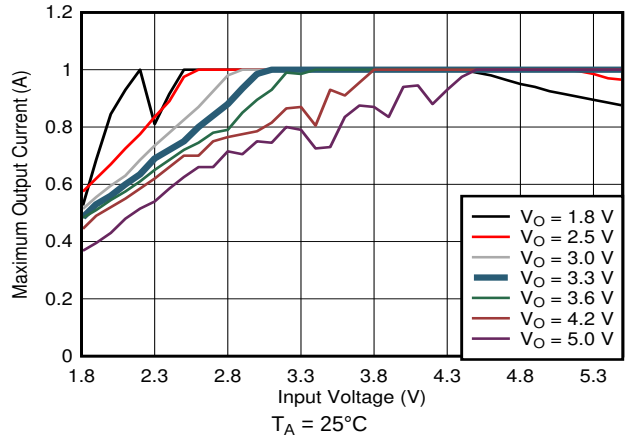


图 18. Typical Output Current Capability versus Input Voltage

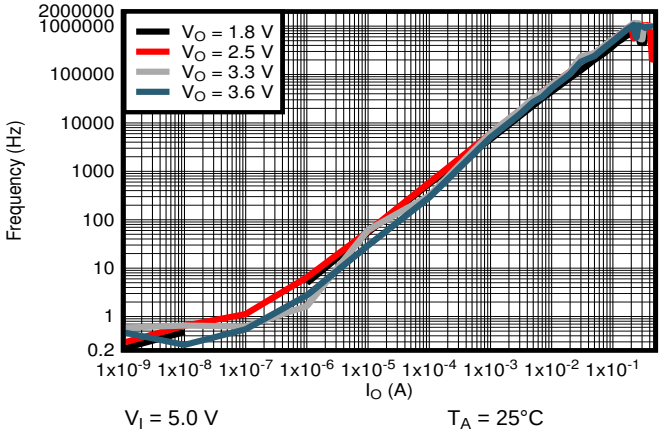


图 19. Typical Burst Switching Frequency versus Output Current

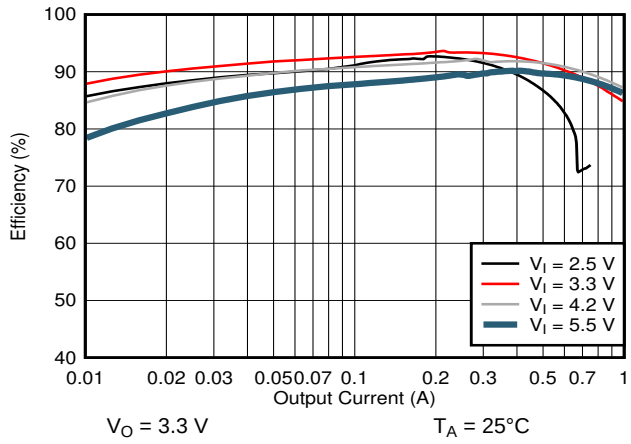


图 20. Efficiency versus Output Current

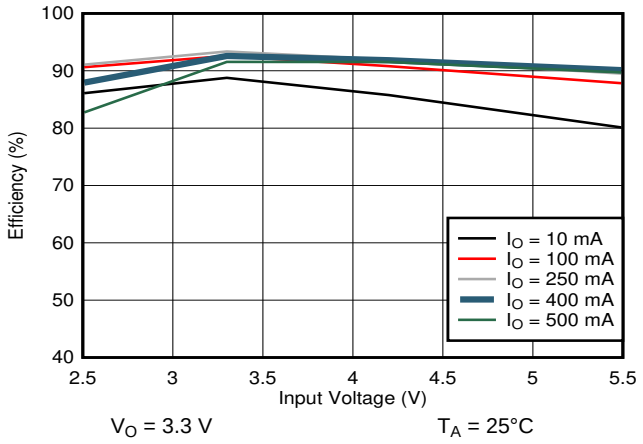


图 21. Efficiency versus Input Voltage

图 22. Switching Waveforms, PFM Boost Operation

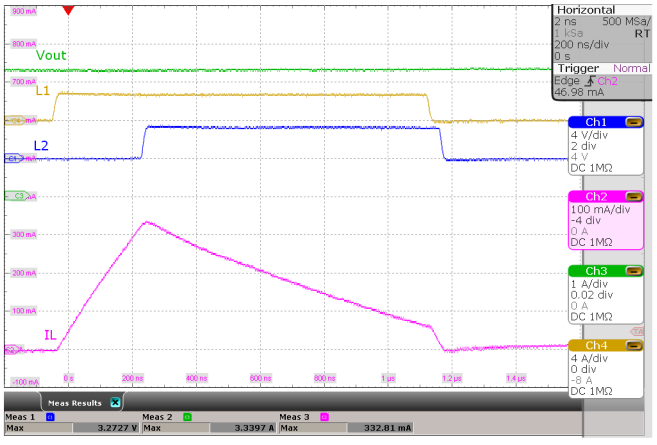


图 23. Switching Waveforms, PFM Buck-Boost Operation

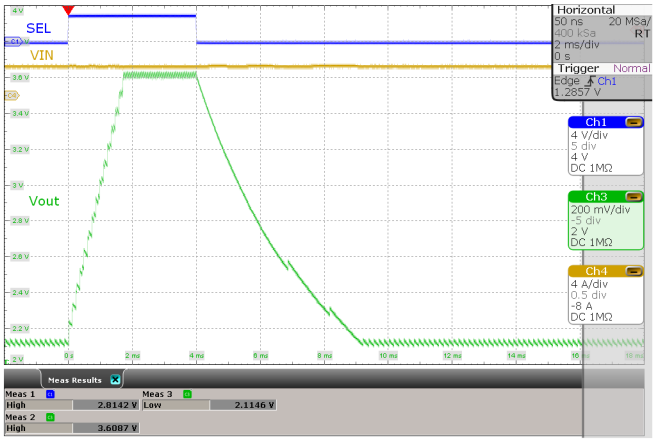
ADVANCE INFORMATION

V_I = 3.3 V, V_O = 3.3 V　　No load

图 24. Switching Waveforms, PFM Buck Operation

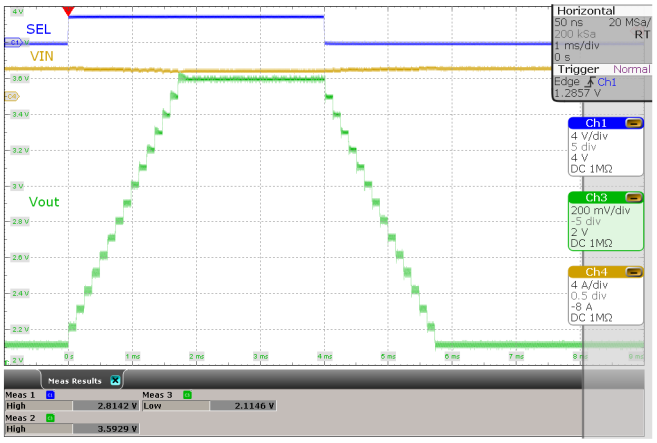
V_I = 4.0 V, V_O = 3.3 V　　No load

图 25. Switching Waveforms, PWM Boost Operation



V_I = 3.3 V, $V_{O(1)}$ = 2.2 V, $V_{O(2)}$ = 3.6 V　　1-kΩ resistive load

图 26. DVS Behavior at Light Load



V_I = 3.3 V, $V_{O(1)}$ = 2.2 V, $V_{O(2)}$ = 3.6 V　　30-Ω resistive load

图 27. DVS Behavior at High Load

ADVANCE INFORMATION

9 Power Supply Recommendations

The TPS63900 device is designed to operate with input supplies from 1.8 V to 5.5 V. The input supply must be stable and free of noise to achieve the full performance of the device. If the input supply is located more than a few centimeters away from the device, additional bulk capacitance can be required. The input capacitance shown in the application schematics in this data sheet is sufficient for typical applications.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of any switching power supply design. A poor layout can cause unstable operation, load regulation problems, increased ripple and noise, and EMI issues.

The following PCB layout design guidelines are recommended:

- Place the input and output capacitors close to the device.
- Minimize the area of the input loop, and use short, wide traces on the top layer to connect the input capacitor to the VIN and GND pins.
- Minimize the area of the output loop, and use short, wide traces on the top layer to connect the output capacitor to the VOUT and GND pins.
- The location of the inductor on the PCB is less important than the location of the input and output capacitors. Place the inductor after the input and output capacitors have been placed close to the device. You can route the traces to the inductor on an inner layer if necessary.

10.2 Layout Example

图 28 shows an example of a PCB layout that follows the recommendations of the previous section.

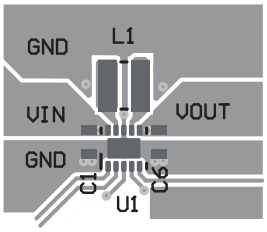


图 28. PCB Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

德州仪器 (TI)，*《TPS63900 EVM 用户指南》*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

12 机械、封装和可订购信息

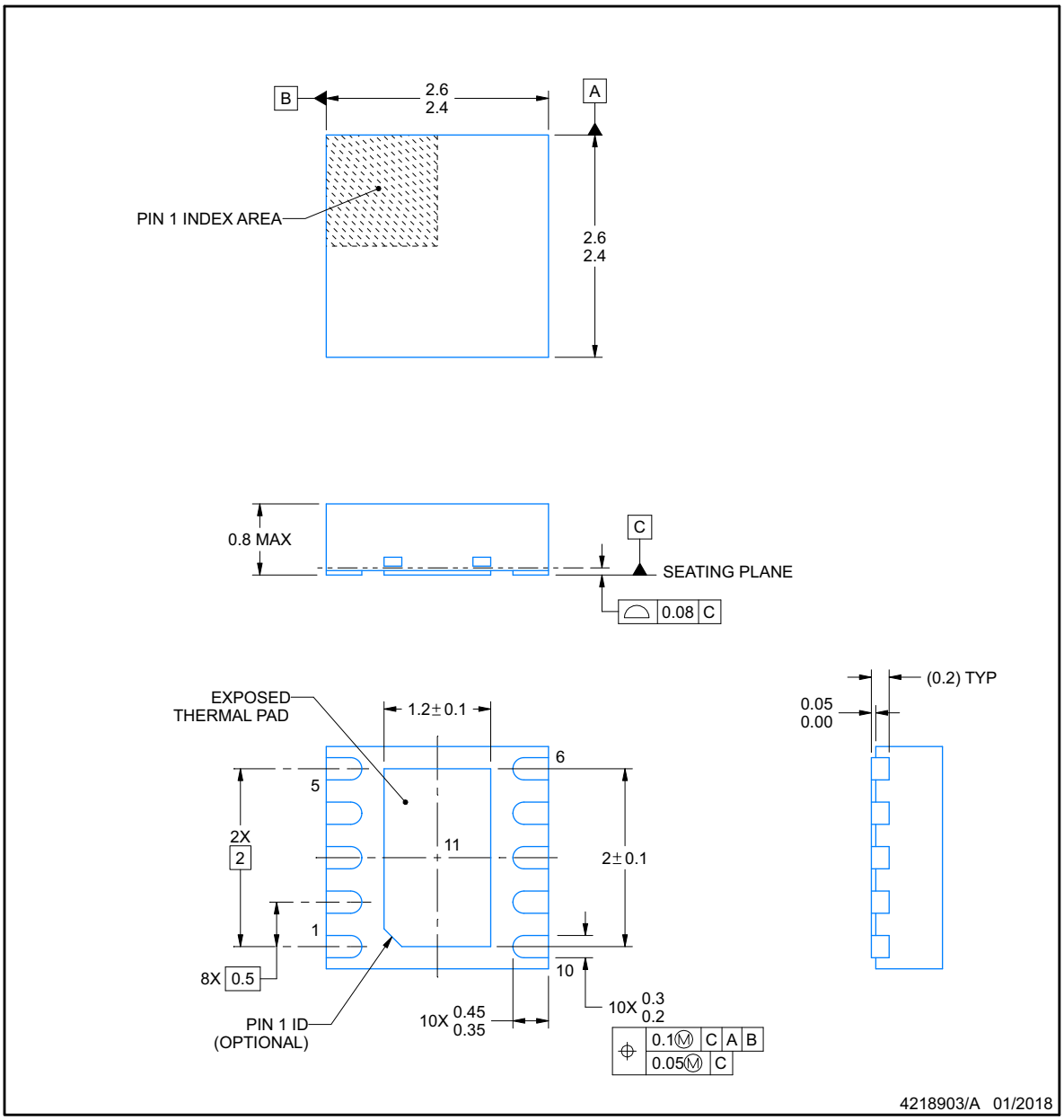
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OUTLINE

DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

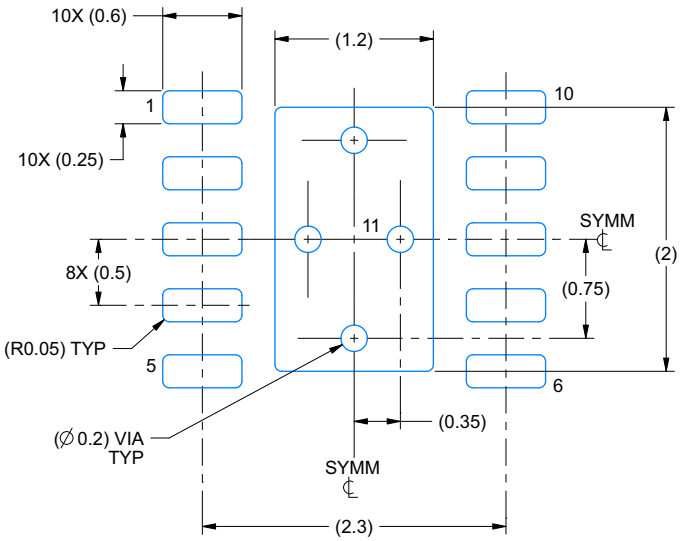
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

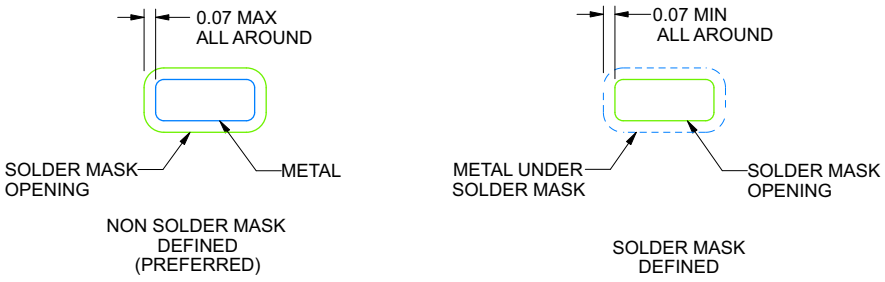
DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218903/A 01/2018

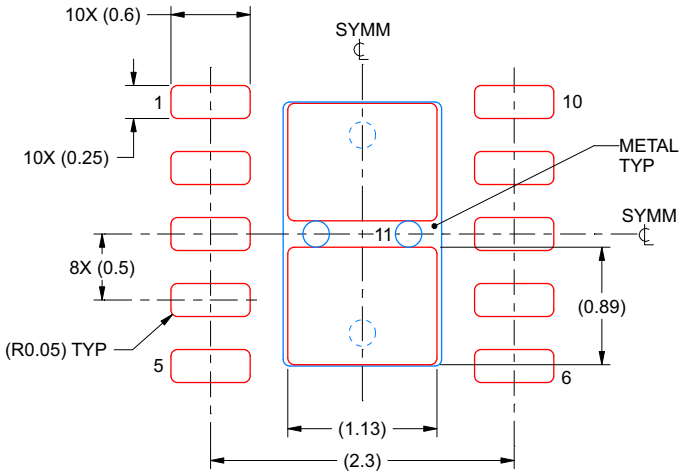
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DSK0010A — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218903/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63900DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	639	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

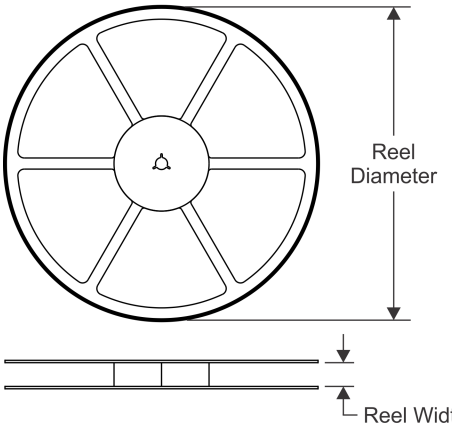
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

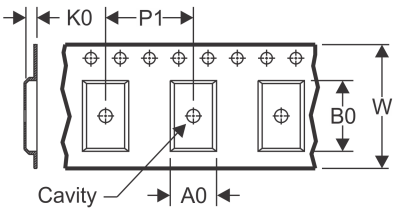
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

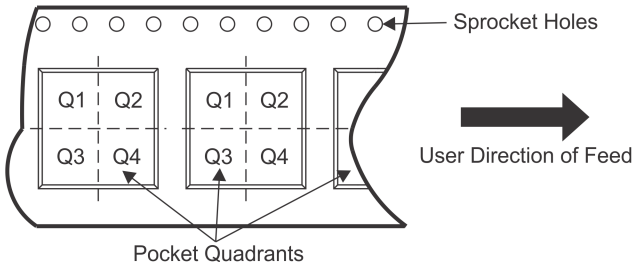


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

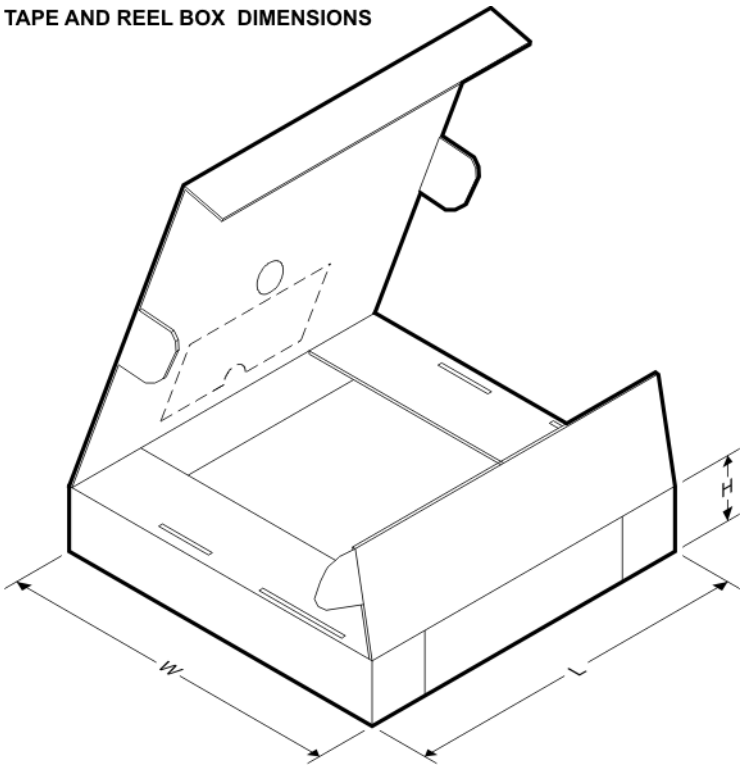
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63900DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



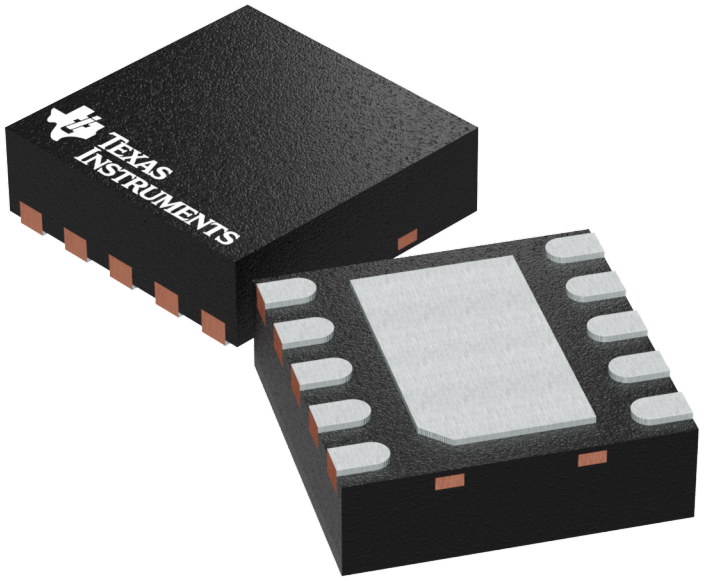
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63900DSKR	SON	DSK	10	3000	210.0	185.0	35.0

DSK 10 WSON - 0.8 mm max height

2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



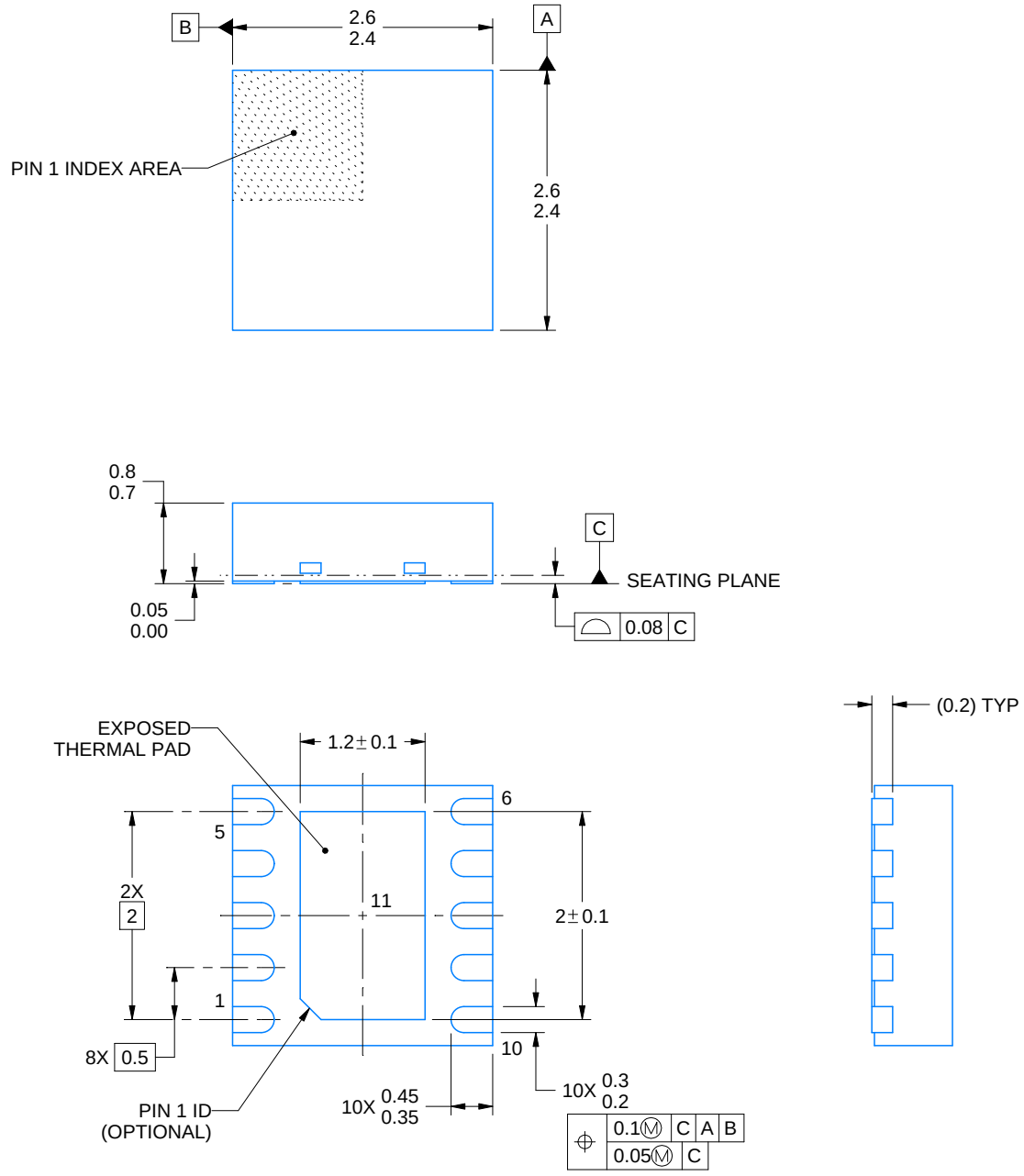
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSK0010A

WSON - 0.8 mm max height

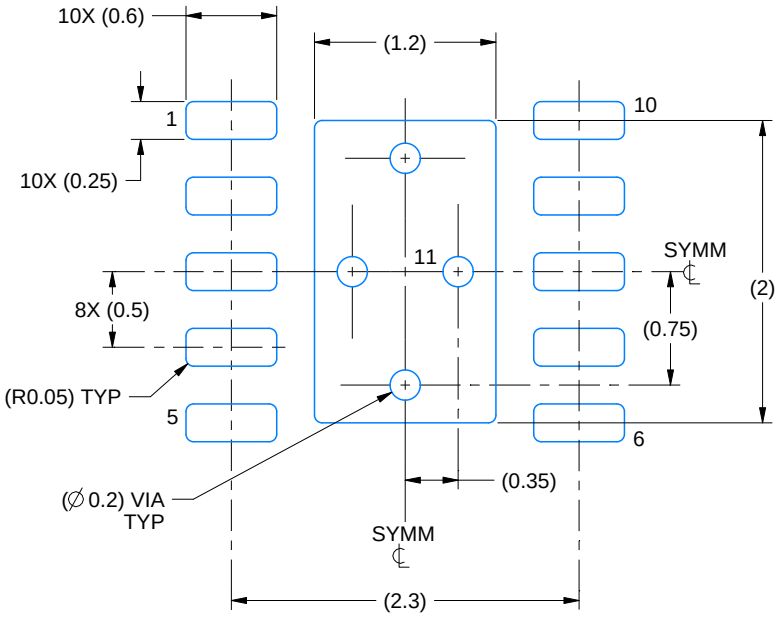
PLASTIC SMALL OUTLINE - NO LEAD



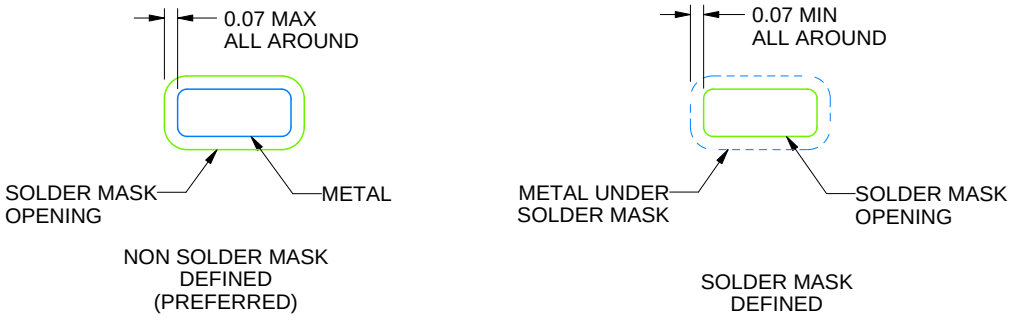
4218903/B 10/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

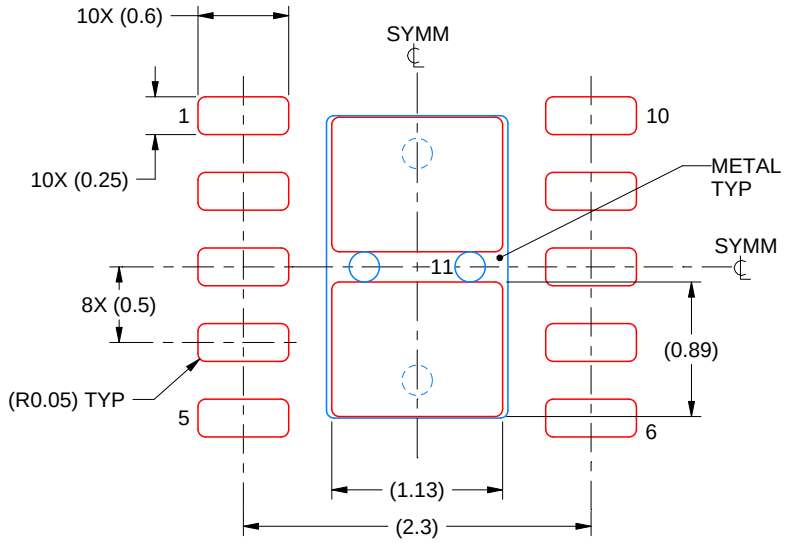


SOLDER MASK DETAILS

4218903/B 10/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218903/B 10/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122