TPS62850x-Q1 2.7-V to 6-V, 1-A / 2-A Automotive Step-Down Converter in SOT583 Package

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- T_J = –40°C to +150°C
- Input voltage range: 2.7 V to 6 V
- Quiescent current 15 µA typical
- Output voltage from 0.6 V to 5.5 V
- Output voltage accuracy ±1% (PWM operation)
- Forced PWM or PWM/PFM operation
- Adjustable switching frequency of 1.8 MHz to 4 MHz
- Precise ENABLE input allows:
  - User-defined undervoltage lockout
  - Exact sequencing
- 100% duty cycle mode
- Active output discharge
- Spread spectrum clocking - optional
- Foldback overcurrent protection - optional
- Power-good output with window comparator

2 Applications

- ADAS camera, ADAS sensor fusion
- Surround view ECU
- Hybrid and reconfigurable cluster
- Head unit, Telematics control unit
- External amplifier

3 Description

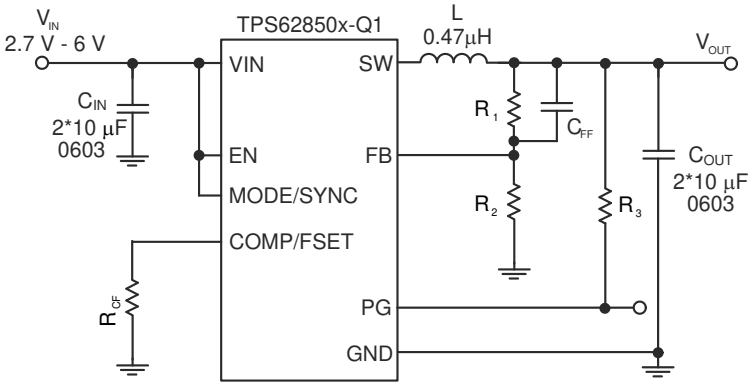
The TPS62850x-Q1 is a family of pin-to-pin 1-A and 2-A high efficiency, easy-to-use synchronous step-down DC/DC converters. They are based on a peak current mode control topology. They are designed for automotive applications such as Infotainment and Advanced Driver Assistance Systems. Low resistive switches allow up to 2-A continuous output current at high ambient temperature. The switching frequency is externally adjustable from 1.8 MHz to 4 MHz and can also be synchronized to an external clock in the same frequency range. In PWM/PFM mode, the TPS62850x-Q1 automatically enter Power Save Mode at light loads to maintain high efficiency across the whole load range. The TPS62850x-Q1 provide a 1% output voltage accuracy in PWM mode which helps design a power supply with high output voltage accuracy.

The TPS62850x-Q1 is available in a SOT583 package.

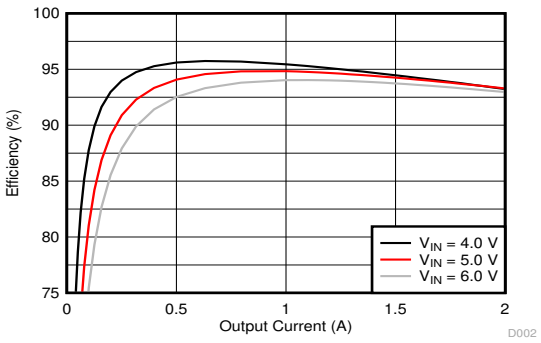
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS628501-Q1	SOT583	2.1 mm x 1.6 mm (incl pins)
TPS628502-Q1	SOT583	2.1 mm x 1.6 mm (incl pins)

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



Efficiency versus I_{OUT}, V_{OUT} = 3.3 V

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2020) to Revision B (November 2020)	Page
• Changed device status from Advance Information to Production Data	1

5 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	Vout DISCHARGE	FOLDBACK CURRENT LIMIT	TYPICAL OUTPUT CAPACITOR	SOFT START	OUTPUT VOLTAGE
TPS628501QDRLRQ1	1 A	ON	OFF	2 x 10 µF	internal 1 ms	adjustable
TPS628502QDRLRQ1	2 A	ON	OFF	2 x 10 µF	internal 1 ms	adjustable
TPS6285010MQDRLRQ1	1 A	ON	OFF	2 x 10 µF	internal 1 ms	fixed 1.8 V
TPS6285020MQDRLRQ1	2 A	ON	OFF	2 x 10 µF	internal 1 ms	fixed 1.8 V

6 Pin Configuration and Functions

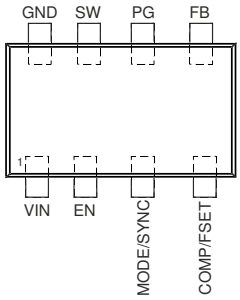


Figure 6-1. 8 Pin SOT583 DRL Packae (Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	This is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB	5	I	Voltage feedback input, connect the resistive output voltage divider to this pin.
GND	8		Ground pin
MODE/SYNC	3	I	The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external frequency. See *Section 7.5* for the detailed specification for the digital signal applied to this pin for external synchronization.
COMP/FSET	4	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized.
PG	6	O	Open-drain power-good output
SW	7		This is the switch pin of the converter and is connected to the internal Power MOSFETs.
VIN	1		Power supply input. Make sure the input capacitor is connected as close as possible between pin VIN and GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	– 0.3	6.5	V
Pin voltage(2)	SW (DC)	– 0.3	V_{IN} + 0.3	V
Pin voltage(2)	SW (AC, less than 10ns)(3)	– 3	10	V
Pin voltage(2)	COMP/FSET, PG	– 0.3	V_{IN} + 0.3	V
Pin voltage(2)	EN, MODE/SYNC, FB	– 0.3	6.5	V
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		6	V
V_{OUT}	Output voltage range	0.6		5.5	V
L	Effective inductance	0.32	0.47	1.2	µH
C_{OUT}	Effective output capacitance(1)	8	10	200	µF
C_{IN}	Effective input capacitance(1)		10		µF
R_{CF}		4.5		100	kΩ
I_{SINK_PG}	Sink current at PG pin	0		2	mA
T_J	Junction temperature	–40		150	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied. Further restrictions may apply. Please see the feature description for COMP/FSET about the output capacitance vs compensation setting and output voltage.

7.4 Thermal Information

THERMAL METRIC(1)		TPS62850x-Q1 DRL (JEDEC)(2) 8 PINS	TPS62850x-Q1 DRL (EVM) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.3	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	n/a	°C/W

THERMAL METRIC[1]		TPS62850x-Q1 DRL (JEDEC)[2] 8 PINS	TPS62850x-Q1 DRL (EVM) 8 PINS	UNIT
Y_{JB}	Junction-to-board characterization parameter	20	n/a	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) JEDEC standard PCB with 4 layers, no thermal vias

7.5 Electrical Characteristics

Over operating junction remperature range (T_J = -40°C to +150°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = V_{IN}, no load, device not switching, MODE = GND, V_{OUT} = 0.6 V		17	36	µA
I_{SD}	Shutdown current	EN = GND, Nominal value at T_J = 25°C, Max value at T_J = 150°C		1.5	48	µA
V_{UVLO}	Undervoltage lock out threshold	V_{IN} rising	2.45	2.6	2.7	V
		V_{IN} falling	2.1	2.5	2.6	V
T_{JSD}	Thermal shutdown threshold	T_J rising		170		°C
	Thermal shutdown hysteresis	T_J falling		15		°C
CONTROL and INTERFACE						
$V_{EN,IH}$	Input threshold voltage at EN, rising edge		1.05	1.1	1.15	V
$V_{EN,IL}$	Input threshold voltage at EN, falling edge		0.96	1.0	1.05	V
V_{IH}	High-level input-threshold voltage at MODE/SYNC		1.1			V
$I_{EN,LKG}$	Input leakage current into EN	V_{IH} = V_{IN} or V_{IL} = GND			125	nA
V_{IL}	Low-level input-threshold voltage at MODE/SYNC				0.3	V
I_{LKG}	Input leakage current into MODE/SYNC				100	nA
t_{Delay}	Enable delay time	Time from EN high to device starts switching; V_{IN} applied already	135	200	520	µs
t_{Delay}	Enable delay time	Time from EN high to device starts switching; V_{IN} applied already, V_{IN} ≥ 3.3 V			480	µs
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good; device not in current limit	0.8	1.3	1.8	ms
f_{SYNC}	Frequency range on MODE/SYNC pin for synchronization		1.8		4	MHz
	Duty cycle of synchronization signal at MODE/SYNC		20		80	%
	Time to lock to external frequency			50		µs
	resistance from COMP/FSET to GND for logic low	internal frequency setting with f = 2.25 MHz	0		2.5	kΩ
	Voltage on COMP/FSET for logic high	internal frequency setting with f = 2.25 MHz		V_{IN}		V
V_{TH_PG}	UVP power good threshold voltage; DC level	rising (%V_{FB})	92	95	98	%
V_{TH_PG}	UVP power good threshold voltage; DC level	falling (%V_{FB})	87	90	93	%

Over operating junction remperature range (T_J = -40°C to +150°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH_PG}	OVP power good threshold voltage; DC level	rising (%V_{FB})	107	110	113	%
	OVP power good threshold voltage; DC level	falling (%V_{FB})	104	107	111	%
$V_{PG,OL}$	Low-level output voltage at PG	I_{SINK_PG} = 2 mA		0.07	0.3	V
$I_{PG,LKG}$	Input leakage current into PG	V_{PG} = 5 V			100	nA
t_{PG}	PG deglitch time	for a high level to low level transition on the power good output		40		µs
OUTPUT						
V_{FB}	Feedback voltage, adjustable version			0.6		V
V_{FB}	Feedback voltage, fixed voltage version	for TPS6285010M, TPS6285020M		1.8		V
$I_{FB,LKG}$	Input leakage current into FB, adjustable version	V_{FB} = 0.6 V		1	70	nA
$I_{FB,LKG}$	Input current into FB, fixed voltage versions			1		µA
V_{FB}	Feedback voltage accuracy	PWM, $V_{IN} \geq V_{OUT}$ + 1 V	-1		1	%
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, $V_{OUT} \geq$ 1.0 V, $C_{out,eff} \geq$ 10 µF, L = 0.47µH	-1		2	%
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, V_{OUT} < 1.0 V, $C_{out,eff} \geq$ 15 µF, L = 0.47µH	-1		3	%
	Load regulation	PWM		0.05		%/A
	Line regulation	PWM, I_{OUT} = 1 A, $V_{IN} \geq V_{OUT}$ + 1 V		0.02		%/V
R_{DIS}	Output discharge resistance				100	Ω
f_{SW}	PWM Switching frequency range	MODE = high, see the FSET pin functionality about setting the switching frequency	1.8	2.25	4	MHz
f_{SW}	PWM Switching frequency range	MODE = low, see the FSET pin functionality about setting the switching frequency	1.8		3.5	MHz
f_{SW}	PWM Switching frequency	with COMP/FSET tied to GND or V_{IN}	2.025	2.25	2.475	MHz
f_{SW}	PWM Switching frequency tolerance	using a resistor from COMP/FSET to GND	-12		12	%
$t_{on,min}$	Minimum on-time of high-side FET	V_{IN} = 3.3 V, T_J = -40°C to 125°C		35	50	ns
$t_{on,min}$	Minimum on-time of low-side FET			10		ns
$R_{DS(ON)}$	High-side FET on-resistance	$V_{IN} \geq$ 5 V		65	120	mΩ
	Low-side FET on-resistance	$V_{IN} \geq$ 5 V		33	70	mΩ
	High-side MOSFET leakage current	T_J = 85°C		2.5		µA
	High-side MOSFET leakage current			0.01	44	µA
	Low-side MOSFET leakage current	T_J = 85°C		3.7		µA
	Low-side MOSFET leakage current			0.01	70	µA
	SW leakage	V(SW) = 0.6V, current into SW pin	-0.05		11	µA
I_{LIMH}	High-side FET switch current limit	DC value, for TPS628502; V_{IN} = 3 V to 6 V	2.85	3.4	3.9	A
I_{LIMH}	High-side FET switch current limit	DC value, for TPS628501; V_{IN} = 3 V to 6 V	2.1	2.6	3.0	A
I_{LIMNEG}	Low-side FET negative current limit	DC value		-1.8		A

7.6 Typical Characteristics

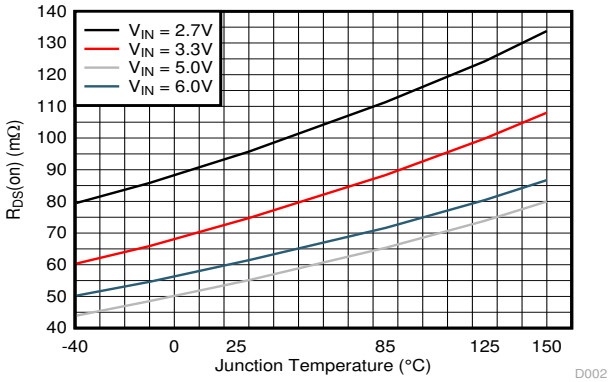


Figure 7-1. $R_{DS\ (ON)}$ of High-side Switch

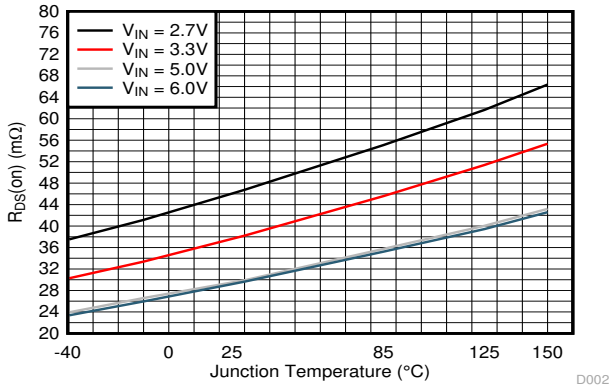


Figure 7-2. $R_{DS\ (ON)}$ of Low-side Switch

8 Parameter Measurement Information

8.1 Schematic

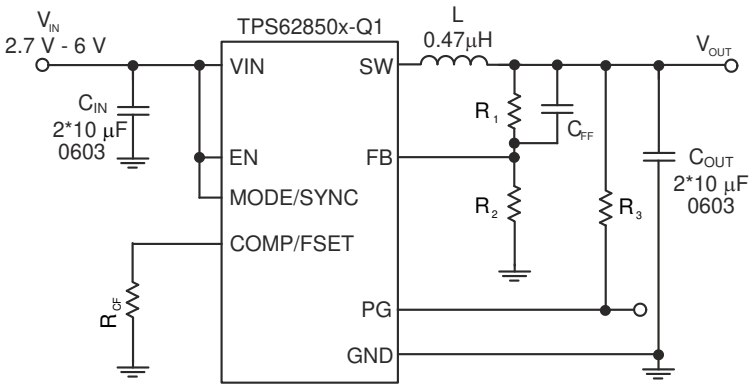


Figure 8-1. Measurement Setup

Table 8-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPS628502QDRLRQ1	Texas Instruments
L	0.47-µH inductor DFE252012PD	Murata
C_{IN}	2 x 10 µF / 6.3 V GCM188D70J106M	Murata
C_{OUT}	2 x 10 µF / 6.3 V GCM188D70J106M for Vout ≥ 1 V	Murata
C_{OUT}	3 x 10 µF / 6.3 V GCM188D70J106M for Vout < 1 V	Murata
R_{CF}	8,06 kΩ	Any
C_{FF}	10 pF	Any
R_1	Depending on VOUT	Any
R_2	Depending on VOUT	Any
R_3	100 kΩ	Any

(1) See the *Third-party Products Disclaimer*.

9 Detailed Description

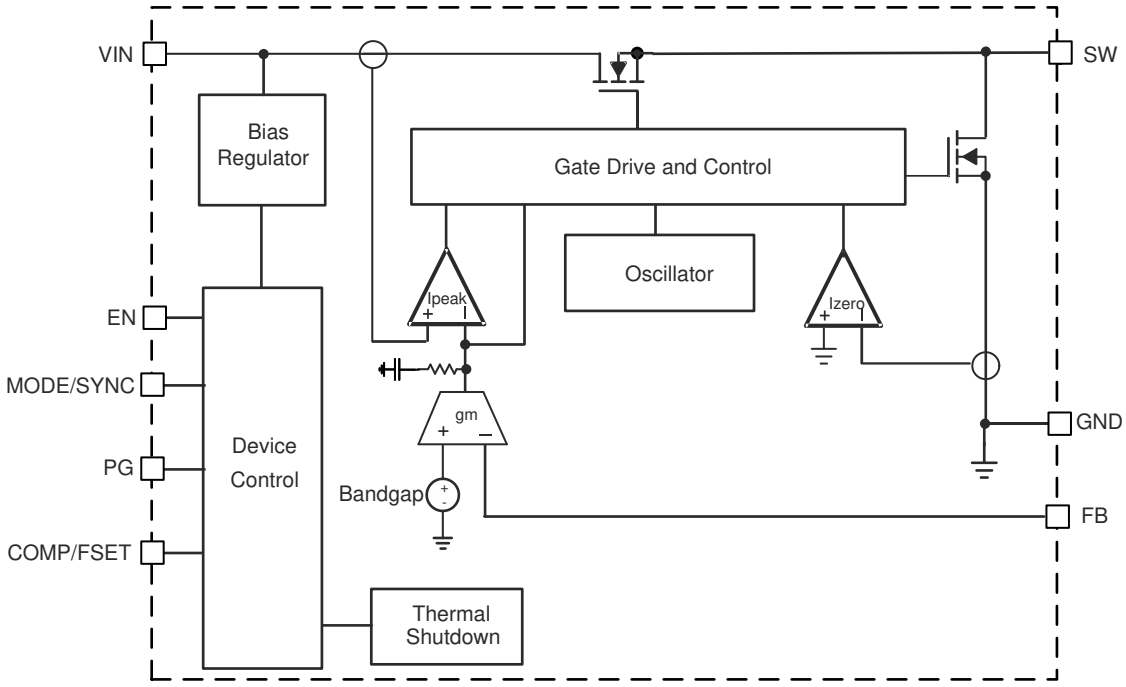
9.1 Overview

The TPS62850x-Q1 synchronous switch mode power converters are based on a peak current mode control topology. The control loop is internally compensated.

To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with the TPS62850x-Q1, the internal compensation has two settings. See *Section 9.3.2*. One out of the two compensation settings is chosen either by a resistor from COMP/FSET to GND, or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors. The devices can be operated without a feedforward capacitor on the output voltage divider, however, using a typically 10-pF feedforward capacitor improves transient response.

The devices support forced fixed frequency PWM operation with the MODE pin tied to a logic high level. The frequency is defined as either 2.25 MHz internally fixed when COMP/FSET is tied to GND or VIN, or in a range of 1.8 MHz to 4 MHz defined by a resistor from COMP/FSET to GND. Alternatively, the devices can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz, applied to the MODE pin with no need for additional passive components. An internal PLL allows you to change from internal clock to external clock during operation. The synchronization to the external clock is done on a falling edge of the clock applied at MODE to the rising edge on the SW pin. This allows a roughly 180° phase shift when the SW pin is used to generate the synchronization signal for a second converter. When the MODE pin is set to a logic low level, the device operates in power save mode (PFM) at low output current and automatically transfers to fixed frequency PWM mode at higher output current. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Precise Enable (EN)

The voltage applied at the enable pin of the TPS62850x-Q1 is compared to a fixed threshold of 1.1 V for a rising voltage. This allows you to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS62850x-Q1 starts operation when the rising threshold is exceeded. For proper operation, the enable (EN) pin must be terminated and must not be left floating. Pulling the enable pin low forces the device into shutdown, with a shutdown current of typically 1 µA. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

9.3.2 COMP/FSET

This pin allows to set three different parameters:

- Internal compensation settings for the control loop (two settings available)
- The switching frequency in PWM mode from 1.8 MHz to 4 MHz
- Enable/disable spread spectrum clocking (SSC)

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows you to adopt the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at start up of the converter, so a change in the resistor during operation only has an effect on the switching frequency but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined setting. Do not leave the pin floating.

The switching frequency has to be selected based on the input voltage and the output voltage to meet the specifications for the minimum on-time and minimum off-time.

Example: V_{IN} = 5 V, V_{OUT} = 0.6 V --> duty cycle = 0.6 V / 5 V = 0.12

- --> $t_{on,min}$ = 1 / fs × 0.12
- --> $f_{sw,max}$ = 1 / $t_{on,min}$ × 0.12 = 1 / 0.05 µs × 0.12 = 2.4 MHz

The compensation range has to be chosen based on the minimum capacitance used. The capacitance can be increased from the minimum value as given in Table 9-1, up to the maximum of 200 µF in both compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1 with spread spectrum clocking (SSC) disabled:

$$R_{CF}(k\Omega) = \frac{18MHz \cdot k\Omega}{fs(MHz)} \quad (1)$$

For compensation (comp) setting 1 with spread spectrum clocking (SSC) enabled:

$$R_{CF}(k\Omega) = \frac{60MHz \cdot k\Omega}{fs(MHz)} \quad (2)$$

For compensation (comp) setting 2 with spread spectrum clocking (SSC) disabled:

$$R_{CF}(k\Omega) = \frac{180MHz \cdot k\Omega}{f_S(MHz)} \quad (3)$$

Table 9-1. Switching Frequency, Compensation, and Spread Spectrum Clocking

R_{CF}	COMPENSATION	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE FOR VOUT < 1 V	MINIMUM OUTPUT CAPACITANCE FOR 1 V ≤ VOUT < 3.3 V	MINIMUM OUTPUT CAPACITANCE FOR VOUT ≥ 3.3 V
10 kΩ .. 4.5 kΩ	for smallest output capacitance (comp setting 1) SSC disabled	1.8 MHz (10 kΩ) .. 4 MHz (4.5 kΩ) according to Equation 1	15 µF	10 µF	8 µF
33 kΩ .. 18 kΩ	for smallest output capacitance (comp setting 1) SSC enabled	1.8 MHz (33 kΩ) .. 4 MHz (18 kΩ) according to Equation 2	15 µF	10 µF	8 µF
100 kΩ .. 45 kΩ	for best transient response (larger output capacitance) (comp setting 2) SSC disabled	1.8 MHz (100 kΩ) ..4 MHz (45 kΩ) according to Equation 3	30 µF	18 µF	15 µF
tied to GND	for smallest output capacitance (comp setting 1) SSC disabled	internally fixed 2.25 MHz	15 µF	10 µF	8 µF
tied to V_{IN}	for best transient response (larger output capacitance) (comp setting 2) SSC enabled	internally fixed 2.25 MHz	30 µF	18 µF	15 µF

Refer to *Section 10.1.3.2* for further details on the output capacitance required depending on the output voltage.

A resistor value that is too high for R_{CF} is decoded as "tied to V_{IN}", a value below the lowest range is decoded as "tied to GND". The minimum output capacitance in Table 9-1 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

9.3.3 MODE / SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin allows you to force PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. The specifications for the minimum on-time and minimum off-time has to be observed when setting the external frequency. For use with external synchronization on the MODE/SYNC pin, the internal switching frequency must be set by R_{CF} to a similar value than the externally applied clock. This ensures that, if the external clock fails, the switching frequency stays in the same range and the compensation settings are still valid.

9.3.4 Spread Spectrum Clocking (SSC)

The device offers spread spectrum clocking as an option. When SSC is enabled, the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288 kHz above the nominal switching frequency. When the device is externally synchronized by applying a clock signal to the MODE/SYNC pin, the TPS62850x-Q1 follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

9.3.5 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents misoperation of the device by switching off both the power FETs. When enabled, the device is fully operational for input voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

9.3.6 Power Good Output (PG)

Power good is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. It is driven by a window comparator. PG is held low when the device is disabled, in undervoltage lockout in thermal shutdown, and not in soft start. When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the output is high impedance.

V_{IN} must remain present for the PG pin to stay low. If the power good output is not used, it is recommended to tie to GND or leave open. The PG indicator features a de-glitch, as specified in the electrical characteristics, for the transition from "high impedance" to "low" of its output.

Table 9-2. PG Status

EN	DEVICE STATUS	PG STATE
X	V_{IN} < 2 V	undefined
low	V_{IN} ≥ 2 V	low
high	2 V ≤ V_{IN} ≤ UVLO OR in thermal shutdown OR V_{OUT} not in regulation OR device in soft start	low
high	V_{OUT} in regulation	high impedance

9.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During a PFM pause, the thermal shutdown is not active. After a PFM pause, the device needs up to 9 µs to detect a junction temperature that is too high. If the PFM burst is shorter than this delay, the device does not detect a junction temperature that is too high.

9.4 Device Functional Modes

9.4.1 Pulse Width Modulation (PWM) Operation

The TPS62850x-Q1 has two operating modes: Forced PWM mode is discussed in this section and PWM/PFM as discussed in *Section 9.4.2*.

With the MODE/SYNC pin set to high, the TPS62850x-Q1 operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP pin to GND or by an external clock signal applied to the MODE/SYNC pin. With an external clock applied to MODE/SYNC, the TPS62850x-Q1 follows the frequency applied to the pin. In general, the frequency range in forced PWM mode is 1.8 MHz to 4 MHz. However, the frequency needs to be in a range the TPS62850x-Q1 can operate at, taking the minimum on-time into account.

9.4.2 Power Save Mode Operation (PWM/PFM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 0.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency. In addition, the frequency set with the resistor on COMP/FSET must be in a range of 1.8 MHz to 3.5 MHz.

9.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as D = VOUT / VIN. The duty cycle increases as the input voltage comes close to the output voltage and the off-time gets smaller. When the minimum off-time of typically 10 ns is reached, the TPS62850x-Q1 skips switching cycles while it approaches 100% mode. In 100% mode, it keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. In 100% mode, the low-side switch is turned off. The maximum dropout voltage in 100% mode is the product of the on-resistance of the high-side switch plus the series resistance of the inductor and the load current.

9.4.4 Current Limit and Short Circuit Protection

The TPS62850x-Q1 is protected against overload and short circuit events. If the inductor current exceeds the current limit I_{LIMH}, the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side switch turns on again only if the current in the low side-switch has decreased below the low side current limit. Due to internal propagation delay, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \cdot t_{PD} \quad (4)$$

where

- I_{LIMH} is the static current limit as specified in the electrical characteristics
- L is the effective inductance at the peak current
- V_L is the voltage across the inductor (V_{IN} - V_{OUT})
- t_{PD} is the internal propagation delay of typically 50 ns

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \cdot 50ns \quad (5)$$

9.4.5 Foldback Current Limit and Short Circuit Protection

This is valid for devices where foldback current limit is enabled.

When the device detects current limit for more than 1024 subsequent switching cycles, it reduces the current limit from its nominal value to typically 1.3 A. Foldback current limit is left when the current limit indication goes away. If device operation continues in current limit, it would, after 3072 switching cycles, try again full current limit for again 1024 switching cycles.

9.4.6 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled and to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active once the TPS62850x-Q1 has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V. Output discharge is not activated during a current limit or foldback current limit event.

9.4.7 Soft Start

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay of about 200 µs then the internal reference and hence V_{OUT} rises with a slope defined by an internally defined slope of 150 µs or 1 ms (OTP option).

9.4.8 Input Overvoltage Protection

When the input voltage exceeds the absolute maximum rating, the device is set to PFM mode so it cannot transfer energy from the output to the input.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Programming the Output Voltage

The output voltage of the TPS62850x-Q1 is adjustable. It can be programmed for output voltages from 0.6 V to 5.5 V, using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from Equation 6. It is recommended to choose resistor values which allow a current of at least 2 µA, meaning the value of R_2 must not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{6}$$

10.1.2 External Component Selection

10.1.2.1 Inductor Selection

The TPS62850x-Q1 is designed for a nominal 0.47-µH inductor with a switching frequency of typically 2.25 MHz. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 0.47 µH cause a larger inductor current ripple which causes larger negative inductor current in forced PWM mode at low or no output current. For a higher or lower nominal switching frequency, the inductance must be changed accordingly. See *Section 7.3* for details.

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PFM transition point, and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 calculates the maximum inductor current.

$$I_{L(\text{max})} = I_{OUT(\text{max})} + \frac{\Delta I_{L(\text{max})}}{2} \tag{7}$$

$$\Delta I_{L(\text{max})} = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{L\,\text{min}} \cdot \frac{1}{f_{SW}} \tag{8}$$

where

- $I_{L(max)}$ is the maximum inductor current
- $\Delta I_{L(max)}$ is the peak-to-peak inductor ripple current
- Lmin is the minimum inductance at the operating point

Table 10-1. Typical Inductors

TYPE	INDUCTANCE	CURRENT [1]	FOR DEVICE	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [LxWxH] mm	MANUFACTURER[2]
XFL4015-471ME	0.47 µH, ±20%	3.5 A	TPS628501 / 502	2.25 MHz	4 x 4 x 1.6	Coilcraft
XFL4015-701ME	0.70 µH, ±20%	3.3 A	TPS628501 / 502	2.25 MHz	4 x 4 x 1.6	Coilcraft
XEL3520-801ME	0.80 µH, ±20%	2.0 A	TPS628501 / 502	2.25 MHz	3.5 x 3.2 x 2.0	Coilcraft
XEL3515-561ME	0.56 µH, ±20%	4.5 A	TPS628501 / 502	2.25 MHz	3.5 x 3.2 x 1.5	Coilcraft
XFL3012-681ME	0.68 µH, ±20%	2.1 A	TPS628501 / 502	2.25 MHz	3.0 x 3.0 x 1.2	Coilcraft

Table 10-1. Typical Inductors (continued)

TYPE	INDUCTANCE	CURRENT (1)	FOR DEVICE	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [LxWxH] mm	MANUFACTURER(2)
XPL2010-681ML	0.68 µH, ±20%	1.5 A	TPS628501	2.25 MHz	2 x 1.9 x 1	Coilcraft
DFE252012PD-R68M	0.68 µH, ±20%	see data sheet	TPS628501 / 502	2.25 MHz	2.5 x 2 x 1.2	Murata
DFE252012PD-R47M	0.47 µH, ±20%	see data sheet	TPS628501 / 502	2.25 MHz	2.5 x 2 x 1.2	Murata
DFE201612PD-R68M	0.68 µH, ±20%	see data sheet	TPS628501 / 502	2.25 MHz	2 x 1.6 x 1.2	Murata
DFE201612PD-R47M	0.47 µH, ±20%	see data sheet	TPS628501 / 502	2.25 MHz	2 x 1.6 x 1.2	Murata

(1) Lower of I_{RMS} at 20°C rise or I_{SAT} at 20% drop.
(2) See the *Third-party Products Disclaimer*.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well.

10.1.3 Capacitor Selection

10.1.3.1 Input Capacitor

For most applications, 10-µF nominal is sufficient and is recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins.

10.1.3.2 Output Capacitor

The architecture of the TPS62850x-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode.

The COMP/FSET pin allows you to select two different compensation settings based on the minimum capacitance used on the output. The maximum capacitance is 200 µF in any of the compensation settings. The minimum capacitance required on the output depends on the compensation setting and output voltage.

For output voltages below 1 V, the minimum increases linearly from 10 µF at 1 V to 15 µF at 0.6 V with the compensation setting for smallest output capacitance. Other compensation ranges are equivalent. See Table 9-1 for details.

10.2 Typical Application

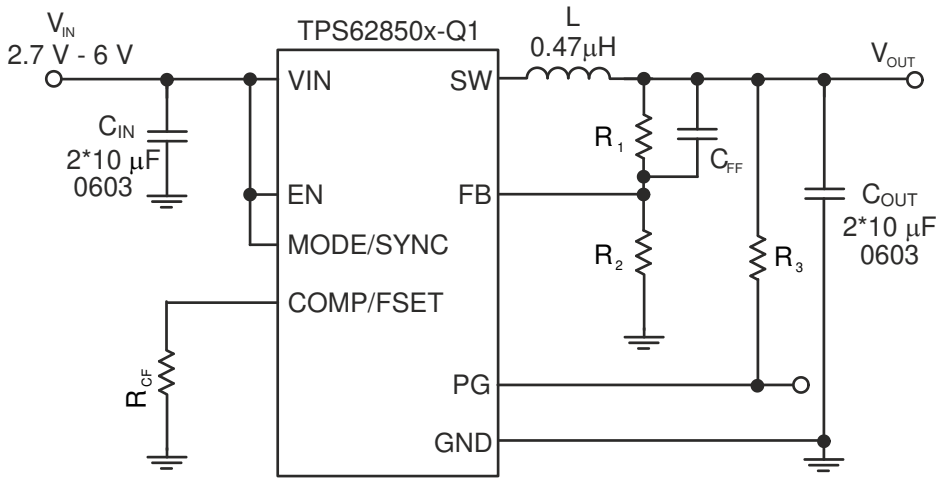


Figure 10-1. Typical Application

10.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

10.2.2 Detailed Design Procedure

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (9)$$

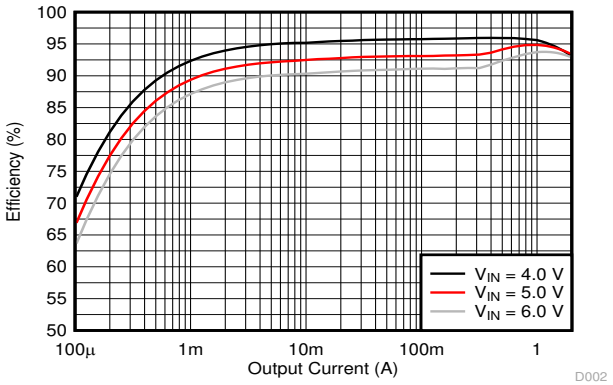
With V_{FB} = 0.6 V:

Table 10-2. Setting the Output Voltage

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	C_{FF}	EXACT OUTPUT VOLTAGE
0.8 V	16.9 kΩ	51 kΩ	10 pF	0.7988 V
1.0 V	20 kΩ	30 kΩ	10 pF	1.0 V
1.1 V	39.2 kΩ	47 kΩ	10 pF	1.101 V
1.2 V	68 kΩ	68 kΩ	10 pF	1.2 V
1.5 V	76.8 kΩ	51 kΩ	10 pF	1.5 V
1.8 V	80.6 kΩ	40.2 kΩ	10 pF	1.803 V
2.5 V	47.5 kΩ	15 kΩ	10 pF	2.5 V
3.3 V	88.7 kΩ	19.6 kΩ	10 pF	3.315 V

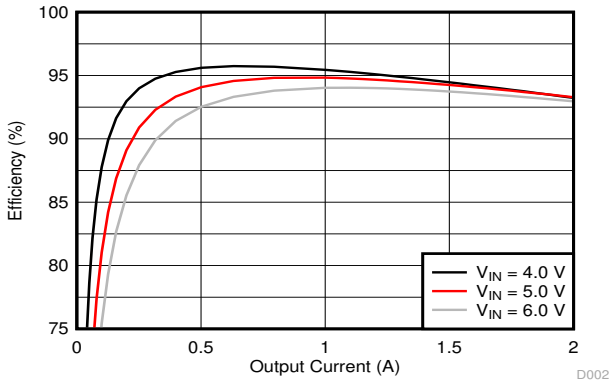
10.2.3 Application Curves

All plots have been taken with a nominal switching frequency of 2.25 MHz when set to PWM mode, unless otherwise noted. The BOM is according to Table 8-1.



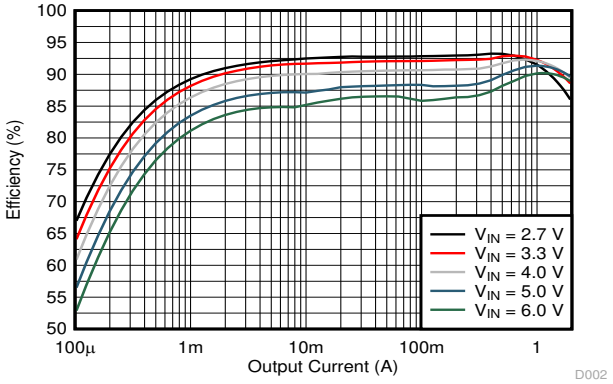
V_{OUT} = 3.3 V PFM T_A = 25°C

Figure 10-2. Efficiency versus Output Current



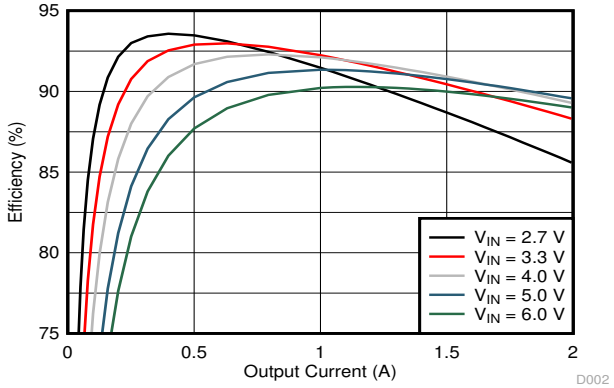
V_{OUT} = 3.3 V PWM T_A = 25°C

Figure 10-3. Efficiency versus Output Current



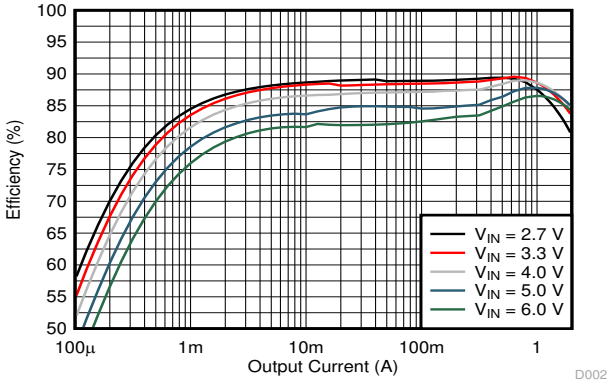
V_{OUT} = 1.8 V PFM T_A = 25°C

Figure 10-4. Efficiency versus Output Current



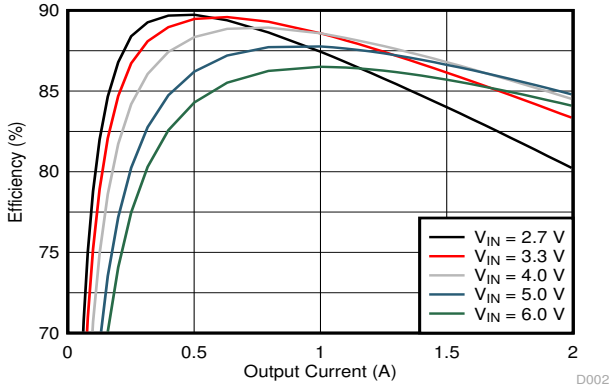
V_{OUT} = 1.8 V PWM T_A = 25°C

Figure 10-5. Efficiency versus Output Current



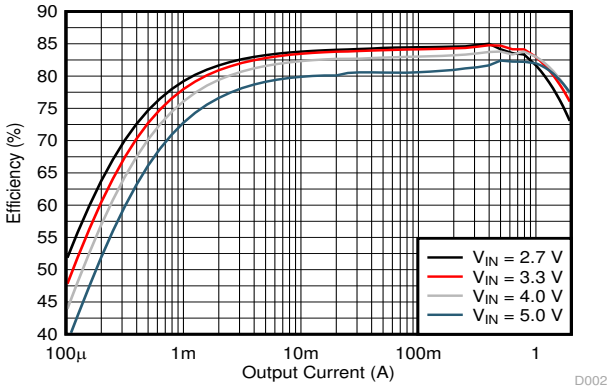
V_{OUT} = 1.1 V PFM T_A = 25°C

Figure 10-6. Efficiency versus Output Current



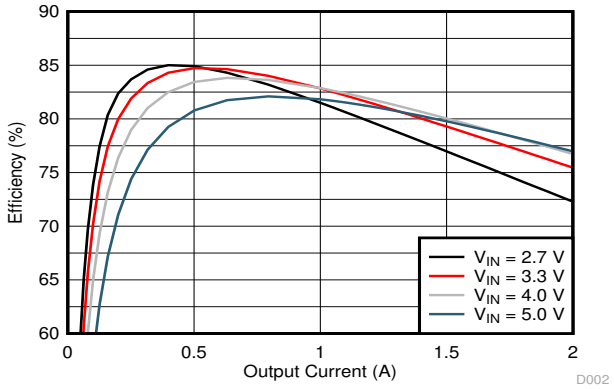
V_{OUT} = 1.1 V PWM T_A = 25°C

Figure 10-7. Efficiency versus Output Current



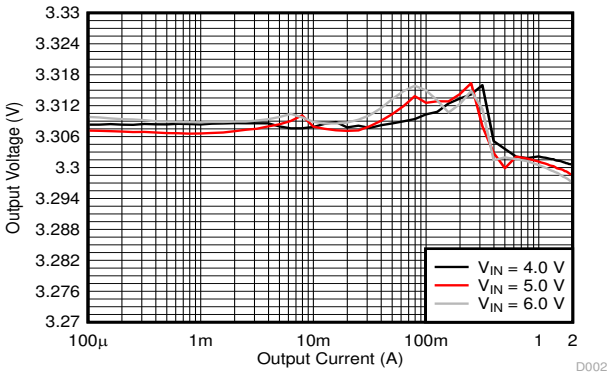
V_{OUT} = 0.6 V PFM T_A = 25°C

Figure 10-8. Efficiency versus Output Current



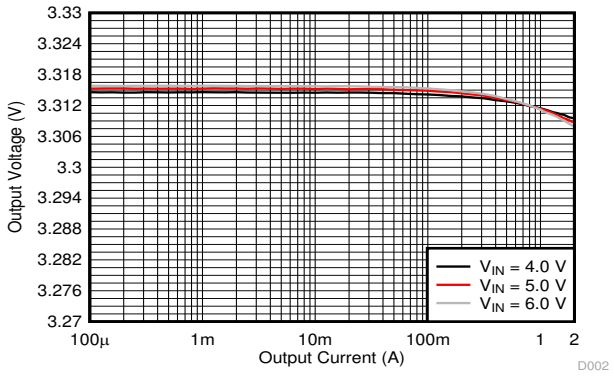
V_{OUT} = 0.6 V PWM T_A = 25°C

Figure 10-9. Efficiency versus Output Current



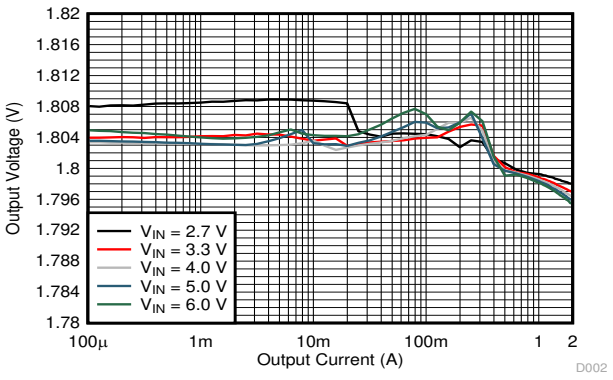
V_{OUT} = 3.3 V PFM T_A = 25°C

Figure 10-10. Output Voltage versus Output Current



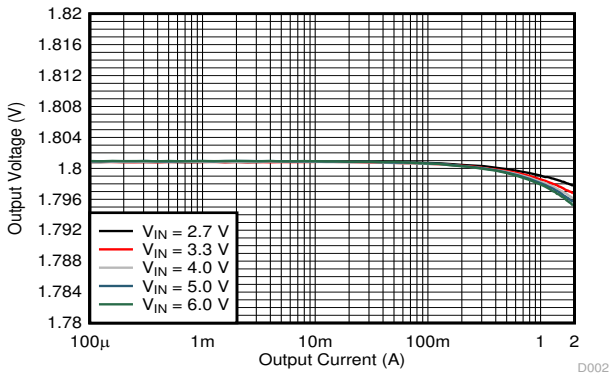
V_{OUT} = 3.3 V PWM T_A = 25°C

Figure 10-11. Output Voltage versus Output Current



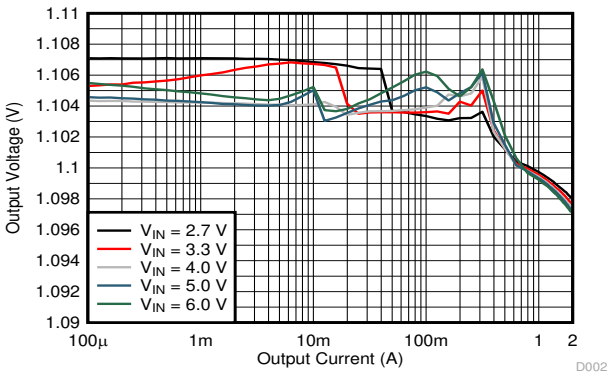
V_{OUT} = 1.8 V PFM T_A = 25°C

Figure 10-12. Output Voltage versus Output Current



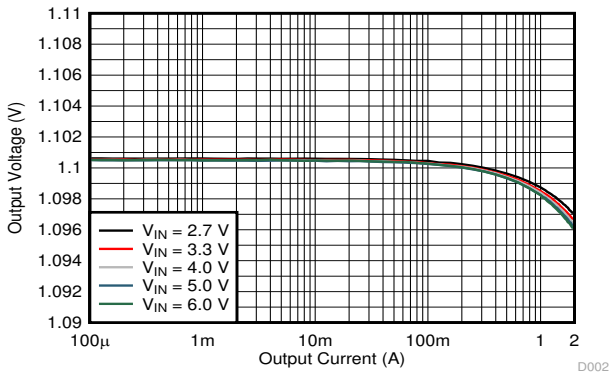
V_{OUT} = 1.8 V PWM T_A = 25°C

Figure 10-13. Output Voltage versus Output Current



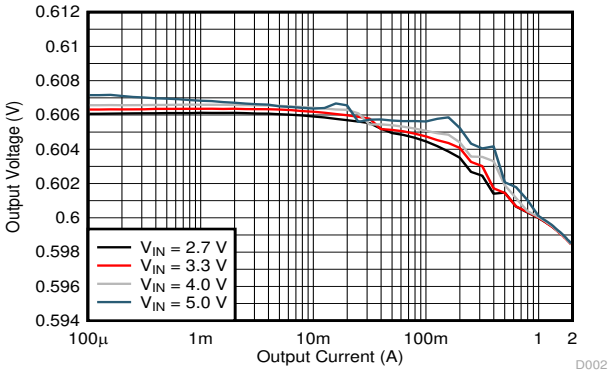
V_{OUT} = 1.1 V PFM T_A = 25°C

Figure 10-14. Output Voltage versus Output Current



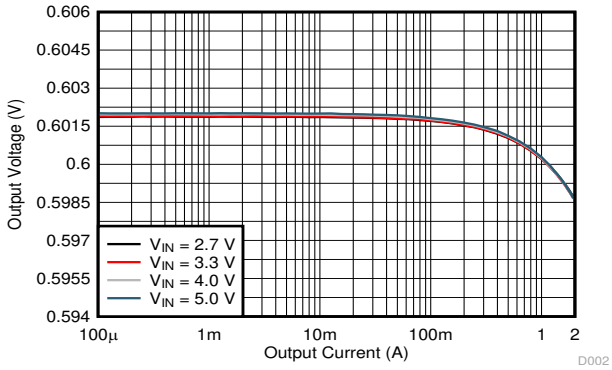
V_{OUT} = 1.1 V PWM T_A = 25°C

Figure 10-15. Output Voltage versus Output Current



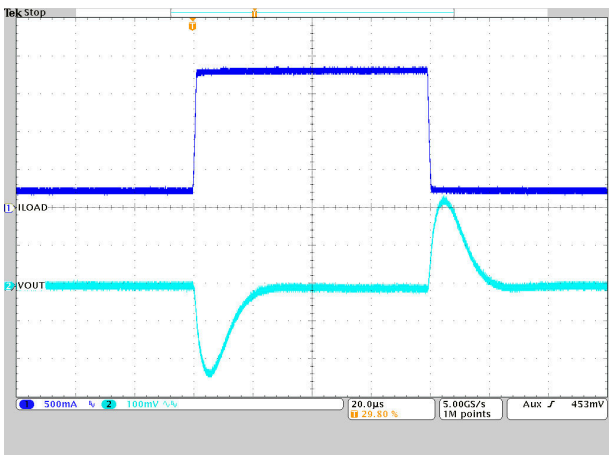
V_{OUT} = 0.6 V PFM T_A = 25°C

Figure 10-16. Output Voltage versus Output Current



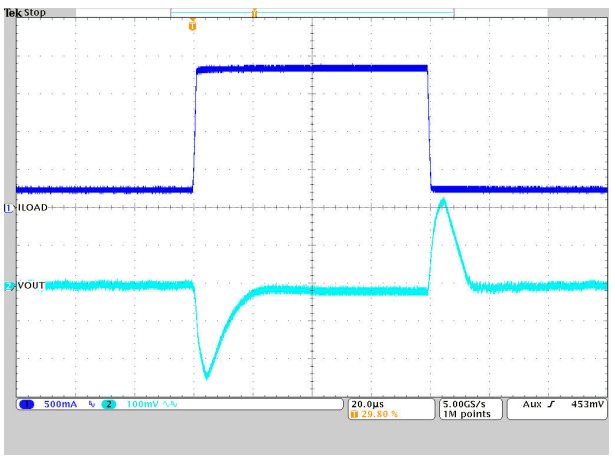
V_{OUT} = 0.6 V PWM T_A = 25°C

Figure 10-17. Output Voltage versus Output Current



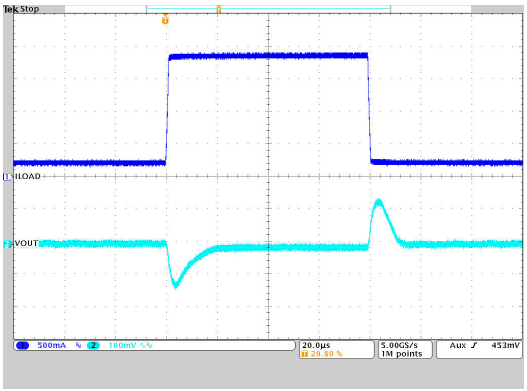
V_{OUT} = 3.3 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-18. Load Transient Response



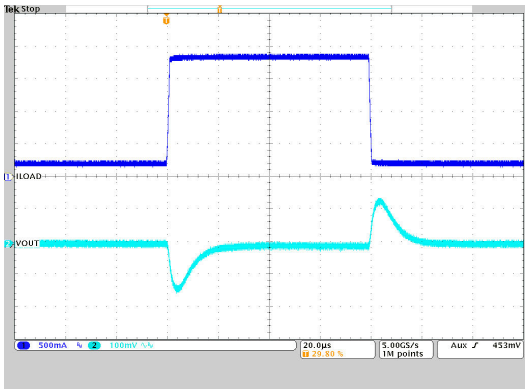
V_{OUT} = 3.3 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-19. Load Transient Response



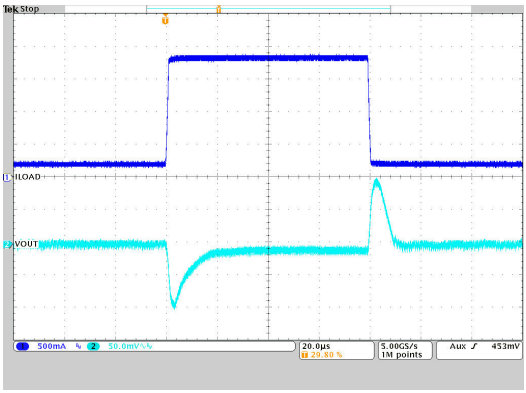
V_{OUT} = 1.8 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-20. Load Transient Response



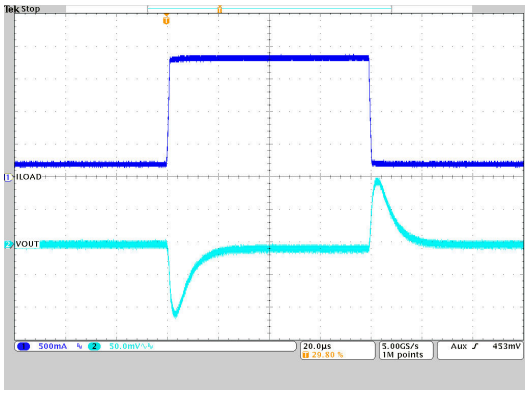
V_{OUT} = 1.8 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-21. Load Transient Response



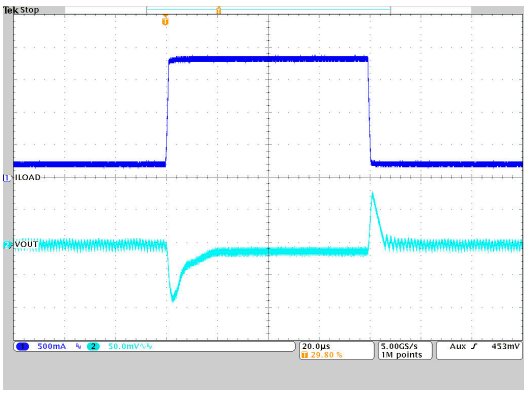
V_{OUT} = 1.2 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-22. Load Transient Response



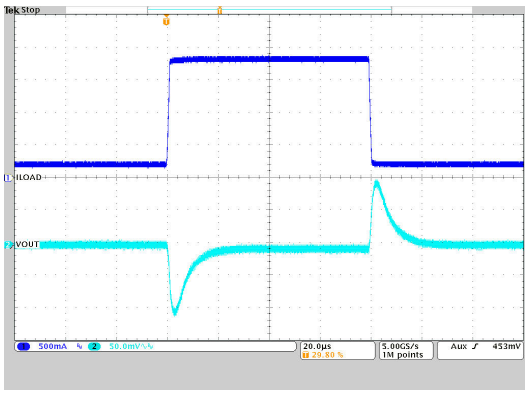
V_{OUT} = 1.2 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-23. Load Transient Response



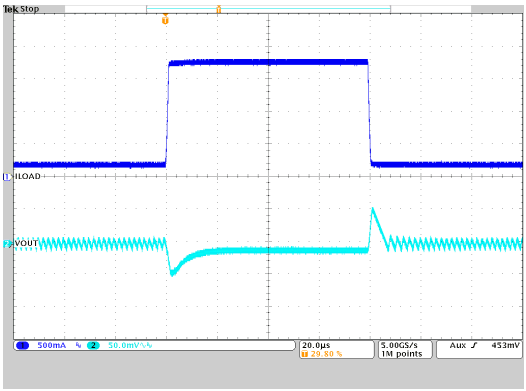
V_{OUT} = 1.0 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-24. Load Transient Response



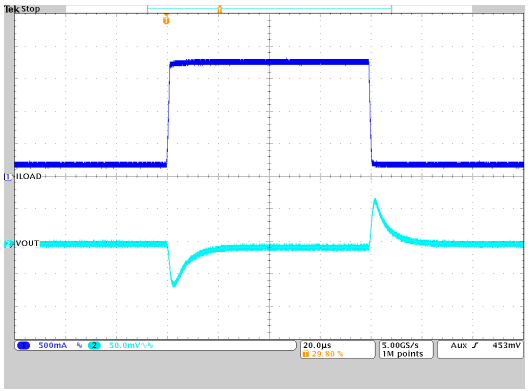
V_{OUT} = 1.0 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-25. Load Transient Response



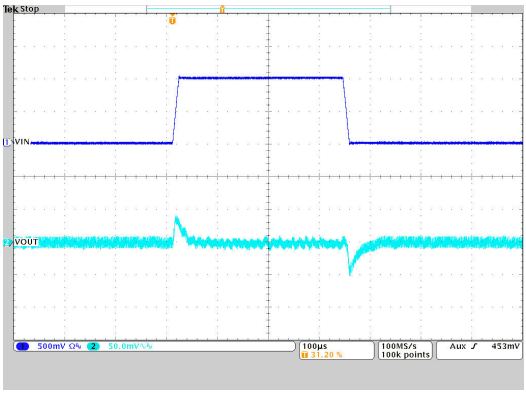
V_{OUT} = 0.6 V PFM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-26. Load Transient Response



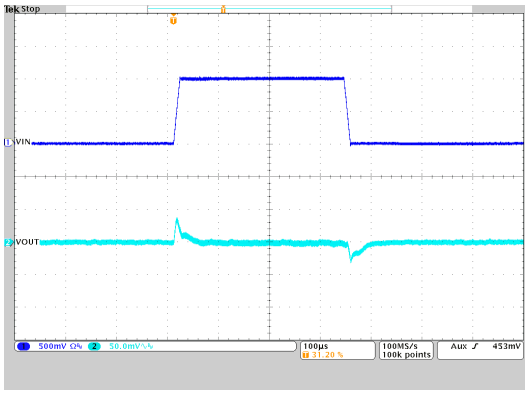
V_{OUT} = 0.6 V PWM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-27. Load Transient Response



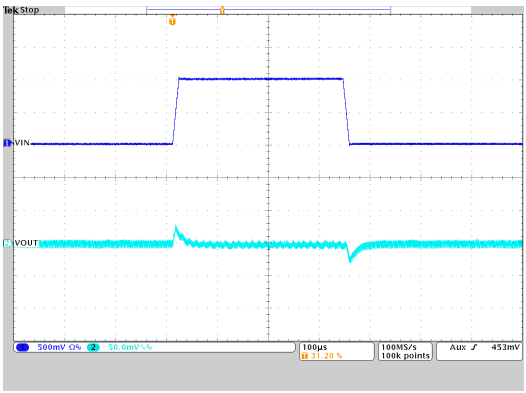
V_{OUT} = 3.3 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-28. Line Transient Response



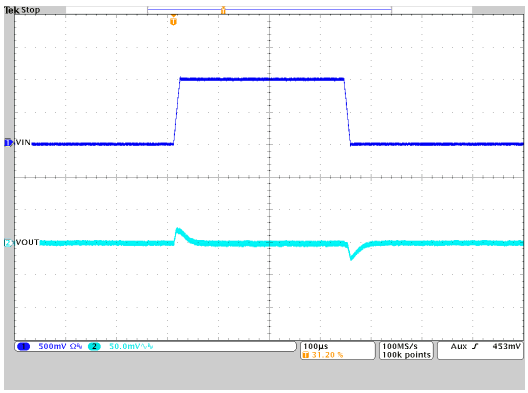
V_{OUT} = 3.3 V PWM T_A = 25°C
I_{OUT} = 2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-29. Line Transient Response



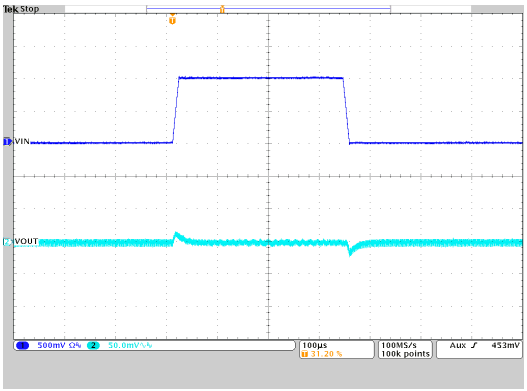
V_{OUT} = 1.8 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-30. Line Transient Response



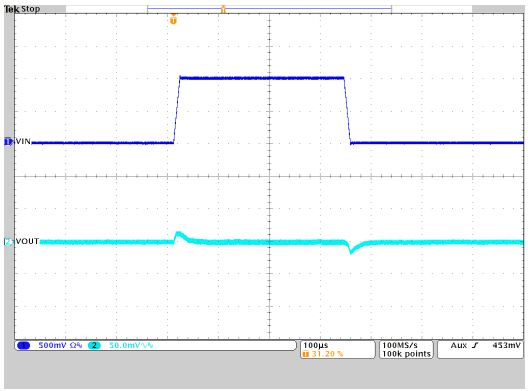
V_{OUT} = 1.8 V PWM T_A = 25°C
I_{OUT} = 2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-31. Line Transient Response



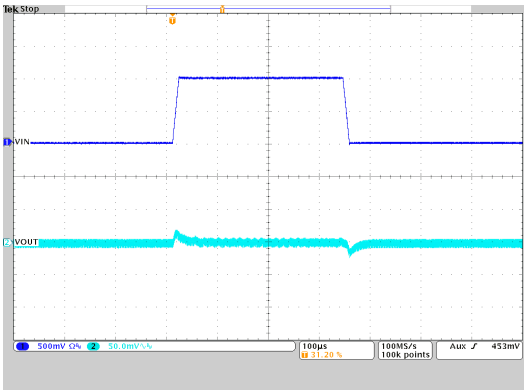
V_{OUT} = 1.2 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-32. Line Transient Response



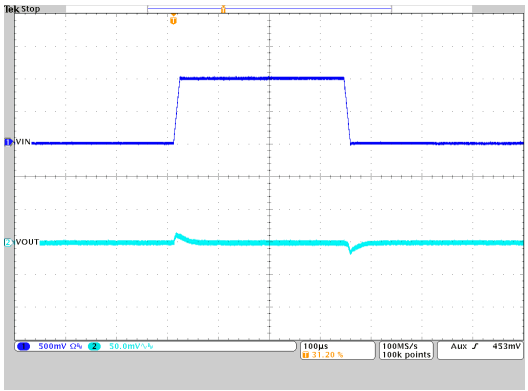
V_{OUT} = 1.2 V PWM T_A = 25°C
I_{OUT} = 2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-33. Line Transient Response



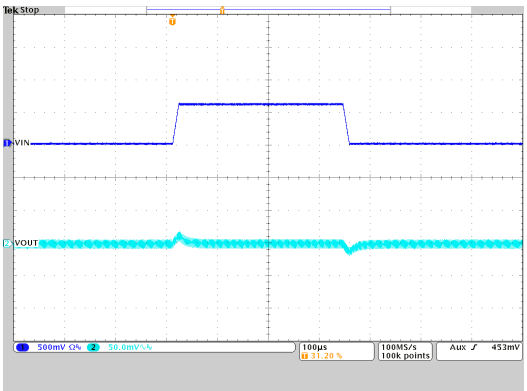
V_{OUT} = 1.0 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-34. Line Transient Response



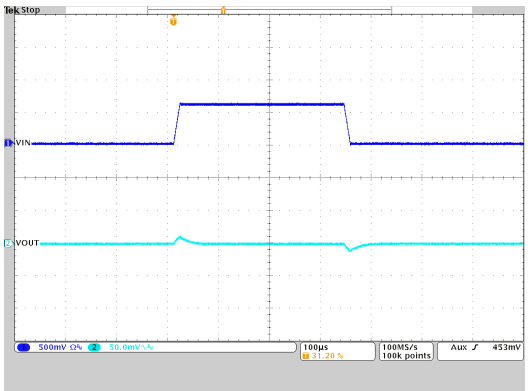
V_{OUT} = 1.0 V PWM T_A = 25°C
I_{OUT} = 2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-35. Line Transient Response



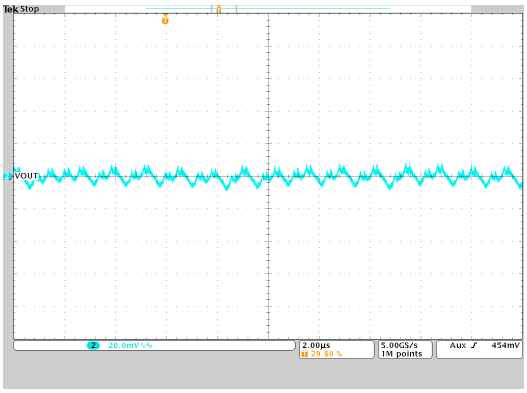
V_{OUT} = 0.6 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 3.0 V to 3.6 V to 3.0 V

Figure 10-36. Line Transient Response



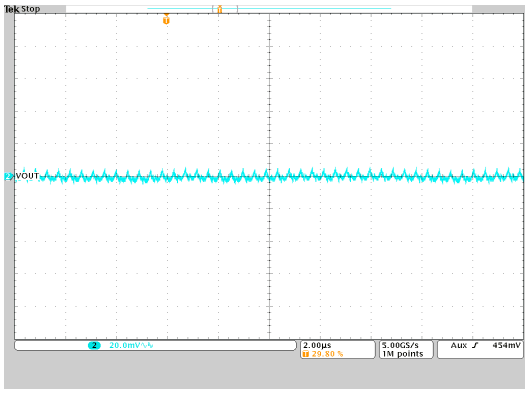
V_{OUT} = 0.6 V PWM T_A = 25°C
I_{OUT} = 2 A V_{IN} = 3.0 V to 3.6 V to 3.0 V

Figure 10-37. Line Transient Response



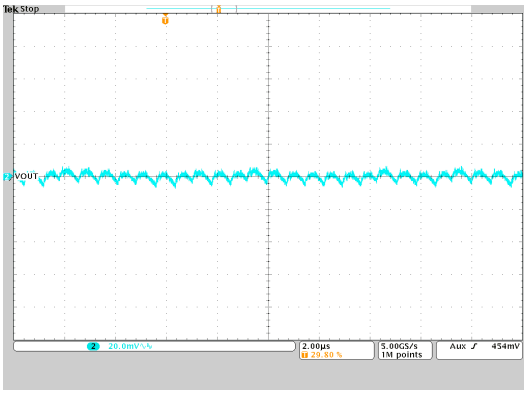
V_{OUT} = 3.3 V PFM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 0.2 A

Figure 10-38. Output Voltage Ripple



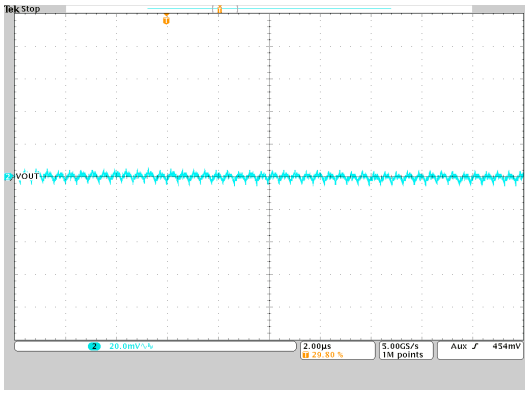
V_{OUT} = 3.3 V PWM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 2 A

Figure 10-39. Output Voltage Ripple



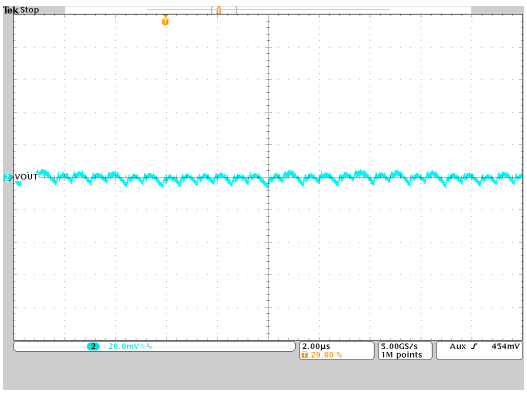
V_{OUT} = 1.8 V PFM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 0.2 A

Figure 10-40. Output Voltage Ripple



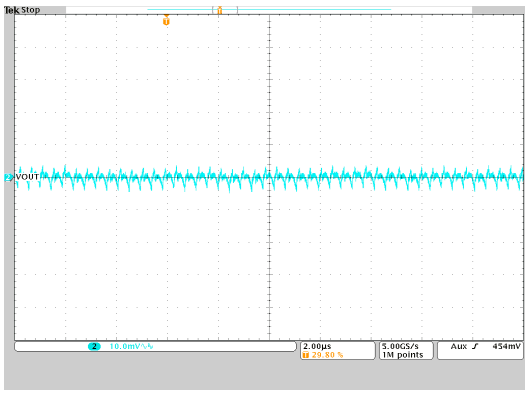
V_{OUT} = 1.8 V PWM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 2 A

Figure 10-41. Output Voltage Ripple



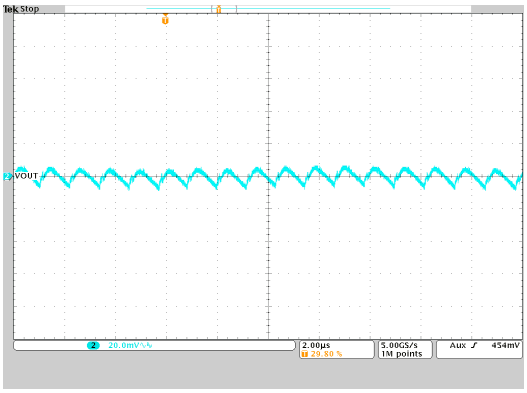
V_{OUT} = 1.2 V PFM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 0.2 A

Figure 10-42. Output Voltage Ripple



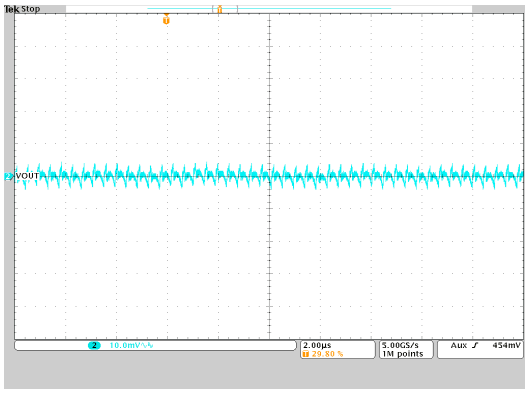
V_{OUT} = 1.2 V PWM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 2 A

Figure 10-43. Output Voltage Ripple



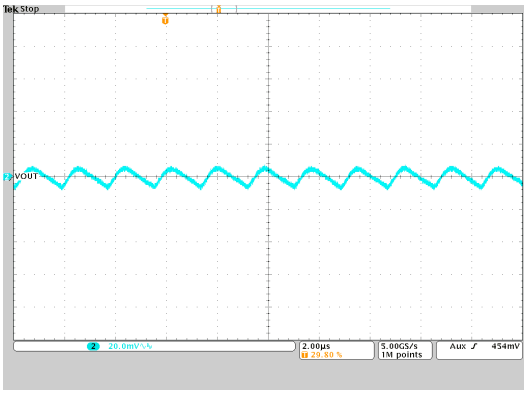
V_{OUT} = 1.0 V PFM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 0.2 A

Figure 10-44. Output Voltage Ripple



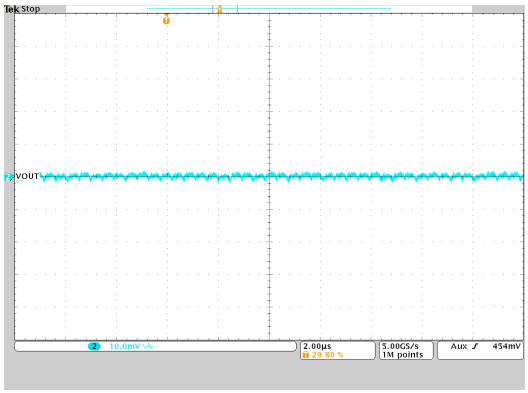
V_{OUT} = 1.0 V PWM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 2 A

Figure 10-45. Output Voltage Ripple



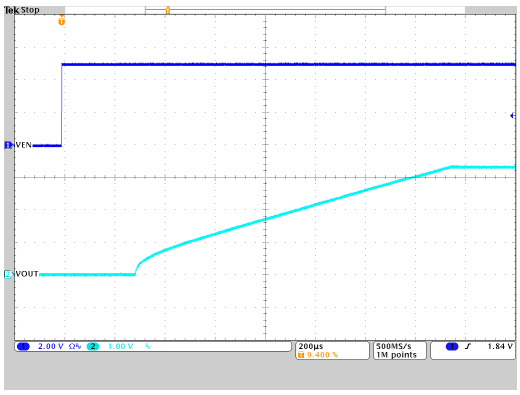
V_{OUT} = 0.6 V PFM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.2 A

Figure 10-46. Output Voltage Ripple



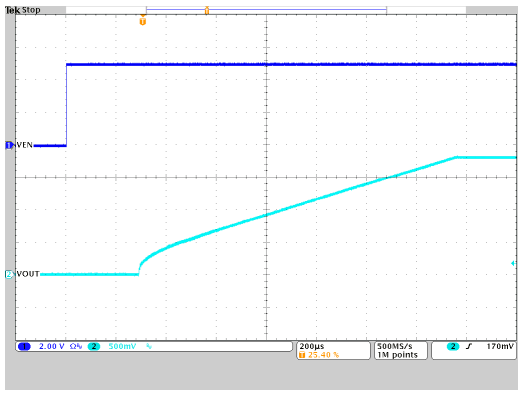
V_{OUT} = 0.6 V PWM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 2 A

Figure 10-47. Output Voltage Ripple



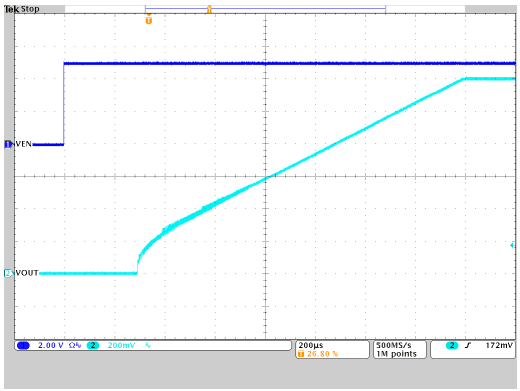
V_{OUT} = 3.3 V PWM or PFM T_A = 25°C
V_{IN} = 5 V C_{SS} = 4.7 nF I_{OUT} = 2 A

Figure 10-48. Start-Up Timing



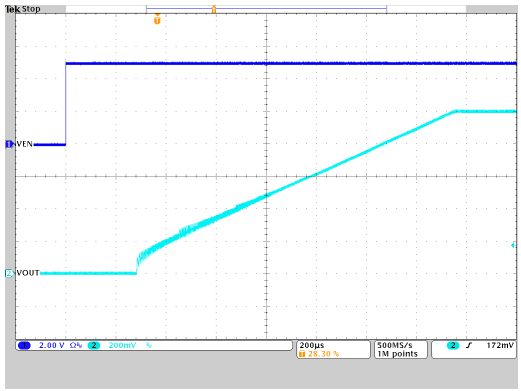
V_{OUT} = 1.8 V PWM or PFM T_A = 25°C
V_{IN} = 5 V C_{SS} = 4.7 nF I_{OUT} = 2 A

Figure 10-49. Start-Up Timing



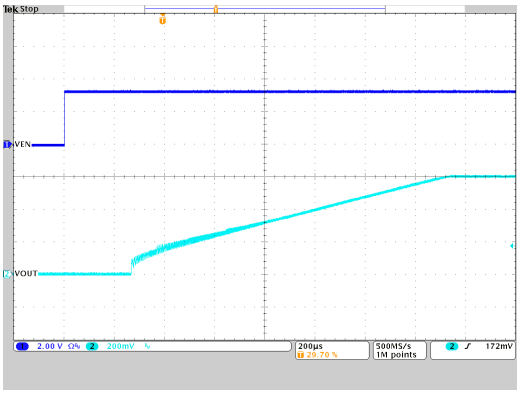
V_{OUT} = 1.2 V PWM or PFM T_A = 25°C
V_{IN} = 5 V C_{SS} = 4.7 nF I_{OUT} = 2 A

Figure 10-50. Start-Up Timing



V_{OUT} = 1.0 V PWM or PFM T_A = 25°C
V_{IN} = 5 V C_{SS} = 4.7 nF I_{OUT} = 2 A

Figure 10-51. Start-Up Timing



V_{OUT} = 0.6 V PWM or PFM T_A = 25°C
V_{IN} = 3.3 V C_{SS} = 4.7 nF I_{OUT} = 2 A

Figure 10-52. Start-Up Timing

10.3 System Examples

10.3.1 Fixed Output Voltage Versions

Versions with an internally fixed output voltage allow you to remove the external feedback voltage divider. This not only allows you to reduce the total solution size but also provides higher accuracy as there is no additional error caused by the external resistor divider. The FB pin needs to be tied to the output voltage directly as shown in Figure 10-53. The application runs with an internally defined switching frequency of 2.25 MHz by connecting COMP/FSET to GND.

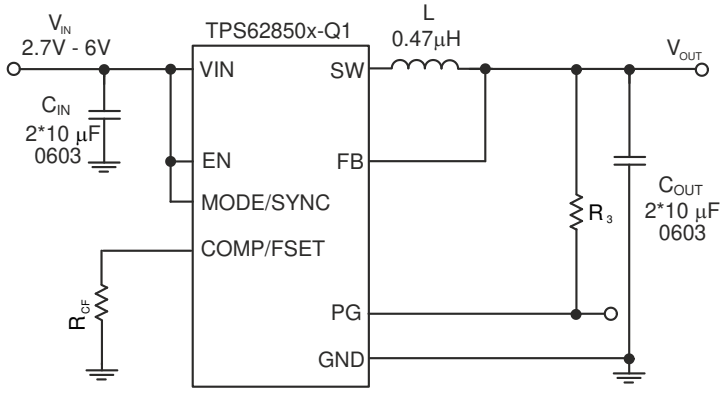


Figure 10-53. Schematic for Fixed Output Voltage Versions

10.3.2 Synchronizing to an External Clock

The TPS62850x-Q1 can be externally synchronized by applying an external clock on the MODE/SYNC pin. There is no need for any additional circuitry as long as the input signal meets the requirements given in the electrical specifications. The clock can be applied / removed during operation, allowing you to switch from an externally defined fixed frequency to power-save mode or to internal fixed frequency operation.

The value of the R_{CF} resistor must be chosen such that the internally defined frequency and the externally applied frequency are close to each other. This ensures a smooth transition from internal to external frequency and vice versa.

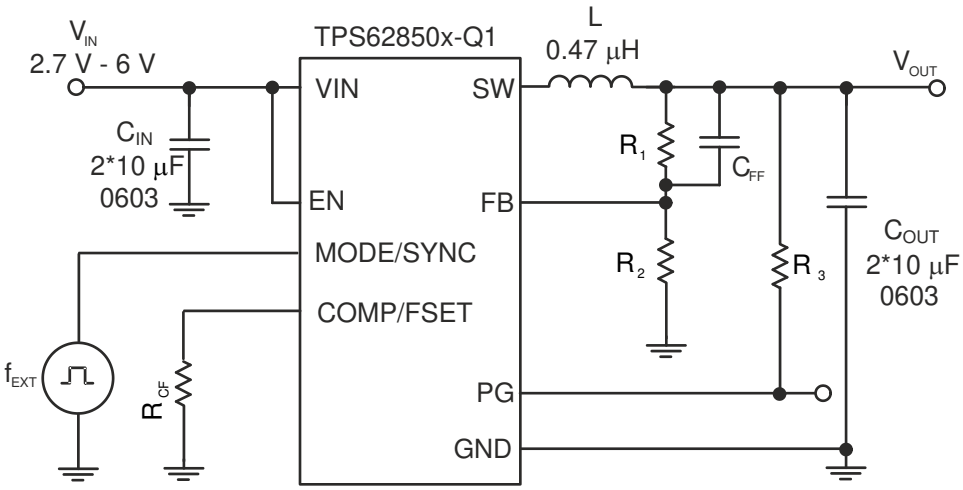
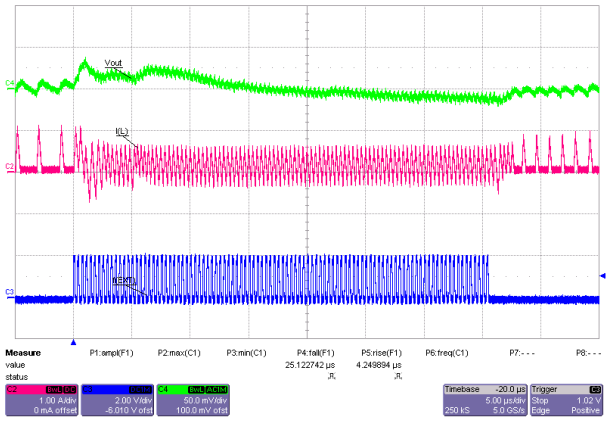
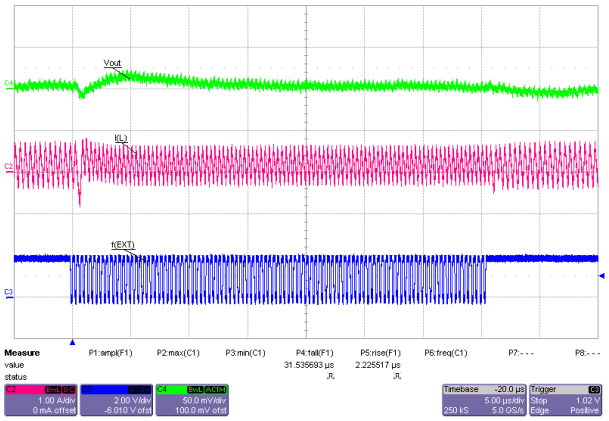


Figure 10-54. Schematic using External Synchronization



V_{IN} = 5 V R_{CF} = 8.06 kΩ I_{OUT} = 0.1 A
V_{OUT} = 1.8 V f_{EXT} = 2.5 MHz

Figure 10-55. Switching from External Syncronization to Power-Save Mode (PFM)



V_{IN} = 5 V R_{CF} = 8.06 kΩ I_{OUT} = 0.1 A
V_{OUT} = 1.8 V f_{EXT} = 2.5 MHz

Figure 10-56. Switching from External Synchronizaion to Internal Fixed Frequency

11 Power Supply Recommendations

The TPS62850x-Q1 device family does not have special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPS62850x-Q1.

12 Layout

12.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS62850x-Q1 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both in *Section 12.2* and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

See for the recommended layout of the TPS62850x-Q1, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances and narrow traces must be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB need to be connected with short wires and not nearby high dv/dt signals (for example, SW). As they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The FB resistors, R_1 and R_2, must be kept close to the IC and be connected directly to the pin and the system ground plane.

The package uses the pins for power dissipation. Thermal vias on the VIN and GND pins help to spread the heat into the pcb.

The recommended layout is implemented on the EVM and shown in the *TPS628502EVM-092 Evaluation Module User's Guide*.

12.2 Layout Example

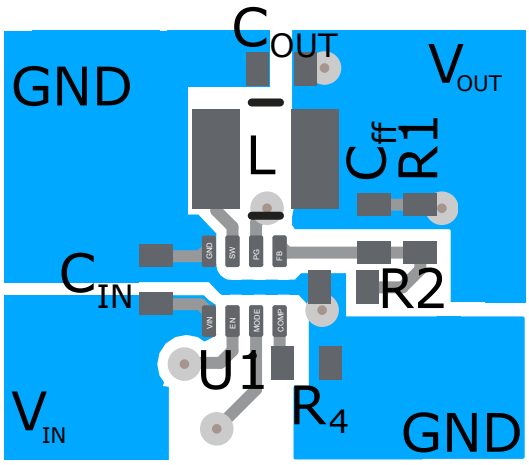


Figure 12-1. Example Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS6285010MQDRLRQ1	PREVIEW	SOT-5X3	DRL	8	4000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		
TPS628501QDRLRQ1	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 125	100Q	Samples
TPS6285020MQDRLRQ1	PREVIEW	SOT-5X3	DRL	8	4000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125	20MQ	
TPS628502QDRLRQ1	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 125	200Q	Samples
XPS628501QDRLRQ1	ACTIVE	SOT-5X3	DRL	8	4000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples
XPS628502QDRLRQ1	ACTIVE	SOT-5X3	DRL	8	4000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

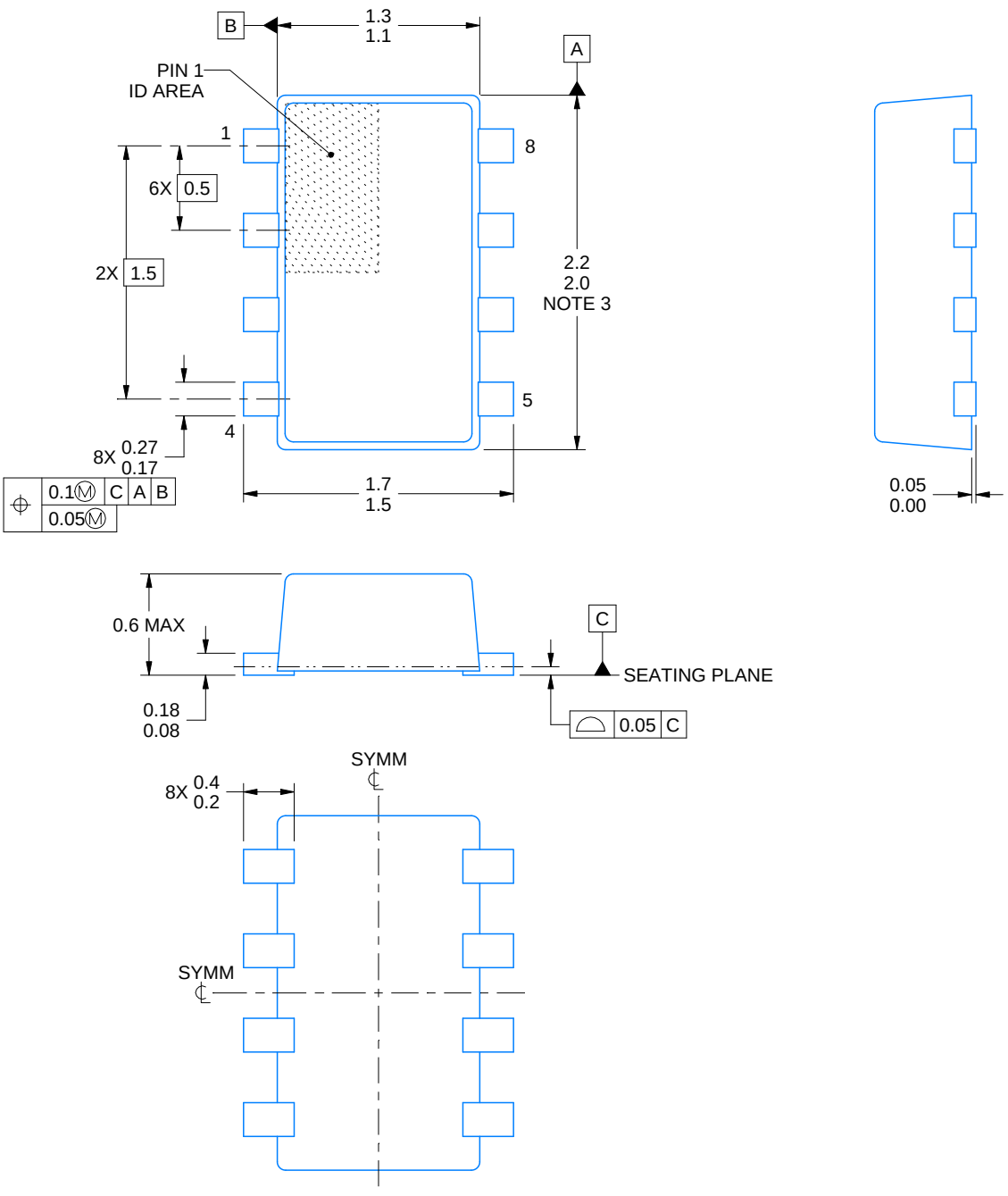
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

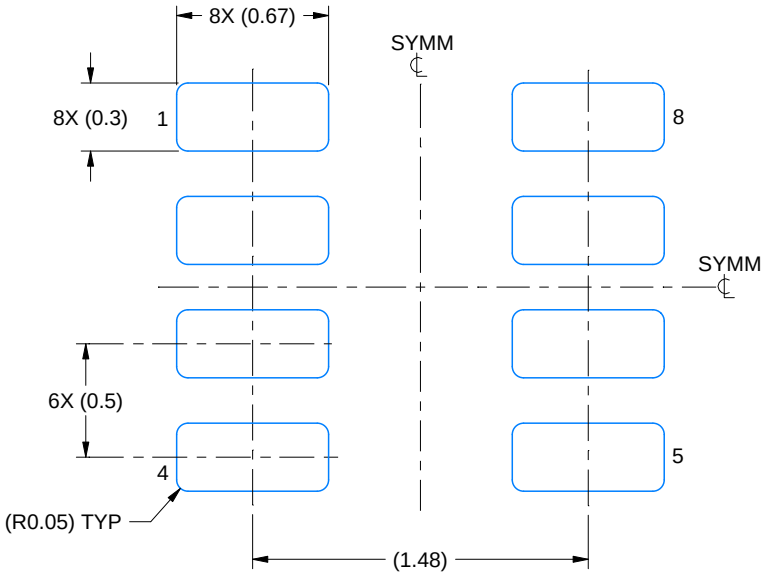
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration TO-236, except minimum foot length.

EXAMPLE BOARD LAYOUT

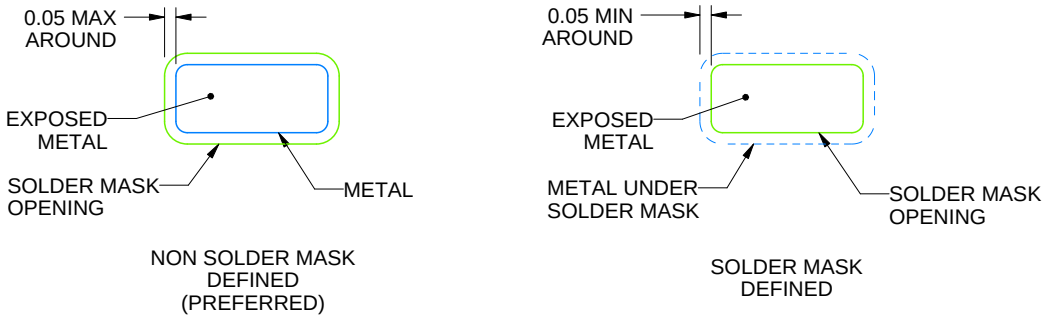
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

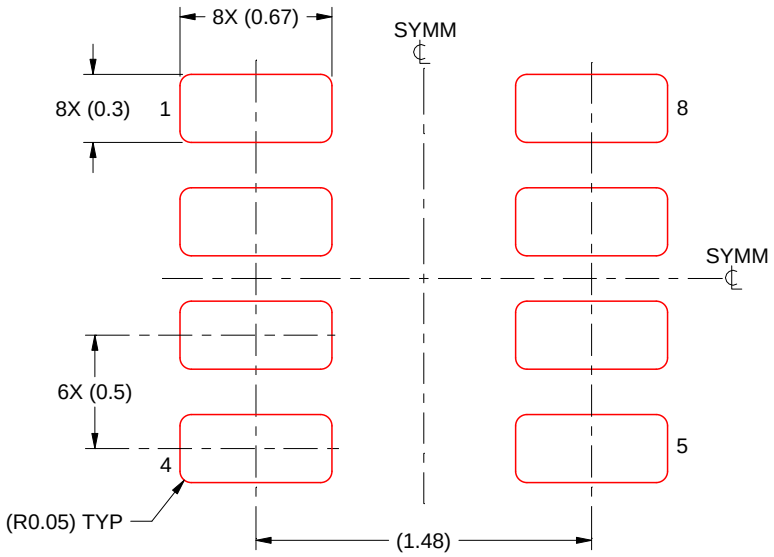
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/B 03/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265