

TPS53014 4.5V 至 28V 输入、D-CAP2™ 同步降压控制器

1 特性

- D-CAP2™ 模式控制
 - 快速瞬态响应
 - 无需外部组件即可实现环路补偿
 - 与陶瓷输出电容器兼容
- 高初始基准精度 ($\pm 1\%$)
- 宽输入电压范围: 4.5V 至 28V
- 输出电压范围: 0.77V 至 7.0V
- 低侧 $R_{DS(on)}$ 无损耗电流感应
- 可调节软启动
- 非灌电流预偏置软启动
- 500kHz 开关频率
- 逐周期过流限制控制
- 用于在轻载时保持高效率的自动跳过 Eco-Mode™
- 过流限制 (OCL) / 过压 (OVP) / 欠压 (UVP) / 欠压闭锁 (UVLO) / 热关断 (TSD) 保护
- 自适应栅极驱动器, 带集成式升压 P 通道场效应晶体管 (PMOS) 开关
- 热补偿 OCP, 4000 ppm/°C
- 10 引脚超小型小外形尺寸封装 (VSSOP)

2 应用

- 用于多种应用的低功率系统负载点 调节
 - 数字电视电源
 - 网络家庭终端设备
 - 数字机顶盒 (STB)
 - DVD 播放器 / 录像机
 - 游戏机和其他

3 说明

TPS53014 是一款单一、自使用启动时间 D-CAP2™ 模式同步降压控制器。TPS53014 可帮助系统设计人员通过一个低成本、低组件数的低待机电流解决方案来完成各种终端设备的电源总线调节器集。TPS53014 的主控制环路使用 D-CAP2 模式控制, 此控制方式无需外部补偿组件即可实现快速瞬态响应。自使用接通时间支持较高负载条件下 PWM 模式与 Eco-mode™ 运行间的无缝转换。Eco-mode 使 TPS53014 能够在较轻负载状况下保持高效率。TPS53014 也能够适应超低 ESR 陶瓷电容器和低等效串联电阻 (ESR) 输出电容器, 例如 POSCAP 或 SP-CAP。此器件在 4.5V 至 28V 的输入电压和 0.77V 至 7V 的输出电压下提供便捷和高效运行。

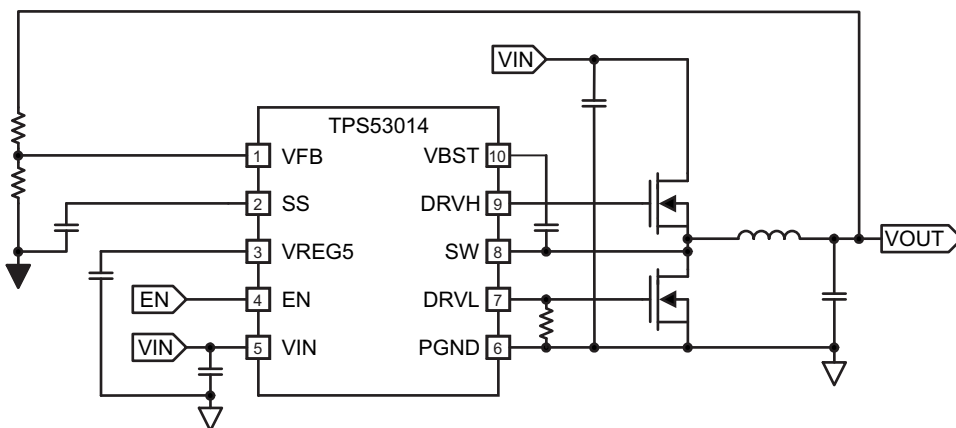
TPS53014 采用 3mm × 3mm 10 引脚 VSSOP (DGS) 封装, 额定环境温度范围为 -40°C 至 +85°C。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS53014	DGS (10)	3.00mm × 3.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

典型应用



目录

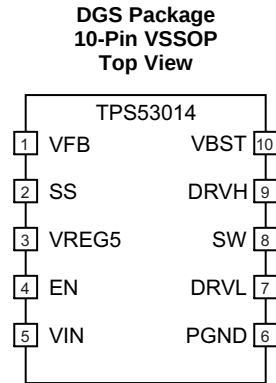
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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2012) to Revision A	Page
• 仅有编辑更改；无技术性更改；为当前内容更新了当前 TI 数据表标准	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	VSSOP-10		
VFB	1	I	D-CAP2 feedback input. Connect to output voltage with resistor divider.
SS	2	O	Soft start programming pin. Connect capacitor from SS pin to GND to program soft start time.
VREG5	3	O	Output of 5-V linear regulator and supply for MOSFET driver. Bypass to GND with a minimum 4.7- μ F high quality ceramic capacitor. VREG5 is active when EN is asserted high.
EN	4	I	Enable. Pull High to enable converter.
VIN	5	I	Supply Input for 5-V linear regulator. Bypass to GND with a minimum 0.1- μ F high quality ceramic capacitor.
PGND	6	I	System ground.
DRVL	7	O	Low-side N-Channel MOSFET gate driver output. PGND referenced driver switches between PGND(OFF) and VREG5(ON).
SW	8	I/O	Switch node connections for both the high-side driver and over current comparator.
DRVH	9	O	High-side N-channel MOSFET gate driver output. SW referenced driver switches between SW(OFF) and VBST(ON).
VBST	10	I	High-side MOSFET gate driver bootstrap voltage input. Connect a capacitor from VBST to SW. An internal diode is connected between VREG5 and VBST

6 Specifications

6.1 Absolute Maximum Ratings

Operating under free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT
Input voltage range	VIN, EN	–0.3 to 30	V
	VBST	–0.3 to 36	
	VBST - SW	–0.3 to 6	
	VFB	–0.3 to 6	
	SW	–0.3 to 30	
	SW (10 nsec transient)	–3.0 to 30	
Output voltage range	DRVH	–2 to 36	V
	DRVH - SW	–0.3 to 6	
	DRVL, VREG5, SS	–0.3 to 6	
	PGND	–0.3 to 0.3	
T _A	Operating ambient temperature range	–40 to 85	°C
T _{STG}	Storage temperature range	–55 to 150	°C
T _J	Junction temperature range	–40 to 150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply input voltage range	VIN	4.5	28	V
Input voltage range	VBST	–0.1	33.5	V
	VBST - SW	–0.1	5.5	
	VFB	–0.1	5.5	
	EN	–0.1	28	
	SW	–1.0	28	
	PGND	–0.1	0.1	
Output Voltage range	DRVH	–1.0	33.5	V
	DRVH - SW	–0.1	5.5	
	DRVL, VREG5, SS	–0.1	5.5	
	PGND	–0.1	0.1	
T _A	Operating free-air temperature	–40	85	°C
T _J	Operating junction temperature	–40	125	°C

6.3 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS53014	UNITS
		DGS (10 PINS)	
θ _{JA}	Junction-to-ambient thermal resistance	172.2	°C/W
θ _{JCTop}	Junction-to-case (top) thermal resistance	44.0	°C/W
θ _{JB}	Junction-to-board thermal resistance	93.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	91.4	°C/W
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) 有关传统和新热指标的更多信息，请参见应用报告《半导体和 IC 封装热指标》（文献编号：SPRA953）。

6.4 Electrical Characteristics

over recommended free-air temperature range, $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{IN}	VIN Supply current	VIN current, T _A = 25°C, EN = 5V, V _{VFB} = 0.8V, V _{SW} = 0 V	660			μA
I _{VINSDN}	VIN Shutdown current	VIN current, T _A = 25°C, No Load , V _{EN} = 0V, VREG5 = OFF	6.0			μA
VFB VOLTAGE and DISCHARGE RESISTANCE						
V _{VFBTHL}	VFB Threshold voltage	T _A = 25°C , V _{OUT} = 1.05 V	765.3	773.0	780.7	mV
TC _{VFB}	VFB Temperature coefficient	Relative to T _A = 25°C ⁽¹⁾	-140		140	ppm/°C
I _{VFB}	VFB Input current	VFB = 0.8V, T _A = 25°C	-150	-10	100	nA
VREG5 OUTPUT						
V _{VREG5}	VREG5 Output voltage	T _A =25°C, 6 V < V _{IN} < 28 V, I _{VREG5} = 5 mA	5.1			V
I _{VREG5}	Output current	VIN = 5.5V, V _{VREG5} = 4.0V, T _A = 25°C	120			mA
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
R _{DRVH}	DRVH resistance	Source, I _{DRVH} = –50mA, T _A = 25°C	3.2			Ω
		Sink, I _{DRVH} = 50mA, T _A = 25°C	1.4			
R _{DRVL}	DRVL resistance	Source, I _{DRVL} = –50mA, T _A = 25°C	6.9			Ω
		Sink, I _{DRVL} = 50mA, T _A = 25°C	0.8			
T _D	Dead time	DRVH-low to DRVL-on ⁽¹⁾	15			ns
		DRVL-low to DRVH-on ⁽¹⁾	20			
INTERNAL BOOST DIODE						
V _{FBST}	Forward voltage	V _{VREG5-VBST} , I _F = 10mA, T _A = 25°C	0.1			V
SOFT START						
I _{SSC}	SS Charge current	VSS = 0V , T _A = 25°C	-7.36	-6.4	-5.44	μA
I _{SSd}	SS Discharge current	VSS = 0.5V , T _A = 25°C	4.5	5.0		mA
TC _{ISSC}	I _{SSC} Temperature coefficient	Relative to T _A = 25°C	-4.5		4.5	nA/°C
UVLO						
V _{UVVREG5}	VREG5 UVLO threshold	VREG5 Rising	4.0			V
		Hysteresis	0.3			
LOGIC THRESHOLD						
V _{ENH}	EN H-level threshold voltage		1.6			V
V _{ENL}	EN L-level threshold voltage				0.5	V
R _{EN}	EN pin resistance to GND	V _{EN} = 12 V	225	450	900	kΩ
CURRENT SENSE						
I _{TRIP}	TRIP Source current	V _{DRVL} = 0.1V, T _A = 25°C	14.3	15	15.8	μA
TC _{VTRIP}	V _{TRIP} Temperature coefficient	Relative to T _A = 25°C	4000			ppm/°C
V _{OCL}	Current limit threshold	R _{TRIP} = 75kΩ, T _A = 25°C	234	336	424	mV
		R _{TRIP} = 27kΩ, T _A = 25°C	121	174	220	
		R _{TRIP} = 6.8kΩ, T _A = 25°C	35	50	63	
ON-TIME TIMER CONTROL						
T _{ON}	On time	V _{OUT} = 1.05 V ⁽¹⁾	250			ns
T _{OFF(MIN)}	Minimum off time	V _{IN} = 4.5 V, V _{VFB} = 0.7 V, T _A = 25°C	230			ns

(1) Ensured by design. Not production tested.

Electrical Characteristics (接下页)

over recommended free-air temperature range, $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect voltage	115%	120%	125%	
T_{OVPDEL}	Output OVP propagation delay				10	μs
V_{UVP}	Output UVP trip threshold	UVP detect voltage	63%	68%	73%	
T_{UVPDEL}	Output UVP delay			1		ms
T_{UVPEN}	Output UVP enable delay	UVP enable delay / soft start time	X1.4	X1.7	X2.0	
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature ⁽¹⁾		150		$^{\circ}\text{C}$
		Hysteresis ⁽¹⁾		25		

6.5 Typical Characteristics

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

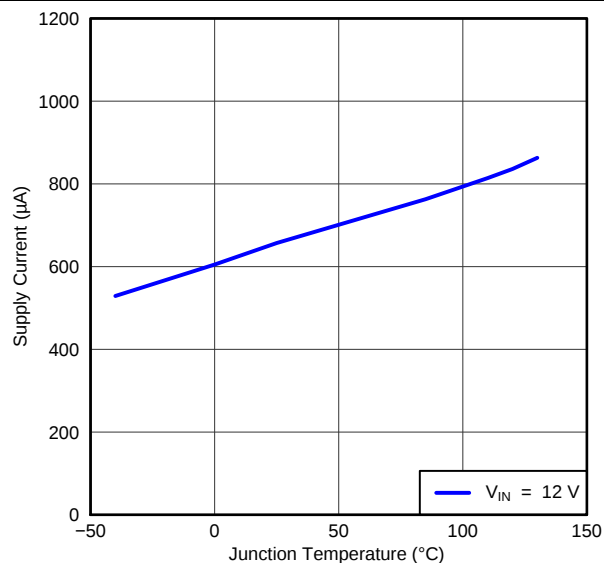


图 1. VIN Supply Current vs Junction Temperature

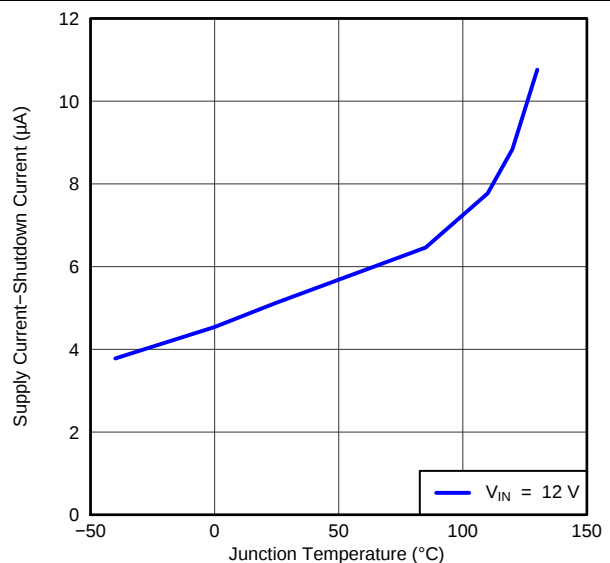


图 2. VIN Shutdown Current vs Junction Temperature

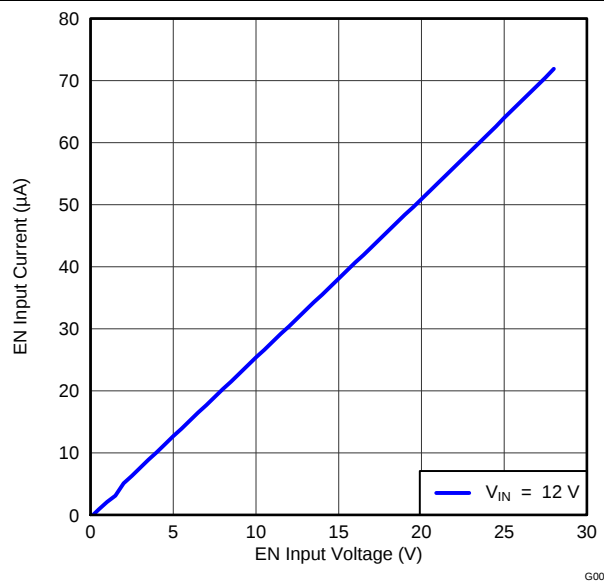


图 3. En Input Current Vs En Input Voltage

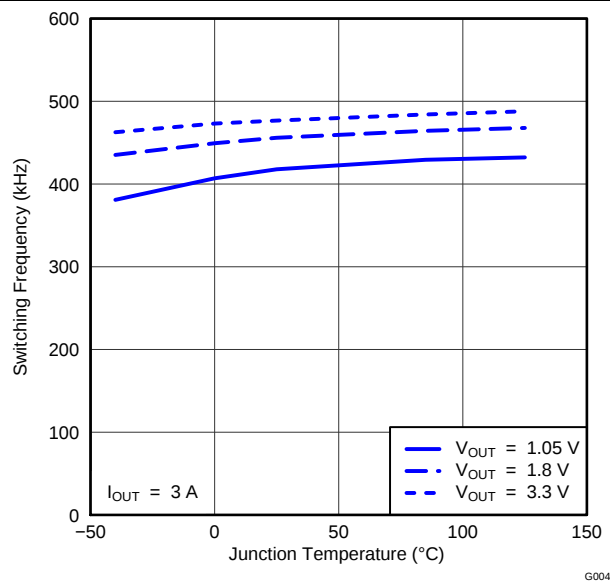
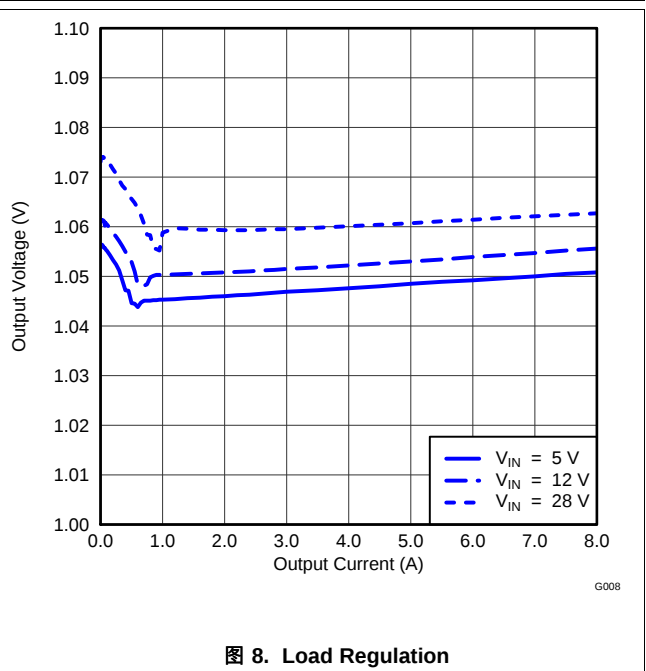
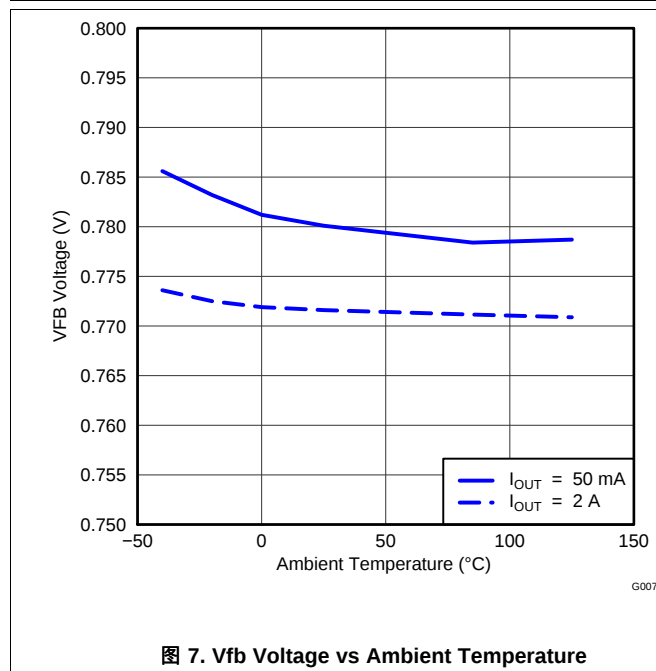
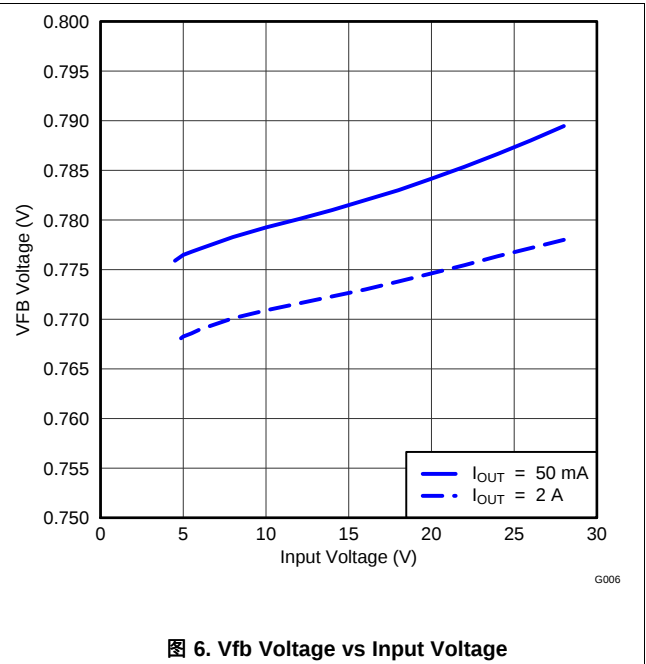
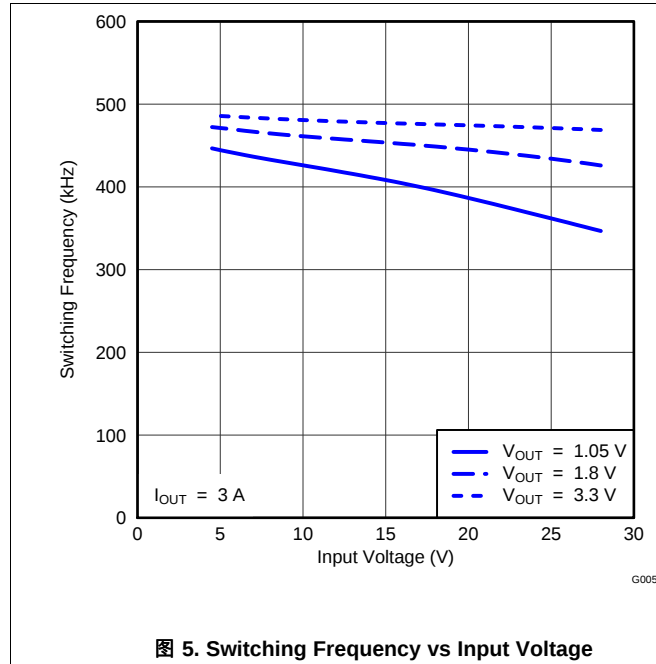


图 4. Switching Frequency vs Junction Temperature

Typical Characteristics (接下页)

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



Typical Characteristics (接下页)

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

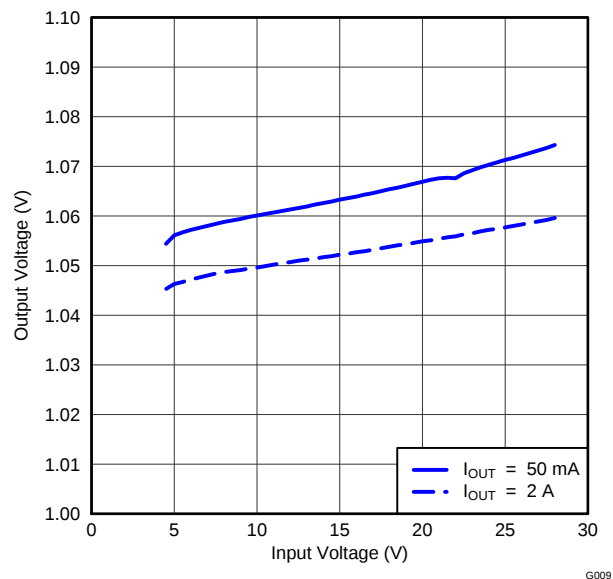


图 9. Line Regulation

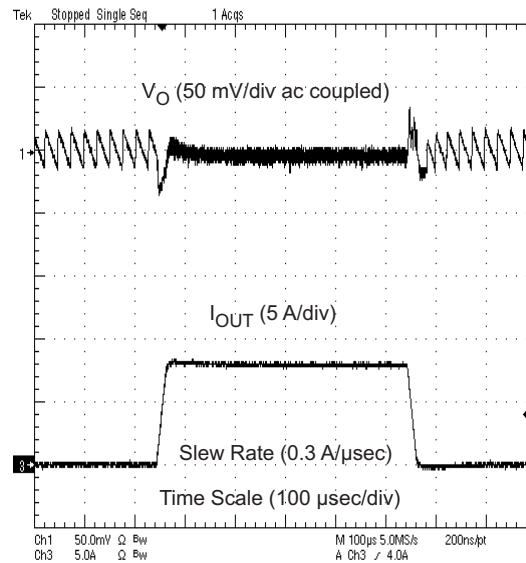


图 10. Transient Response

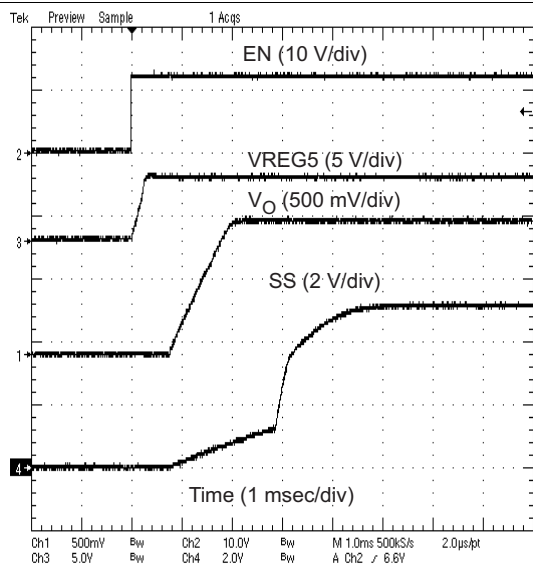


图 11. Start Up Waveforms

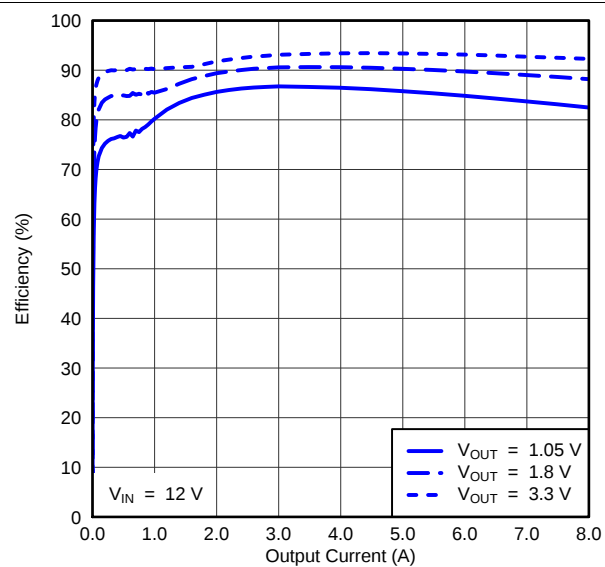


图 12. Efficiency

Typical Characteristics (接下页)

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

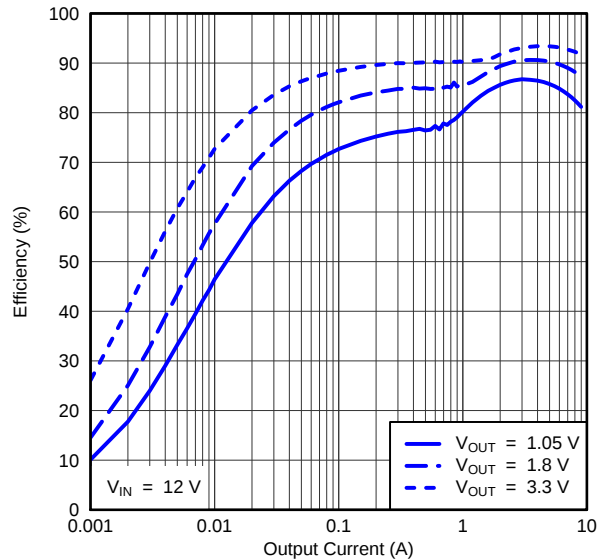


图 13. Light Load Efficiency

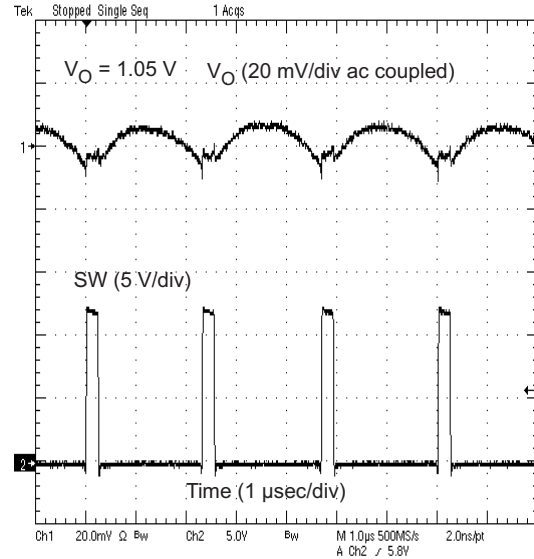


图 14. Output Voltage Ripple, $I_{OUT} = 8\text{ A}$

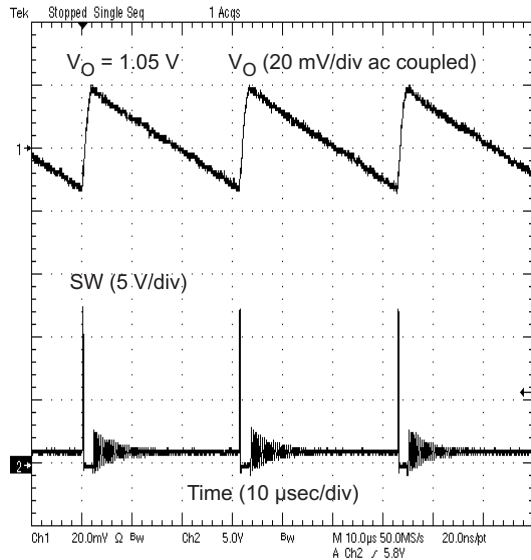


图 15. Output Voltage Ripple, $I_{OUT} = 50\text{ mA}$

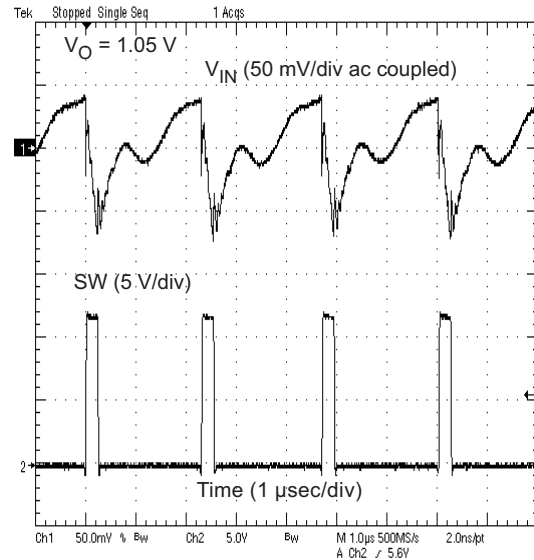


图 16. Input Voltage Ripple, $I_{OUT} = 8\text{ A}$

Typical Characteristics (接下页)

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

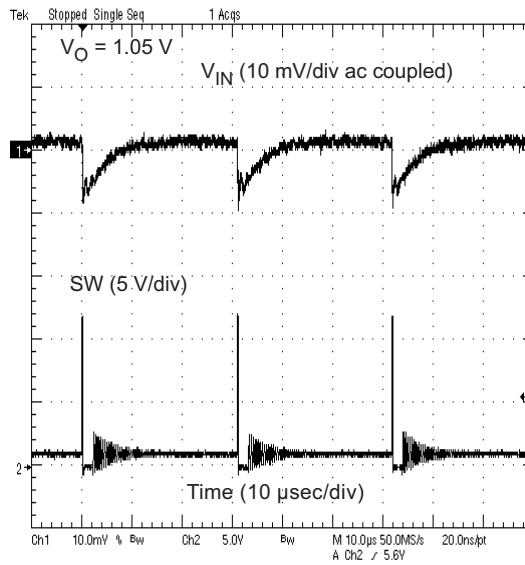


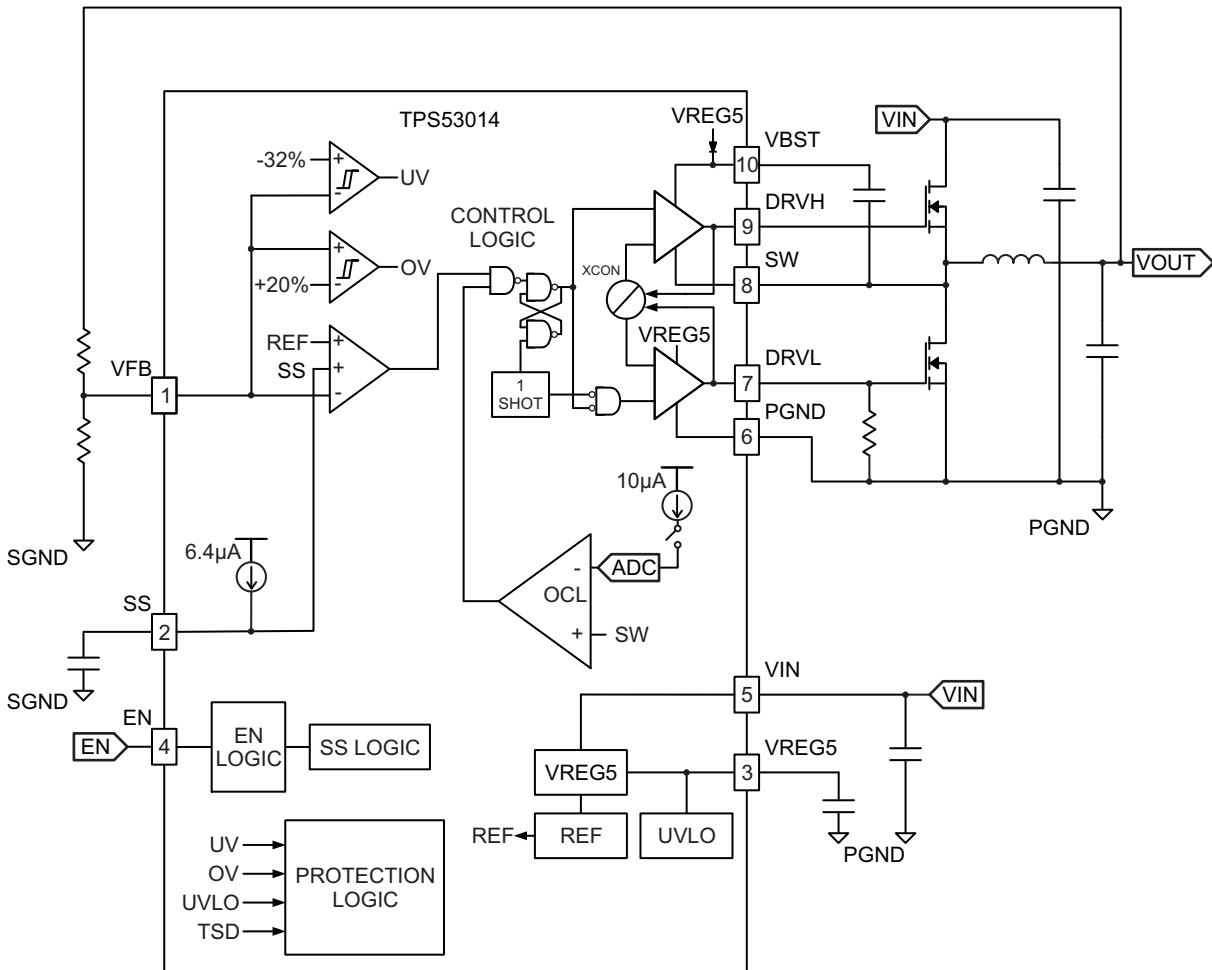
图 17. Input Voltage Ripple, $I_{OUT} = 50\text{ mA}$

7 Detailed Description

7.1 Overview

The TPS53014 is single synchronous step-down (buck) controller. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the required amount of output capacitance to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS53014 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ control mode. D-CAP2™ control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off when the internal timer expires. This timer is set by the converter input voltage VIN, and the output voltage VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the nominal output voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

Feature Description (接下页)

7.3.2 Auto-Skip Eco-Mode™ Control

The TPS53014 is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point where its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost half as is was in the continuous conduction mode because it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation IOX(LL) current can be calculated in 公式 1 with 500kHz used as fsw.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Drivers

TPS53014 contains two high-current resistive MOSFET gate drivers. The low-side driver is a PGND referenced, VREG5 powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET whose source is connected to PGND. The high-side driver is a floating SW referenced, VBST powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET. To maintain the VBST voltage during the high-side driver ON time, a capacitor is placed from SW to VBST. Each driver draws average current equal to Gate Charge (Q_g @ $V_{gs} = 5V$) times Switching frequency (fsw). To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFETs body diodes.

7.3.4 5-Volt Regulator

The TPS53014 has an internal 5V Low-Dropout (LDO) Regulator to provide a regulated voltage for all both drivers and the ICs internal logic. A high-quality 4.7μF or greater ceramic capacitor from VREG5 to GND is required to stabilize the internal regulator.

7.3.5 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6.4-μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in 公式 2. VFB voltage is 0.773 V and SS pin source current is 6.4-μA.

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{FB}(V)}{I_{SS}(\mu A)} = \frac{C_{SS}(nF) \times 0.773 V}{6.4\mu A} \quad (2)$$

The TPS53014 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than internal feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-biased output, and ensures that the output voltage (VO) starts and ramps up smoothly into regulation from pre-biased startup to normal mode operation.

7.3.6 Overcurrent Protection

TPS53014 has a cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET $R_{DS(on)}$ during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53014 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET $R_{DS(on)}$ current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, a resistor should be connected between DRV1 and PGND. The recommended values are given in 表 1.

表 1. OCL Resistor Values

RESISTER VALUE (kΩ)	V _{trip} (V)
6.8	0.050
11	0.087
18	0.125
27	0.174
39	0.224
56	0.274
75	0.336

I_{OCL} is determined by 公式 3.

$$I_{OCL} = \left(\frac{(V_{IN} - V_{OUT})}{2 \times L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \right) + \frac{V_{TRIP}}{R_{DS(ON)}} \quad (3)$$

The trip voltage is set between 0.05 V to 0.336 V over all operational temperature, including the 4000ppm/°C temperature slope compensation for the temperature dependency of the R_{DS(on)}. If the load current exceeds the overcurrent limit, the voltage will begin to drop. If the over-current conditions continues the output voltage will fall below the under voltage protection threshold and the TPS53014 will shut down.

7.3.7 Over/Undervoltage Protection

TPS53014 monitors a resistor divided feedback voltage to detect over and under voltage. If the feedback voltage is higher than 120% of the reference voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage is lower than 68% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, TPS53014 latches OFF both top and bottom MOSFET drivers. This function is enabled approximately 1.7 × T_{SS} after power-on. The OVP and UVP latch off is reset when EN goes low.

7.3.8 UVLO Protection

TPS53014 has under voltage lock out protection (UVLO) that monitors the voltage of VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the device is shut off. All output drivers are OFF. The UVLO is non-latch protection.

7.3.9 Thermal Shutdown

TPS53014 monitors its temperature. If the temperature exceeds the threshold value (typically 150°C), the device shuts off. When the temperature falls below the threshold, the IC starts again. When VIN starts up and VREG5 output voltage is below its nominal value, the thermal shutdown threshold is kept lower than 150°C. As long as VIN rises, T_J must be kept less than 110°C.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Application

A typical application schematic is shown in 图 18.

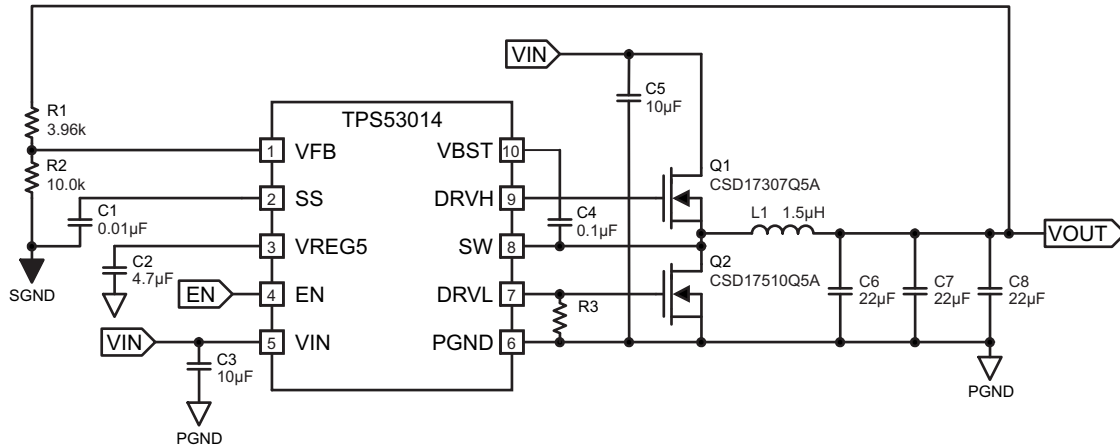


图 18. Application Schematic

8.1.1 Detailed Design Procedure

8.1.1.1 Component Selection

8.1.1.1.1 Inductor

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve S/N ratio and contribute to stable operation. 公式 4 can be used to calculate the value for L_{OUT} .

$$L_{OUT} = \frac{V_{IN(MAX)} - V_{OUT}}{I_{L(RIPPLE)} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} \quad (4)$$

The inductors current ratings needs to support both the RMS (thermal) current and the peak (saturation) current. The RMS and peak inductor current can be estimated as follows:

$$I_{L(RIPPLE)} = \frac{V_{IN(MAX)} - V_{OUT}}{L_{OUT} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} \quad (5)$$

$$I_{L(PEAK)} = \frac{V_{TRIP}}{R_{DS(ON)}} + I_{L(RIPPLE)} \quad (6)$$

$$I_{L(RMS)} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times I_{L(RIPPLE)}^2} \quad (7)$$

Note:

The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

Typical Application (接下页)

8.1.1.1.2 Output Capacitor

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. Ceramic output capacitors with X5R dielectric or better are recommended .

$$C_{OUT} = \frac{I_{L(RIPPLE)}}{8 \times V_{OUT(RIPPLE)}} \times \frac{1}{f_{SW}} \quad (8)$$

$$C_{OUT} = \frac{\Delta I_{LOAD}^2}{2 \times V_{OUT} \times \Delta V_{OS}} \times L_{OUT} \quad (9)$$

$$C_{OUT} = \frac{\Delta I_{LOAD}^2}{2 \times K \times \Delta V_{US}} \times L_{OUT} \quad (10)$$

Where:

$$K = (V_{IN} - V_{OUT}) \times \frac{T_{ON}}{T_{ON} - T_{OFF(MIN)}}$$

- ΔV_{OS} = The allowable amount of overshoot voltage in load transition
- ΔV_{US} = The allowable amount of undershoot voltage in load transition
- $T_{OFF(MIN)}$ = Minimum off time

Select the capacitance value greater than the largest value calculated from [公式 8](#), [公式 9](#) and [公式 10](#). The minimum recommended output capacitance is 44 μF .

8.1.1.1.3 Input Capacitor

The TPS53014 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10- μF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.1.1.1.4 Bootstrap Capacitor

The TPS53014 requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1- μF high-quality ceramic capacitor is recommended. The capacitor voltage rating should be greater than 10 V.

8.1.1.1.5 VREG5 Capacitor

The TPS53014 requires that the VREG5 regulator is bypassed. A minimum 4.7- μF high-quality ceramic capacitor must be connected between the VREG5 and PGND for proper operation. The capacitor voltage rating should be greater than 10 V.

8.1.1.1.6 Choose Output Voltage Resistors

The output voltage is set with a resistor divider from output voltage node to the VFB pin. TI recommends using 1% tolerance or better resistors. Select R2 between 10 k Ω and 100 k Ω and use [公式 12](#) to calculate R1.

$$R1 = \left(\frac{V_{OUT}}{V_{VFB}} - 1 \right) \times R2 \quad (12)$$

9 Layout

9.1 Layout Guidelines

- Keep the input switching current loop as small as possible.
- Place the input capacitor close to the top switching FET. Keep the output current loop as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin (VFB) of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

10 器件和文档支持

10.1 接收文档更新通知

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53014DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	53014	Samples
TPS53014DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	53014	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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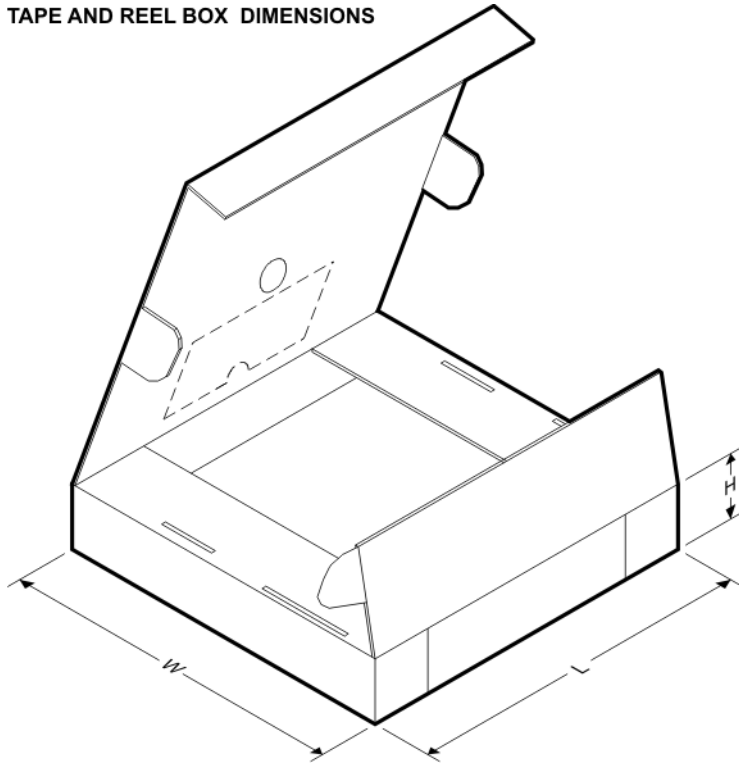
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53014DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

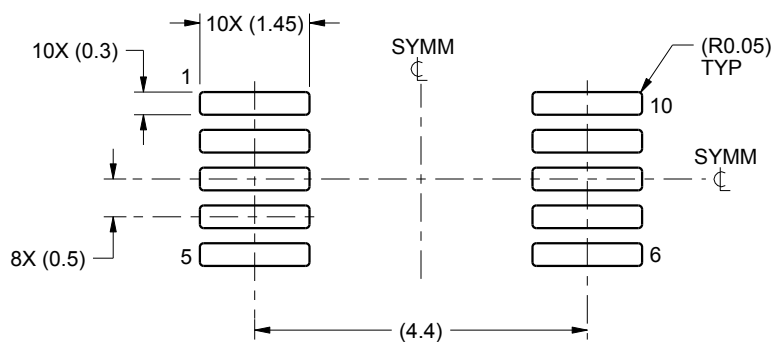
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53014DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

EXAMPLE BOARD LAYOUT

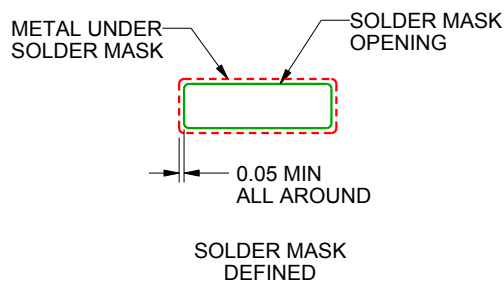
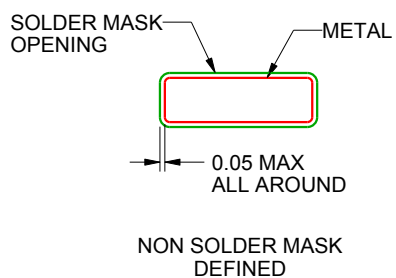
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

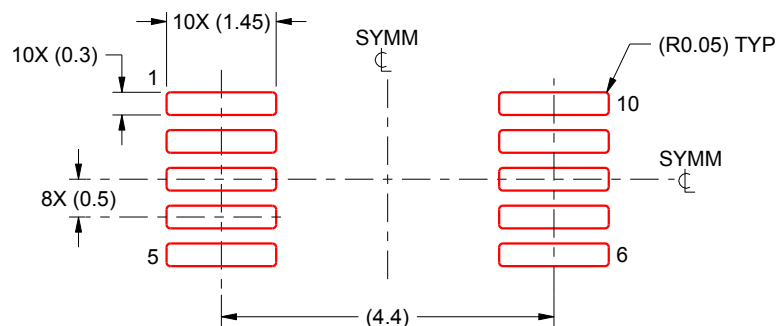
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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