TEXAS INSTRUMENTS
LM25149
ZHCSLO5 – DECEMBER 2020

具有超低 I_Q 和集成式有源 EMI 滤波器的 LM25149 42V 同步降压直流/直流控制器

1 特性

- 两个集成式 EMI 缓解机制
  - 有源 EMI 滤波器，可提高低频下的 EMI 性能
  - 双随机扩频 (DRSS)，可提高低频和高频频带上的 EMI 性能
  - EMI 平均降低了 25dBµV
  - 减小了 50% 的外部差分模式滤波器大小并降低了系统成本
- 多功能同步降压直流/直流控制器
  - 3.5V 至 42V 的宽输入电压范围
  - 1% 精度、3.3V/5V/12V 固定电压或 0.8V 至 36V 可调输出电压
  - 150°C 最大结温
  - 关断模式电流：2.2µA
  - 空载待机电流：9µA
- 开关频率范围为 100kHz 至 2.2MHz
  - 同步输入和同步输出功能
- 固有保护特性，可实现稳健的设计
  - 内部断续模式过流保护
  - 使能和 PGOOD 功能
  - VCC、VDDA 和栅极驱动 UVLO 保护
  - 内部或外部环路补偿
  - 具有迟滞功能的热关断保护
- 使用 LM25149 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 楼宇自动化
- 工业运输
- 无线基础设施

3 说明

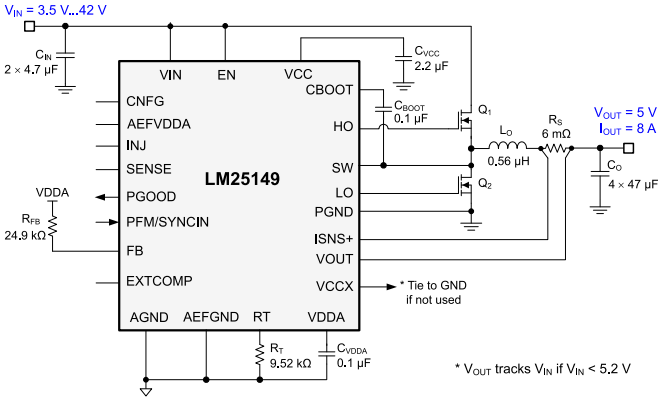
LM25149 是一款 42V 同步降压直流/直流控制器，适合高电流单输出应用。请参阅勘误表。该器件使用峰值电流模式控制架构，可轻松实现环路补偿、快速瞬态响应和出色的负载和线路调节性能。LM25149 可设置为以交错模式（并联输出）运行，可实现精确的电流共享，适合高电流应用。LM25149 可在低至 3.5V 的输入电压和接近 100% 的占空比（如果需要）下运行。

LM25149 有两个独特的 EMI 降低特性：有源 EMI 滤波器和双随机扩频 (DRSS)。有源 EMI 滤波器可感测直流输入总线上的任何噪声或纹波电压，并注入异相消除信号以降低噪声或纹波电压。DRSS 将低频三角调制与高频随机调制相结合，以优化低频和高频射频频带中的 EMI 性能。

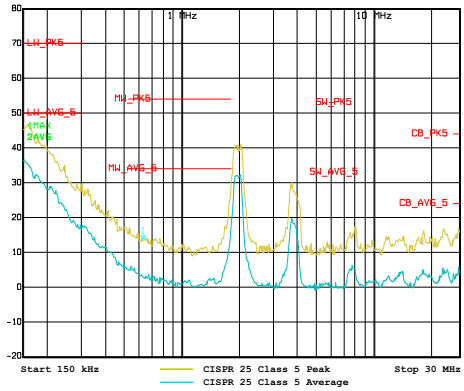
器件信息

器件型号	封装(1)	封装尺寸（标称值）
LM25149	VQFN (24)	3.5mm × 5.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录



典型应用原理图



CISPR 25 EMI 性能 150kHz 至 30MHz

ADVANCE INFORMATION

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

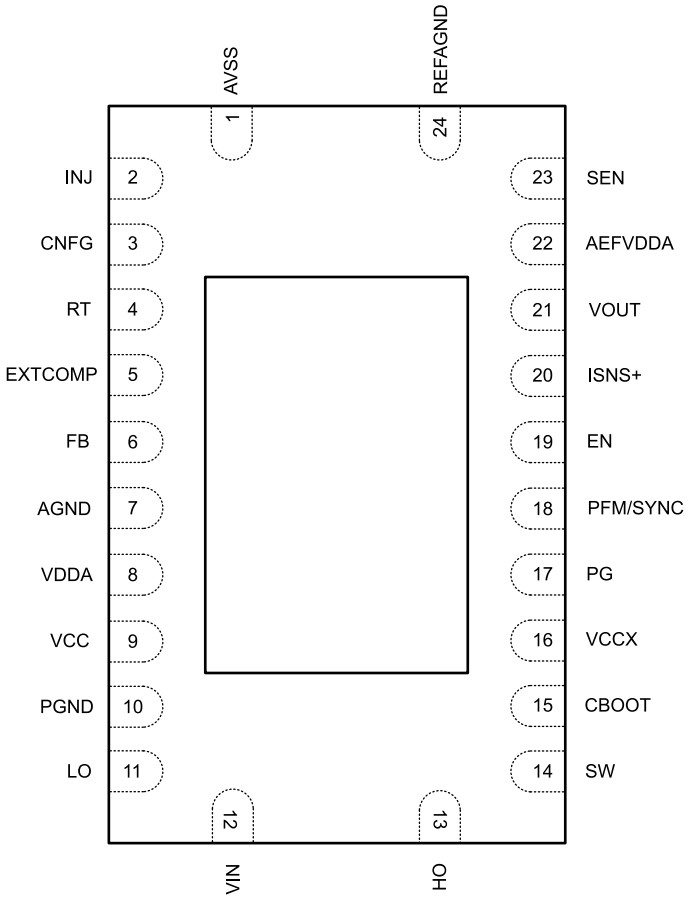
DATE	REVISION	NOTES
December 2020	*	Initial release

5 Description (continued)

Additional features of the LM25149 include 150°C maximum junction temperature operation, user-selectable diode emulation for lower current consumption at light-load conditions, open-drain Power-Good flag for fault reporting and output monitoring, precision enable input, monotonic start-up into prebiased load, integrated VCC bias supply regulator, internal 2.8-ms soft-start time, and thermal shutdown protection with automatic recovery.

The LM25149 controller comes in a 3.5-mm × 5.5-mm thermally-enhanced, 24-pin VQFN package with wettable flank pins to facilitate optical inspection during manufacturing.

6 Pin Configuration and Functions



Connect the exposed pad to AGND and PGND on the PCB.

图 6-1. 24-Pin VQFN RGY Package with Wettable Flanks (Top View)

表 6-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	AVSS	G	Active EMI bias ground connection
2	INJ	O	Active EMI injection output
3	CNFG	1	Connect a resistor to ground to set primary/secondary, spread spectrum enable/disable, or interleaved operation. After start-up, CNFG is used to enable AEF.
4	RT	I	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 100 kHz and 2.2 MHz.
5	EXTCOMP	O	The output of the transconduction amplifier. If used, connect the compensation network from EXTCOMP to AGND.
6	FB	I	Connect FB to VDDA to set the output voltage to 3.3 V. Connect FB through 24.9 kΩ to set the output voltage to 5 V, or a resistor divider from VOUT to FB to set the output voltage level between 0.8 V to 55 V. The regulation threshold is 0.8 V.
7	AGND	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits
8	VDDA	O	Internal analog bias regulator. Connect a ceramic decoupling capacitor from VDDA to AGND.
9	VCC	P	VCC bias supply pin. Connect ceramic capacitors between VCC and PGND.
10	PGND	G	Power ground connection pin for low-side NMOS gate driver
11	LO	O	Low-side gate driver signal
12	VIN	P	Supply voltage input source for the VCC regulators

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表 6-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
13	HO	O	High-side gate driver turnon output
14	SW	P	Switching node of the buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
15	CBOOT	P	High-side driver supply for bootstrap gate drive
16	VCCX	P	Optional input for an external bias supply. If V_{VCCX} > 4.3 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled.
17	PG	P	An open-collector output that goes low if VOUT is outside the specified regulation window
18	PFM/SYNC	I	Connect PFM to AGND to enable diode emulation mode. Connect PFM to VDDA to operate the LM5149-Q1 in forced PWM (FPWM) mode with continuous conduction at light loads. PFM can also be used as a synchronization input to synchronize the internal oscillator to an external clock.
19	EN	I	An active-high input (V_{EN} 1) enables the output. If the output is not enabled, the LM5149-Q1 is in shutdown mode.
20	ISNS+	I	Current sense amplifier input. Connect the ISNS+ to the inductor side of the external current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used) using a low-current Kelvin connection.
21	VOUT	I	Output voltage sense and the current sense amplifier input. Connect VOUT to the output side of the current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used).
22	AEFVDDA	P	Active EMI bias power. Connect a ceramic capacitor between AEFVDDA and AVSS.
23	SENSE	I	Active EMI sense input
24	REFAGND	G	Active EMI reference ground

(1) P = Power, G = Ground, I = Input, O = Output.

6.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet reliability and robustness standards. Standard quad-flat no-lead (QFN) packages do not have solderable or exposed pins and terminals that are easily viewed. It is therefore difficult to visually determine whether or not the package is successfully soldered onto the printed-circuit board (PCB). The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The LM25149 is assembled using a 24-pin VQFN package with wettable flanks to provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN to PGND	–0.3	47	V
Pin voltage	SW to PGND	–0.3	47	V
Pin voltage	SW to PGND transient < 20 ns	–5		V
Pin voltage	CBOOT to SW	–0.3	6.5	V
Pin voltage	CBOOT to SW, transient < 20 ns	–5		V
Pin voltage	HO to SW, transient < 20 ns	–5		V
Pin voltage	LO to PGND, transient < 20 ns	–1.5	0.3	V
Pin voltage	EN/UVLO to PGND	–0.3	47	V
Pin voltage	VCC, VCCX, VDDA, PG, FB, CNFG, PFM/SYNC, RT, EXTCOMP to AGND	–0.3	6.5	V
Pin voltage	VOUT , ISNS+	–0.3	36	V
Pin voltage	VOUT to ISNS+	–0.3	0.3	V
Pin voltage	PGND to AGND	–0.3	0.3	V
Pin voltage	AEFVDDA to AEFGND	–0.3	5.5	V
Pin voltage	INJ to AEFGND	–0.3	5.5	V
Pin voltage	SEN to AEFGND	–0.3	47	V
Pin voltage	AEFGND to AVSS	–0.3	0.3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		3.5		42	V
V_{OUT}	Output voltage range		0.8		36	V
	Pin voltage	SW to PGND	–0.3		42	V
	Pin voltage	CBOOT to SW	–0.3	5	5.25	V
	Pin voltage	FB, EXTCOMP, RT to AGND	–0.3		5.25	V
	Pin voltage	EN to PGND	–0.3		42	V
	Pin voltage	VCC, VCCX, VDDA to PGND	–0.3	5	5.25	V

ADVANCE INFORMATION

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Pin voltage	VOUT, ISNS+ to PGND	–0.3		36	V
	PGND to AGND		–0.3		0.3	V
	Pin voltage	AEFVDDA	–0.3		5	V
	Pin voltage	INJ to AEFGND	–0.3		5	V
	Pin voltage	SEN to AEFGND	–0.3		36	V
	Pin voltage	AEFGND to AVSS	–0.3		0.3	V
T_J	Operating junction temperature		–40		150	°C

7.4 Thermal Information

THERMAL METRIC(1)		LM5149-Q1 RGY (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics

7.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{IN} = 8 V to 18 V. Typical values are at T_J = 25°C and V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN)						
I_{Q-VIN1}	VIN shutdown current	Non-switching, V_{EN} = 0 V, V_{FB} = V_{REF} + 50 mV		2.2	3.8	µA
I_{Q-VIN2}	VIN standby current	Non-switching, 0.5 V ≤ V_{EN} ≤ 1 V		104		µA
$I_{STANDBY1}$	Sleep current, 3.3 V	1.03 V ≤ V_{EN} ≤ 47 V, V_{VOUT} = 3.3 V, in regulation, no-load, not switching, V_{PFM}/V_{SYNC} = 0 V		9.5	19.6	µA
$I_{STANDBY2}$	Sleep current, 5 V	V_{EN} = 5 V, V_{VOUT} = 5 V, in regulation, no-load, not switching, V_{PFM}/SYNC = 0 V		10	17.2	µA
ENABLE (EN)						
V_{SDN}	Shutdown to standby threshold	V_{EN} rising		0.5		V
$V_{EN-HIGH}$	Enable voltage rising threshold	V_{EN} rising, enable switching	0.95	1.0	1.05	V
I_{EN-HYS}	Enable hystersis	V_{EN} = 1.1 V	8	10	12	µA
INTERNAL LDO (VCC)						
$V_{VCC-REG}$	VCC regulation voltage	I_{VCC} = 0 mA to 100 mA	4.7	5	5.3	V
$V_{VCC-UVLO}$	VCC UVLO rising threshold		3.3	3.4	3.5	V
$V_{VCC-HYST}$	VCC UVLO hysteresis			130		mV
$I_{VCC-REG}$	Internal LDO short-circuit current limit		110	170		mA
INTERNAL LDO (VDDA)						
$V_{VDDA-REG}$	VDDA regulation voltage		4.75	5	5.25	V
$V_{VDDA-UVLO}$	VDDA UVLO rising	V_{VCC} rising, V_{VCCX} = 0 V	3.1	3.2	3.3	V
$V_{VDDA-HYST}$	VDDA UVLO hysteresis	V_{VCCX} = 0 V		120		mV

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{IN} = 8 V to 18 V. Typical values are at T_J = 25°C and V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{VDDA}	VDDA resistance	V_{VCCX} = 0 V		5.5		Ω
EXTERNAL BIAS (VCCX)						
$V_{VCCX-ON}$	$VCCX_{(ON)}$ rising threshold		4.1	4.3	4.4	V
$V_{VCCX-HYST}$	VCCX hysteresis voltage	V_{VCCX} = 5 V		130		mV
R_{VCCX}	VCCX resistance	V_{VCCX} = 5 V		2		Ω
REFERENCE VOLTAGE						
V_{FB}	Regulated FB voltage		795	800	808	mV
OUTPUT VOLTAGE (VOUT)						
$V_{OUT-3.3V-INT}$	3.3-V output voltage setpoint	R_{FB} = 0 Ω, V_{IN} = 3.8 V to 42 V, internal COMP	3.267	3.3	3.33	V
$V_{OUT-3.3V-EXT}$	3.3-V output voltage setpoint	R_{FB} = 0 Ω, V_{IN} = 3.8 V to 42 V, external COMP	3.267	3.3	3.33	V
$V_{OUT-5V-INT}$	5-V output voltage setpoint	R_{FB} = 24.9 kΩ, V_{IN} = 5.5 V to 42 V, internal COMP	4.95	5.0	5.05	V
$V_{OUT-5V-EXT}$	5-V output voltage setpoint	R_{FB} = 24.9 kΩ, V_{IN} = 5.5 V to 42 V, external COMP	4.95	5.0	5.05	V
$V_{OUT-12V-INT}$	12-V output setpoint	R_{FB} = 48.7 kΩ, V_{IN} = 24 V to 42 V, Internal COMP	11.88	12	12.12	V
$V_{OUT-12V-EXT}$	12-V output setpoint	R_{FB} = 48.7 kΩ, V_{IN} = 24 V to 42 V, external COMP COMP	11.88	12	12.12	V
$R_{FB-OPT2}$	5-V output select		24.3	24.9	25.5	kΩ
$R_{FB-OPT3}$	12-V output select		47.5	48.7	49.9	kΩ
ERROR AMPLIFIER (COMP)						
$g_{m-EXTERNAL}$	EA transconductance, external compensation	FB to COMP	1020	1200		µS
$g_{m-INTERNAL}$	EA transconductance, internal compensation	FB to COMP, EXTCOMP 100 kΩ to VDDA		30		µS
I_{FB}	Error amplifier input bias current				75	nA
$V_{COMP-CLAMP}$	COMP clamp voltage	V_{FB} = 0 V		2.1		V
$I_{COMP-SRC}$	EA source current	V_{COMP} = 1 V, V_{FB} = 0.4 V		180		µA
$I_{COMP-SINK}$	EA sink current	V_{COMP} = 1 V, V_{FB} = 0.8 V		160		µA
R_{COMP}	Internal compensation	EXTCOMP 100 kΩ to VDDA		400		kΩ
C_{COMP}	Internal compensation	EXTCOMP 100 kΩ to VDDA		50		pF
$C_{COMP-HF}$	Internal compensation	EXTCOMP 100 kΩ to VDDA		1		pF
PULSE FREQUENCY MODULATION (PFM)						
V_{PFM-LO}	PFM detection threshold low		0.8			V
V_{PFM-HI}	PFM decection threshold high				2.0	V
V_{ZC-SW}	Zero-cross threshold			-5.5		mV
V_{ZC-DIS}	Zero-cross threshold disable	PFM = VDDA, 1000 SW cycles after first HO pulse		100		mV
$F_{SYNCIN3}$	Frequency sync range	R_{RT} = 10 kΩ, ± 20% of the nominal oscillator frequency	1760		2640	kHz
$t_{SYNC-MIN3}$	Minimum pulse width of external synchronization signal		20		250	ns
$t_{SYNCIN-HO}$	Delay from PFM faling edge to HO rising edge			25		ns
$t_{PFM-FILTER}$	SYNCIN to PFM mode		15		30	µs
DUAL RANDOM SPREAD SPECTRUM (DRSS)						

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{IN} = 8 V to 18 V. Typical values are at T_J = 25°C and V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Δf_C	Distance from the nominal switching frequency			7.8		%
f_m	Modulation frequency		13		21	kHz
SWITCHING FREQUENCY						
V_{RT}	RT pin regulation voltage	10 kΩ < R_{RT} < 100 kΩ		0.5		V
f_{SW1}	Switching frequency 1	V_{IN} = 12 V, R_{RT} = 100 kΩ to AGND		220		kHz
f_{SW2}	Switching frequency 2	V_{IN} = 12 V, R_{RT} = 9.52 kΩ to AGND	1.98	2.2	2.42	MHz
f_{SW3}	Switching frequency 3	V_{IN} = 12 V, R_{RT} = 220 kΩ to AGND		100		kHz
$SLOPE_1$	Internal slope compensation 1	R_{RT} = 10 kΩ		500		mV/µs
$SLOPE_2$	Internal slope compensation 2	R_{RT} = 100 kΩ		50		mV/µs
$t_{ON(min)}$	Minimum on-time			49	59	ns
$t_{OFF(min)}$	Minimum off-time			60	85	ns
POWER GOOD (PG)						
V_{PG-UV}	Power Good UV trip level	Falling with respect to the regulated voltage	90%	92%	94%	
V_{PG-OV}	Power Good OV trip level	Rising with respect to the regulation voltage	108%	110%	112%	
$V_{PG-UV-HYST}$	Power Good UV hysteresis	Falling with respect to the regulated output		3.4%		
$V_{PG-OV-HYST}$	Power Good OV hysteresis	Rising with respect to the regulation voltage		3.4%		
$t_{PG-RISING-DLY}$	OV filter time	V_{OUT} rising		25		µs
$t_{PG-FALL-DLY}$	UV filter time	V_{OUT} falling		25		µs
V_{PG-OL}	PG voltage	Open collector, I_{PG} = 4 mA			0.8	V
SYNCHRONIZATION OUTPUT (PG pin)						
$V_{SYNCOUT-LO}$	SYNCOUT-LO low-state voltage	CNFG pin = 54.9 kΩ or 71.5 kΩ to VDDA (Primary), $I_{SYNCOUT}$ = 4 mA			0.8	V
$V_{SYNCOUT-HO}$	SYNCOUT-HO high-state voltage	CNFG pin = 54.9 kΩ, or 71.5 kΩ to VDDA (Primary) $I_{SYNCOUT}$ = 4 mA.	2.0			V
$t_{SYNCOUT}$	Delay from HO rising edge to SYNCOUT (PGOOD pin in Primary mode)	V_{PFM} = 0 V, F_{SW} set by R_{RT} = 100 kΩ		2.1		µs
STARTUP (Soft Start)						
t_{SS-INT}	Internal fixed soft-start time		1.9	2.8	3.6	ms
BOOT CIRCUIT						
$V_{BOOT-DROP}$	Internal diode forward drop	I_{CBOOT} = 20 mA, VCC to CBOOT	0.63	0.8		V
I_{BOOT}	CBOOT to SW quiescent current, not switching	V_{EN} = 5 V, $V_{CBOOT-SW}$ = 5 V	130			nA
$V_{BOOT-SW-UV-R}$	CBOOT-SW UVLO rising threshold	$V_{CBOOT-SW}$ falling		2.83		V
$V_{BOOT-SW-UV-F}$	CBOOT-SW UVLO falling threshold	$V_{CBOOT-SW}$ falling		2.59		V
$V_{BOOT-SW-UV-HYS}$	CBOOT-SW UVLO hysteresis			0.24		V
V_{HO-LOW}	HO low-state output voltage	I_{HO} = 100 mA		0.038		V
HIGH-SIDE GATE DRIVER (HO)						
$V_{HO-HIGH}$	HO high-state output voltage	I_{HO} = –100 mA		0.08		V
$t_{HO-RISE}$	HO rise time (10% to 90%)	C_{LOAD} = 2.7 nF		7		ns
$t_{HO-FALL}$	HO fall time (90% to 10%)	C_{LOAD} = 2.7 nF		7		ns
I_{HO-SRC}	HO peak source current	V_{HO} = V_{SW} = 0 V, V_{CBOOT} = 5 V, V_{VCCX} = 5 V		2.2		A

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T_J = –40°C to +150°C, V_{IN} = 8 V to 18 V. Typical values are at T_J = 25°C and V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{HO-SINK}$	HO peak sink current	V_{VCCX} = 5 V		3.2		A
LOW-SIDE GATE DRIVER (LO)						
V_{LO-LOW}	LO low-state output voltage	I_{HO} = 100 mA		0.038		V
$V_{LO-HIGH}$	LO high-state output voltage	I_{HO} = –100 mA		0.08		V
$t_{LO-RISE}$	LO rise time (10% to 90%)	C_{LOAD} = 2.7 nF		7		ns
$t_{LO-FALL}$	LO fall time (90% to 10%)	C_{LOAD} = 2.7 nF		7		ns
I_{LO-SRC}	LO peak source current	V_{HO} = V_{SW} = 0 V, V_{CBOOT} = 5 V, V_{VCCX} = 5 V		2.2		A
$I_{LO-SINK}$	LO peak sink current	V_{VCCX} = 5 V		3.2		A
ADAPTIVE DEADTIME CONTROL						
t_{DEAD1}	HO off to LO on deadtime			12		ns
t_{DEAD2}	LO off to HO on deadtime			13		ns
INTERNAL HICCUP MODE						
HIC_{DLY}	Hiccup mode activation delay	V_{ISNS+} – V_{VOUT} > 60 mV		512		cycles
HIC_{CYCLES}	HICCUP mode fault	V_{ISNS+} – V_{VOUT} > 60 mV		16384		cycles
OVERCURRENT PROTECTION						
V_{CS-TH}	Current limit threshold	Measured from ISNS+ to VOUT	54	60	66	mV
$t_{DELAY-ISNS+}$	ISNS+ delay to output			45		ns
G_{CS}	CS amplifier gain		9.5	10	10.5	V/V
$I_{BIAS-ISNS+}$	CS amplifier input bias current				15	nA
CONFIGURATION						
$R_{CONF-OPT1}$	Primary, no spread spectrum		28.7	29.4	30.1	kΩ
$R_{CONF-OPT2}$	Primary, with spread spectrum		40.2	41.2	43.2	kΩ
$R_{CONF-OPT3}$	Primary, Interleaved, no spread spectrum		53.6	54.9	57.6	kΩ
$R_{CONF-OPT4}$	Primary, Interleaved, with spread spectrum		69.8	71.5	73.2	kΩ
$R_{CONF-OPT5}$	Secondary		88.7	90.9	93.1	kΩ
THERMAL SHUTDOWN						
T_{J-SD}	Thermal shutdown threshold (1)	Temperature rising		175		°C
T_{J-HYS}	Thermal shutdown hysteresis (1)			15		°C

(1) Specified by design. Not production tested.

7.6 Active EMI Filter

T_J = –40°C to 150°C, $V_{AEFVDDA}$ = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Active EMI Filter						
$V_{AEF-UVLO-R}$	Voltage AEF UVLO rising threshold			4.15		V
$V_{AEF-UVLO-F}$	Voltage AEF UVLO falling threshold			3.5		V
$V_{AEF-HYST}$	Voltage AEF UVLO hysteresis			650		mV
A_{OL}	DC gain				68	dB
F_{BW-AEF}	Unity gain bandwidth			300		MHz
$V_{AEF-HIGH}$	AEF voltage rising threshold	Enable AEF			2	V
$V_{AEF-LOW}$	AEF voltage falling threshold	Disable AEF	0.8			V
$V_{AEF-REF}$	AEF reference voltage			2.5		V

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8 Detailed Description

8.1 Overview

The LM25149 is a switching controller that features all of the functions necessary to implement a high-efficiency synchronous buck power supply operating over a wide input voltage range from 3.5 V to 42 V. The LM25149-Q1 is configured to provide a fixed 3.3-V, 5-V, or 12-V output, or an adjustable output between 0.8 V to 36 V. This easy-to-use controller integrates high-side and low-side MOSFET drivers capable of sourcing 2.2-A and sinking 3.2-A peak current. Adaptive dead-time control is designed to minimize body diode conduction during switching transitions.

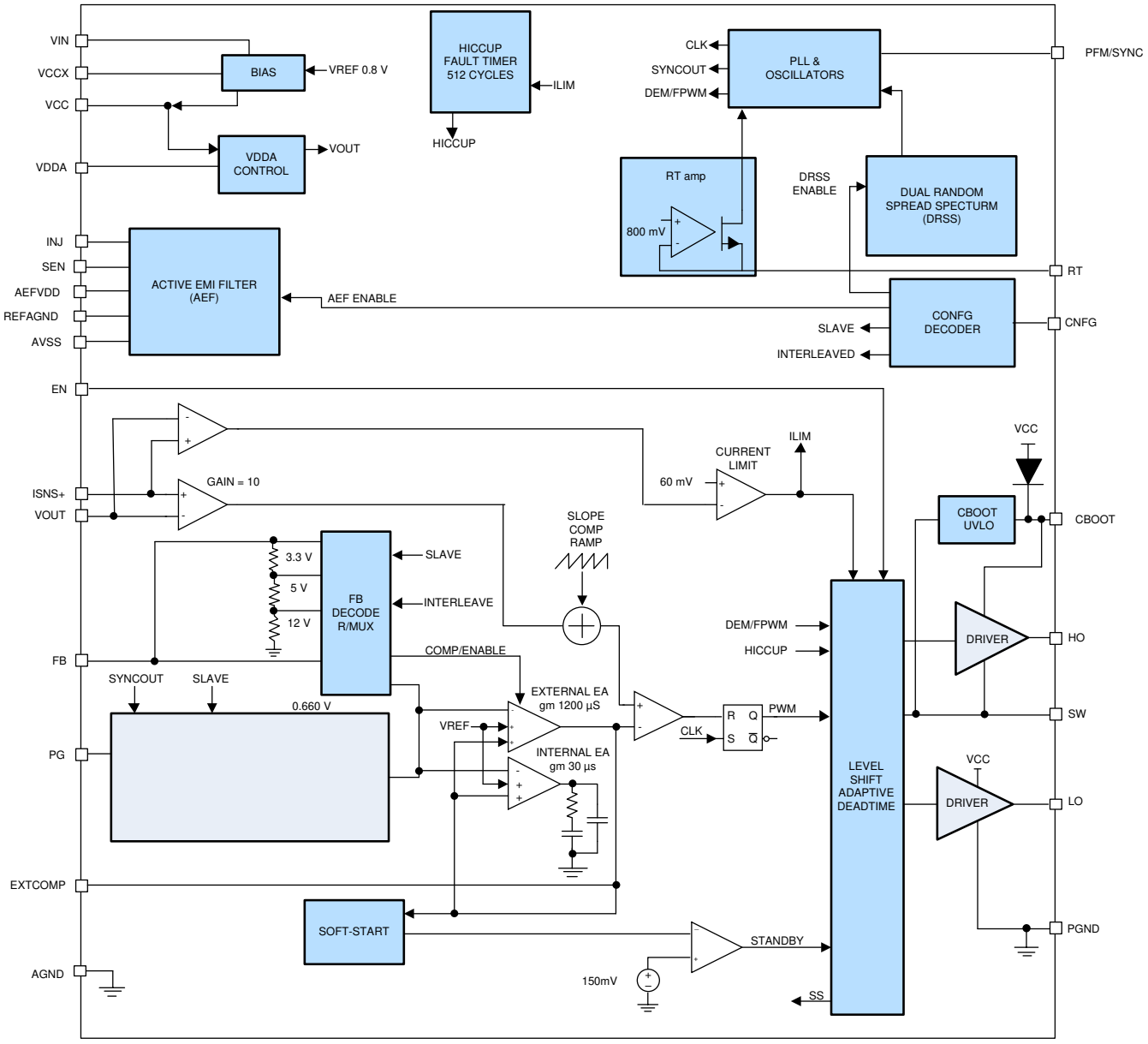
Current-mode control using a shunt resistor or inductor DCR current sensing provides inherent line feedforward, cycle-by-cycle peak current limiting, and easy loop compensation. It also supports a wide duty cycle range for high input voltage and low-dropout applications as well as when a high step-down conversion ratio (for example, 10-to-1) is required. The oscillator frequency is user-programmable between 100 kHz to 2.2 MHz, and the frequency can be synchronized as high as 2.5 MHz by applying an external clock to the PFM/SYNC pin.

An external bias supply can be connected to VCCX to maximize efficiency in high input voltage applications. A user-selectable diode emulation feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions. Fault protection features include current limiting, thermal shutdown, UVLO, and remote shutdown capability.

The LM25149 incorporates features to simplify the compliance with automotive EMI requirements (CISPR 25). Active EMI filter (AEF) and Dual Random Spread Spectrum (DRSS) techniques reduce the peak harmonic EMI signature.

The LM25149 is provided in a 24-pin VQFN package with a wettable flank pinout and an exposed pad to aid in thermal dissipation.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Voltage Range (V_{IN})

The LM25149 operational input voltage range is from 3.5 V to 42 V. The device is intended for step-down conversions from 12-V, 24-V, and 48-V automotive supply rails. The application circuit in 图 9-4 shows all the necessary components to implement an LM25149 based wide-V_{IN} single-output step-down regulator using a single supply. The LM25149 uses an internal LDO to provide a 5-V VCC bias rail for the gate drive and control circuits (assuming the input voltage is higher than 5 V with additional voltage margin necessary for the sub-regulator dropout specification).

In high input voltage applications, take extra care to ensure that the VIN and SW pins do not exceed their absolute maximum voltage rating of 47 V during line or load transient events. Voltage excursions that exceed the input voltage can damage the IC.

8.3.2 High-Voltage Bias Supply Regulator (VCC, VCCX, VDDA)

The LM25149 contains an internal high-voltage VCC bias regulator that provides the bias supply for the PWM controller and the gate drivers for the external MOSFETs. The input voltage pin (VIN) can be connected directly to an input voltage source up to 42 V. However, when the input voltage is below the VCC setpoint level, the VCC voltage tracks V_{IN} minus a small voltage drop.

The VCC regulator output current limit is 110 mA (minimum). At power up, the controller sources current into the capacitor connected at the VCC pin. When the VCC voltage exceeds 3.3 V and the EN pin is connected to a voltage greater than 1 V, the soft-start sequence begins. The output remains active unless the VCC voltage falls below the VCC UVLO falling threshold of 3.1 V (typical) or EN is switched to a low state. Connect a ceramic capacitor from VCC to PGND. The recommended range of the VCC capacitor is from 2.2 µF to 10 µF.

An internal 5-V linear regulator generates the VDDA bias supply. Bypass VDDA with a 470-nF ceramic capacitor to achieve a low-noise internal bias rail. Normally VDDA is 5 V. However, there is one condition where VDDA regulates at 3.3-V, this is in PFM mode with a light or no-load on the output.

Minimize the internal power dissipation of the VCC regulator by connecting VCCX to a 5-V output or to an external 5-V supply. If the VCCX voltage is above 4.3 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. Tie VCCX to PGND if it is unused. Never connect VCCX to a voltage greater than 6.5 V. If an external supply is connected to VCCX to power the LM25149, V_{IN} must be greater than the external bias voltage during all conditions to avoid damage to the controller.

8.3.3 Enable (EN)

The EN pin can be connected to a voltage as high as 42 V. The LM25149 has a precision enable. When the EN voltage is greater than 1 V, V_{OUT} is enabled. If the EN pin is pulled below 0.5 V, the LM25149 is in shutdown with an I_Q of 2.2 µA (typical) current draw from V_{IN}. When the enable voltage is between 0.5 V and 1 V, the LM25149 is in standby mode. When the controller is in standby mode, the VCC regulator is active, and the controller is not switching. Under these conditions, the I_Q current is 100 µA typical. The LM25149 is enabled with a logic level voltage greater then 2.0 V, and a voltage less than 0.4 V disables the LM25149. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2}, as shown in 图 8-4, to establish a precision UVLO level. TI does not recommend leaving the EN pin floating.

Use 方程式 1 and 方程式 2 to calculate the UVLO resistors given the required input turnon and turnoff voltages.

$$R_{UV1} = \frac{V_{IN(on)} - V_{IN(off)}}{I_{HYS}} \tag{1}$$

$$R_{UV2} = R_{UV1} \cdot \frac{V_{EN}}{V_{IN(on)} - V_{EN}} \tag{2}$$

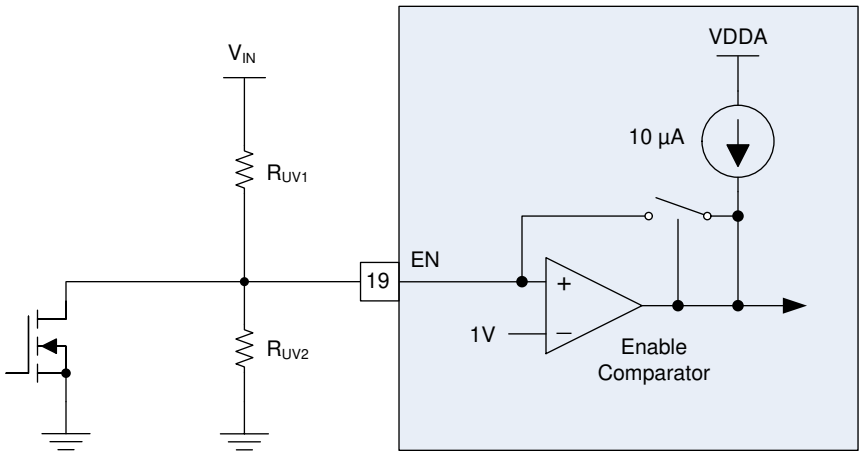

图 8-1. Programmable Input Voltage UVLO Turnon

8.3.4 Power Good Monitor (PG)

The LM25149 includes an output voltage monitoring signal for V_{OUT} to simplify sequencing and supervision. The Power Good signal is used for start-up sequencing of downstream converters, fault protection, and output monitoring. The power-good output (PG) switches to a high impedance open-drain state when the output voltage is in regulation. The PG switches low when the output voltage drops below the lower power-good threshold (92% typical) or rises above the upper power-good threshold (110% typical). A 25-µs deglitch filter prevents false tripping of the power-good signal during transients. TI recommends a pullup resistor of 100 kΩ (typical) from PG to the relevant logic rail. PG is asserted low during soft start and when the buck regulator is disabled.

When the LM25149 is configured as a primary controller, the PG pin is becomes a synchronization clock output for the Secondary controller. The synchronization signal is a logic level, 180° out-of-phase with the primary HO driver output.

8.3.5 Switching Frequency (RT)

The LM25149 oscillator is programmed by a resistor between RT and AGND to set an oscillator frequency between 100 kHz to 2.2 MHz. Calculate the RT resistance for a given switching frequency using 方程式 3.

$$R_T(k\Omega) = \frac{\frac{10^6}{F_{SW}(kHz)} - 53}{45} \tag{3}$$

Under low V_{IN} conditions when the on-time of the high-side MOSFET exceeds the programmed oscillator period, the LM25149 extends the switching period until the PWM latch is reset by the current sense ramp exceeding the controller compensation voltage.

The approximate input voltage level at which this occurs is given by 方程式 4, where t_{SW} is the switching period and $t_{OFF(min)}$ is the minimum off-time of 60 ns.

$$V_{IN(min)} = V_{OUT} \cdot \frac{t_{SW}}{t_{SW} - t_{OFF(min)}} \tag{4}$$

8.3.6 Active EMI Filter

Active EMI filter provides a higher level of EMI attenuation and a smaller solution size than a standard passive π-filters. Passive π-filter use large inductors and capacitors to attenuate the ripple and noise on the input DC

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bus. Passive filters are typically most effective at reducing the switching frequency harmonics to comply with EMI in the low-frequency range, less than 30 MHz.

Active EMI filter has a high gain, wide bandwidth (approximately 20 MHz), and a low output impedance that can source and sink current. It senses (at the SEN pin) any noise or ripple voltage on the DC input bus and injects (at the INJ pin) a cancellation signal out of phase with the noise source to reduce the conducted emissions.

To maintain low I_Q at light loads, the LM25149 automatically enables active EMI filter when the load current is greater than 40% of the current limit value, and disables active EMI filter when the load current is less then 30% of the current limit value. Active EMI filter is disabled by pulling the CNFG pin below 0.8 V after the LM25149 has been configured.

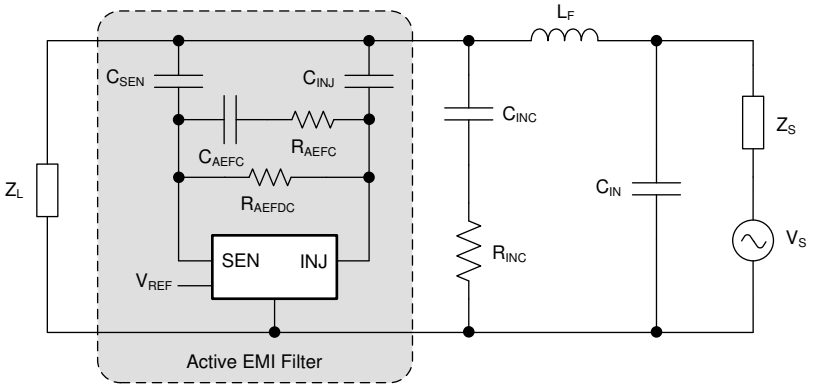

图 8-2. Active EMI Filter

8.3.7 Dual Random Spread Spectrum (DRSS)

The LM25149 provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. DRSS combines a low-frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low-frequency triangular modulation improves performance in lower radio frequency bands, while the high-frequency random modulation improves performance in higher radio frequency bands.

Spread spectrum works by converting a narrowband signal into a wideband signal that spreads the energy over multiple frequencies. Since industry standards require different spectrum analyzer resolution bandwidth (RBW) settings for different frequency bands, the RBW has an impact on the spread spectrum performance. For example, the CISPR 25 spectrum analyzer RBW in the frequency band from 150 kHz to 30 MHz is 9 kHz. For frequencies greater than 30 MHz, the RBW is 120 kHz. DRSS is able to simultaneously improve the EMI performance in the high and low RBWs with its low-frequency triangular modulation profile and high frequency cycle-by-cycle random modulation. DRSS can reduce conducted emissions by 15 dBμV in the low-frequency band (150 kHz to 30 MHz), and 5 dBμV in the high-frequency band (30 MHz to 108 MHz).

To enable DRSS, connect either a 41.2-kΩ or 71.5-kΩ resistor from CNFG to AGND. DRSS is disabled when an external clock is applied to the PFM/SYNC pin.

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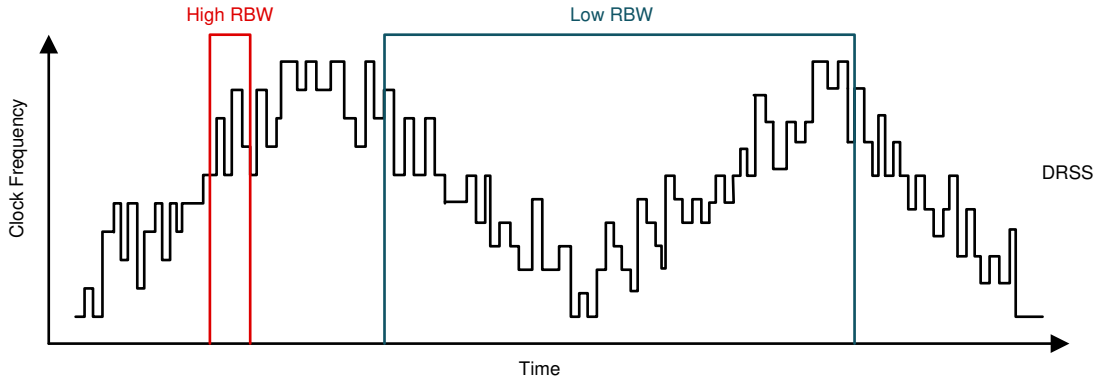

图 8-3. Dual Random Spread Spectrum Implementation

8.3.8 Soft-Start

The LM25149 has an internal 2.8-ms soft-start timer (typical). The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

8.3.9 Output Voltage Setpoint (FB)

The LM25149 output can be independently configured for one of three fixed output voltages without external feedback resistors, or adjusted to the desired voltage using an external resistor divider. Set the output to 3.3-V by connecting FB directly to VDDA. Alternatively, set the output to either 5-V or 12-V by installing a 24.9-kΩ or 49.9 kΩ resistor, between FB and VDDA, respectively. See 表 8-1. The configuration settings are latched and cannot be changed until the LM25149 is powered down (with the VCC voltage decreasing below its falling UVLO threshold) and then powered up again (VCC rises above the 3.4 V typical).

表 8-1. Feedback Configuration Resistors

PULLUP RESISTOR TO V_{DDA}	V_{OUT}
0 Ω	3.3 V
24.9 kΩ	5 V
49 kΩ	12 V
NA	External FB divider

Alternatively, set the output voltage with an external resistive divider from the output to the FB pin. The output voltage adjustment range is between 0.8 V to 36 V. The regulation threshold at FB is 0.8 V (V_{REF}). Use 方程式 5 to calculate the upper and lower feedback resistors, designated R_{FB1} and R_{FB2}.

$$R_{FB1} = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \cdot R_{FB2} \tag{5}$$

The recommended starting value for R_{FB2} is between 10 kΩ and 20 kΩ.

If a low-I_Q mode is required, take care when selecting the external resistors. The extra current drawn from the external divider is added to the LM25149 $I_{STANDBY}$ current (9 µA typical). The divider current reflected to V_{IN} is divided down by the ratio of V_{OUT} / V_{IN}.

8.3.10 Minimum Controllable On-Time

There are two limitations to the minimum output voltage adjustment range: the LM25149 voltage reference of 0.8 V and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio V_{OUT} / V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy 方程式 6.

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$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \cdot F_{SW} \tag{6}$$

where

- $t_{ON(min)}$ is 49 ns (typical)
- F_{SW} is the switching frequency

If the desired voltage conversion ratio does not meet the above condition, the LM25149 transitions from fixed switching frequency operation to a pulse-skipping mode to maintain output voltage regulation. For example, if the desired output voltage is 5 V with an input voltage of 24 V and switching frequency of 2.1 MHz, the voltage conversion ratio test in 方程式 7 is satisfied.

$$\frac{5\,V}{24\,V} > 59\,ns \cdot 2.1\,MHz$$

$$0.208 > 0.124 \tag{7}$$

For wide-V_{IN} applications and low output voltages, an alternative is to reduce the LM25149 switching frequency to meet the requirement of 方程式 6.

8.3.11 Error Amplifier and PWM Comparator (FB, EXTCOMP)

The LM25149 has a high-gain transconductance amplifier that generates an error current proportional to the difference between the feedback voltage and an internal precision reference (0.8 V). The control loop compensation is configured two ways. The first is using the internal compensation amplifier, which has a transconductance of 30 µS. Internal compensation is configured by connecting the EXTCOMP pin through a 100-kΩ resistance to VDDA. If a 100-kΩ resistor is not detected, the LM25149 defaults to the external loop compensation network. The transconductance of the amplifier for external compensation is 1200 µS. This is latched and cannot be re-configured on the fly. Use an external compensation network if higher performance is required to meet a stringent transient response. To re-configure the compensation (internal or external), remove power and allow VCC to drop below its VCC_{UVLO} threshold, which is 3.3 V typical.

A type-II compensation network is generally recommended for peak current-mode control.

8.3.12 Slope Compensation

The LM25149 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor downslope using 方程式 8.

$$L_{O\text{-}IDEAL}(\mu H) = \frac{V_{OUT}(V) \cdot R_S(m\Omega)}{24 \cdot F_{SW}(MHz)} \tag{8}$$

- A lower inductance value generally increases the peak-to-peak inductor current, which minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value generally decreases the peak-to-peak inductor current, reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

8.3.13 Inductor Current Sense (ISNS+, VOUT)

There are two methods to sense the inductor current of the buck power stage. The first uses a current sense resistor (also known as a shunt) in series with the inductor, and the second avails of the DC resistance of the inductor (DCR current sensing).

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8.3.13.1 Shunt Current Sensing

图 8-4 illustrates inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For optimal current sense accuracy and overcurrent protection, use a low inductance ±1% tolerance shunt resistor between the inductor and the output, with a Kelvin connection to the LM25149 current sense amplifier.

If the peak viltage signal sensed from ISNS+ to VOUT exceeds the current limit threshold of 60 mV, the current limit comparator immediately terminates HO output for cycle-by-cycle current limiting. Calculate the shunt resistance using 方程式 9.

$$R_S = \frac{V_{CS\text{-}TH}}{I_{OUT(CL)} + \frac{\Delta I_L}{2}} \tag{9}$$

where

- $V_{CS\text{-}TH}$ is current sense threshold of 60 mV
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients
- ΔI_L is the peak-to-peak inductor ripple current

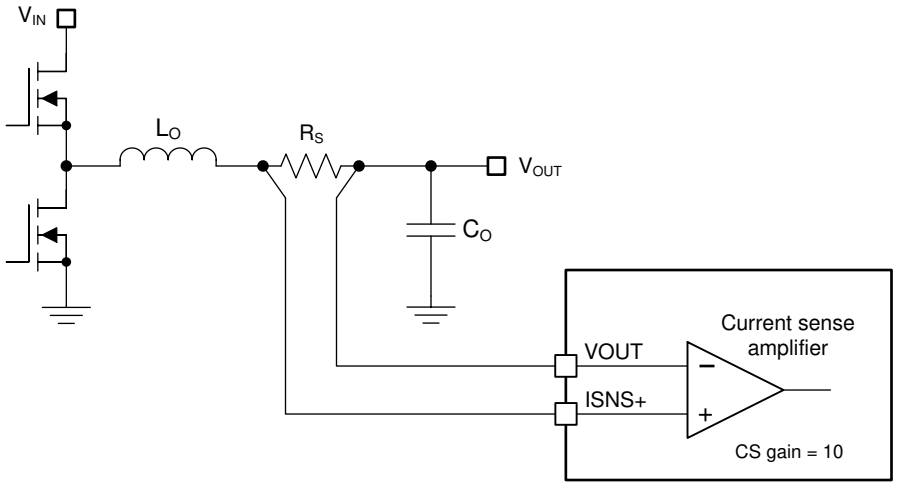

图 8-4. Shunt Current Sensing Implementation

The SS voltage is clamped 150 mV above FB during an overcurrent condition. Sixteen overcurrent events must occur before the SS clamp is enabled. This ensures that SS can be pulled low during brief overcurrent events, preventing output voltage overshoot during recovery.

8.3.13.2 Inductor DCR Current Sensing

For high-power applications that do not require accurate current-limit protection, inductor DCR current sensing is preferable. This technique provides lossless and continuous monitoring of the inductor current using an RC sense network in parallel with the inductor. Select an inductor with a low DCR tolerance to achieve a typical current limit accuracy within the range of 10% to 15% at room temperature. Components R_{CS} and C_{CS} in 图 8-5 create a low-pass filter across the inductor to enable differential sensing of the voltage across the inductor DCR.

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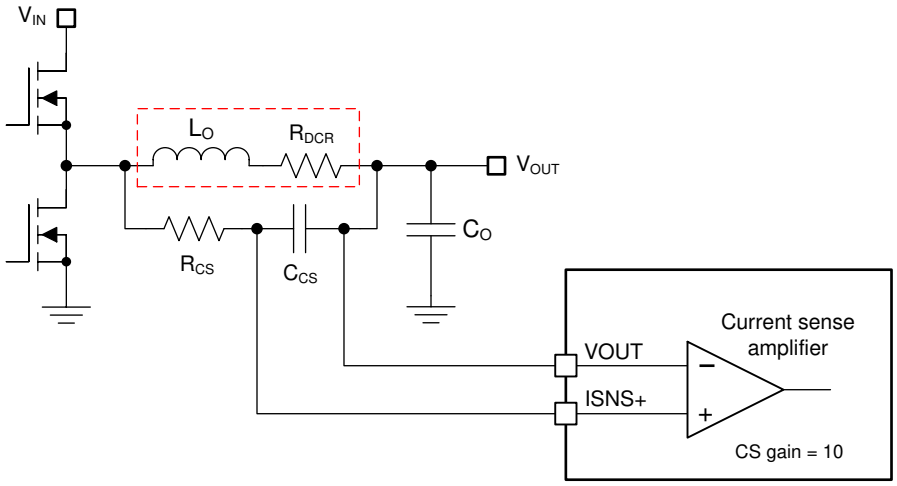

图 8-5. Inductor DCR Current Sensing Implementation

The voltage drop across the sense capacitor in the s-domain is given by 方程式 10. When the $R_{CS}C_{CS}$ time constant is equal to L_O/R_{DCR}, the voltage developed across the sense capacitor, C_{CS}, is a replica of the inductor DCR voltage and accurate current sensing is achieved. If the $R_{CS}C_{CS}$ time constant is not equal to the L_O/R_{DCR} time constant, there is a sensing error as follows:

- $R_{CS}C_{CS} > L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is attenuated.
- $R_{CS}C_{CS} < L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is amplified.

$$V_{CS}(s) = \frac{1 + s \cdot \frac{L_O}{R_{DCR}}}{1 + s \cdot R_{CS} \cdot C_{CS}} \cdot R_{DCR} \cdot \left(I_{OUT(CL)} + \frac{\Delta I_L}{2} \right) \quad (10)$$

Choose the C_{CS} capacitance greater than or equal to 0.1 μF to maintain a low-impedance sensing network, thus reducing the susceptibility of noise pickup from the switch node. Carefully observe 节 *11.1* to make sure that noise and DC errors do not corrupt the current sense signals applied between the ISNS+ and VOUT pins.

8.3.14 Hiccup Mode Current Limiting

The LM25149 includes an internal hiccup-mode protection function. After an overload is detected, 512 cycles of cycle-by-cycle current limiting occurs. The 512-cycle counter is reset if four consecutive switching cycles occur without exceeding the current limit threshold. Once the 512-cycle counter has expired, the internal soft start is pulled low, the HO and LO driver outputs are disabled, and the 16384 counter is enabled. After the counter reaches 16384, the internal soft start is enabled and the output restarts. The hiccup-mode current limit is disabled during soft start until the FB voltage exceeds 0.4 V.

8.3.15 High-Side and Low-Side Gate Drivers (HO, LO)

The LM25149 contains N-channel MOSFET gate drivers and an associated high-side level shifter to drive the external N-channel MOSFET. The high-side gate driver works in conjunction with an internal bootstrap diode D_{BOOT} and bootstrap capacitor C_{BOOT}. During the conduction interval of the low-side MOSFET, the SW voltage is approximately 0 V and C_{BOOT} charges from VCC through the internal D_{BOOT}. TI recommends a 0.1-μF ceramic capacitor connected with short traces between the C_{BOOT} and SW pins.

The LO and HO outputs are controlled with an adaptive dead-time methodology so that both outputs (HO and LO) are never on at the same time, preventing cross conduction. Before the LO driver output is allowed to turn on, the adaptive dead-time logic first disables HO and waits for the HO-SW voltage to drop below 2.0 V typical. LO is allow to turn on after a small delay (HO fall to LO rising delay). Similarly, the HO turnon is delayed until the LO voltage has dropped below 2.0 V. This technique ensures adequate dead-time for any size N-channel MOSFET component or parallel MOSFET configurations.

Caution is advised when adding series gate resistors, as this can impact the effective dead-time. The selected N-channel high-side MOSFET determines the appropriate bootstrap capacitance value C_{BOOT} in according to 方程式 11.

$$C_{BOOT} = \frac{Q_G}{\Delta V_{CBOOT}} \tag{11}$$

where

- Q_G is the total gate charge of the high-side MOSFET at the applicable gate drive voltage
- ΔV_{BOOT} is the voltage variation of the high-side MOSFET driver after turnon

To determine C_{BOOT}, choose ΔV_{BOOT} so that the available gate drive voltage is not significantly impacted. An acceptable range of ΔV_{BST} is 100 mV to 300 mV. The bootstrap capacitor must be a low-ESR ceramic capacitor, typically 0.1 µF. Use high-side and low-side MOSFETs with logic-level gate threshold voltages.

表 8-2. Errata

ITEM	OBSERVED BEHAVIOR	ROOT CAUSE	COMMENTS
1	Early zero-cross detection just above 20% load, LO turns off early.	Root cause identified	Solution is to use an external Boot diode with A0 silicon. A1 silicon will not require an external Boot diode.

8.3.16 Output Configurations (CNFG)

The LM25149 can be configured as a primary controller (interleaved mode) or as a secondary controller for paralleling the outputs for high-current applications with a resistor R_{CNFG}. This resistor also configures if Spread Spectrum is enabled or disabled. See 表 8-3. Once the VCC voltage is above 3.3 V (typical), the CNFG pin is monitored and latched. The configuration cannot be changed on the fly the LM25149 must be powered down, and VCC must drop below 3.3 V. 图 8-6 shows the configuration timing diagram.

When the LM25149 is configured with Spread Spectrum enabled, as a primary controller with spread spectrum (R_{CNFG} 41.2 kΩ or 71.5 kΩ), the LM25149 cannot be synchronized to an external clock.

表 8-3. Configuration Modes

R_{CNFG}	PRIMARY/ SECONDARY	SPREAD SPECTRUM	DUAL-PHASE
29.9 kΩ	Primary	OFF	Disabled
41.2 kΩ	Primary	ON	Disabled
54.9 kΩ	Primary	OFF	Enabled
71.5 kΩ	Primary	ON	Enabled
90.9 kΩ	Secondary	N/A	Enabled

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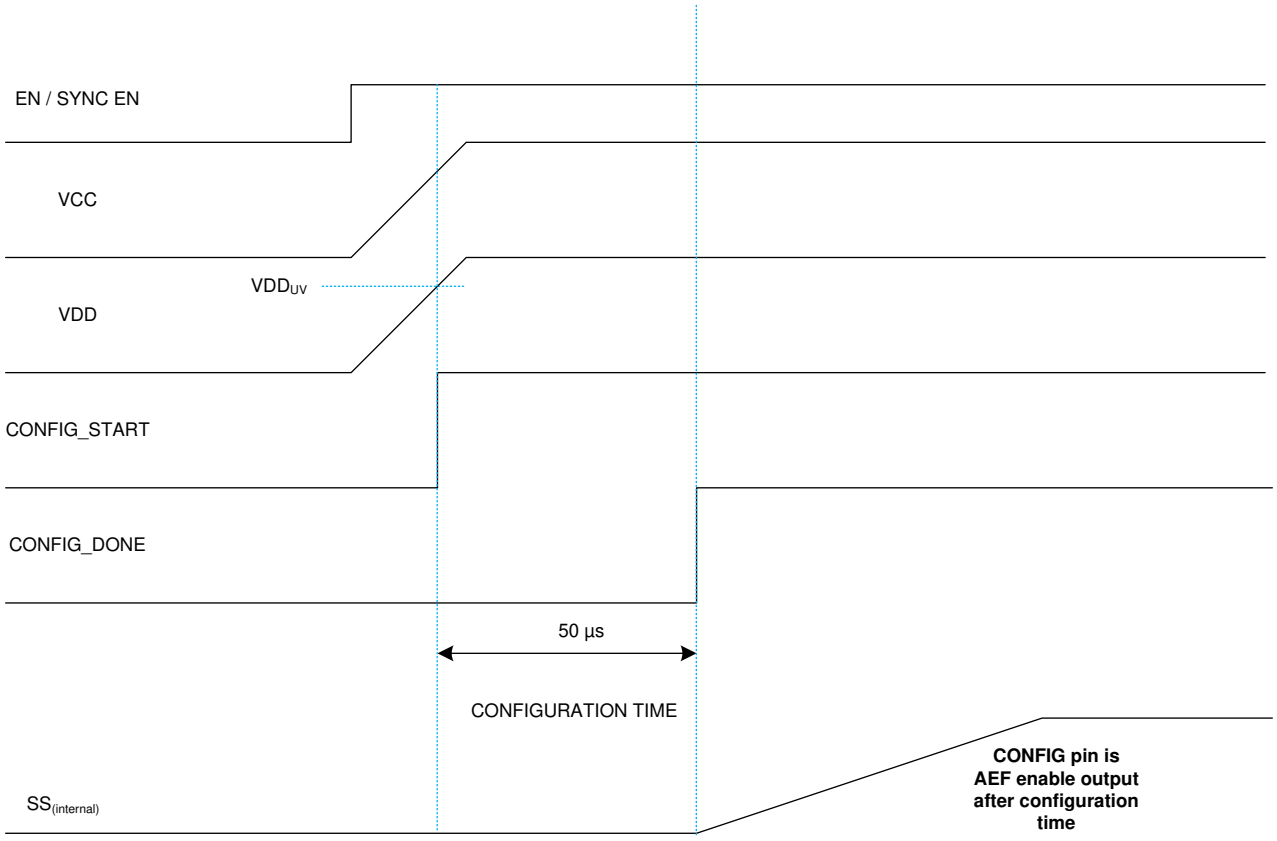

图 8-6. Configuration Timing

After the configuration has been latched, the CNFG pin become an enable input for active EMI filter, where a logic high (> 2 V) enables active EMI filter and a logic low (< 0.8 V) disabled AEF.

8.3.17 Single-Output Two-phase Operation

To configure for two-phase operation, two LM25149 controllers are required. The LM25149 can only be configured in a single or dual-phase configuration. Additional phases cannot be added. Refer to 图 8-7. Configure the first controller (CNTRL1) as a primary controller and the second controller (CNTRL2) as a secondary. To configure CNTRL1 as a primary controller, install a 54-kΩ or a 71.5-kΩ resistor from CNFG to AGND. To configure the CNTRL2 as a secondary controller, install a 90.9-kΩ resistor from CNFG to AGND. This disables the error amplifier of CNTRL2, placing it into a high-impedance state. Connect the EXTCOMP pins of the primary and secondary together. The PG/SYNCOUT of the primary is a logic-level output. Refer to 节 7.5 for voltage levels. Connect PG/SYNCOUT of the primary to PFM/SYNC (SYNCIN) of the secondary controller. The SYNCOUT of the primary controller is 180° out-of-phase and facilitates interleaved operation. RT is not used for the oscillator when the LM25149 is in secondary controller mode, but instead is used for slope compensation. Therefore, select the RT resistance to be the same as that of the primary controller. The oscillator is derived from the primary controller. When in primary/secondary mode, enable both controllers simultaneously for start-up. After the power supply has started, pull the secondary EN pin low (< 0.8 V) for phase shedding to reduce the I_Q current.

If an external SYNCIN signal is applied after start-up while in primary/secondary mode, there is a two-clock cycle delay before the LM25149 locks on to the external synchronization signal.

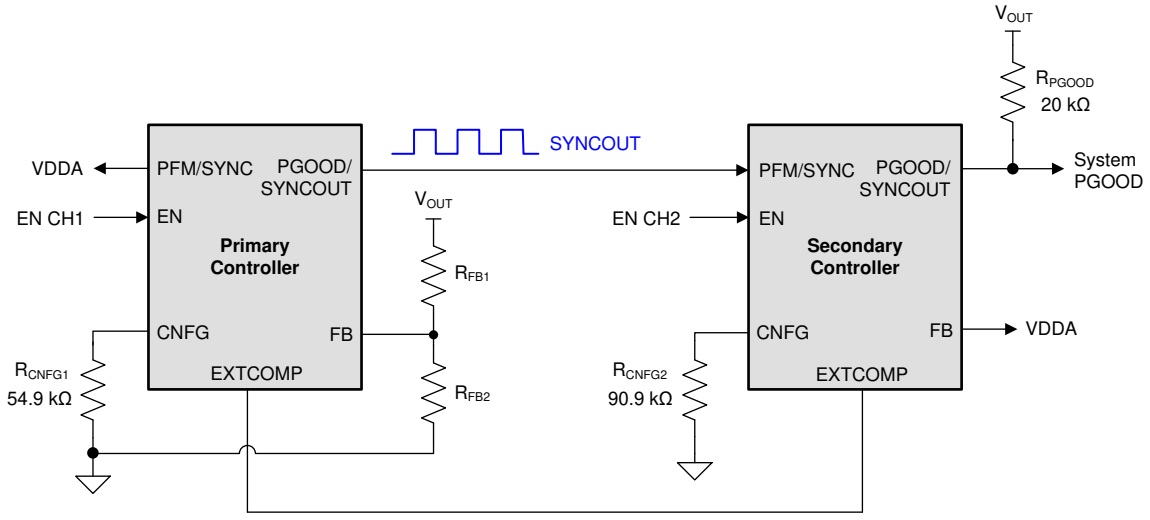

图 8-7. Schematic Configured for Single-Output Multi-Phase Operation

In PFM pulse skipping to reduce the I_Q current, the primary controller disables its synchronization clock output, so phase shedding is not supported. Phase shedding is supported in FPWM only. In FPWM, enable or disable the secondary controller as needed to support higher load current or better light-load efficency, respectively. When the secondary is disabled abd then re-enabled, its internal soft start is be pulled low and the LM25149 goes through a normal soft-start turnon.

For more information, see *Benefits of a Multiphase Buck Converter* and *Multiphase Buck Design From Start to Finish*.

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8.4 Device Functional Modes

8.4.1 Standby Modes

The LM25149 operates with peak current-mode control such that the compensation voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges very slowly. As a result, the compensation voltage does not demand the driver output pulses on a cycle-by-cycle basis. When the LM25149 controller detects 16 missed switching cycles, it enters standby mode and switches to a low I_Q state to reduce the current drawn from the input. For the LM25149 to go into standby mode, the controller must be programmed for diode emulation ($V_{PFM/SYNC}$ < 0.4 V).

In standby modes and normal mode, the typical low-I_Q is 9 μA with a 3.3-V output.

8.4.2 Pulse Frequency Modulation and Synchronization (PFM/SYNC)

A synchronous buck regulator implemented with a low-side synchronous MOSFET rather than a diode has the capability to sink negative current from the output during light-load, overvoltage, and pre-bias start-up conditions. The LM25149 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation mode, the low-side MOSFET is switched off when reverse current flow is detected by sensing of the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss during light-load conditions; the disadvantage of diode emulation mode is slower light-load transient response.

Diode emulation is configured with the PFM/SYNC pin. To enable diode emulation and thus achieve low-I_Q curren at light loads, connect PFM/SYNC to AGND. If FPWM or continuous conduction mode (CCM) operation is desired, tie PFM/SYNC to VDDA. Note that diode emulation is automatically engaged to prevent reverse current flow during a prebias start-up in PFM. A gradual change from DCM to CCM operation provides monotonic start-up performance.

To synchronize the LM25149 to an external source, apply a logic-level clock to the PFM/SYNC pin. The LM25149 can be synchronized to ±20% of the programmed frequency up to a maximum of 2.5 MHz. If there is an RT resistor and a synchronization signal, the LM25149 ignores the RT resistor and synchronizes to the external clock. Under low-V_{IN} conditions when the minimum off-time is reached, the synchronization signal is ignored, allowing the switching frequency to be reduce to maintain output voltage regulation.

8.4.3 Thermal Shutdown

The LM25149 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs.
2. Pulls SS and PG/SYNC low.
3. Turns off the VCC regulator.
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical).

This is a non-latching protection, and, as such, the device cycles into and out of thermal shutdown if the fault persists.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The following section discuss the output inductor, input and output capacitors, power MOSFETs, and EMI input filter.

9.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at nominal input voltage. Choose the inductance using 方程式 12 based on a peak inductor current given by 方程式 13.

$$L_O = \frac{V_{OUT}}{\Delta I_L \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{12}$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \tag{13}$$

Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current and higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as its core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

9.1.1.2 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is larger than that given by 方程式 14.

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$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot F_{SW} \sqrt{\Delta V_{OUT}^2 - \left(R_{ESR} \cdot \Delta I_L\right)^2}} \quad (14)$$

图 9-1 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as fast as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

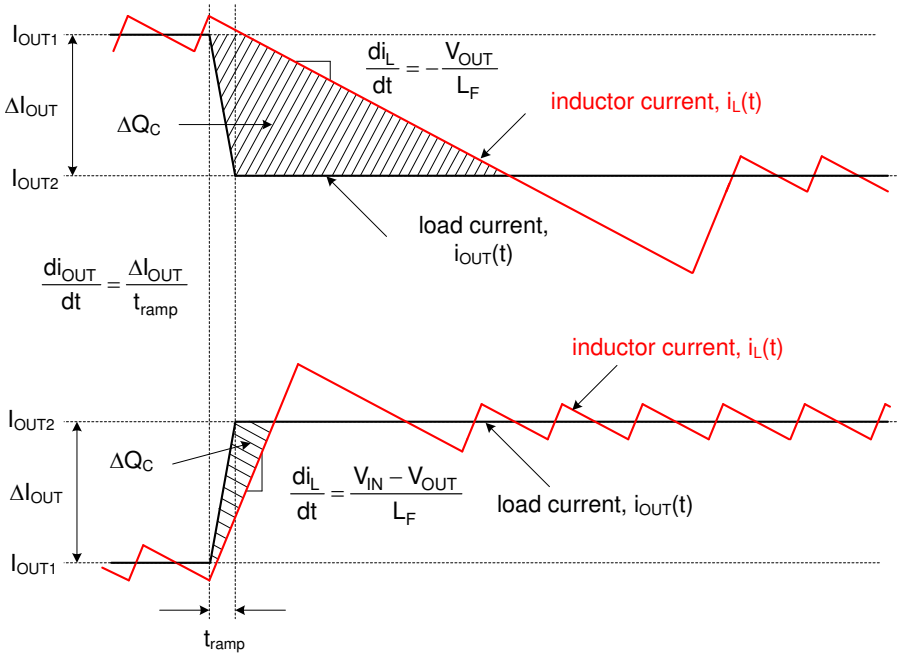

图 9-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 12-V input to low output voltage (for example, 3.3 V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT} / L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below its nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance should be larger than:

$$C_{OUT} \geq \frac{L_O \cdot \Delta I_{OUT}^2}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^2} \quad (15)$$

The ESR of a capacitor is provided in the manufacturer's data sheet either explicitly as a specification or implicitly in the impedance versus frequency curve. Depending on type, size, and construction, electrolytic capacitors have significant ESR, 5 mΩ and above, and relatively large ESL, 5 nH to 20 nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors, on the other hand, have

low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in 方程式 14 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Two to four 47-µF, 10-V, X7R capacitors in 1206 or 1210 footprint is a common choice for a 5-V output. Use 方程式 15 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with its low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with its large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

9.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. The input capacitor RMS current for a single-channel buck regulator is given by 方程式 16.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1-D) + \frac{\Delta I_L^2}{12} \right)} \tag{16}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the input capacitors should be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sinks I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage amplitude is given by 方程式 17.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \tag{17}$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by 方程式 18.

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \tag{18}$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and four 10-µF 50-V X7R ceramic decoupling capacitors are usually sufficient for 12-V battery automotive applications. Select the input bulk capacitor based on its ripple current rating and operating temperature range.

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Of course, a two-channel buck regulator with 180° out-of-phase interleaved switching provides input ripple current cancellation and reduced input capacitor current stress. The above equations represent valid calculations when one output is disabled and the other output is fully loaded.

9.1.1.4 Power MOSFETs

The choice of power MOSFETs has significant impact on DC/DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS}, respectively), and vice versa. As a result, the product of $R_{DS(on)}$ and Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance of a given package ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in a LM25149 application are as follows:

- $R_{DS(on)}$ at V_{GS} = 5 V
- Drain-source voltage rating, BV_{DSS}, typically 40 V, 60 V, or 80 V, depending on the maximum input voltage
- Gate charge parameters at V_{GS} = 5 V
- Output charge, Q_{OSS}, at the relevant input voltage
- Body diode reverse recovery charge, Q_{RR}
- Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G versus V_{GS} plot in the MOSFET data sheet. With a Miller plateau voltage typically in the range of 2 V to 3 V, the 5-V gate drive amplitude of the LM25149 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

The MOSFET-related power losses for one channel are summarized by the equations presented in 表 9-1, where suffixes one and two represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included. Consult the *Quickstart Calculator*, available for download from the LM25149 product folder, to assist with power loss calculations.

表 9-1. MOSFET Power Losses

POWER LOSS MODE	HIGH-SIDE MOSFET	LOW-SIDE MOSFET
MOSFET conduction(2) (3)	$P_{cond1} = D \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)1}$	$P_{cond2} = D' \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)2}$
MOSFET switching	$P_{sw1} = \frac{V_{IN} \cdot F_{SW}}{2} \left[\left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_R + \left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_F \right]$	Negligible
MOSFET gate drive(1)	$P_{Gate1} = V_{CC} \cdot F_{SW} \cdot Q_{G1}$	$P_{Gate2} = V_{CC} \cdot F_{SW} \cdot Q_{G2}$
MOSFET output charge(4)	$P_{Coss} = F_{SW} \cdot (V_{IN} \cdot Q_{oss2} + E_{oss1} - E_{oss2})$	
Body diode conduction	N/A	$P_{cond_{BD}} = V_F \cdot F_{SW} \left[\left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_{dt1} + \left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_{dt2} \right]$
Body diode reverse recovery(5)	$P_{RR} = V_{IN} \cdot F_{SW} \cdot Q_{RR2}$	

(1) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally added series gate resistance and the relevant driver resistance of the LM25149.
(2) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500 ppm/°C. The MOSFET junction temperature, T_J, and its rise over ambient temperature is dependent upon the device total power dissipation and its thermal impedance. When operating at or near minimum input voltage, make sure that the MOSFET $R_{DS(on)}$ is rated for the available gate drive voltage.
(3) D' = 1 – D is the duty cycle complement.
(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turnoff. During turnon, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turnon, but this is offset by the stored energy E_{oss2} on C_{oss2}.
(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on-time (or D interval) and typically incurs most of the switching losses. It is, therefore, imperative to choose a high-side MOSFET that balances conduction and switching loss contributions. The total power dissipation in the high-side MOSFET is the sum of the losses due to conduction, switching (voltage-current overlap), output charge, and typically two-thirds of the net loss attributed to body diode reverse recovery.

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1 – D interval). The low-side MOSFET switching loss is negligible as it is switched at zero voltage – current just commutates from the channel to the body diode or vice versa during the transition deadtimes. LM25149, with its adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, it is critical to optimize the low-side MOSFET for low $R_{DS(on)}$. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery. The LM25149 is well suited to drive TI's portfolio of NexFET™ power MOSFETs.

9.1.1.5 EMI Filter

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^{2}}{P_{IN}} \right| \tag{19}$$

The Passive EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
- Input filter inductor L_{IN} is usually selected between 1 μH and 10 μH, but it can be lower to reduce losses in a high-current design.
- Calculate input filter capacitor C_F.

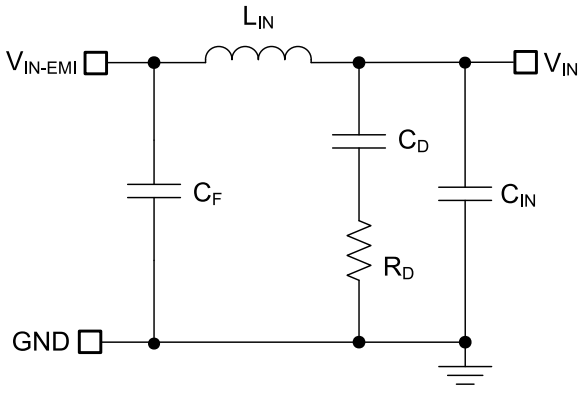

图 9-2. Passive π-Stage EMI Filter for Buck Regulator

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying it by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by 方程式 20.

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$$Attn = 20\log\left(\frac{I_{L(PEAK)}}{\pi^2 \cdot F_{SW} \cdot C_{IN}} \cdot \sin(\pi \cdot D_{MAX}) \cdot \frac{1}{1\,\mu V}\right) - V_{MAX} \quad (20)$$

where

- V_{MAX} is the allowed dB μ V noise level for the applicable conducted EMI specification, for example CISPR 25 Class 5
- C_{IN} is the existing input capacitance of the buck regulator
- D_{MAX} is the maximum duty cycle
- I_{PEAK} is the peak inductor current

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the passive EMI filter capacitance C_F from 方程式 21.

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \cdot F_{SW}}\right)^2 \quad (21)$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small so that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. The resonant frequency of the passive filter is given by 方程式 22.

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{IN} \cdot C_F}} \quad (22)$$

The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D should have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added input damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for input damping with a value given by 方程式 23.

$$C_D \geq 4 \cdot C_{IN} \quad (23)$$

Select the input damping resistor R_D using 方程式 24.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (24)$$

9.1.2 Error Amplifier and Compensation

A Type-II compensator using a transconductance error amplifier (EA) is shown in 图 9-3. The dominant pole of the EA open-loop gain is set by the EA output resistance, $R_{O\text{-}EA}$, and effective bandwidth-limiting capacitance, C_{BW}, as shown by 方程式 25.

$$G_{EA(open\,loop)}(s) = -\frac{g_m \cdot R_{O\text{-}EA}}{1 + s \cdot R_{O\text{-}EA} \cdot C_{BW}} \quad (25)$$

The EA high-frequency pole is neglected in the above expression. The compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network, is calculated in 方程式 26.

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \cdot \frac{g_m \cdot R_{O\text{-}EA} \cdot \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{26}$$

where

- V_{REF} is the feedback voltage reference of 0.8 V
- g_m is the EA gain transconductance of 1200 µS
- $R_{O\text{-}EA}$ is the error amplifier output impedance of 64 MΩ

$$\omega_{Z1} = \frac{1}{R_{COMP} \cdot C_{COMP}} \tag{27}$$

$$\omega_{p1} = \frac{1}{R_{O\text{-}EA} \cdot \left(C_{COMP} + C_{HF} + C_{BW}\right)} \cong \frac{1}{R_{O\text{-}EA} \cdot C_{COMP}} \tag{28}$$

$$\omega_{p2} = \frac{1}{R_{COMP} \cdot \left(C_{COMP} \left\| \left(C_{HF} + C_{BW}\right)\right.\right)} \cong \frac{1}{R_{COMP} \cdot C_{HF}} \tag{29}$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, R_{COMP} << $R_{O\text{-}EA}$ and C_{COMP} >> C_{BW} and C_{HF}, so the approximations are valid.

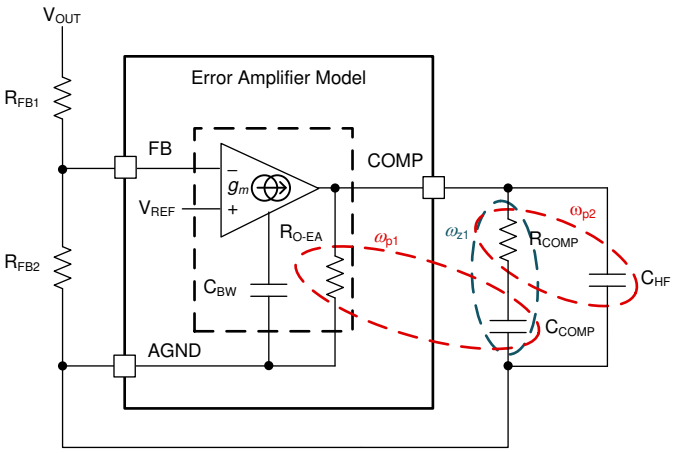

图 9-3. Error Amplifier and Compensation Network

9.2 Typical Application

图 9-4 shows the schematic diagram of a single-output synchronous buck regulator with output voltage of 5 V and a rated load current of 8 A. In this example, the target half-load and full-load efficiencies are 93.5% and 92.5%, respectively, based on a nominal input voltage of 12 V that ranges from 5.5 V to 36 V. The switching frequency is set at 2.1 MHz by resistor R_{RT}. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve efficiency. An output voltage of 3.3 V is also feasible simply by connecting FB to VDDA.

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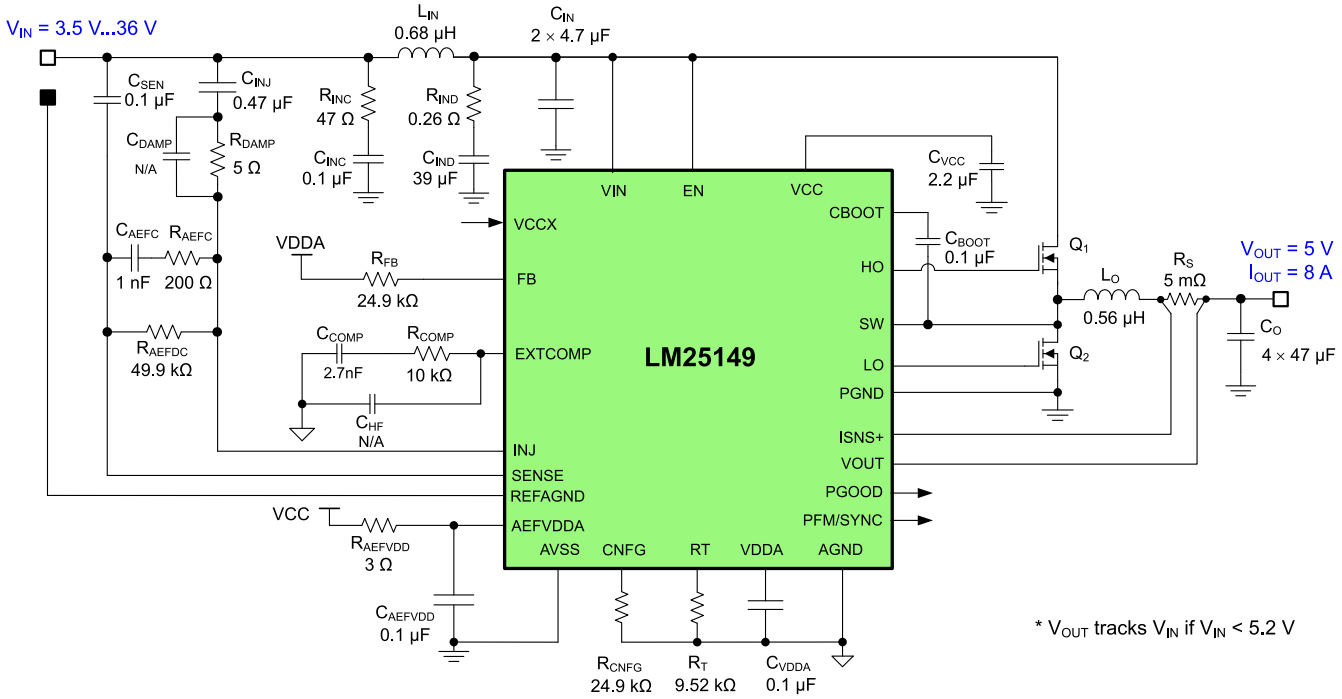

图 9-4. Application Circuit 1 With LM25149 Buck Regulator at 2.1 MHz

Note

This and subsequent design examples are provided herein to showcase the LM25149 controller in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to ensure stability, particularly at low input voltage and high output current operating conditions. See *节 10* for more detail.

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9.2.1 Design Requirements

表 9-2 shows the intended input, output, and performance parameters for this automotive design example.

表 9-2. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	8 V to 18 V
Min transient input voltage (cold crank)	5.5 V
Max transient input voltage (load dump)	36 V
Output voltage	5 V
Output current	8 A
Switching frequency	2.1 MHz
Output voltage regulation	±1%
Standby current, no-load	10 µA
Shutdown current	2.2 µA
Soft-start time	3 ms

The switching frequency is set at 2.1 MHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 60 kHz with a phase margin greater than 50°.

The selected buck regulator powertrain components are cited in 表 9-3, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in 节 *9.1.1.4*. This design uses a low-DCR, metal-powder composite inductor, and ceramic output capacitor implementation.

表 9-3. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	2	10 µF, 50 V, X7S, 1210, ceramic	Taiyo Yuden	UMJ325KB7106KMHT
			Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106K250AB
C_O	4	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47 µF, 10 V, X7S, 1210, ceramic	TDK	CGA6P1X7S1A476M250AC
L_O	1	0.56 µH, 3.6 mΩ, 13 A, 6.6 × 6.6 × 4.8 mm	Würth Electronik	744373490056
		0.68 µH, 4.5 mΩ, 22 A, 6.95 × 6.6 × 2.8 mm	Cyntec	VCMV063T-R68MN2T
Q_1	1	40 V, 4.6 mΩ, 7 nC, SON 5 × 6	Infineon	IAUC60N04S6L039
Q_2	1	40 V, 3.7 mΩ, 9 nC, SON 5 × 6	Infineon	IAUC80N04S6L032
R_S	1	Shunt, 5 mΩ, 0508, 1 W	Susumu	KRL2012E-M-R005-F-T5
U_1	1	LM2514942-V buck controller	Texas Instruments	LM25149RGYR

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9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25149 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Custom Design With Excel Quickstart Tool

Select components based on the regulator specifications using the *Quickstart Calculator* available for download from the LM25149 product folder.

9.2.2.3 Buck Inductor

1. Use 方程式 30 to calculate the required buck inductance based on a 30% inductor ripple current at nominal input voltages.

$$L_O = \frac{V_{OUT}}{\Delta I_{LO} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) = \frac{5\,V}{2.4\,A \cdot 2.1\,MHz} \cdot \left(1 - \frac{5\,V}{12\,V}\right) = 0.58\,\mu H \tag{30}$$

2. Select a standard inductor value of 0.56 µH. Use 方程式 31 to calculate the peak inductor currents at maximum steady-state input voltage. Subharmonic oscillation occurs with a duty cycle greater than 50% for peak current-mode control. For design simplification, the LM25149 has an internal slope compensation ramp proportional to the switching frequency that is added to the current sense signal to damp any tendency toward subharmonic oscillation.

$$I_{LO(PK)} = I_{OUT} + \frac{\Delta I_{LO}}{2} = I_{OUT} + \frac{V_{OUT}}{2 \cdot L_O \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) = 8\,A + \frac{5\,V}{0.56\,\mu H \cdot 2.1\,MHz} \cdot \left(1 - \frac{5\,V}{18\,V}\right) = 9.53\,A \tag{31}$$

3. Based on 方程式 8, use 方程式 32 to cross-check the inductance to set a slope compensation close to the ideal one times the inductor current downslope.

$$L_{O(sc)} = \frac{V_{OUT} \cdot R_S}{24 \cdot F_{SW}} = \frac{5\,V \cdot 5\,m\Omega}{24 \cdot 2.1\,MHz} = 0.5\,\mu H \tag{32}$$

9.2.2.4 Current-Sense Resistance

1. Calculate the current-sense resistance based on a maximum peak current capability of at least 25% higher than the peak inductor current at full load to provide sufficient margin during start-up and load-on transients. Calculate the current sense resistances using 方程式 33.

$$R_S = \frac{V_{CS\text{-}TH}}{1.25 \cdot I_{LO(PK)}} = \frac{60\,mV}{1.25 \cdot 9.53\,A} = 5.04\,m\Omega \tag{33}$$

where

- V_{CS-TH} is the 60-mV current limit threshold

2. Select a standard resistance value of 5 mΩ for the shunt. An 0508 footprint component with wide aspect ratio termination design provides 1-W power rating, low parasitic series inductance, and compact PCB layout. Carefully adhere to the layout guidelines in 节 *11.1* to make sure that noise and DC errors do not corrupt the differential current-sense voltages measured at the ISNS+ and VOUT pins.
3. Place the shunt resistor close to the inductor.
4. Use Kelvin-sense connections, and route the sense lines differentially from the shunt to the LM25149.
5. The CS-to-output propagation delay (related to the current limit comparator, internal logic, and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay $t_{DELAY-ISNS+}$ of 40 ns, use 方程式 34 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LO-PK(SC)} = \frac{V_{CS-TH}}{R_S} + \frac{V_{IN(max)} \cdot t_{DELAY-ISNS+}}{L_O} = \frac{60\,mV}{5\,m\Omega} + \frac{18\,V \cdot 45\,ns}{0.56\,\mu H} = 13.5\,A \quad (34)$$

6. Based on this result, select an inductor with saturation current greater than 16 A across the full operating temperature range.

9.2.2.5 Output Capacitors

1. Use 方程式 35 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load) assuming a load transient deviation specification of 1.5% (75 mV for a 5-V output).

$$C_{OUT} \geq \frac{L_O \cdot \Delta I_{OUT}^{\,2}}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^{\,2}} = \frac{0.56\,\mu H \cdot (8\,A)^2}{(5\,V + 75\,mV)^2 - (5\,V)^2} = 47.4\,\mu F \quad (35)$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select four 47-µF, 10-V, X7S, 1210 ceramic output capacitors. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory.
3. Use 方程式 36 to estimate the peak-peak output voltage ripple at nominal input voltage.

$$\Delta V_{OUT} = \sqrt{\left(\frac{\Delta I_{LO}}{8 \cdot F_{SW} \cdot C_{OUT}}\right)^2 + \left(R_{ESR} \cdot \Delta I_{LO}\right)^2} = \sqrt{\left(\frac{2.54\,A}{8 \cdot 2.1\,MHz \cdot 44\,\mu F}\right)^2 + \left(1\,m\Omega \cdot 2.54\,A\right)^2} = 4.3\,mV \quad (36)$$

where

- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors
- 44 µF is the total effective (derated) ceramic output capacitance at 5 V

4. Use 方程式 37 to calculate the output capacitor RMS ripple current using and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO(RMS)} = \frac{\Delta I_{LO}}{\sqrt{12}} = \frac{2.54\,A}{\sqrt{12}} = 0.73\,A \quad (37)$$

9.2.2.6 Input Capacitors

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage. As mentioned earlier, dual-channel interleaved operation significantly reduces the input ripple amplitude. In general, the ripple current splits between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

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1. Select the input capacitors with sufficient voltage and RMS ripple current ratings.
2. Use 方程式 38 to calculate the input capacitor RMS ripple current assuming a worst-case duty-cycle operating point of 50%.

$$I_{CIN(RMS)} = I_{OUT} \cdot \sqrt{D \cdot (1-D)} = 8A \cdot \sqrt{0.5 \cdot (1-0.5)} = 4\,A \tag{38}$$

3. Use 方程式 39 to find the required input capacitance.

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} = \frac{0.5 \cdot (1-0.5) \cdot 8\,A}{2.1MHz \cdot (120\,mV - 2m\Omega \cdot 8\,A)} = 9.2\ \mu F \tag{39}$$

where

- ΔV_{IN} is the input peak-to-peak ripple voltage specification
- R_{ESR} is the input capacitor ESR

4. Recognizing the voltage coefficient of ceramic capacitors, select two 10-µF, 50-V, X7R, 1210 ceramic input capacitors. Place these capacitors adjacent to the power MOSFETs. See 节 *11.1.1* for more detail.
5. Use four 10-nF, 50-V, X7R, 0603 ceramic capacitors near the high-side MOSFET to supply the high di/dt current during MOSFET switching transitions. Such capacitors offer high self-resonant frequency (SRF) and low effective impedance above 100 MHz. The result is lower power loop parasitic inductance, thus minimizing switch-node voltage overshoot and ringing for lower conducted and radiated EMI signature. Refer to 节 *11.1* for more detail.

9.2.2.7 Frequency Set Resistor

Calculate the RT resistance for a switching frequency of 2.1 MHz using 方程式 40. Choose a standard E96 value of 9.53 kΩ.

$$R_T(k\Omega) = \frac{\frac{10^6}{F_{SW}(kHz)} - 53}{45} = \frac{\frac{10^6}{2100\,kHz} - 53}{45} = 9.4k\Omega \tag{40}$$

9.2.2.8 Feedback Resistors

If an output voltage setpoint other than 3.3 V or 5 V is required (or to measure a bode plot when using either of the fixed output voltage options), determine the feedback resistances using 方程式 41.

$$R_{FB1} = R_{FB2} \cdot \left(\frac{V_{OUT1}}{V_{REF}} - 1 \right) = 15k\Omega \cdot \left(\frac{5\,V}{1.2\,V} - 1 \right) = 47.5k\Omega \tag{41}$$

9.2.2.9 Compensation Components

Choose compensation components for a stable control loop using the procedure outlined as follows:

1. Based on a specified loop gain crossover frequency, f_C, of 60 kHz, use 方程式 42 to calculate R_{COMP}, assuming an effective output capacitance of 100 µF. Choose a standard value for R_{COMP} of 10 kΩ.

$$R_{COMP} = 2\pi \cdot f_C \cdot \frac{V_{OUT}}{V_{REF}} \cdot \frac{R_S \cdot G_{CS}}{g_m} \cdot C_{OUT} = 2\pi \cdot 60kHz \cdot \frac{5\,V}{0.8\,V} \cdot \frac{5m\Omega \cdot 10}{1200\,\mu S} \cdot 100\,\mu F = 9.82k\Omega \tag{42}$$

2. To provide adequate phase boost at crossover while also allowing a fast settling time during a load or line transient, select C_{COMP} to place a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Choose a standard value for C_{COMP} of 2.7 nF.

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$$C_{COMP} = \frac{10}{2\pi \cdot f_C \cdot R_{COMP}} = \frac{10}{2\pi \cdot 60\,kHz \cdot 10\,k\Omega} = 2.65\ nF \quad (43)$$

Such a low capacitance value also helps to avoid output voltage overshoot when recovering from dropout (when the input voltage is less than the output voltage setpoint and V_{COMP} is railed high).

3. Calculate C_{HF} to create a pole at the ESR zero and to attenuate high-frequency noise at COMP. C_{BW} is the bandwidth-limiting capacitance of the error amplifier. C_{HF} may not be significant enough to be necessary in some designs, like this one. C_{HF} can be unpopulated, or used with a small 22 pF for more noise filtering.

$$C_{HF} = \frac{1}{2\pi \cdot f_{ESR} \cdot R_{COMP}} - C_{BW} = \frac{1}{2\pi \cdot 500\,kHz \cdot 10\,k\Omega} - 31\,pF = 0.8\ pF \quad (44)$$

Note

Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

For technical solutions, industry trends, and insights for designing and managing power supplies, please refer to TI's technical articles.

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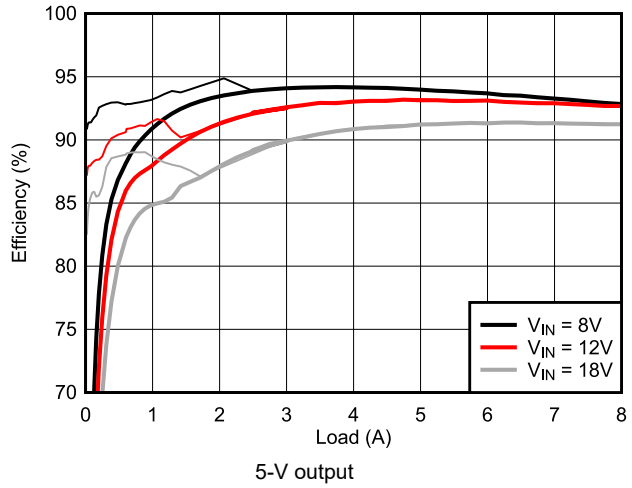
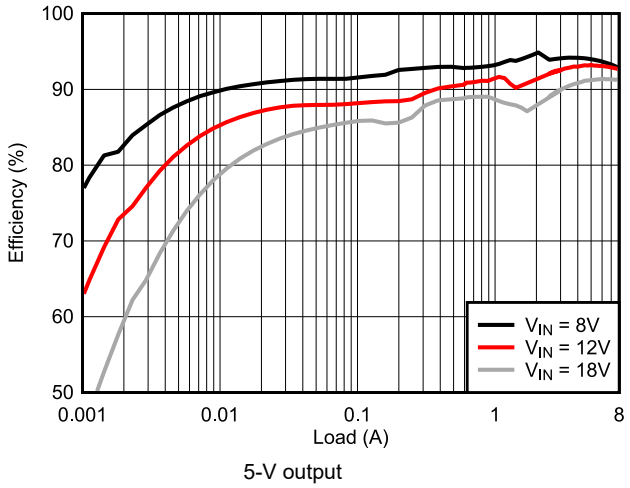
9.2.3 Application Curves



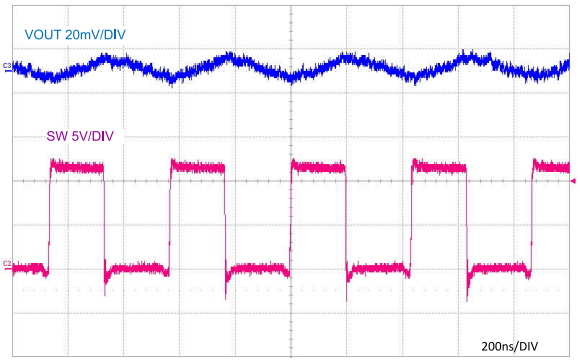
5-V output

图 9-5. Efficiency versus I_{OUT}



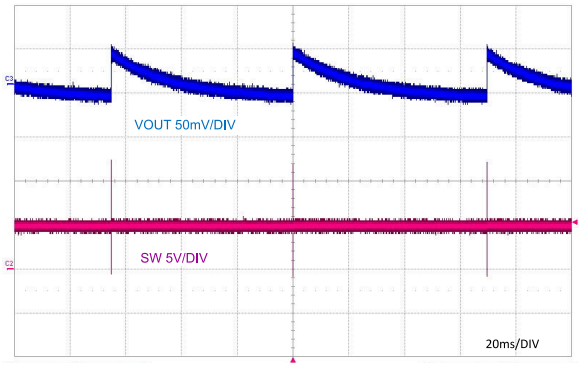
5-V output

图 9-6. Efficiency versus I_{OUT}, Log Scale



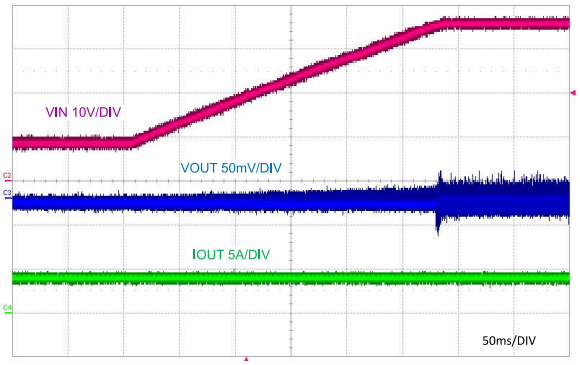
8-A resistive load

图 9-7. Full load Switching



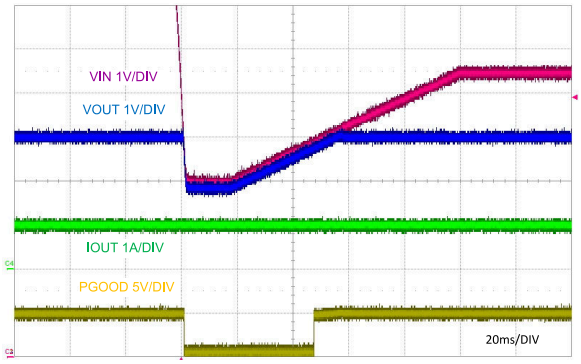
No load

图 9-8. PFM Switching



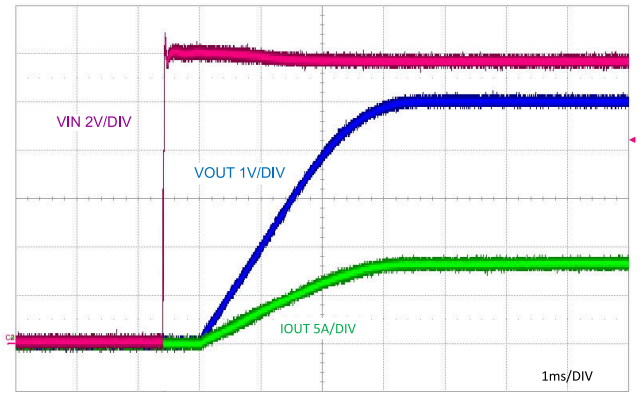
V_{IN} ramps from 12 to 40 V 5-A load

图 9-9. Line Transient



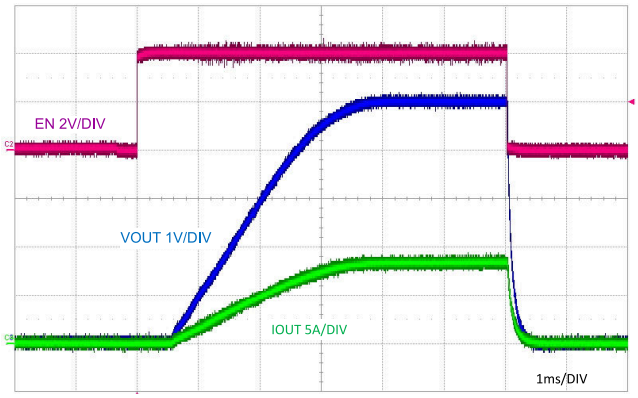
V_{IN} falls to 3.8 V 5-A load

图 9-10. Cold-Crank Response to V_{IN} = 3.8 V



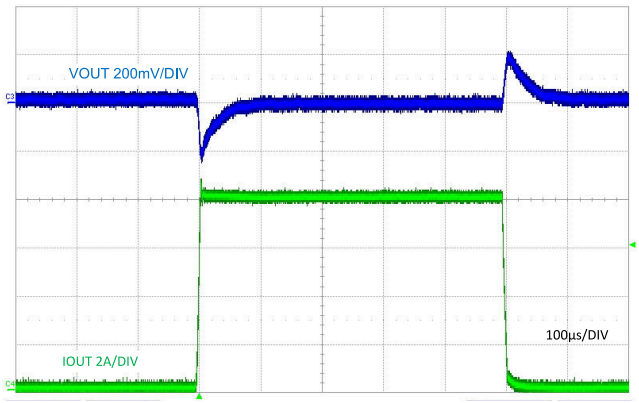
V_{IN} step to 12 V 8-A resistive load

图 9-11. Start-Up Characteristic



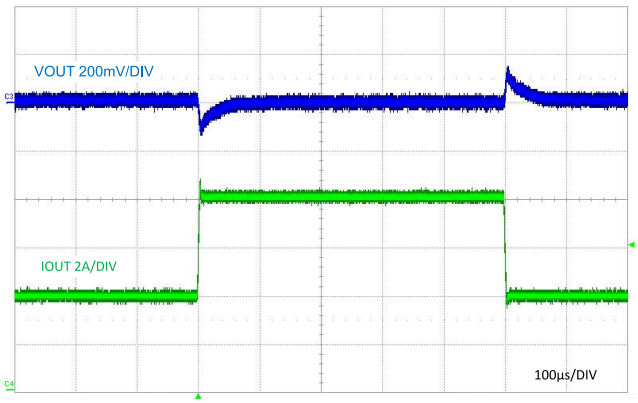
V_{IN} = 12 V 8-A resistive load

图 9-12. ENABLE ON and OFF Characteristic



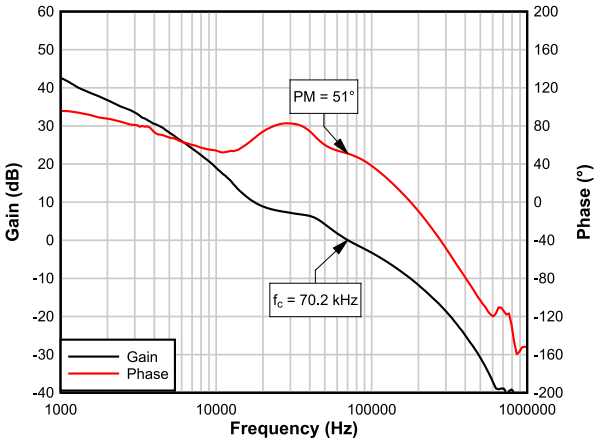
V_{IN} = 12 V FPWM

图 9-13. Load Transient, 0 A to 8 A



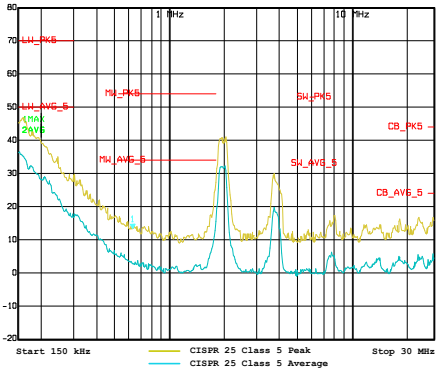
V_{IN} = 12 V FPWM

图 9-14. Load Transient, 4 A to 8 A



V_{IN} = 12 V 8-A resistive load

图 9-15. Bode Plot, 5-V Output



V_{IN} = 13.8 V 150 kHz to 30 MHz 7-A resistive load

图 9-16. CISPR 25 Class 5 Conducted EMI

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10 Power Supply Recommendations

The LM25149 buck controller is designed to operate from a wide input voltage range of 3.5 V to 80 V. The characteristics of the input supply must be compatible with 节 7.1 and 节 7.3. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with 方程式 45.

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \cdot \eta} \tag{45}$$

where

- η is the efficiency

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide parallel input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The application report *Simple Success with Conducted EMI for DC-DC Converters* (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

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11 Layout

11.1 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuit (with high current and voltage slew rates) to achieve a robust and reliable design. As expected, certain issues must be considered before designing a PCB layout using the LM25149. The high-frequency power loop of a buck regulator power stage is denoted by loop 1 in the shaded area of 图 11-1. The topological architecture of a buck regulator means that particularly high di/dt current flows in the components of loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important are the gate drive loops of the high-side and low-side MOSFETs, denoted by 2 and 3, respectively, in 图 11-1.

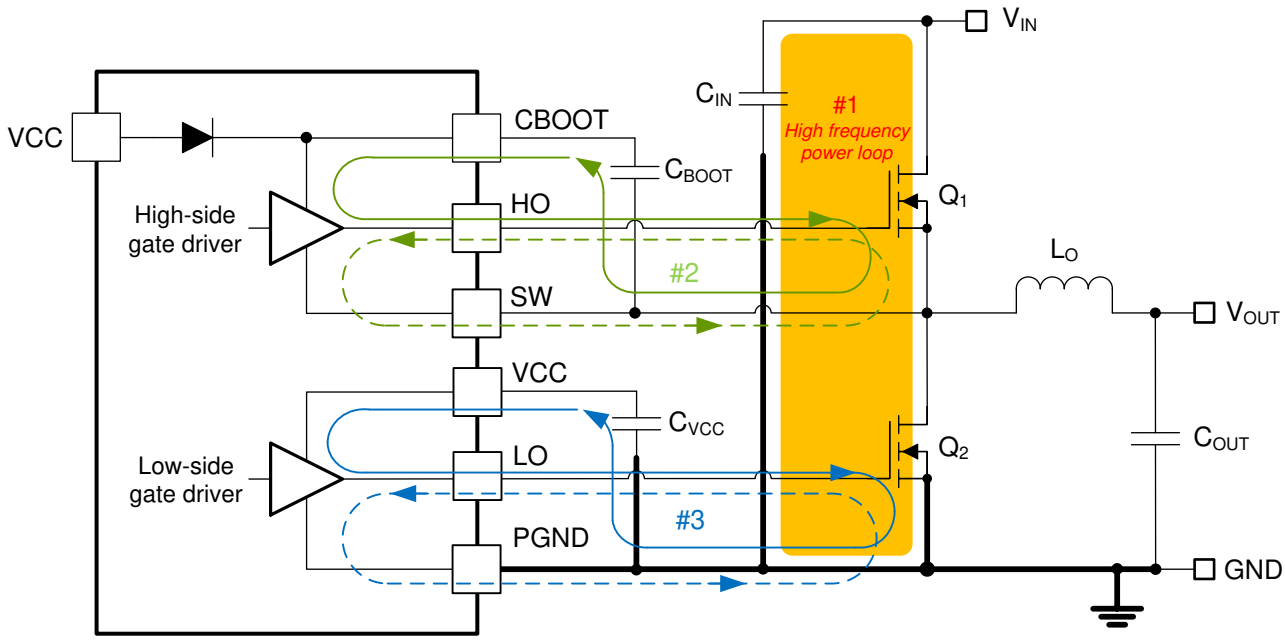

图 11-1. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

11.1.1 Power Stage Layout

1. Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). Insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
2. The DC/DC regulator has several high-current loops. Minimize the area of these loops in order to suppress generated switching noise and optimize switching performance.
   - Loop 1: The most important loop area to minimize is the path from the input capacitor or capacitors through the high- and low-side MOSFETs, and back to the capacitor or capacitors through the ground connection. Connect the input capacitor or capacitors negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor or capacitors positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop 1 of 图 11-1.
   - Another loop, not as critical as loop 1, is the path from the low-side MOSFET through the inductor and output capacitor or capacitors, and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor or capacitors at ground as close as possible.

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3. The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
4. Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
5. The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop 1 in 图 11-1 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (greater than 50 MHz) ringing at the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the PCB layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

11.1.2 Gate-Drive Layout

The LM25149 high-side and low-side gate drivers incorporate short propagation delays, adaptive dead-time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turnon and turnoff transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop 2: high-side MOSFET, Q_1. During the high-side MOSFET turnon, high current flows from the bootstrap (boot) capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace. Refer to loop 2 of 图 11-1.
- Loop 3: low-side MOSFET, Q_2. During the low-side MOSFET turnon, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground. Refer to loop 3 of 图 11-1.

TI strongly recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

1. Connections from gate driver outputs, HO and LO, to the respective gates of the high-side or low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Be aware that peak gate drive currents can be as high as 3.3 A. Use 0.65 mm (25 mils) or wider traces. Use via or vias, if necessary, of at least 0.5 mm (20 mils) diameter along these traces. Route HO and SW gate traces as a differential pair from the LM25149 to the high-side MOSFET, taking advantage of flux cancellation.
2. Minimize the current loop path from the VCC and HB pins through their respective capacitors as these provide the high instantaneous current, up to 3.3 A, to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitor, C_{BST}, close to the CBOOT and SW pins of the LM25149 to minimize the area of loop 2 associated with the high-side driver. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the LM25149 to minimize the area of loop 3 associated with the low-side driver.

11.1.3 PWM Controller Layout

With the proviso to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

1. Separate power and signal traces, and use a ground plane to provide noise shielding.

2. Place all sensitive analog traces and components related to COMP, FB, ISNS+, and RT away from high-voltage switching nodes such as SW, HO, LO, or CBOOT to avoid mutual coupling. Use internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) and current sense (ISNS+ and VOUT) traces from power traces and components.
3. Locate the upper and lower feedback resistors (if required) close to the FB pin, keeping the FB trace as short as possible. Route the trace from the upper feedback resistor to the required output voltage sense point at the load.
4. Route the ISNS+ and VOUT sense traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor (if shunt current sensing is used) or to the sense capacitor (if inductor DCR current sensing is used).
5. Minimize the loop area from the VCC and VIN pins through their respective decoupling capacitors to the PGND pin. Locate these capacitors as close as possible to the LM25149.

11.1.4 Active EMI Layout

Active EMI layout is critical for enhanced EMI performance. Layout considerations are as follows:

1. Connect AVSS to a quiet GND connection, further from IC if possible. Keep decoupling capacitor $C_{AEFVDDA}$ close to the AEFVDDA pin and AVSS GND connection. See capacitor C23 in 图 11-2.
2. Route the SEN and INJ traces differentially as close together as possible on an internal quiet layer. Avoid noisy layer or layers carrying high-voltage traces.
3. Place the active EMI compensation components C_{AEFC}, R_{AEFC}, and R_{AEFDC} close together and near the V_{IN-EMI} node to the input filter inductor.
4. C_{SEN} and C_{INJ} components should be placed directly outside of the compensation loop.
5. Place input compensation components R_{AEFC} and C_{AEFC} nearby the other Active EMI components. Ensure the GND connection is far away from any noise sources. Do not connect the input compensation GND near the powerstage.
6. Route REFAGND directly to the GND of the input power connector. Do not tie to the GND plane connection. The REFAGND trace can partially shield the SEN and INJ differential pair on the way to the input power connector.

11.1.5 Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by the following:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input voltage (affecting bias regulator LDO voltage drop and hence its power dissipation)
- Thermal characteristics of the package and operating environment

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM25149 controller is available in a small 4-mm × 4-mm 24-pin VQFN PowerPAD package to cover a range of application requirements. 节 *11.1.5* summarizes the thermal metrics of this package.

The 24-pin VQFN package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate of the LM25149 device (ground). This allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The exposed pad of the LM25149 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal and solder-side ground plane or planes are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this provide a plane for the power stage currents to flow but it also represents a thermally conductive path away from the heat generating devices.

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The thermal characteristics of the MOSFETs also are significant. The drain pads of the high-side MOSFETs are normally connected to a VIN plane for heat sinking. The drain pads of the low-side MOSFETs are tied to the SW plane, but the SW plane area is purposely kept as small as possible to mitigate EMI concerns.

11.1.6 Ground Plane Design

As mentioned previously, TI recommends using one or more of the inner PCB layers as a solid ground plane. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. In particular, a full ground plane on the layer directly underneath the power stage components is essential. Connect the source terminal of the low-side MOSFET and return terminals of the input and output capacitors to this ground plane. Connect the PGND and AGND pins of the controller at the DAP and then connect to the system ground plane using an array of vias under the DAP. The PGND nets contain noise at the switching frequency and can bounce because of load current variations. The power traces for PGND, VIN, and SW can be restricted to one side of the ground plane, for example on the top layer. The other side of the ground plane contains much less noise and is ideal for sensitive analog trace routes.

11.2 Layout Example

图 11-2 shows a single-sided layout of a synchronous buck regulator with discrete power MOSFETs, Q1 and Q2, in SON 5-mm × 6-mm case size. The power stage is surrounded by a GND pad geometry to connect an EMI shield if needed. The design uses layer 2 of the PCB as a power-loop return path directly underneath the top layer to create a low-area switching power loop of approximately 2 mm². This loop area, and hence parasitic inductance, must be as small as possible to minimize EMI as well as switch-node voltage overshoot and ringing.

The high-frequency power loop current flows through MOSFETs Q1 and Q2, through the power ground plane on layer 2, and back to VIN through the 0603 ceramic capacitors C15 through C18. The currents flowing in opposing directions in the vertical loop configuration provide field self-cancellation, reducing parasitic inductance. 图 11-4 shows a side view to illustrate the concept of creating a low-profile, self-canceling loop in a multilayer PCB structure. The layer-2 GND plane layer, shown in 图 11-3, provides a tightly-coupled current return path directly under the MOSFETs to the source terminals of Q2.

Four 10-nF input capacitors with small 0402 or 0603 case size are placed in parallel very close to the drain of Q1. The low equivalent series inductance (ESL) and high self-resonant frequency (SRF) of the small footprint capacitors yield excellent high-frequency performance. The negative terminals of these capacitors are connected to the layer-2 GND plane with multiple 12-mil (0.3-mm) diameter vias, further minimizing parasitic loop inductance.

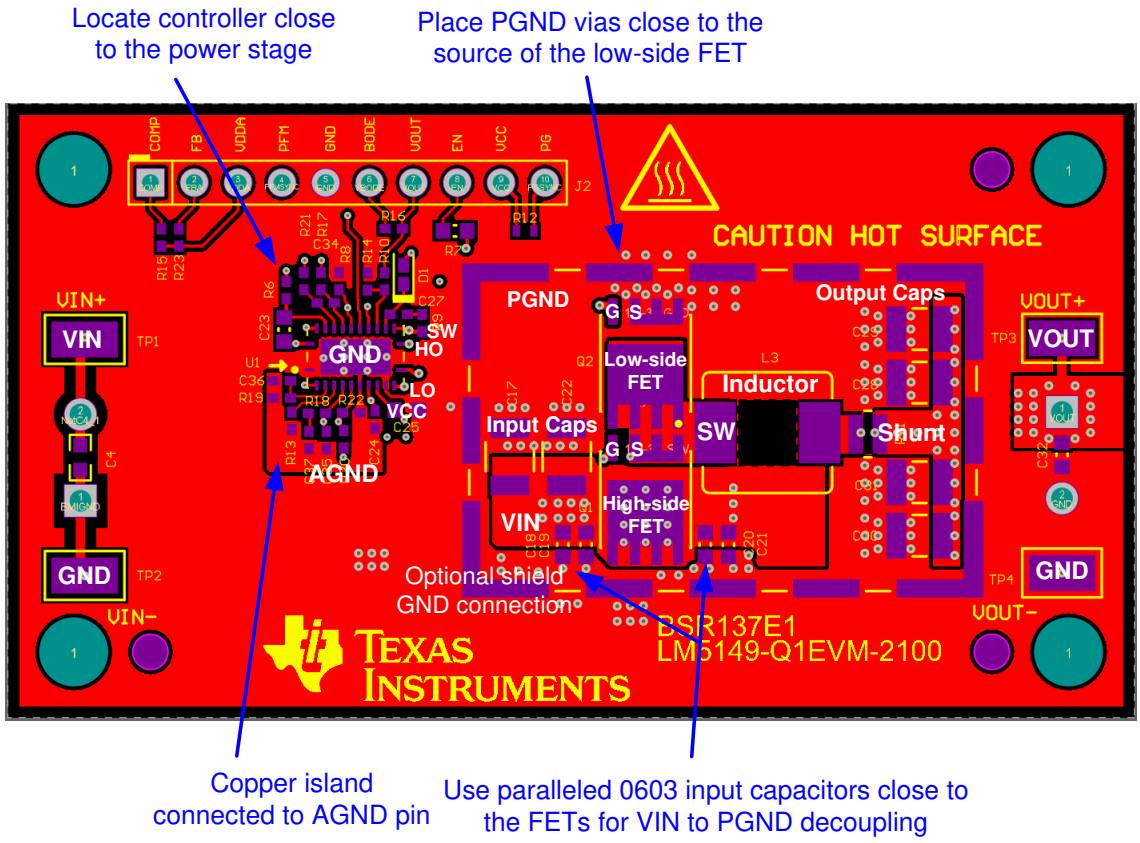

图 11-2. PCB Top Layer – High Density, Single-sided Design

Additional guidelines to improve noise immunity and reduce EMI are as follows:

- Make the ground connections to the LM25149 controller as shown in 图 11-2. Create a power ground directly connected to all high-power components and an analog ground plane for sensitive analog components. The analog ground plane for AGND and power ground plane for PGND must be connected at a single point directly under the IC – at the die attach pad (DAP).

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- Connect the MOSFETs (switch node) directly to the inductor terminal with short copper connections (without vias) as this net has high dv/dt and contributes to radiated EMI. The single-layer routing of the switch-node connection means that switch-node vias with high dv/dt do not appear on the bottom side of the PCB. This avoids e-field coupling to the reference ground plane during the EMI test. VIN and PGND plane copper pours shield the polygon connecting the MOSFETs to the inductor terminal, further reducing the radiated EMI signature.
- Place the *EMI filter* components on the bottom side of the PCB so that they are shielded from the power stage components on the top side.

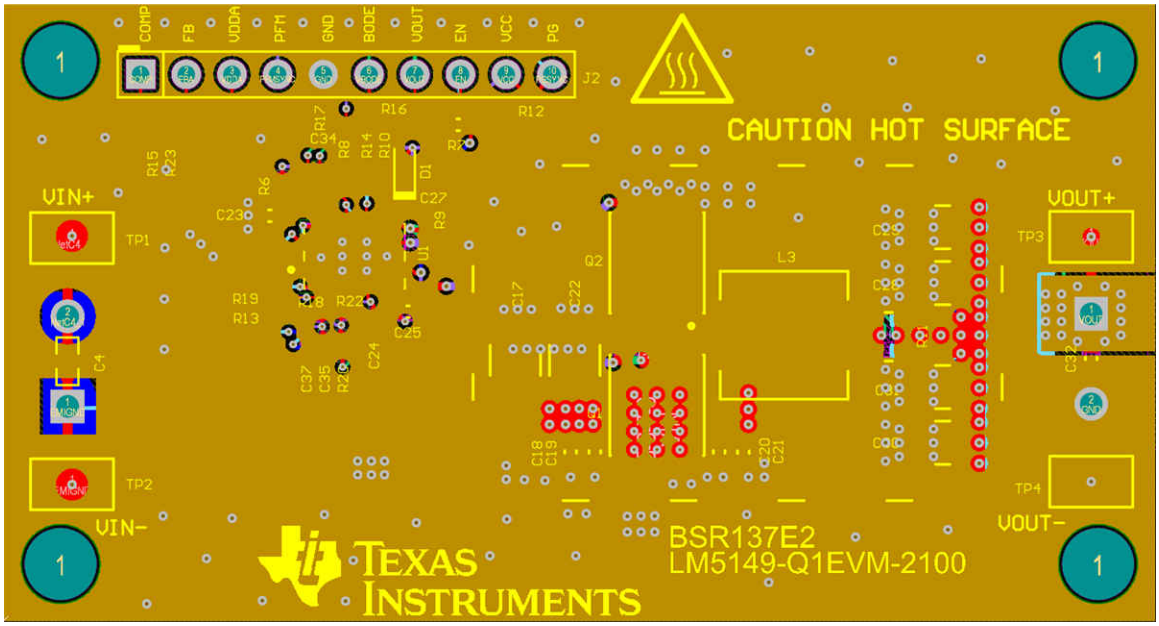

图 11-3. Layer 2 Full Ground Plane Directly Under the Power Components

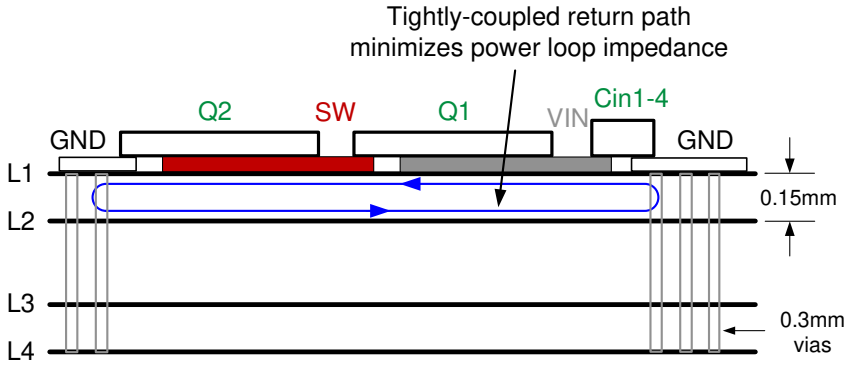

图 11-4. PCB Stack-up Diagram With Low L1-L2 Intra-layer Spacing [1]

[1] See *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout* for more detail.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

With an input operating voltage as low as 3.5 V and up to 100 V as specified in 表 12-1, the LM5140/1/3/6/9-Q1 family of synchronous buck controllers from TI provides flexibility, scalability and optimized solution size for a range of applications. These controllers enable DC/DC solutions with high density, low EMI and increased flexibility. All controllers are rated for a maximum operating junction temperature of 150°C and have AEC-Q100 grade 1 qualification.

表 12-1. Automotive Synchronous Buck DC/DC Controller Family

DC/DC CONTROLLER	SINGLE or DUAL	V_{IN} RANGE	CONTROL METHOD	GATE DRIVE VOLTAGE	SYNC OUTPUT	PRGRAMMABLE DITHER
LM5140-Q1	Dual	3.8 V to 65 V	Peak current mode	5 V	180° phase shift	N/A
LM25141-Q1	Single	3.8 V to 42 V	Peak current mode	5 V	N/A	Yes
LM5141-Q1	Single	3.8 V to 65 V	Peak current mode	5 V	N/A	Yes
LM5143-Q1	Dual	3.5 V to 65 V	Peak current mode	5 V	90° phase shift	Yes
LM5149-Q1	Single	3.5 V to 80 V	Peak current mode	5 V	180° phase shift	Yes
LM5146-Q1	Single	5.5 V to 100 V	Voltage mode	7.5 V	180° phase shift	N/A

For development support see the following:

- LM5149-Q1 Quickstart Calculator
- LM5149-Q1 Simulation Models
- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center
- TI Designs:
  - *ADAS 8-Channel Sensor Fusion Hub Reference Design with Two 4-Gbps Quad Deserializers*
  - *Automotive EMI and Thermally Optimized Synchronous Buck Converter Reference Design*
  - *Automotive High Current, Wide V_{IN} Synchronous Buck Controller Reference Design Featuring LM5141-Q1*
  - *25W Automotive Start-Stop Reference Design Operating at 2.2 MHz*
  - *Synchronous Buck Converter for Automotive Cluster Reference Design*
  - *137W Holdup Converter for Storage Server Reference Design*
  - *Automotive Synchronous Buck With 3.3V @ 12.0A Reference Design*
  - *Automotive Synchronous Buck Reference Design*
  - *Wide Input Synchronous Buck Converter Reference Design With Frequency Spread Spectrum*
  - *Automotive Wide V_{IN} Front-end Reference Design for Digital Cockpit Processing Units*
- Technical Articles:
  - *High-Density PCB Layout of DC/DC Converters*
  - *Synchronous Buck Controller Solutions Support Wide V_{IN} Performance and Flexibility*
  - *How to Use Slew Rate for EMI Control*
- To view a related device of this product, see the LM5141

12.1.2 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25149 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

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In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- User's Guides:
  - *LM5149-Q1 Synchronous Buck Controller High Density EVM*
  - *LM5141-Q1 Synchronous Buck Controller EVM*
  - *LM5143-Q1 Synchronous Buck Controller EVM*
  - *LM5146-Q1 EVM User's Guide*
  - *LM5145 EVM User's Guide*
- Application Reports:
  - *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout Application Report*
  - *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*
  - *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*
- Technical Briefs:
  - *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics*
- White Papers:
  - *An Overview of Conducted EMI Specifications for Power Supplies*
  - *An Overview of Radiated EMI Specifications for Power Supplies*
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*

12.2.1.1 PCB Layout Resources

- Application Reports:
  - *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - *AN-1149 Layout Guidelines for Switching Power Supplies*
  - *AN-1229 Simple Switcher PCB Layout Guidelines*
  - *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Seminars:
  - *Constructing Your Power Supply – Layout Considerations*

12.2.1.2 Thermal Design Resources

- Application Reports:
  - *AN-2020 Thermal Design by Insight, Not Hindsight*
  - *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - *Semiconductor and IC Package Thermal Metrics*
  - *Thermal Design Made Simple with LM43603 and LM43602*
  - *PowerPAD™ Thermally Enhanced Package*
  - *PowerPAD Made Easy*
  - *Using New Thermal Metrics*

ADVANCE INFORMATION

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

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12.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25149RGYR	PREVIEW	VQFN	RGY	24	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 150		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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