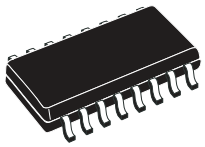
STGAP2D

Galvanically isolated 4 A half-bridge gate driver

Datasheet - production data



SO-16

Features

- 1700 V dual channel gate driver
- Driver current capability: 4 A sink / source at 25 °C
- dV/dt transient immunity ± 100 V/ns
- Overall input-output propagation delay: 80 ns
- UVLO function
- Interlocking function
- Dedicated SD and BRAKE pins
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shutdown protection
- Standby function

Applications

- Motor driver for industrial drives, factory automation, home appliances and fans.
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

Description

The STGAP2D is a half-bridge gate driver which isolates the gate driving channels from the low voltage control and interface circuitry.

The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for high power inverter applications such as motor drivers in industrial applications.

The device integrates protection functions: dedicated SD and BRAKE pins are available, UVLO and thermal shutdown are included to easily design high reliability systems, and the interlocking function prevents outputs from being high at the same time.

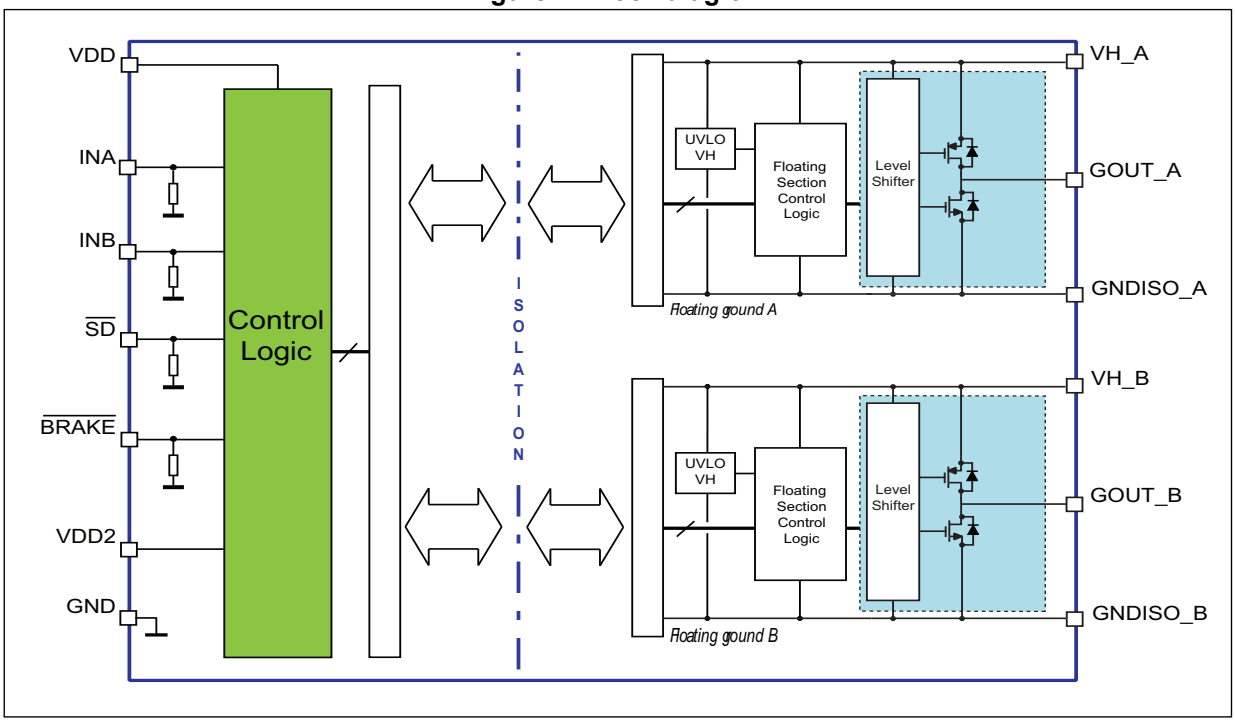
The input to output propagation delay results are contained within 80 ns, providing high PWM control accuracy.

A standby mode is available in order to reduce idle power consumption.

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin description and connection diagram

Figure 2. Pin connection (top view)

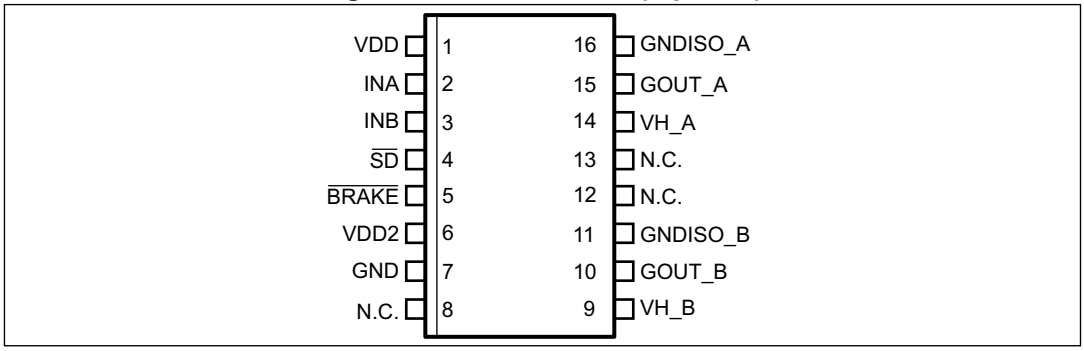


Table 1. Pin description

Pin #	Pin Name	Type	Function
1	VDD	Power supply	Control logic supply voltage.
2	INA	Logic input	Control logic input for Channel A, active high.
3	INB	Logic input	Control logic input for Channel B, active high.
4	$\overline{SD}$	Logic input	Shutdown input, active low.
5	$\overline{BRAKE}$	Logic input	Control logic input, active low.
6	VDD2	Power supply	Must be connected to VDD.
7	GND	Power supply	Control logic ground.
9	VH_B	Power supply	Channel B gate driving positive supply.
10	GOUT_B	Analog output	Channel B Sink/Source output.
11	GNDISO_B	Power supply	Channel B gate driving isolated ground.
14	VH_A	Power supply	Channel A gate driving positive supply.
15	GOUT_A	Analog output	Channel A Sink/Source output.
16	GNDISO_A	Power supply	Channel A gate driving isolated ground.
Others			Not connected.

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD, VDD2	Logic supply voltage vs. GND		-0.3	6.5	V
V_{LOGIC}	Logic pins voltage vs. GND		-0.3	6.5	V
VH_x	Positive supply voltage (VH_x vs. GNDISO_x)		-0.3	28	V
V_{OUT}	Voltage on gate driver outputs (GOUT_x vs. GNDISO_x)		- 0.3	VH_x + 0.3	V
V_{iso}	Input to output isolation voltage (GND vs. GNDISO_x)	DC or peak	-1700	+1700	V
T_J	Junction temperature		-40	150	°C
T_S	Storage temperature		-50	150	°C
P_{Din}	Power Dissipation input chip	T_A = 25 °C		10	mW
P_{Dout}	Power Dissipation output chip	T_A = 25 °C		1.16	W
ESD	HBM (human body model)		2		kV

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	SO-16	90	°C/W

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD, VDD2	Logic supply voltage vs. GND	-	3	5.5	V
V_{LOGIC}	Logic pins voltage vs. GND	-	0	5.5	V
VH_x	Positive supply voltage (VH_x vs. GNDISO-x)	-		26	V
F_{SW}	Maximum switching frequency(1)	-		1	MHz

Table 4. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
T_{OUT}	Pulse width	-	100		ns
T_J	Operating Junction Temperature	-	-40	125	°C

1. Actual limit depends on power dissipation and T_J.

4 Electrical characteristics

4.1 Electrical characteristics

Table 5. Electrical characteristics (T_J = 25 °C, VH_x = 15 V, VDD = 5 V, unless otherwise specified)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics							
t_{Don}	INA, INB, SD, BRAKE	Input to output propagation delay ON		40	80	100	ns
t_{Doff}	INA, INB, SD, BRAKE	Input to output propagation delay OFF		40	80	100	ns
t_r		Rise time	C_L = 4.7 nF, 10% ÷ 90%		30		ns
t_f		Fall time	C_L = 4.7 nF, 10% ÷ 90%		30		ns
MT		Matching time(1)	DT = 5 V			20	ns
$t_{deglitch}$	INA, INB, SD, BRAKE	Inputs deglitch filter			20	40	ns
CMTI(2)		Common-mode transient immunity, $\|dV_{ISO}/dt\|$	V_{CM} = 1500 V, see *Figure 9*	100			V/ns
Supply voltage							
VH_{on}	-	VH_x UVLO turn-on threshold		8	9.1	10.5	V
VH_{off}	-	VH_x UVLO turn-off threshold		7	8.4	9.5	V
VH_{hyst}	-	VH_x UVLO hysteresis		0.5	0.9	1.4	V
I_{QHU_A}, I_{QHU_B}	-	VH_x under-voltage quiescent supply current	VH_x = 4 V		150	250	µA
I_{QH_A}, I_{QH_B}	-	VH_x quiescent supply current			1.3	2.5	mA
I_{QHSBY_A}, I_{QHSBY_B}	-	Standby VH_x quiescent supply current			400	600	µA
SafeClp	-	GOFF active clamp	I_{GOFF} = 0.2 A; VH floating		2	2.5	V
I_{QDD}	-	VDD quiescent supply current			1	2	mA
I_{QDDSBY}	-	Standby VDD quiescent supply current	Standby mode		40	80	µA
Logic inputs							
V_{il}	INA, INB, SD, BRAKE	Low level logic threshold voltage		0.29 · VDD	1/3 · VDD	0.37 · VDD	V

Table 5. Electrical characteristics (T_J = 25 °C, VH_x = 15 V, VDD = 5 V, unless otherwise specified)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ih}	INA, INB, SD, BRAKE	High level logic threshold voltage		0.62 · VDD	2/3 · VDD	0.72 · VDD	V
I_{logic_h}	INA, INB, SD, BRAKE	Logic inputs high-level input bias current	V_{logic} = 5 V	33	50	77	µA
I_{logic_l}	INA, INB, SD, BRAKE	Logic inputs low-level input bias current	V_{logic} = 0 V			1	µA
R_{pd}	INA, INB, SD, BRAKE	Logic inputs pull-down resistor		65	100	150	kΩ
Driver buffer section							
I_{GON}	-	Source short-circuit current	T_J = 25 °C		4		A
			T_J = -40 ÷ +125 °C(2)	3		5	
I_{GOFF}	-	Sink short-circuit current	T_J = 25 °C		4		A
			T_J = -40 ÷ +125 °C(2)	3		5	
V_{GONH}	-	G_{ON} output high level voltage	I_{GON} = 100 mA	VH_x-0.14	VH_x-0.11		V
V_{GOFFL}	-	G_{OFF} output low level voltage	I_{GOFF} = 100 mA		84	95	mV
R_{GON}	-	Source R_{DS_ON}	I_{GON} = 100 mA		1.11	1.4	Ω
R_{GOFF}	-	Sink R_{DS_ON}	I_{GOFF} = 100 mA		0.84	0.95	Ω
Over-temperature protection							
T_{SD}	-	Shutdown temperature		170			°C
T_{hys}	-	Temperature hysteresis			20		°C
Standby							
t_{STBY}	-	Standby time	See *Section 5.6*	200	280	350	µs
t_{WUP}	-	Wake-up time	See *Section 5.6*	10	20	35	µs
t_{awake}	-	Wake-up delay	See *Section 5.6*	90	140	200	µs
$t_{stbyfilt}$	-	Standby filter	See *Section 5.6*	200	280	600	ns

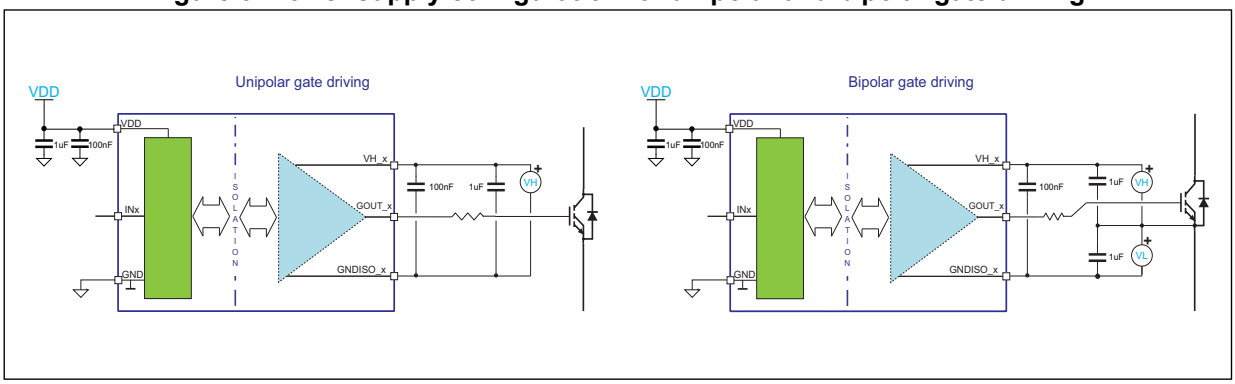
1. MT = max ($|t_{Don(A)} - t_{Don(B)}|$, $|t_{Doff(A)} - t_{Doff(B)}|$, $|t_{Doff(A)} - t_{Don(B)}|$, $|t_{Doff(B)} - t_{Don(A)}|$)
2. Characterization data, not tested in production.

5 Functional description

5.1 Gate driving power supply and UVLO

The STGAP2D is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows to implement either unipolar or bipolar gate driving.

Figure 3. Power supply configuration for unipolar and bipolar gate driving



Under-voltage protection is available on the VH_x supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH_x voltage goes below the VHoff threshold, the output buffer goes into “safe state”. When VH_x voltage reaches the VHon threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH_x supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors, which are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with a value in the range between 1 µF and 10 µF should be placed close to it.

5.2 Power-up, power-down and 'safe state'

The following conditions define the “safe state”:

- GOFF = ON state
- GON = high impedance

Such conditions are maintained at power-up of the isolated side (VH_x < VHon) and during the entire device power-down phase (VH < VHoff), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on.
If the VH_x positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put into safe state, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage side, the device output state depends on the input pins' status.

5.3 Control inputs

The device is controlled through the following logic inputs:

- SD: active low shutdown input;
- BRAKE: active low brake input;
- INA, INB: active high logic inputs for channel A and channel B driver outputs.

The operation of the driver IOs is described in *Table 6*.

Table 6. Inputs truth table (applicable when device is not in UVLO or “safe state”)

	Input pins(1)				Output pins	
	$\overline{SD}$	$\overline{BRAKE}$	INA	INB	GOUT_A	GOUT_B
	L	X	X	X	Low	Low
	H	L	X	X	Low	**HIGH**
	H	H	L	L	Low	Low
	H	H	H	L	**HIGH**	Low
	H	H	L	H	Low	**HIGH**
Interlocking	H	H	H	H	Low	Low

1. X: Don‘t care

A deglitch filter allows input signals with a duration shorter than $t_{deglitch}$ to be ignored, thereby preventing noise spikes potentially present in the application from generating unwanted commutations.

5.4 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with the LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced into "safe state" until the communication link is properly established again.

5.5 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the T_{SD} temperature threshold, the device is forced into "safe state". The device operation is restored as soon as the junction temperature is lower than T_{SD} - T_{hys}.

5.6 Standby function

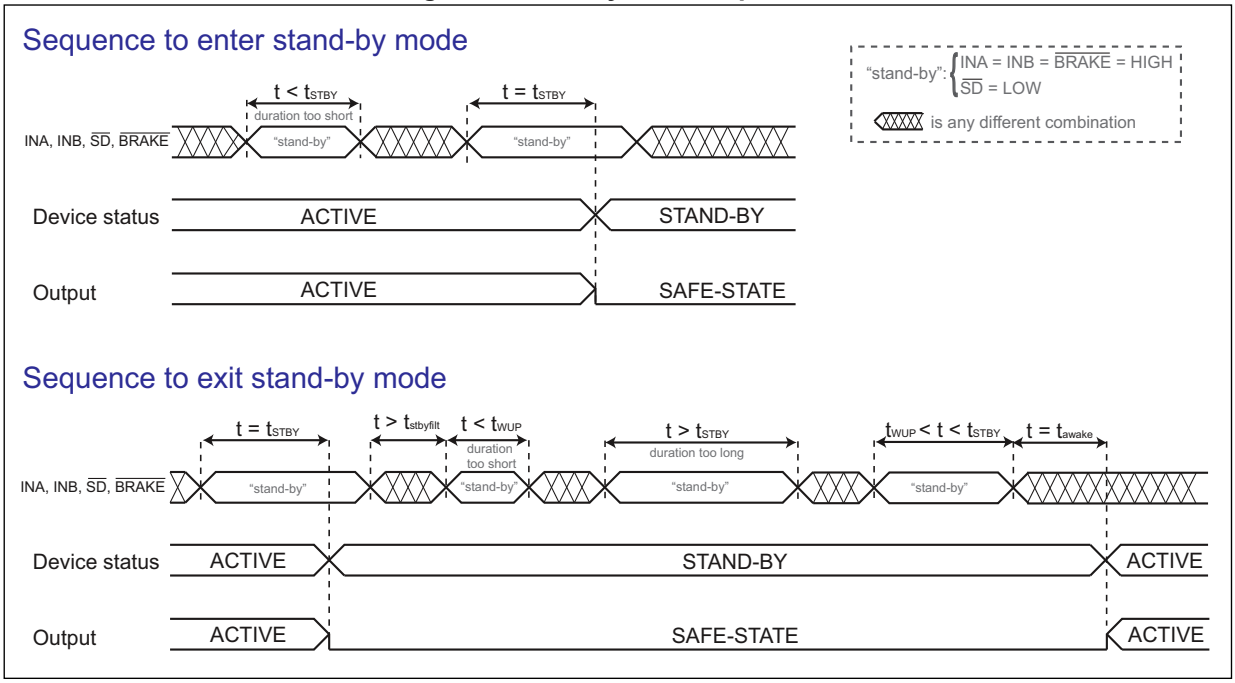
In order to reduce the power consumption of both control interface and gate driving sides the device can be put into standby mode. In standby mode the quiescent current from VDD

and VH_x supply pins is reduced to I_{QDDS} and I_{QHS_x} respectively, and the output remains in 'safe state' (the output is actively forced low).

The way to enter standby is to keep the SD low while keeping the other input pins (INA, INB, and BRAKE) high (“standby” value) for a time longer than t_{STBY}. During standby the inputs can change from the “standby” value.

To exit standby, inputs must be put in any combination different from the “standby” value for a time longer than $t_{stbyfilt}$, and then in the “standby” value for a time t such as $t_{WUP} < t < t_{STBY}$. When the input configuration is changed from the “standby” value the output is enabled and set according to inputs state. after a time t_{awake}.

Figure 4. Standby state sequences



6 Typical application diagram

Figure 5. Typical application diagram - Half-bridge configuration

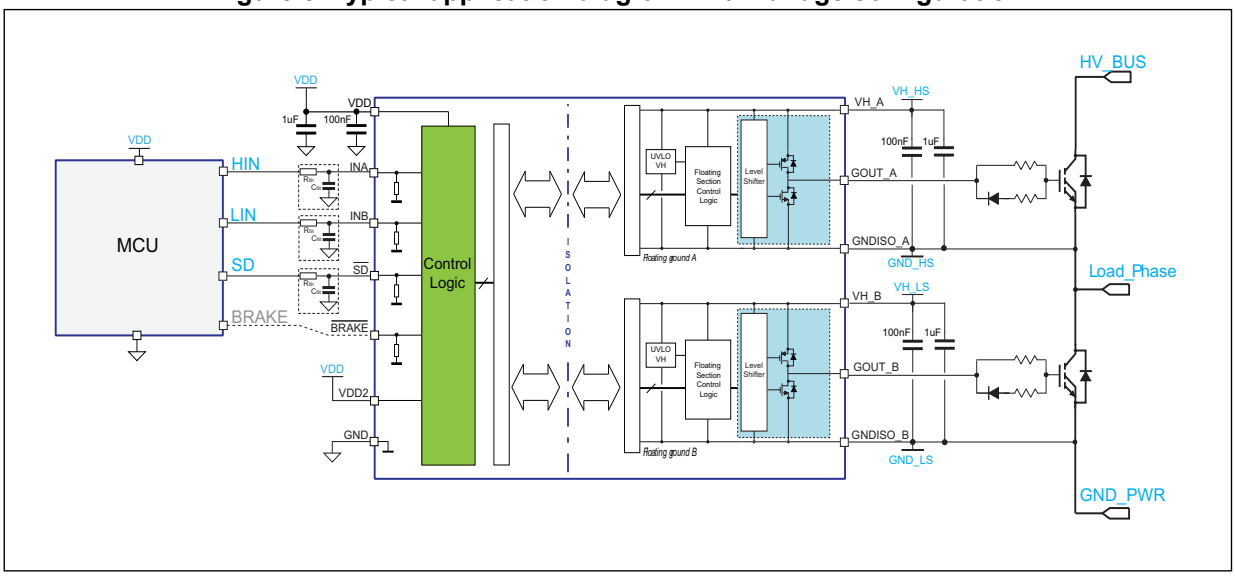
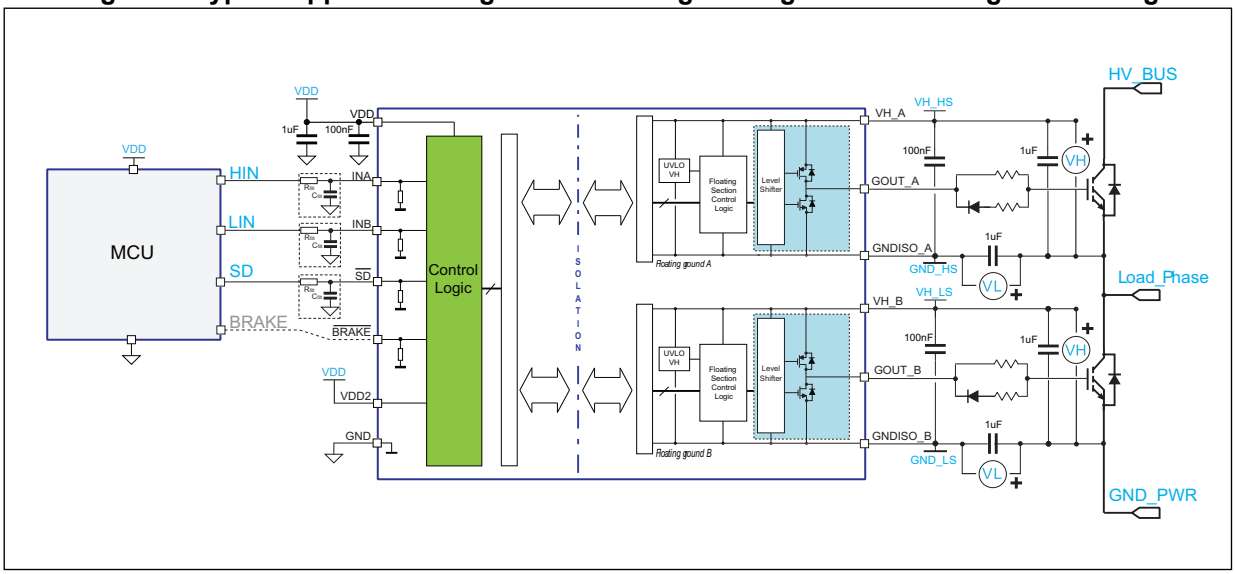


Figure 6. Typical application diagram - Half-bridge configuration with negative driving



7 Layout

7.1 Layout guidelines and considerations

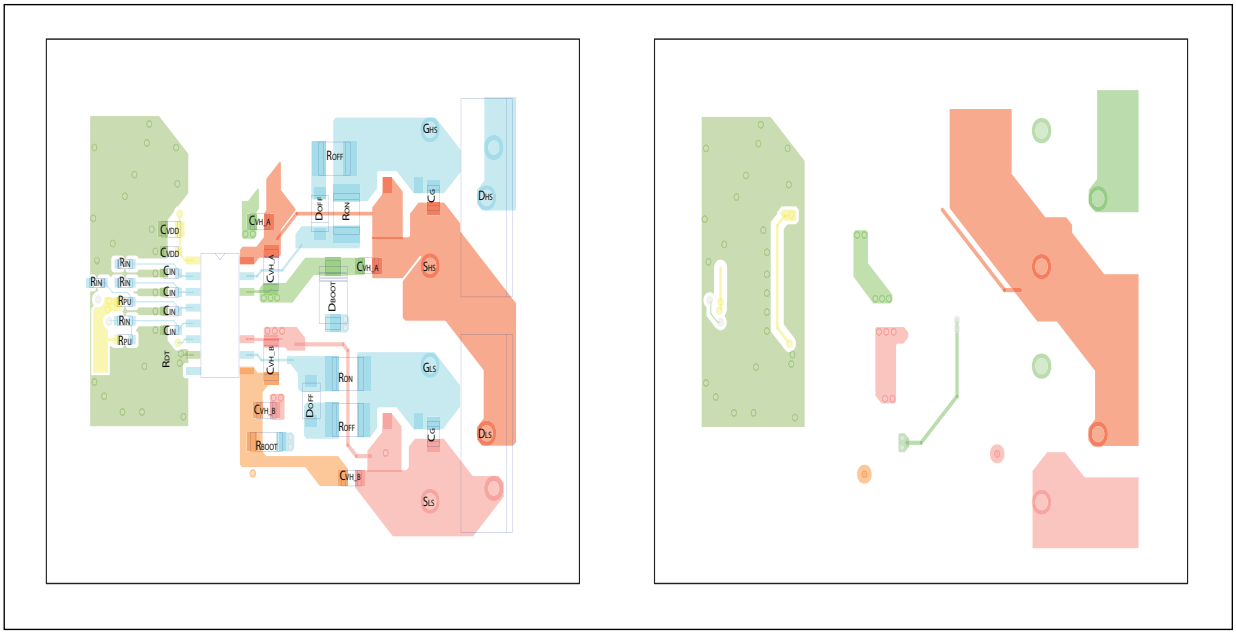
In order to optimize the PCB layout, the following considerations should be taken into account:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pin. A 100 nF capacitor must be placed between VDD and GND and between VH_x and GNDISO_x, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current, a second capacitor with a value in the range between 1 µF and 10 µF should also be placed close to the supply pins.
- As good practice, it is suggested to add filtering capacitors close to logic inputs of the device (INA, INB, BRAKE, SD); in particular for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver, so as to minimize the gate loop area and inductance that might bring noise or ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should be no trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH_x and GNDISO_x pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

7.2 Layout example

An example of the STGAP2D Half-Bridge PCB layout with main signals highlighted by different colors is shown in *Figure 7*. It is recommended to follow this example for proper positioning and connection of filtering capacitors.

Figure 7. Suggested PCB layout for Half-Bridge configuration



8 Testing and characterization information

Figure 8. Timings definition

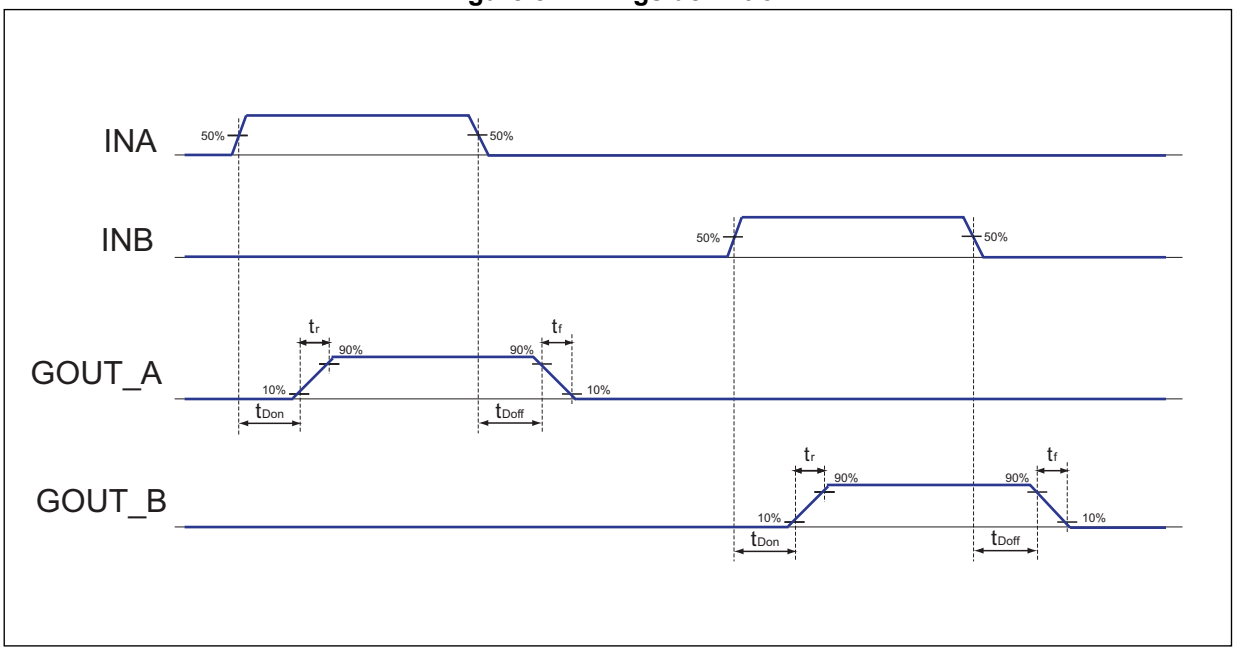
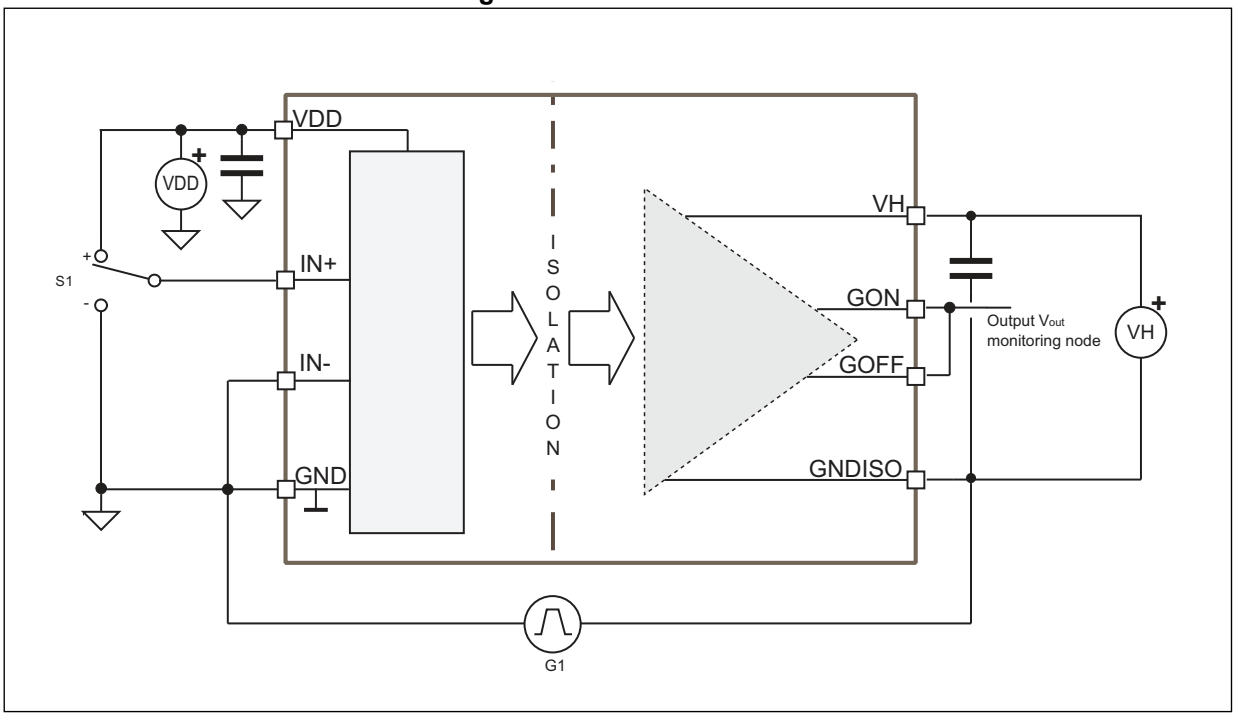


Figure 9. CMTI test circuit



9 Package information

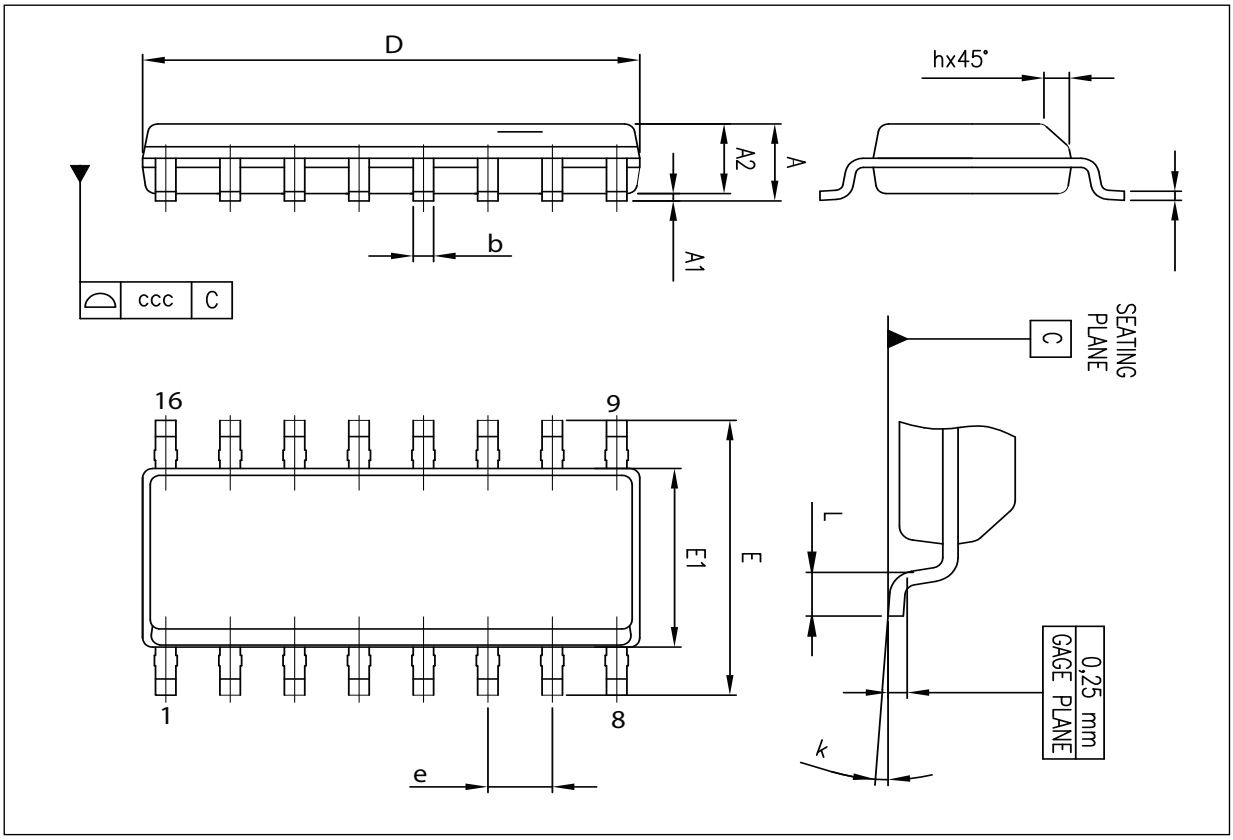
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 7. SO-16 narrow package dimensions

Dim.	mm			
	Min.	Typ.	Max.	NOTES
A			1.75	
A1	0.10		0.25	
A2	1.25			
B	0.31		0.51	
C	0.17		0.25	
D	9.80	9.90	10.00	(1) (3)
E	5.80	6.00	6.20	
E1	3.80	3.90	4.00	(2) (3)
E		1.27		
H	0.25		0.50	
L	0.40		1.27	
K	0		8	DEGREES
Ccc			0.10	

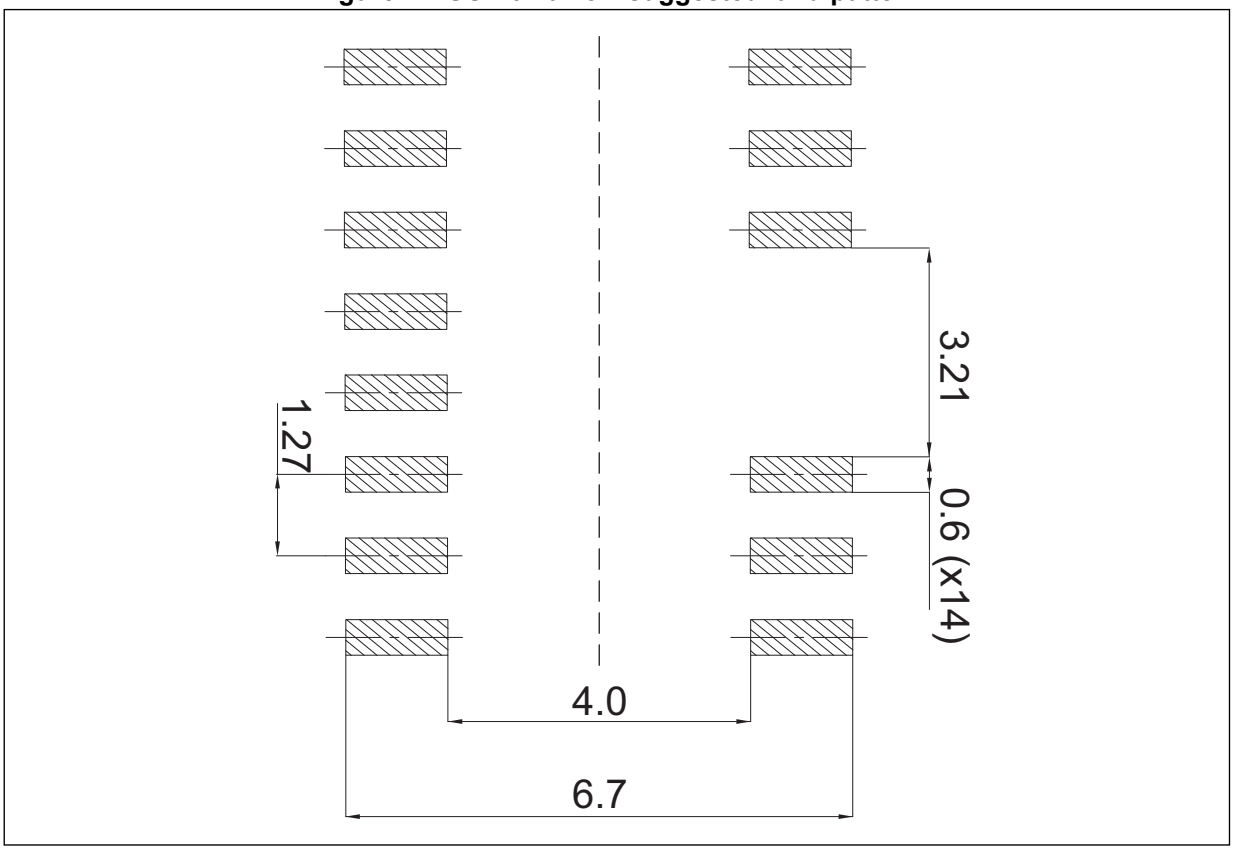
1. *Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).*
2. *Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*
3. *Dimensions referred to the bottom side of the package.*

Figure 10. SO-16 narrow package outline



10 Suggested land pattern

Figure 11. SO-16 narrow suggested land pattern



11 Ordering information

Table 8. Device summary

Order code	Output configuration	Package marking	Package	Packaging
STGAP2DM	GOUT	GAP2DM	SO-16	Tube
STGAP2DMTR	GOUT	GAP2DM	SO-16	Tape and reel

12 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Aug-2018	1	Initial release.