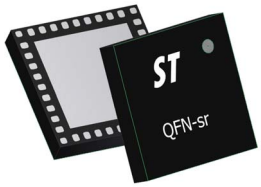
L7292

Five buck regulators power management unit

Datasheet - production data



VQFN 5 x 5 x 0.9 40L

Features

- Key specification
  - Vin range from 2.7 V to 5.5 V
- Interface
  - Two-wire I^2C serial interface supports 3.4-Mbit protocol (high speed mode)
  - 8-bit register bank
  - Random and Sequential Read modes
  - Automatic address incrementing
- Programmable buck regulators
  - Regulators with programmable DC set point and soft-start
  - Buck regulators include integrated PMOS and NMOS switching elements
  - Up to 90% efficiency
  - PWM and PFM modes
  - Two pins to select four sets of DC voltages
  - ± 1% feedback voltage accuracy
  - All regulators with auto discharge function on reset.
  - Programmable bucks
- Support functions
- 128-bit EEPROM for:
  - Default Vout
  - Power up sequence
  - Reset IC delay time
  - Regulator enable
- Integrated voltage monitor with digital filters
- Thermal protection
- Package: VQFN 5 x 5 x 0.9 40L

Applications

- SSD (Solid-State Drive), portable phone, etc.

Description

The L7292 is a power management device designed for consumer applications. Five bucks provide voltages for the µController and Flash memory with efficiency up to 90% in light-load condition.

The device communicates with the µController via an I^2C serial interface operating at clock speeds up to 3.4 Mbit/s.

The regulators operate at 1.3 MHz switching frequency and enter automatically in the PFM operation to maintain high efficiency over the entire load current range.

The device can be forced into the PWM mode by writing a bit in the serial port register.

Low quiescent current (e.g.: All SW reg. ON with no load Iq = 175 µA).

The L7292 device has a DSM mode to reduce the quiescent current at the minimum value (1 x SW reg. ON with no load Iq = 60 µA).

Table 1. Device summary

Regulator	Vout range [V]	DC Iload [A]
BUCK1	0.9 - 1.6	1.0
BUCK2	1.5 - 2.1	0.8
BUCK3	0.7 - 1.3	0.5
BUCK4	0.7 - 1.3	1.0
BUCK5	0.7 - 1.3	1.6

This is information on a product in full production. www.st.com

Contents

1 Package

QFN 5 x 5 x 0.9 40L package

Figure 1. I²C ext. components

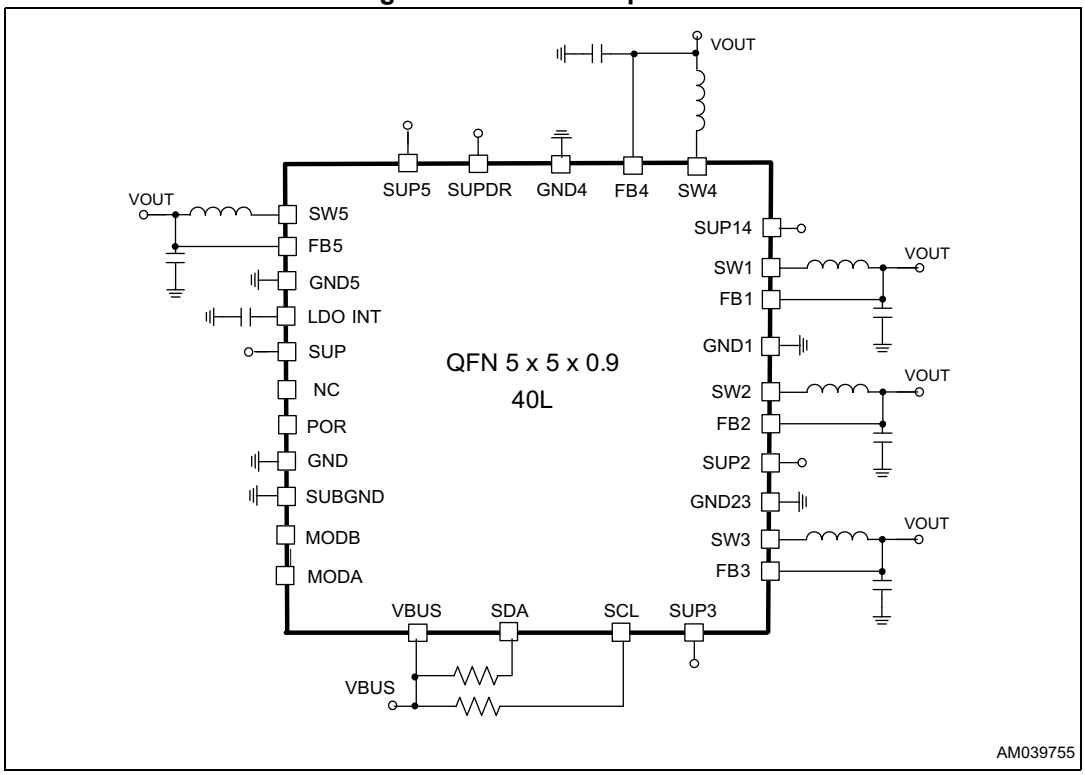
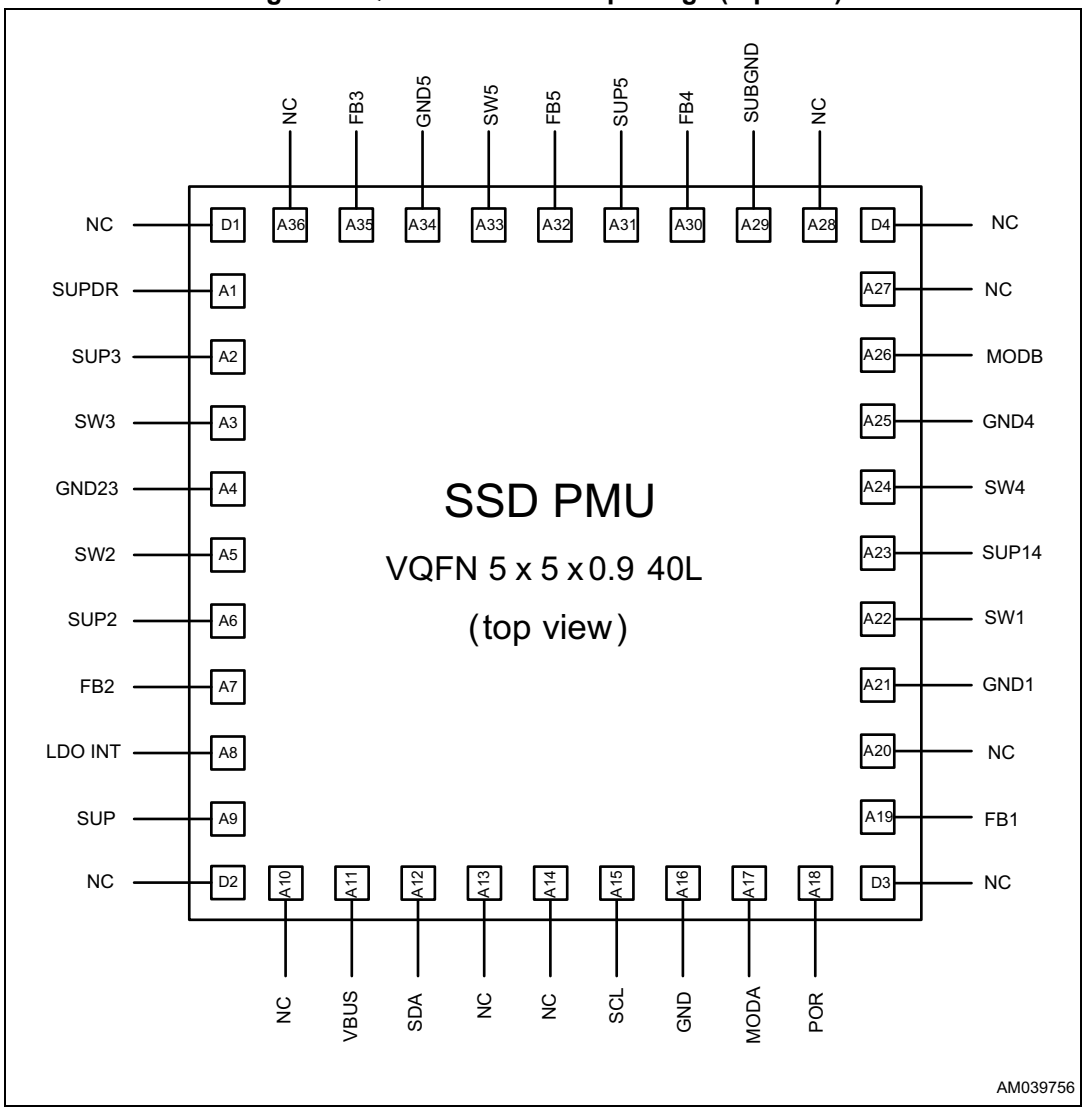


Figure 2. QFN 5 x 5 x 0.9 40L package (top view)



2 Pin description

Table 2. Pinout

Pin no.	Pin name	Type	Description
D1	NC		
A1	SUPDR	P	Power supply
A2	SUP3	P	Power supply
A3	SW3	O	BUCK3 regulator switch node
A4	GND23	G	BUCK2 and BUCK3 ground
A5	SW2	O	BUCK2 regulator switch node
A6	SUP2	P	BUCK2 power supply
A7	FB2	I	BUCK2 regulator feedback
A8	LDO INT	I	Supply voltage to internal circuits
A9	SUP	P	Power supply
D2	NC		
A10	NC		
A11	VBUS	P	Serial port supply
A12	SDA	I/O	I^2C serial data line
A13	NC		
A14	NC		
A15	SCL	I	I^2C serial clock line
A16	GND	G	Analog and digital ground
A17	MODA	I	With MODB pin, SET A, B, C, and D selection
A18	POR	O	Power-on reset
D3	NC		
A19	FB1	I	BUCK1 regulator feedback
A20	NC		
A21	GND1	G	Ground
A22	SW1	O	BUCK1 regulator switch node
A23	SUP14	P	BUCK1 and BUCK4 power supply
A24	SW4	O	BUCK4 regulator switch node
A25	GND4	G	BUCK4 ground
A26	MODB	I	With MODA pin, SET A, B, C, and D selection
A27	NC		
D4	NC		
A28	NC		

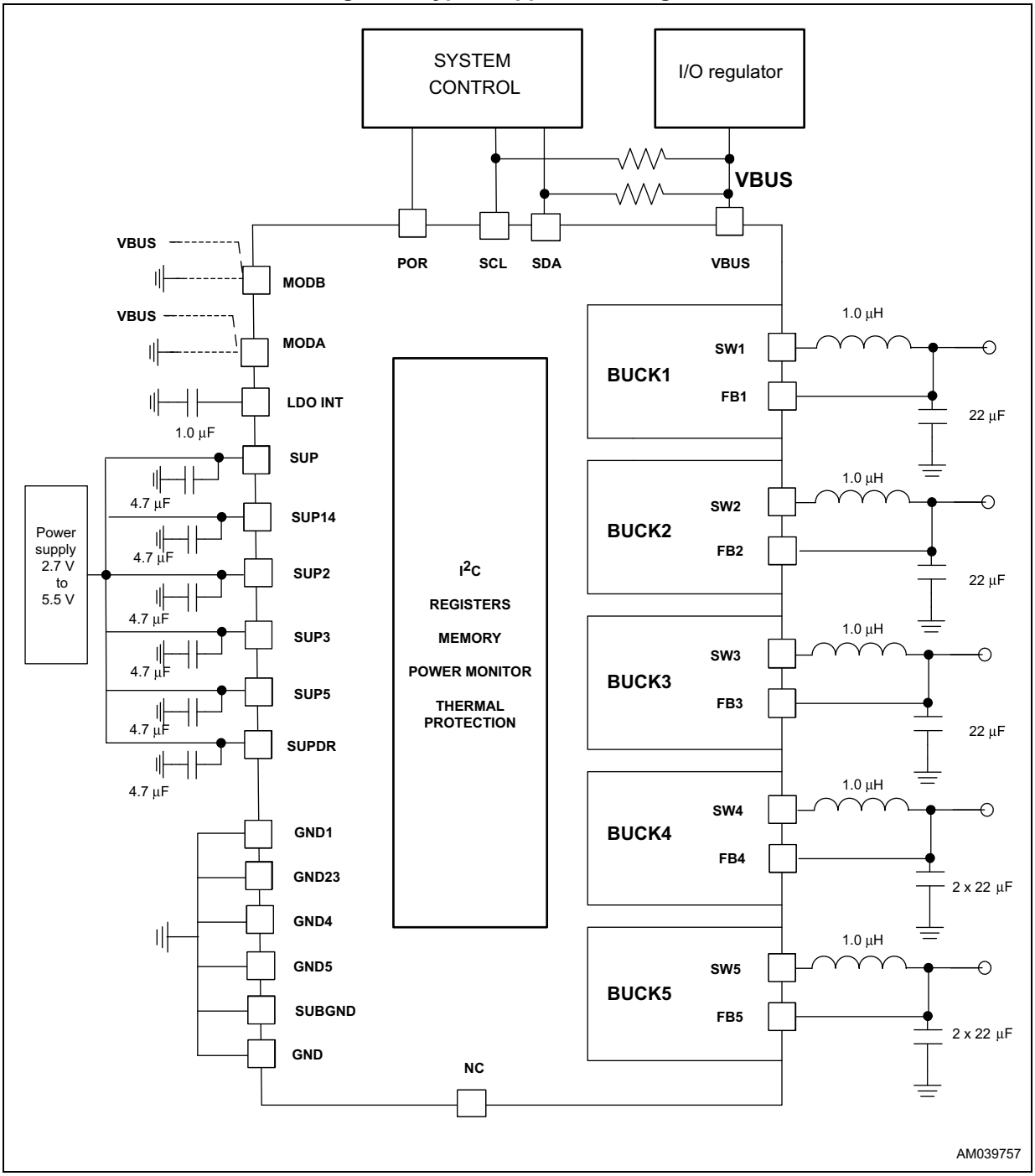
Table 2. Pinout (continued)

Pin no.	Pin name	Type	Description
A29	SUBGND	G	Substrate ground
A30	FB4	I	BUCK4 regulator feedback
A31	SUP5	P	BUCK5 power supply
A32	FB5	I	BUCK5 regulator feedback
A33	SW5	O	BUCK5 regulator switch node
A34	GND5	G	Ground
A35	FB3	I	BUCK3 regulator feedback
A36	NC		

Note: *P → power supply*
G → ground
O → output
I/O → input/output
I → input.

3 Typical application

Figure 3. Typical application diagram



4 Absolute maximum ratings

The absolute maximum rating is the maximum stress that can be applied to a device without causing permanent damage. However, extended exposure to maximum ratings may affect long-term device reliability.

Table 3. Absolute maximum ratings

Parameter	Rating
SUP, SUP14 - 2 - 3 - 5, SUPDR	-0.3 V - 7 V
VBUS	-0.3 V - 7 V
SW 1 - 5	-0.3 V - 7 V
FB 1 - 5	-0.3 V - 4 V
SDA, SCL, POR, MODA, MODB	-0.3 V - VBUS
LDO INT	-0.3 V - 2.5 V
LDO	-0.3 V - 7 V
Operating ambient temperature	-30 °C to 85 °C
Operating virtual junction temperature	170 °C
Thermal resistance, junction to ambient	
QFN 5 x 5 x 0.9 40L	
30 °C/W	
Storage temperature	-55 °C to 150 °C
Solder temperature - 10 s duration	250 °C

5 Electrical characteristics

All specifications are for -30 °C < T_A < 85°C, ALL SUPx = 5 V, VBUS = 3.3 V (≤ VSUP) unless otherwise noted.

5.1 Recommended operating conditions

Performance specifications do not apply when the device is operated outside the recommended conditions, unless otherwise indicated.

Table 4. Recommended operating conditions

Parameter	Min.	Typ.	Max.	Unit
SUP, SUP14 - 2 - 3 - 5, SUPDR voltage(1)	2.7		5.5	V
VBUS voltage	1.72		3.63	
Ambient temperature, T_A	-30		85	°C
Total power dissipation, with device appropriately mounted(2) QFN 5 x 5 x 0.9 40L			2.2	W

1. The “min.” value reported is referring to the typical value of undervoltage threshold distribution.
2. Device mounted on the multilayer PCB with appropriate thermal optimization. If multiple ratings are listed for the same parameter, all apply simultaneously.

5.2 Bias DC characteristics

Table 5. Bias DC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
LDO INT output voltage	Cout = 1.0 µF, Iload = 0		1.8		V
Deep sleep mode quiescent supply current	VSUP = 5 V REGCTRL bit 7 = 1 BUCK1 - 2 - 4 - 5 = OFF BUCK3 = ON no load		60		µA
Quiescent supply current	VSUP = 5 V REGCTRL bit 7 = 0 BUCK1 - 2 - 3 - 4 - 5 = ON no load		175		µA

5.3 Interface

5.3.1 I^2C electrical specification

Table 6. I^2C electrical specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
Digital high level input voltage, V_{IH}	SDA, SCL	0.7 * VBUS		VBUS + 0.3	V
Digital low level input voltage, V_{IL}	SDA, SCL	-0.3		0.3 * VBUS	V
Digital low level output voltage, V_{OL}	SDA I_{LOAD} = 1 mA	-0.3		0.3 * VBUS	V
Digital high level output voltage, V_{OH}	SDA I_{LOAD} = 1 mA	0.7 * VBUS		VBUS + 0.3	V
Input bias current	SDA, SCL = VBUS			1	µA
Input bias current	SDA, SCL = 0 V	-1			µA
Input capacitance	SDA			10	pF

Note: For others parameters refer to I^2C bus specifications.

5.3.2 MODA, MODB

Table 7. MODA, MODB

Parameter	Conditions	Min.	Typ.	Max.	Unit
Digital high level input voltage, V_{IH}	MODA, MODB	0.7 * VBUS		VBUS + 0.3	V
Digital low level input voltage, V_{IL}	MODA, MODB	-0.3		0.3 * VBUS	V

5.4 EEPROM

Table 8. EEPROM

Parameter	Conditions	Min.	Typ.	Max.	Unit
Programming time	1 page = 8 bytes parallel programming			30	ms
Allowable write cycles				1000	
Write voltage		2.9			V

5.5 Voltage monitor and POR generator

Table 9. Voltage monitor and POR generator

Parameter		Conditions	Min.	Typ.	Max.	Unit
Undervoltage threshold rising	SUP	Enable to regulators softstart	2.75	2.8	2.9	V
Undervoltage threshold falling	SUP	POR signal only	2.65	2.7	2.8	V
Undervoltage threshold hysteresis	SUP		0.05	0.1	0.2	
Undervoltage threshold falling	BUCK1 ,2, 3, 4, 5			Vout - 15%(1)		
Regulators disable	BUCK1, 2, 3, 4, 5		2.45	2.5	2.6	V
DLY1 POR rising delay	PORZ	2 ms step programmability	-10%	8 - 10 - 12 - 14 -16 - 18 - 20 -22 - 24	+10%	ms
POR low level output voltage, V_{OL}	PORZ	I_{OL} = 1 mA			0.3	V
POR pull-up		Internal pull-up to VBUS -30 °C to 125 °C	100	200	300	kΩ
POR high level output voltage, V_{OH}			80 % VBUS			V
POR low level output voltage, V_{OL}					20% VBUS	V

1. Valid before POR signal enable.

6 Voltage regulators

6.1 BUCK1 switching regulator

Unless otherwise noted, typical values at T_A = 25 °C, Vin = 5.0 V.

The max. values are at Tj = 125 °C and the worst case process.

Table 10. BUCK1 switching regulator

Parameter	Conditions	Min.	Typ.	Max.	Unit
DC bias current	No load , PFM mode		20		µA
Output DC voltage range	Steady state, I_{LOAD} < 1 A	0.9		1.6	V
Output voltage step size	Single step change		25		mV
Load current	Internal FET, steady state			1	A
Current limit threshold	Integrated FET current		2.5(1)		A
PFM current peak	Programmable peak current		0.8		A
DC line regulation	3.3 V < VSUP < 5 V, Iout = 1 A		0.4(1)		%/V
DC load regulation	While in PWM PSR1CFG bit 7 = 1		0.2(1)		%/A
Switching frequency	Programmable		1.3		MHz
Output voltage accuracy	While In PWM	-2		+2	%
Transient response	Load transient time = 10 µs. Referring to CCM, Vout = 1.2 V, load current from 0 to 80% Imax.		±3(1)		%
Soft-start time	Vin = 3.3 V, output voltage ramp from 0 to 95% of final Vout = 1.2 V, R load =1.4 Ω.	250(1)	360(1)		µs
Integrated high-side PFET R_{DS}	Vin =5 V		109		mΩ
	Vin = 3.3 V		132		
Integrated low-side NFET R_{DS}	Vin = 5 V		58		
	Vin = 3.3 V		65		
Efficiency	Vin = 5.0 V, Vout = 1.2 V, Iload = 1 mA		82(2)		%
	Vin =3.3 V, Vout = 1.2 V, Iload = 1 mA		84(2)		
	Vin = 5.0 V, Vout = 1.2 V, Iload = 1 A		81(2)		
	Vin = 3.3 V, Vout = 1.2 V, Iload = 1 A		82(2)		
FB input impedance			0.2		MΩ
Input capacitor			4.7		µF
Output filter capacitor			22		µF
Output filter capacitor ESR				20	mΩ
Output filter inductance			1.0		µH

1. Guaranteed by design.
2. Efficiency measured between the SUP14 PIN and BUCK1 POUT and while the BUCK4 is off. L = 1 µH, DC resistance max. = 0.036 Ω.

6.2 BUCK2 switching regulator

Unless otherwise noted, typical values at T_A = 25 °C, Vin = 5.0 V.

The max. values are at Tj = 125 °C and the worst case process.

Table 11. BUCK2 switching regulator

Parameter	Conditions	Min.	Typ.	Max.	Unit
DC bias current	No load , PFM mode		20		µA
Output DC voltage range	Steady state, I_{LOAD} < 0.8 A	1.5		2.1	V
Output voltage step size	Single step change		37.5		mV
Load current range	Internal FET, steady state			0.8	A
Current limit threshold	Integrated FET current		2.5(1)		A
PFM current peak	Programmable		0.8		A
DC line regulation	3.3 V < VSUP < 5 V, Iout = 0.8 A		0.4(1)		%/V
DC load regulation	While in PWM PSR2CFG bit 7 = 1		0.1(1)		%/A
Switching frequency	Programmable		1.3		MHz
Output voltage accuracy	While in PWM	-2		+2	%
Transient response	Load transient time = 10 µs Referring to CCM, Vout = 1.8 V, load current from 0 to 80% Imax.		±3(1)		%
Soft-start time	Vin = 3.3 V, output voltage ramp from 0 to 95% of final Vout = 1.8 V, max. load = 3.6 Ω.	210(1)	245(1)		µs
Integrated high-side PFET R_{DS}	Vin = 5 V		172		mΩ
	Vin = 3.3 V		216		
Integrated low-side NFET R_{DS}	Vin = 5 V		88		
	Vin = 3.3 V		106		
Efficiency	Vin = 5.0 V, Vout = 1.8 V, Iload = 1 mA		83(2)		%
	Vin = 3.3 V, Vout = 1.8 V, Iload = 1 mA		85(2)		
	Vin = 5.0 V, Vout = 1.8 V, Iload = 0.8 A		84(2)		
	Vin = 3.3 V, Vout = 1.8 V, Iload = 0.8 A		86(2)		
FB input impedance			0.2		MΩ
Input capacitor			4.7		µF
Output filter capacitor			22		µF
Output filter capacitor ESR				20	mΩ
Output filter inductance			1.0		µH

1. Guaranteed by design.
2. Efficiency measured between the SUP2 PIN and BUCK2 POUT. L = 1 µH, DC resistance max. = 0.036 Ω.

6.3 BUCK3 switching regulator

Unless otherwise noted, typical values at T_A = 25 °C, Vin = 5.0 V.

The max. values are at Tj = 125 °C and the worst case process.

Table 12. BUCK3 switching regulator

Parameter	Conditions	Min.	Typ.	Max.	Unit
DC bias current	PFM mode Deep sleep mode no load		20		µA
Output DC voltage range	Steady state, I_{LOAD} < 1 A	0.7		1.3	V
Output voltage step size	Single step change		25		mV
Load current range	Internal FET, steady state			0.5	A
Current limit threshold	Integrated FET current		2.0(1)		A
PFM current peak	Programmable		0.8		A
DC line regulation	3.3 V < VSUP < 5 V, Iout = 0.5 A		0.4(1)		%/V
DC load regulation	While in PWM PSR3CFG bit 7 = 1		0.1(1)		%/A
Switching frequency	Programmable		1.3		MHz
Output voltage accuracy	While in PWM	-2		+2	%
Transient response	Load transient time = 10 µs. Referring to CCM, Vout = 1.1 V, load current from 0 to 80% Imax.		±3(1)		%
Soft-start time	Vin = 3.3 V, output voltage ramp from 0 to 95% of final Vout = 1.1 V Rload = 3.0 Ω.	130(1)	160(1)		µs
Integrated high-side PFET R_{DS}	Vin = 5 V		172		mΩ
	Vin = 3.3 V		216		
Integrated low-side NFET R_{DS}	Vin = 5 V		88		
	Vin = 3.3 V		106		
Efficiency	Vin = 5.0 V, Vout = 1.1 V, Iload = 1 mA		78(2)		%
	Vin = 3.3 V, Vout = 1.1 V, Iload = 1 mA		81(2)		
	Vin = 5.0 V, Vout = 1.1 V, Iload = 0.5 A		80(2)		
	Vin = 3.3 V, Vout= 1.1 V, Iload = 0.5 A		81(2)		
FB input impedance			0.2		MΩ
Input capacitor			4.7		µF
Output filter capacitor			22		µF
Output filter capacitor ESR				20	mΩ
Output filter inductance			1.0		µH

1. Guaranteed by design.
2. Efficiency measured between the SUP3 PIN and BUCK3 POUT. L = 1 µH, DC resistance max. = 0.036 Ω.

6.4 BUCK4 switching regulator

Unless otherwise noted, typical values at T_A = 25 °C, Vin = 5.0 V.

The max. values are at Tj = 125 °C and the worst case process.

Table 13. BUCK4 switching regulator

Parameter	Conditions	Min.	Typ.	Max.	Unit
DC bias current	No load , PFM mode		20		µA
Output DC voltage range	Steady state, I_{LOAD} < 1 A	0.7		1.3	V
Output voltage step size	Single step change		25		mV
Load current range	Internal FET, steady state			1.0	A
Current limit threshold	Integrated FET current		3.0(1)		A
PFM current peak	Programmable		0.8		A
DC line regulation	3.3 V < VSUP < 5 V Iout = 1 A		0.4(1)		%/V
DC load regulation	While in PWM PSR4CFG bit 7 = 1		0.2(1)		%/A
Switching frequency	Programmable		1.3		MHz
Output voltage accuracy	While In PWM	-2		+2	%
Transient response	Load transient time = 10 µs. Referring to CCM, Vout = 1.1 V, load current from 0 to 80% Imax.		±3(1)		%
Soft-start time	Vin = 3.3 V, output voltage ramp from 0 to 95% of final Vout = 1.1 V, Rload = 1.5 Ω.		360(1)		µs
Integrated high-side PFET R_{DS}	Vin = 5 V		109		mΩ
	Vin = 3.3 V		132		
Integrated low-side NFET R_{DS}	Vin = 5 V		58		
	Vin = 3.3 V		65		
Efficiency	Vin = 5.0 V, Vout = 1.1 V, Iload = 1 mA		82(2)		%
	Vin = 3.3 V, Vout = 1.1 V, Iload = 1 mA		83(2)		
	Vin = 5.0 V, Vout = 1.1 V, Iload = 1 A		81(2)		
	Vin = 3.3 V, Vout = 1.1 V, Iload = 1 A		82(2)		
FB input impedance			0.2		MΩ
Input capacitor			4.7		µF
Output filter capacitor			44		µF
Output filter capacitor ESR				20	mΩ
Output filter inductance			1.0		µH

1. Guaranteed by design.
2. Efficiency measured between the SUP14 PIN and BUCK4 POUT and while the BUCK1 is off. L= 1 µH, DC resistance max = 0.036 Ω.

6.5 BUCK5 switching regulator

Unless otherwise noted, typical values at T_A = 25 °C, Vin = 5.0 V.

The max. values are at Tj = 125 °C and the worst case process.

Table 14. BUCK5 switching regulator

Parameter	Conditions	Min.	Typ.	Max.	Unit
DC bias current	No load , PFM mode		20		µA
Output DC voltage range	Steady state, I_{LOAD} < 1.6 A	0.7		1.3	V
Output voltage step size	Single step change		25		mV
Load current range	Internal FET, steady state			1.6	A
Current limit threshold	Integrated FET current		4.0(1)		A
PFM current peak	Programmable		0.8(1)		A
DC line regulation	3.3 V < VSUP < 5 V, Iload = 1.6 A		0.5(1)		%/V
DC load regulation	While in PWM PSR5CFG bit 7 = 1		0.1(1)		%/A
Switching frequency	Programmable		1.3		MHz
Output voltage accuracy	While in PWM	-2		+2	%
Transient response	Load transient time = 10 µs. Referring to CCM, Vout = 1.1 V, load current from 0 to 80% Imax.		±3(1)		%
Integrated high-side PFET R_{DS}	Vin = 5 V		89		mΩ
	Vin = 3.3 V		105		
Integrated low-side NFET R_{DS}	Vin = 5 V		58		
	Vin = 3.3 V		65		
Efficiency	Vin = 5.0 V, Vout = 1.1 V, Iload = 1 mA		82(2)		%
	Vin = 3.3 V, Vout = 1.1 V, Iload = 1 mA		84(2)		
	Vin = 5.0 V, Vout = 1.1 V, Iload = 1.6 A		78(2)		
	Vin = 3.3 V, Vout = 1.1 V, Iload = 1.6 A		78(2)		
FB input impedance			0.2		MΩ
Input capacitor			4.7		µF
Output filter capacitor			44		µF
Output filter capacitor ESR				20	mΩ
Output filter inductance			1.0		µH

1. Guaranteed by design.
2. Efficiency measured between the SUP5 PIN and BUCK5 POUT. L = 1 µH, DC resistance max. = 0.036 Ω.

6.6 Thermal shutdown

Table 15. Thermal shutdown

Parameter	Conditions	Min.	Typ.	Max.	Unit
Thermal shutdown temp. rising		150	160	170	°C
Thermal shutdown temp. falling		120	130	140	

7 General description

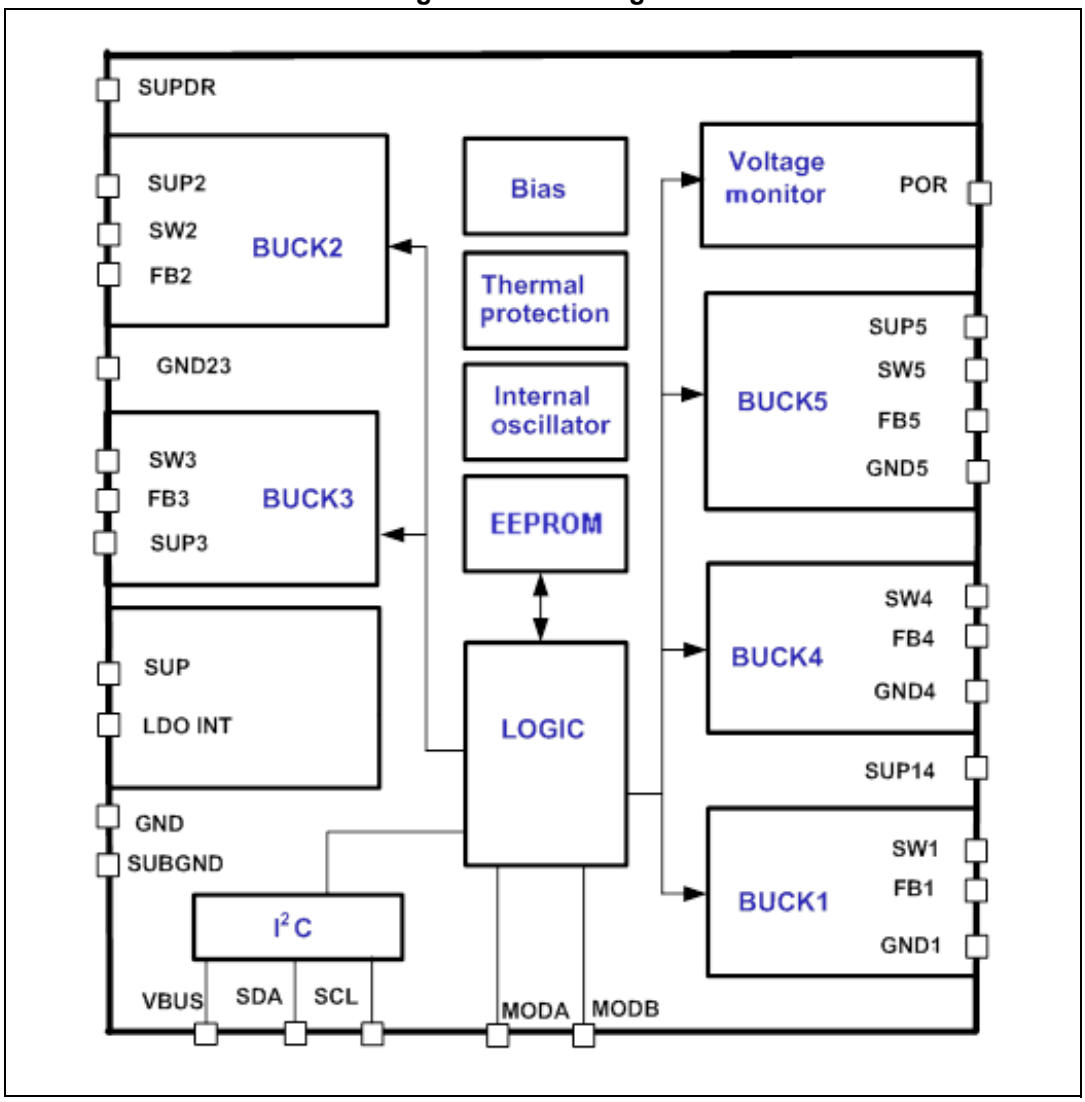
The PMU is an integrated circuit designed to supply the µController and memory in applications supplied by a battery or 5 V. Each regulator is independent from the others and can be enabled or disabled by the I^2C serial port.

A 128-bit EEPROM is embedded in the device to store the default conditions used in each power up:

- The order in which the PSRs start during a power up sequence
- The programmable delay at the beginning and at the end of the power up sequence
- The programmable delay between each regulator start-up
- Excluding from the power up sequence any number of regulators
- The undervoltage mask and digital deglitch programmability for all regulators and for external and internal supplies
- Switching node slew rate programmability, disabling of synchronous rectification, PFM disabling for all switching regulators.

All regulators employ synchronous rectification and have an automatic transition between PWM and PFM. A voltage monitor and thermal protection are present for a better control of system functionality.

Figure 4. Block diagram



8 I²C interface

8.1 Description

This device features an I²C interface and can be operated from a VDD power supply. The I²C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 7-bit device type identifier code in accordance with the I²C bus definition. The device behaves as a slave in the I²C protocol, with all operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and a Read/Write bit (RW), terminated by an acknowledge bit. When writing data to the device, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an ACK for Write and after a NoACK for Read.

8.2 Signal description

8.2.1 Serial clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from the serial clock (SCL) to VDD. In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

8.2.2 Serial data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus.

A pull-up resistor must be connected from serial data (SDA) to VDD.

Figure 5. I²C Start and Stop conditions

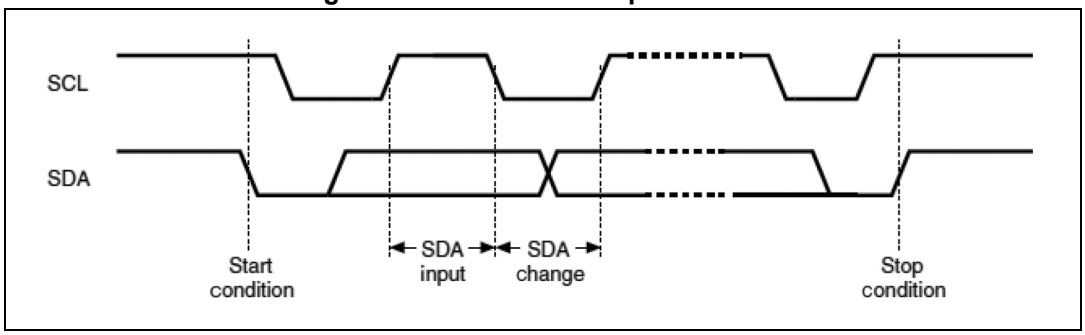
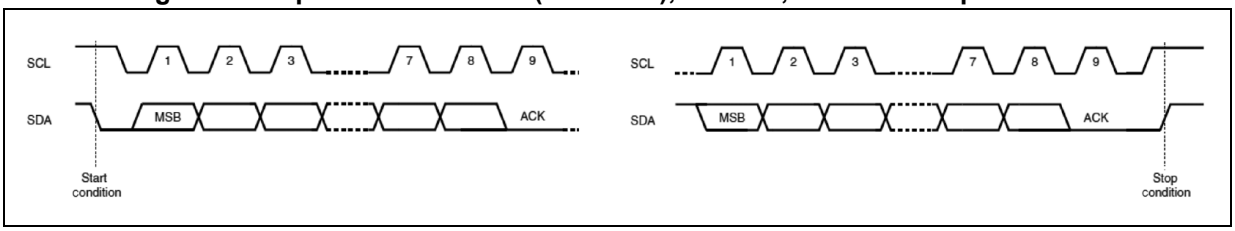


Figure 6. I²C protocol: bit order (MSB first), ACK bit, Start and Stop condition



8.3 I²C device operation

The device supports the I²C protocol. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

8.3.1 Start condition

The start is identified by a falling edge of Serial Data (SDA) while the Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a write cycle) Serial Data (SDA) and the Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

8.3.2 Stop condition

The Stop is identified by a rising edge of Serial Data (SDA) while the Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoACK can be followed by a Stop condition.

The Stop condition can be substituted by a repeated Start condition. In this case the bus remains busy and another communication can start immediately.

8.3.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it is the bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

8.3.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of the Serial Clock (SCL). For the correct device operation, Serial Data (SDA) must be stable during the rising edge of the Serial Clock (SCL), and the Serial Data (SDA) signal must change only when the Serial Clock (SCL) is driven low.

8.3.5 Register bank addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code (on Serial Data (SDA), the most significant bit first). The device select code consists of a 7-bit device type identifier which for the L7292 device is 0x7C.

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations. If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus.

8.3.6 Write operations

Following a Start condition the bus master sends a device select code with the Read/Write bit (RW) reset to 0. The device acknowledges this and waits for one address bytes. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

A Write instruction issued on a Read Only or a reserved address does not modify the register contents.

8.3.7 Byte Write

After the device selects the code and the address byte, the bus master sends one data byte. After the data byte the device responds with an ACK bit, also if the address is read only or reserved. The bus master terminates the transfer by generating a Stop condition or a repeated Start condition.

8.3.8 Sequential Write

The Sequential Write mode allows up to all bytes to be written in a single Write cycle. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 7. Byte Write

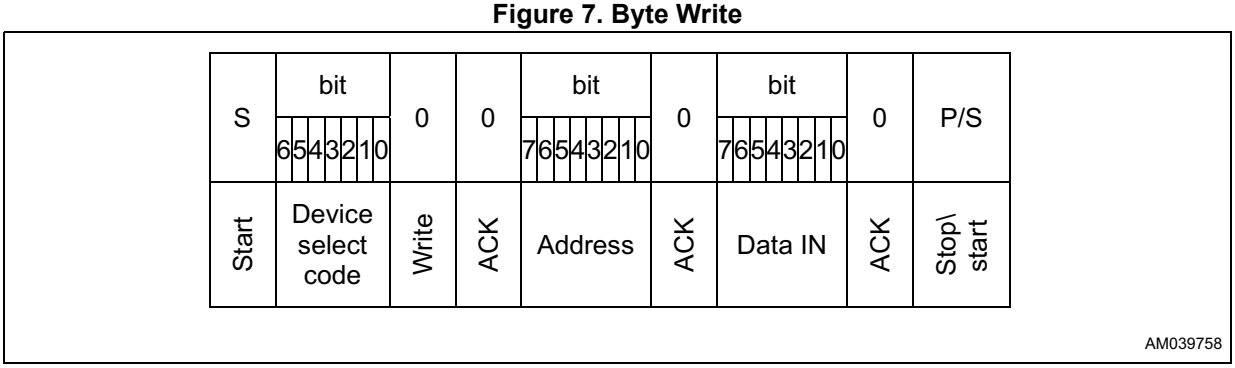
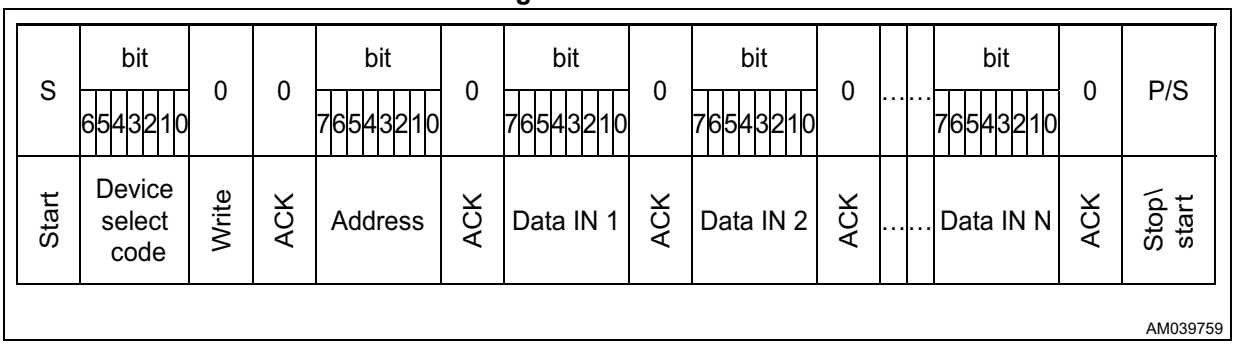


Figure 8. Multi-write



8.3.9 Read operations

Following a Start condition the bus master sends a device select code with the Read/Write bit (RW) set to 1. After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next register address.

8.3.10 Random Address Read

A dummy Write is first performed to load the address into this address counter but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the Read/Write bit (RW) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition or a repeated Start condition.

8.3.11 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the Read/Write bit (RW) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition or a repeated Start condition, without acknowledging the byte.

8.3.12 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition or a repeated Start condition. The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output.

After the last memory address, the address counter “rolls-over”, and the device continues to output data from the memory address 00h.

8.3.13 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer.

Figure 9. Current Address Read

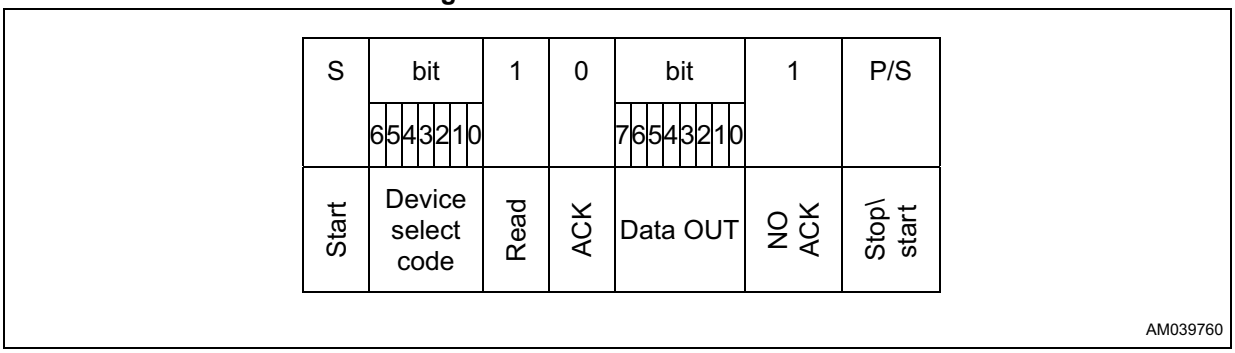


Figure 10. Random Address Read

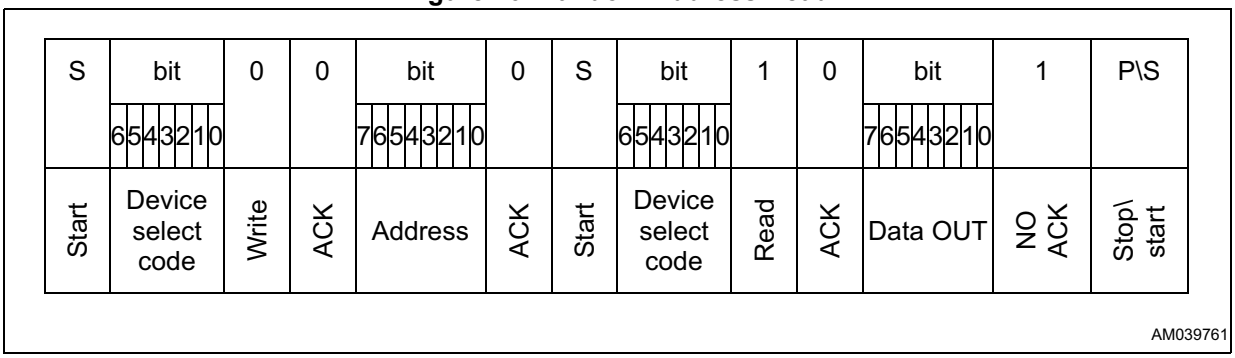


Figure 11. Sequential Current Address Read

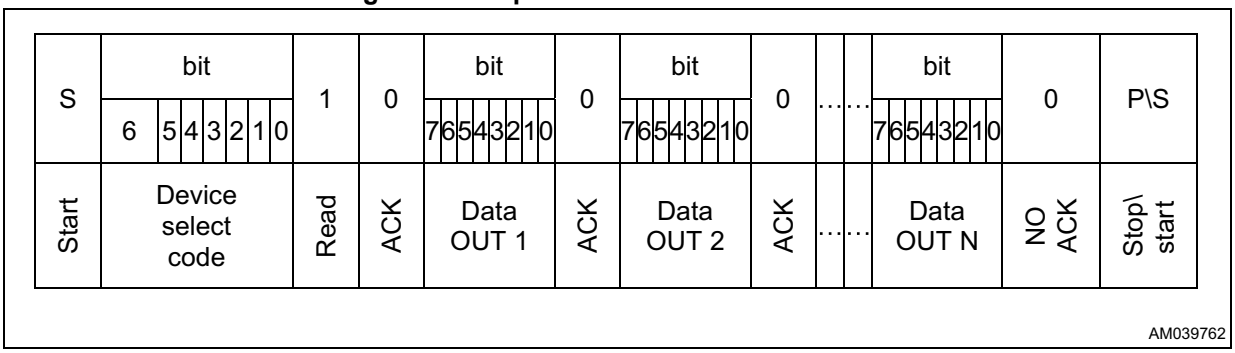
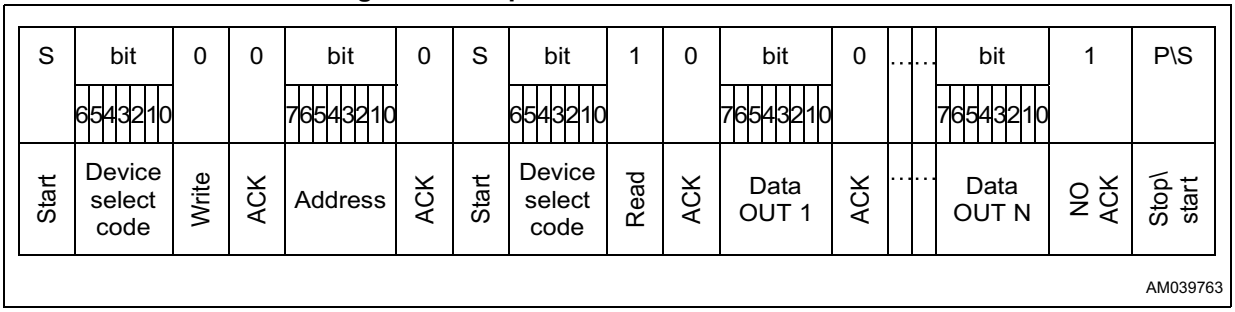


Figure 12. Sequential Random Address Read



8.4 High speed mode support

The device supports the I²C high speed mode to operate up to 3.4 Mbit/s. If the bus master wants to operate in the HS-mode a proper initial sequence in the fast-mode (max. 400 kbit/s) should be sent as described in the I²C bus specification:

1. Start condition (S)
2. 8-bit master code (00001XXX)
3. Not acknowledge bit (A)

After this sequence the bus switches into the high speed mode until first Stop condition.

9 Register map

An internal register bank can be accessed by the I^2C interface. The size of the address space is 64 (address word length = 6 bits). Not every register bit can be accessed in the read/write mode; there are also the read only and reserved bit. A read only bit can be only read and a write operation has no effect. A reserved bit returns '0' when read and a write operation has no effect.

9.1 General overview

Table 16. Register map overview

Address	Name	Description	Bit Name Read/write Reset value							
			7	6	5	4	3	2	1	0
0x01	PSR1VL	Power switching regulator 1 voltage level	PSR1VLEN R/W 0x0	PSR1OCDISR/W 0x0	Reserved	VL[4:0] R/W Default defined by MOD pins				
0x02	PSR3VL	Power switching regulator 3 voltage level	PSR3VLEN R/W 0x0	PSR3OCDISR/W 0x0	Reserved	VL[4:0] R/W Default defined by MOD pins				
0x03	PSR2VL	Power switching regulator 2 voltage level	PSR2VLEN R/W 0x0	PSR2OCDISR/W 0x0	Reserved	VL[4:0] R/W Default defined by MOD pins				
0x04	PSR4VL	Power switching regulator 4 voltage level	PSR4VLEN R/W 0x0	PSR4OCDISR/W 0x0	Reserved	L[4:0] R/W Default defined by MOD pins				
0x05	PSR5VL	Power switching regulator 5 voltage level	PSR5VLEN R/W 0x0	PSR5OCDISR/W 0x0	Reserved	VL[4:0] R/W Default defined by MOD pins				
0x07	PSR1CFG	Power switching regulator 1 configuration	PFMDIS R/W 0x0	ORDER[2:0] R/W 0x2			SLEW[1:0] R/W 0x3		LSDIS R/W 0x0	UVM R/W 0x0
0x08	PSR3CFG	Power switching regulator 3 configuration	PFMDIS R/W 0x0	ORDER[2:0] R/W 0x0			RSLEW[1:0] R/W 0x3		LSDIS R/W 0x0	UVM R/W 0x0
0x09	PSR2CFG	Power switching regulator 2 configuration	PFMDIS R/W 0x0	ORDER[2:0] R/W 0x3			RSLEW[1:0] R/W 0x3		LSDIS R/W 0x0	UVM R/W 0x0
0x0A	PSR4CFG	Power switching regulator 4 configura-tion	PFMDIS R/W 0x0	ORDER[2:0] R/W 0x0			RSLEW[1:0] R/W 0x3		LSDIS R/W 0x0	UVM R/W 0x0
0x0B	PSR5CFG	Power switching regulator 5 configura-tion	PFMDIS R/W 0x0	ORDER[2:0] R/W 0x1			RSLEW[1:0] R/W 0x3		LSDIS R/W 0x0	UVM R/W 0x0

Table 17. Register map overview (continued)

Address	Name	Description	Bit Name Read/write Reset value							
			7	6	5	4	3	2	1	0
0x0A	PSR4CFG	Power switching regulator 4 configuration	PFMDIS R/W 0x0	ORDER[2:0] R/W 0x0			RSLEW[1:0] R/W 0x3		LSDIS R/W 0x0	UVM R/W 0x0
0x0B	PSR5CFG	Power switching regulator 5 configuration	PFMDIS R/W 0x0	ORDER[2:0] R/W 0x1			RSLEW[1:0] R/W 0x3		LSDIS R/W 0x0	UVM R/W 0x0
0x0C	SEQCFG	Power-ON/OFF sequence configuration	DLY1 R/W 0x1	DLY2 R/W 0x1		DLY1CFG R/W 0x1		DLY1 R/W 0x0		
0x0D	PSCFG	Power supply configuration	- Reserved 0x0			EUVM R/W 0x0	IUVM R/W 0x0	- Reserved 0x0		- Reserved 0x0
0x0E	REGCTRL	Regulator control	DSM(1) R/W 0x0	LDO pull-down R/W 0x1	PSR5DIS R/W 0x0	PSR4DIS R/W 0x0	PSR2DIS R/W 0x0	PSR3DIS R/W 0x0	PSR1DIS R/W 0x0	LDODIS R/W 0x0
0x0F	SETCTRL	Setting control	- Reserved 0x0				BUSY R	SDI R	CMDR/W 0x0	
0x10	STATUS	Device status	- Reserved 0x0	TEMPFL R	PSR5FL R	PSR4FL R	PSR2FL R	PSR3FL R	PSR1FL R	LDOFL R

1. Every time the DSM bit is written or erased all the other bits have to include the wanted status.

9.2 Detailed register description

9.2.1 PSR1VL.VL - voltage level

Voltage level = 0.9 V + VL * 25 mV

Table 18. PSR1VL.VL voltage level

VL	Voltage level
0x00	0.9
0x01	0.925
0x02	0.95
0x03	0.975
0x04	1
0x05	1.025
0x06	1.05
0x07	1.075
0x08	1.1
0x09	1.125
0x0A	1.15
0x0B	1.175
0x0C	1.2
0x0D	1.225
0x0E	1.25
0x0F	1.275
0x10	1.3
0x11	1.325
0x12	1.35
0x13	1.375
0x14	1.4
0x15	1.425
0x16	1.45
0x17	1.475
0x18	1.5
0x19	1.525
0x1A	1.55
0x1B	1.575
0x1C - 0xFF	1.6

9.2.2 PSR2VL.VL - voltage level

Voltage level = 1.5 V + VL * 37.5 mV

Table 19. PSR2VL.VL voltage level

VL	Voltage level
0x00	1.5
0x01	1.5375
0x02	1.575
0x03	1.6125
0x04	1.65
0x05	1.6875
0x06	1.725
0x07	1.7625
0x08	1.8
0x09	1.8375
0x0A	1.875
0x0B	1.9125
0x0C	1.95
0x0D	1.9875
0x0E	2.025
0x0F	2.0625
0x10 - 0xFF	2.1

9.2.3 PSR3VL.VL - PSR4VL.VL - PSR5VL.VL - voltage level

Voltage level = 0.7 V + VL * 25 mV

Table 20. PSR3VL.VL - PSR4VL.VL - PSR5VL.VL - voltage level

VL	Voltage level
0x00	0.7
0x01	0.725
0x02	0.75
0x03	0.775
0x04	0.8
0x05	0.825
0x06	0.85
0x07	0.875
0x08	0.9
0x09	0.925
0x0A	0.95
0X0B	0.975
0x0C	1
0x0D	1.025
0x0E	1.05
0x0F	1.075
0x10	1.1
0x11	1.125
0x12	1.15
0x13	1.175
0x14	1.2
0x15	1.225
0x16	1.25
0x17	1.275
0x18 - 0xFF	1.3

9.2.4 PSRxLV.PSRxLVEN - voltage level selection enable

- 0: voltage level selection register disabled; voltage level is selected via MOD pins.
- 1: voltage level selection register enabled; output voltage changed according to the register selection.

9.2.5 PSRxLV.PSRxOCDIS - overcurrent disable

- 0: overcurrent for the regulator is enabled.
- 1: overcurrent for the regulator is disabled.

9.2.6 PSRxCFG.PFMDIS - PFM disable

- 0: PFM mode enabled.
- 1: PWM mode forced in the light-load mode.

9.2.7 YYYxCFG.ORDER - order in power up sequence

- 0x0: first regulator to be turned on.
- 0x1: second regulator to be turned on.
- …
- 0x5 - 0x7: last regulator to be turned on.

9.2.8 PSRxCFG.RSLEW - driver slew rate

- 0x0: 500 V/µs
- 0x1: 1000 V/µs
- 0x2 1500 V/µs
- 0x3: 2000 V/µs

9.2.9 PSRxCFG.LSDIS - low side disable

- 0: low side enabled.
- 1: low side disabled.

9.2.10 YYYxCFG.UVM - mask undervoltage fault

- 0: undervoltage generates fault.
- 1: undervoltage does not generate fault.

9.2.11 SEQCFG.DLY2 - Delay 2

Delay between two sequence steps.

- 0x0: 0 ms / no delay
- 0x1: 0.5 ms
- 0x2: 1.0 ms
- 0x3: 2.0 ms

9.2.12 SEQCFG.DLY1CFG - Delay 1 configuration

Delay before/after power up sequence configuration.

- 0x0: no delay.
- 0x1: delay before POR rising edge.
- 0x2: delay before starting sequence.
- 0x3: delay before starting sequence and before POR rising edge.

9.2.13 SEQCFG.DLY1 - Delay 1

Delay before de-assert POR (if enabled) and before starting sequence (if enabled).

If SEQCFG Bit 7 = 0

- 0x0: 10 ms
- 0x1: 12 ms
- 0x2: 14 ms
- 0x3: 16 ms
- 0x4: 18 ms
- 0x5: 20 ms
- 0x6: 22 ms
- 0x7: 24 ms

If SEQCFG Bit 7 = 1

- Delay1 = 8 ms

9.2.14 PSCFG.EUVM - external undervoltage mask

Mask external supply undervoltage fault.

- 0: undervoltage generates fault.
- 1: undervoltage does not generate fault.

9.2.15 PSCFG.IUVM - internal undervoltage mask

Mask internal supply undervoltage fault.

- 0: undervoltage generates fault.
- 1: undervoltage does not generate fault.

9.2.16 PSCFG.DEGL - deglitch

Digital deglitch filter time duration for regulator output voltage monitor

- 0x0: 0 µs
- 0x1: 1 µs
- 0x2: 2 µs
- 0x3: 5 µs

9.2.17 REGCTRL.DSM - deep sleep mode

- 0: deep sleep mode disabled.
- 1: deep sleep mode enabled.

9.2.18 REGCTRL.LDO pull-down

- 0: pull-down but not in DSM.
- 1: always pull-down.

9.2.19 REGCTRL.YYYxDIS - PSRx/LDO disable

- 0: regulator is turned on.
- 1: regulator is turned off.

9.2.20 SETCTRL.BUSY - busy

EEPROM busy, new operation not allowed.

- 0: new operation can be commanded.
- 1: no new operation can be commanded; all registers are locked, writing operation will not have effect.

9.2.21 SETCTRL.SDI - setting data integrity

Setting data integrity status.

- 0: OK, data integrity check passed.
- 1: fault, data integrity check not passed.

9.2.22 SETCTRL.CMD - command

Operation to be executed on setting data registers: address 0x00-0x0E.

- 0x0: no operation.
- 0x1: save as default.
- 0x2: restore default.
- 0x3: restore factory default.

9.2.23 STATUS.YYYxFL - fault

Temperature, PSRx and LDO fault status.

- 0: no fault.
- 1: fault detected.

10 EEPROM

EEPROM description

128 bits of the user accessible EEPROM are provided in the device.

The EEPROM can be managed using the SETCTRL (“Setting Control”) register.

The registers 0x00 through 0x0E (15 registers of 8 bits) are user-accessible and can be saved in the EEPROM to retain data at power-down. The EEPROM is managed as a whole block, meaning that all bits from registers 0x00 to 0x0E are loaded and saved at once in a single operation when accessing the EEPROM.

The SETCTRL (setting control) register is used to operate on the EEPROM.

To commence a **write operation** of the whole 0x00 - 0x0E block, the operations needed are as follows:

- Value 0x1 must be written via a serial interface to the SETCTRL.CMD bits (reg. 0x0F [1:0]).
- The SETCTRL.BUSY bit (reg. 0x0F [3]) will stay high for the duration of the EEPROM writing process, and can be **optionally** polled to assess the write status.
- The SETCTRL.CMD (reg. 0x0F [2]) can be **optionall**y used to check if the operation was successful (bit low).

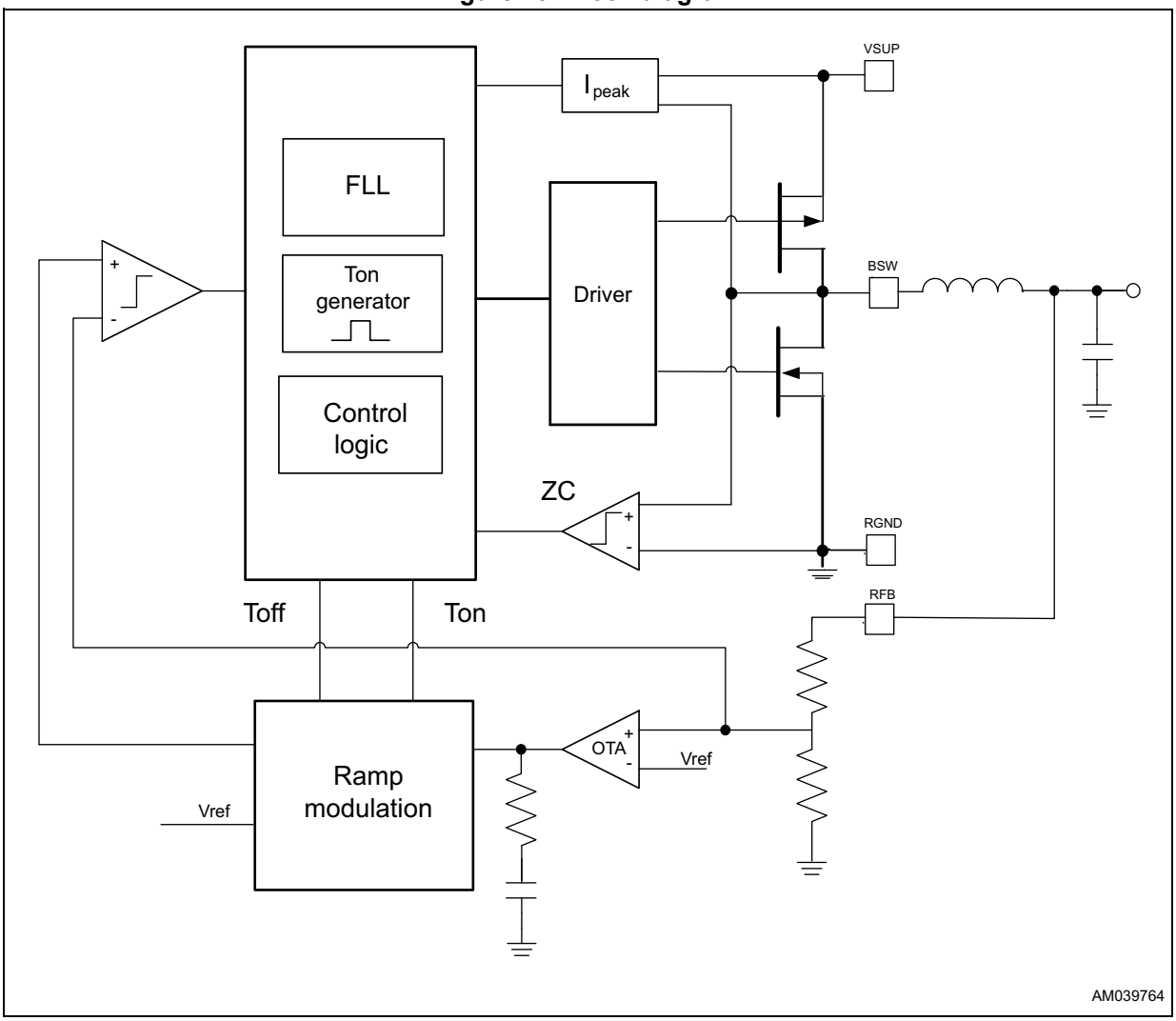
To commence a **read operation** of the whole 0x00 - 0x0E block, the operations needed are as follows:

- Value 0x2 must be written via a serial interface to the SETCTRL.CMD bits (reg. 0x0F [1:0]).
- The SETCTRL.BUSY bit (reg. 0x0F [3]) will stay high for the duration of the EEPROM reading process, and can be **optionally** polled to assess the read status.
- The SETCTRL.CMD (reg. 0x0F [2]) can be **optionally** used to check if the operation was successful (bit low).

To load the hard-coded default settings for registers 0x00 to 0x0E, value 0x3 must be written via a serial interface to the SETCTRL.CMD bits (reg. 0x0F[1:0]).

11 Buck regulator description

Figure 13. Block diagram



The PMU includes five synchronous buck regulators, PWM control, adaptive TON and pseudo fixed frequency imposed by FLL at medium to high loads and PFM mode control at light-loads to reduce the switching power losses and improve efficiency.

Main functionalities are:

- MOD selection
- Regulator sequence programmability
- Soft-start
- PWM
- PFM
- Forced PWM in light-load
- Current limiting
- Short-circuit protection
- Deep sleep mode
- Forced pull-down

11.1 MOD selection - pin MODA, MODB

Connecting the pins MODA and MODB to GND or VBUS the default VOUT of switching regulators changes according to *Table 22*.

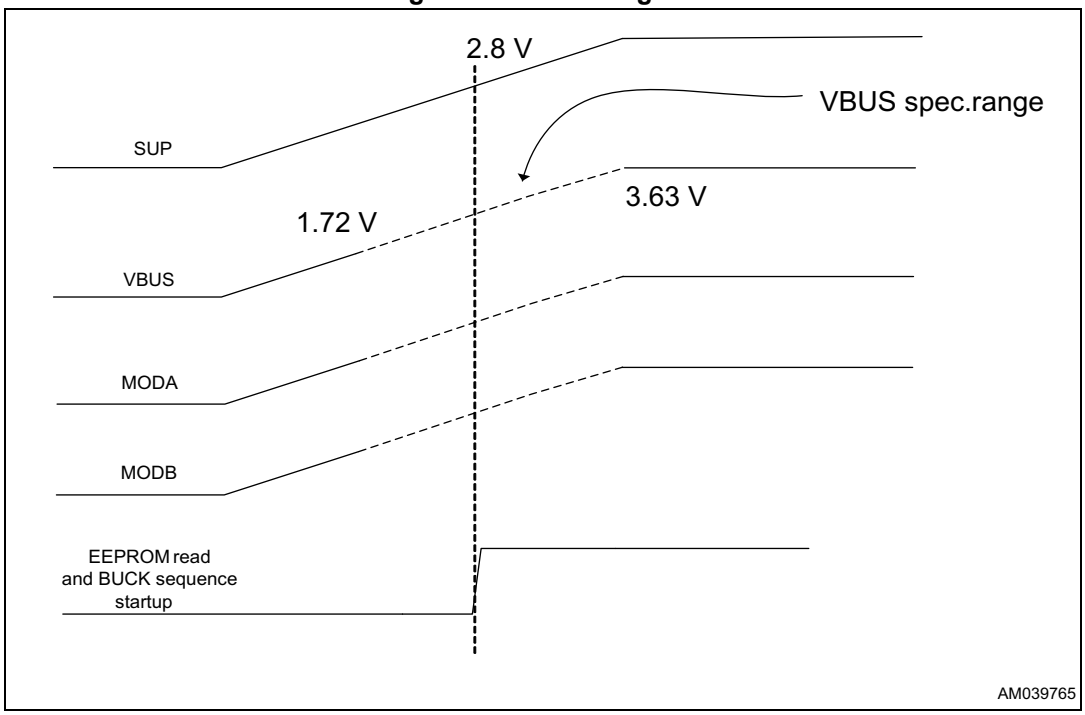
Table 21. Models selection

Pin	SET A	SET B	SET C	SET D
MODA	GND	VBUS	GND	VBUS
MODB	GND	GND	VBUS	VBUS

Table 22. Regulators output voltage

BUCK	SET A VOUT [V]	SET B VOUT[V]	SET C VOUT[V]	SET D VOUT [V]
BUCK1	1.2	1.5	1.35	1.35
BUCK2	1.8	1.8	1.8	1.8
BUCK3	1.1	1.0	1.0	1.1
BUCK4	1.1	1.0	1.0	1.1
BUCK5	1.1	1.0	1.0	1.1

Figure 14. Block diagram



The MODA and MODB status is latched inside the L7292 device when SUP ≥ 2.8 V and VBUS is > 70% of its min. value (70% of 1.72 V). After that the EEPROM is read and the wanted power up sequence enabled.

11.2 VOUT selection

By writing the PSRxVLEN (bit 7) = 1 in the register:

- PSR1VL for BUCK1
- PSR2VL for BUCK2
- PSR3VL for BUCK3
- PSR4VL for BUCK4
- PSR5VL for BUCK5

It is possible to change the default output voltage of each regulator. This operation disables the MODA and MODB functionality.

In *Table 23* are reported the output voltage ranges selectable by register map bits and the status when in the DSM mode.

Table 23. VOUT ranges

Regulator	Vout min. [V]	Vout max. [V]	Max. DC CURRENT [A]	Vout step [mV]	DSM mode
BUCK1	0.9	1.6	1.0	25	Off
BUCK2	1.5	2.1	0.8	37.5	Off
BUCK3	0.7	1.3	0.5	25	On
BUCK4	0.7	1.3	1.0	25	Off
BUCK5	0.7	1.3	1.6	25	Off

11.3 Regulator sequence programmability

The device offers a wide power-on sequence programmability. For each regulator it is possible to define the initial status (enable or disable each regulator) and the order in the power up sequence. Other settings are:

SEQCFG.DLY2 - Delay 2 - delay between two sequence steps

- 0x0: 0 ms / no delay
- 0x1: 0.5 ms
- 0x2: 1.0 ms
- 0x3: 2.0 ms

SEQCFG.DLY1CFG - Delay 1 - configuration delay before/after power up sequence configuration

- 0x0: no delay
- 0x1: delay before POR rising edge
- 0x2: delay before starting sequence
- 0x3: delay before starting sequence and before POR rising edge.

SEQCFG.DLY1 - Delay 1 - delay before de-assert POR (if enabled) and before starting sequence (if enabled)

If SEQCFG Bit 7 = 0

- 0x0: 10 ms
- 0x1: 12 ms
- 0x2: 14 ms
- 0x3: 16 ms
- 0x4: 18 ms
- 0x5: 20 ms
- 0x6: 22 ms
- 0x7: 24 ms

If SEQCFG Bit 7 = 1

- Delay1 = 8 ms

At the power up two conditions have to be asserted before to enable the ON phase of switching regulators.

1. LDO INT voltage = 1.8 V
2. SUP voltage ≥ 2.8 V

When these conditions are asserted the default conditions stored in the EEPROM are performed.

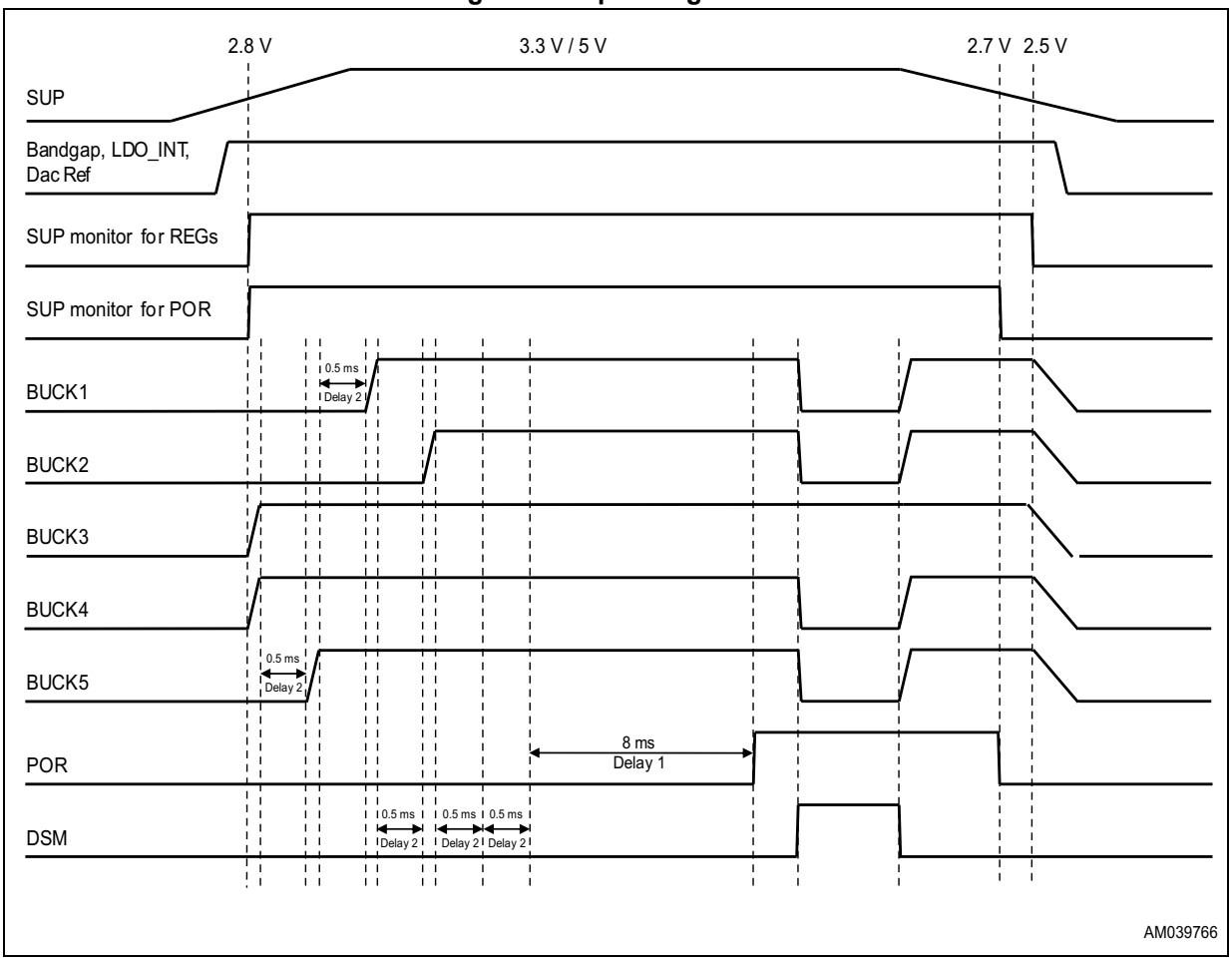
During this phase the comparators related to each BUCKx and Vsupply track the output voltage with the threshold defined by the regulator adjustment bits.

After the BUCKx, Vsupplyx, and LDO INT are good, a programmable reset delay timeout begins. After the programmed delay, the POR pin is pulled high through the internal pull-up resistor to VBUS enabling the entire functionalities.

The timing detail is as follows (based on the default soft-start order and delays programmed in the EEPROM): when the last start-up of regulators has ended (BUCK2 is the last one in soft-start sequence, by default), it starts the count of two Delay 2, and then the POR delay count (Delay 1) begins.

This means that with the default settings (Dly 1 = 8 ms, Dly 2 = 0.5 ms), the POR is released and starts to be pulled up through the internal resistor 9 ms after the end of the start-up routine of the last regulator.

Figure 15. Operating mode



11.4 Soft-start

To limit the inrush current in each buck regulator a soft-start circuit is embedded inside. This feature is performed using a sequence of 96 pulses of three current levels to increase the output voltage in a controlled manner.

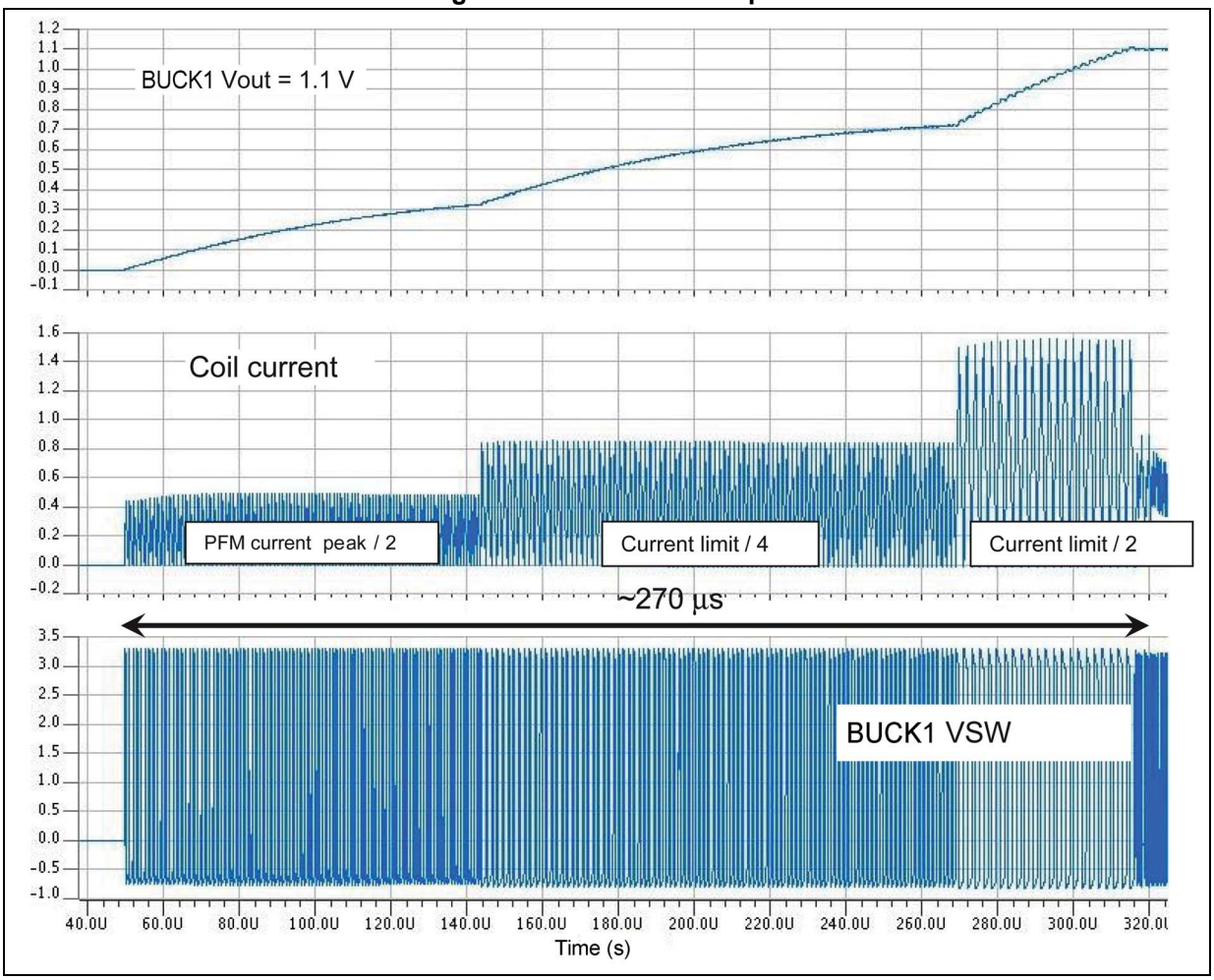
The complete the sequence is:

- 96 current pulses at PFM current peak / 2
- 96 current pulses at current limit / 4
- 96 current pulses at current limit / 2

According to the load current during the soft-start one or all of the three current levels could be used.

For example, in light-load condition only the “PFM current peak” step could be enough to reach the target Vout in short time. If the load current is higher, the “current limit / 4" step is enabled (*Figure 16*); if again this isn't enough, the “current limit / 2" is applied.

Figure 16. Soft-start example



11.5 PWM mode

In the PWM operative mode, the output voltage is regulated using a quasi constant on-time control in conjunction with a modulated ramp signal which reproduces the output voltage ripple in order to achieve loop stability and to be unaffected by the external capacitor ESR value.

The OTA output generates a voltage proportional to the difference between the reference voltage and Vout in order to minimize the DC error on Vout.

The ramp output is compared with VOUT to trigger the Ton event. The duration of Ton is managed by a FLL that controls dynamically the on-time duration so that the PSR can achieve a relatively constant switching frequency. The advantage of the constant frequency is to minimize the EMI and to give the possibility to add a fixed filter to remove residual noise. In addition a slew rate programmability of the switching output is implemented.

11.6 PFM mode

To maintain high efficiency in light-load condition the device enters automatically the PFM mode for a load current of around IDCM/2 or lower. This happens when the inductor current becomes discontinuous.

During the PFM operation, the converter fixes the output voltage to the nominal DC value plus ½ Vout ripple that is affected by the output capacitor, the current ripple in the inductor and the load current.

In this phase the high-side PMOS current is limited at IDCM and the pulses frequency is proportional to the load current. When the PMOS current reaches IDCM the PMOS is switched OFF while the NMOS is forced ON. This is valid until a zero current is detected, then the regulator output is set in high impedance until Vout crosses the nominal value.

11.7 Forced PWM

When enabled, the buck regulator always operates in the PWM mode regardless of the output current. In the light-load the efficiency will be worse than in the PFM mode due to the inductor current becoming negative.

This function enables the ability to have a constant frequency in light-load condition and also reduces the output voltage ripple.

11.8 Current limiting

According to the max. load current, an I_{LIMIT} is embedded in each regulator to protect the device and any external components from overload conditions.

When the high-side PMOS current reaches the I_{LIMIT}, the regulator output is forced in high impedance for around 1 µs, allowing the inductor current to decrease to a safe level before allowing another on-time to happen.

11.9 Short-circuit protection

In case the high-side PMOS current reaches the current limit and Vout falls below the short-circuit voltage threshold, the regulator is switched off permanently, until another full power-up of the whole device is performed.

11.10 Deep sleep mode

This feature is enabled when the device has to provide the minimum functionality of the system, to reduce the quiescent current and to be ready to restart the operative conditions when needed.

The device can be placed in the “Deep Sleep Mode” (DSM) by writing bit 7 REGCTRL = 1 in this mode.

- Regulator 3 is enabled - no load current, in the PFM mode.
- Regulators 1 - 2 - 4 - 5 are OFF.

In *Table 24* are reported the quiescent current values: in the left column the case of all regulators ON with no load, while the in right column the DSM condition.

Table 24. Quiescent current

Regulator	Quiescent current (no load) [µA]	DSM quiescent current (no load) [µA]
BUCK1	20	0
BUCK2	20	0
BUCK3	20	20
BUCK4	20	0
BUCK5	20	0
BIAS	75	40
TOT.	**175**	**60**

During the DSM phase it is possible to enable/disable the regulators writing in the REGCTRL register the proper enable bit. This allows the possibility to start the post DSM phase with a different regulators setting. The DSM functionality is not enabled if POR is low.

11.11 Forced pull-down

When the regulator is disabled by a bit or forced by a POR the regulator switching node is pulled down through a discharge MOSFET switch, in order to discharge the output voltage.

11.12 Voltage monitor

The voltage monitor of SUP is always enabled with the threshold as described in *Table 9: Voltage monitor and POR generator on page 14*?. When a fault happens (2.7 V) the POR signal is driven low, while the REGs are switched OFF only when the SUP voltage reaches 2.5 V.

The regulators voltage monitors are enabled only during the soft-start sequence until the POR signal is asserted. After that, all PSRs voltage monitors are disabled and only “short-circuit protection” is enabled.

11.13 Thermal protection

When die temperature reaches the overtemperature condition (> 150 °C) all the regulators are automatically disabled, POR is asserted and the buck SW output pins are pulled low through a discharge MOSFET switch. To avoid unstable conditions a 30 °C hysteresis is applied. When the die temperature reaches the low threshold all the regulators start the power up sequence following the default conditions.

11.14 Fault summary

Figure 17. Operative mode

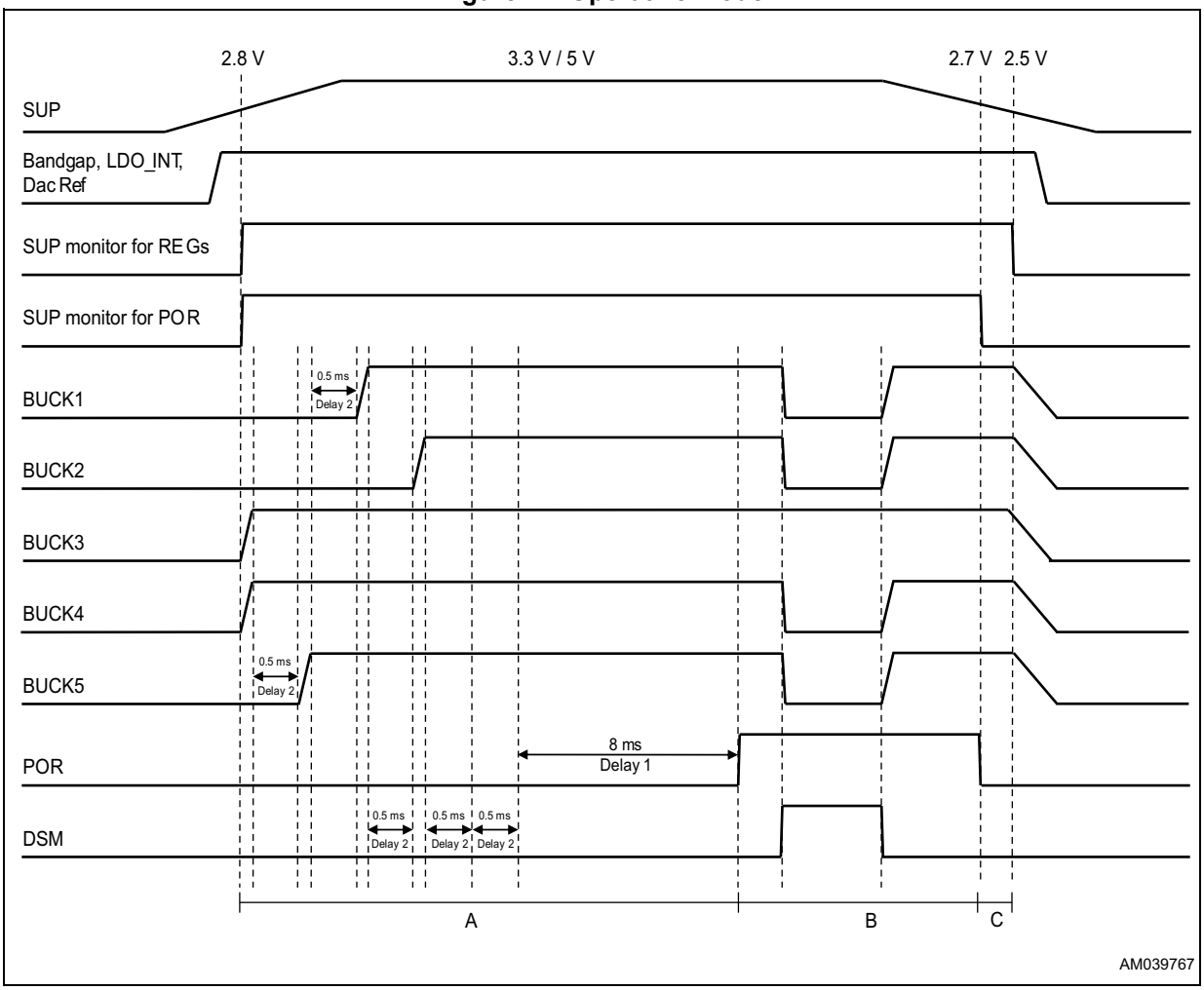


Table 25. Protections

Protection	A (POR low) start-up	B (POR high) steady state	C (POR low) power-down
Overcurrent	Enabled for regulators with VOUT in target. When an overcurrent event occurs the regulator is forced in tristate for 1 µs, then it continues regulating.	The regulator is forced in tristate for 1 µs, then it continues regulating.	The regulator is forced in tristate for 1 µs, then it continues regulating.
Undervoltage	Enabled with UVth = 85% of VOUT. When a fault occurs a soft-start is performed again.	Disabled	Disabled
Short-circuit	Disabled	Switch-off of failed reg. for overcurrent + Vout < 0.5 V.	Switch-off of failed reg. for overcurrent + Vout < 0.5 V.

Table 26. Fault summary

Fault type	Register bit	POR	BUCK1 - 2 - 3 - 4 - 5 action
SUP undervoltage		Yes	No actions on ALL regulators until SUP ≤ 2.5 V is reached, and then all OFF and SW outputs pulled low through the resistor.
VBUCK 1 - 2 - 3 - 4 - 5 undervoltage	PSR1 - 2 - 3 - 4 - 5 FL	No	Enabled at power up before POR rising.
Overtemperature	TEMPFL	Yes	ALL regulators OFF and SW outputs pulled low through the resistor. Restart with a soft-start when the temperature falls below the lower threshold.

11.15 Noisy immunity improvement

In order to avoid false overcurrent detection that could be triggered by a very noisy application environment, it is strongly recommended to set to 0 the hidden “OCTON” (OverCurrentTON) bits:

- PSR1 reg 0x22 bit[1]=0, writing “C8” in the register
- PSR2 reg 0x28 bit[1]=0, writing “C8” in the register
- PSR3 reg 0x25 bit[1]=0, writing “C8” in the register
- PSR4 reg 0x2B bit[1]=0, writing “C8” in the register
- PSR5 reg 0x2E bit[1]=0, writing “C8” in the register

This setting keeps always on the current limiter comparator.

The typical current consumption of the comparator is 40 µA. If OCTON bits = 1 (that is the default), the current consumption is reduced by the PSR duty cycle, if OCTON bits = 0 the current consumption is 40 µA constant.

12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

12.1 VQFN 5 x 5 x 0.9 40L package information

Figure 18. VQFN 5 x 5 x 0.9 40L package outline

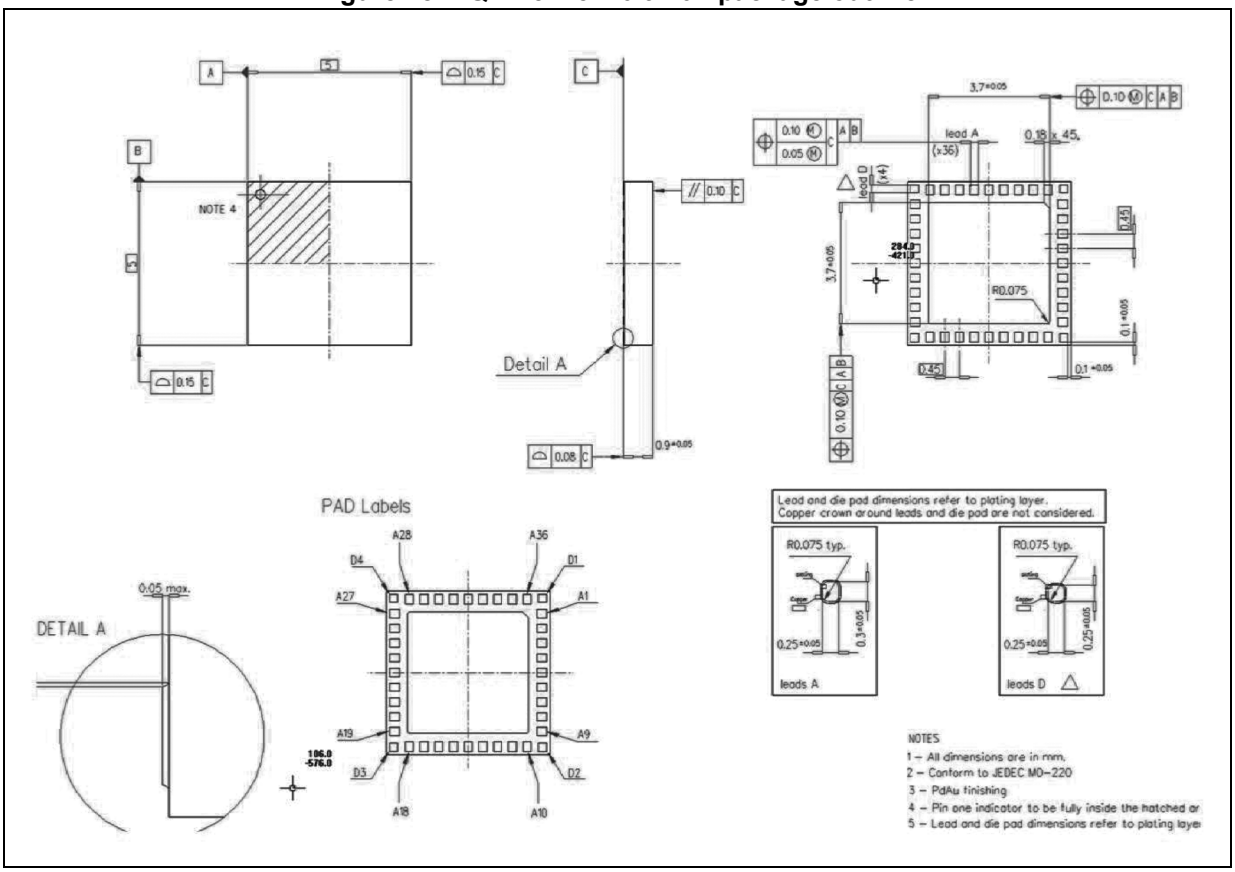


Table 27. VQFN 5 x 5 x 0.9 40L package mechanical data

Symbol	Dimensions for PLANT 994D (mm)			
	Min.	Typ.	Max.	Notes
A	0.80	0.90	1.00	(1)
A1	0.02	0.05	0.08	(2), (3)
A2		0.75		
A3		0.13		
D		5.00		
D2	3.65	3.70	3.75	
E		5.00		
E2	3.65	3.70	3.75	
b	0.22	0.25	0.28	
L	0.27	0.3	0.33	
Lead D	0.22	0.25	0.28	
e		0.45		
e1		2.25		
e2		2.275		
aaa			0.15	
bbb			0.10	
ddd			0.05	
eee			0.10	(4)
Fff			0.08	(5)

1. VQFN-Sr stands for “Very Thin Quad Flat Non-leaded - Single Row”. Low profile: The total profile height (Dim. A) is measured from the seating plane to the top of the component.s
2. The terminal A1 corner must be identified on the top surface through a inked or laser mark dot. A distinguishing feature is allowable on the bottom surface of the package, chamfer at the die paddle corner to identify the terminal A1. Exact shape of each corner is optional.
3. Terminal A1 corner index area.
4. The tolerance of the position that controls the location of the pattern of pads with respect to datum A and B. For each pad there is a cylindrical tolerance zone eee perpendicular to datum C and located on the true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each pad must lie within this tolerance zone.
5. The tolerance of the position that controls the location of the pads within the matrix with respect to each other. For each pad there is a cylindrical tolerance zone fff perpendicular to datum C and located on the true position as defined by e. The axis perpendicular to datum C of each pad must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each pad must lie simultaneously in both tolerance zones.

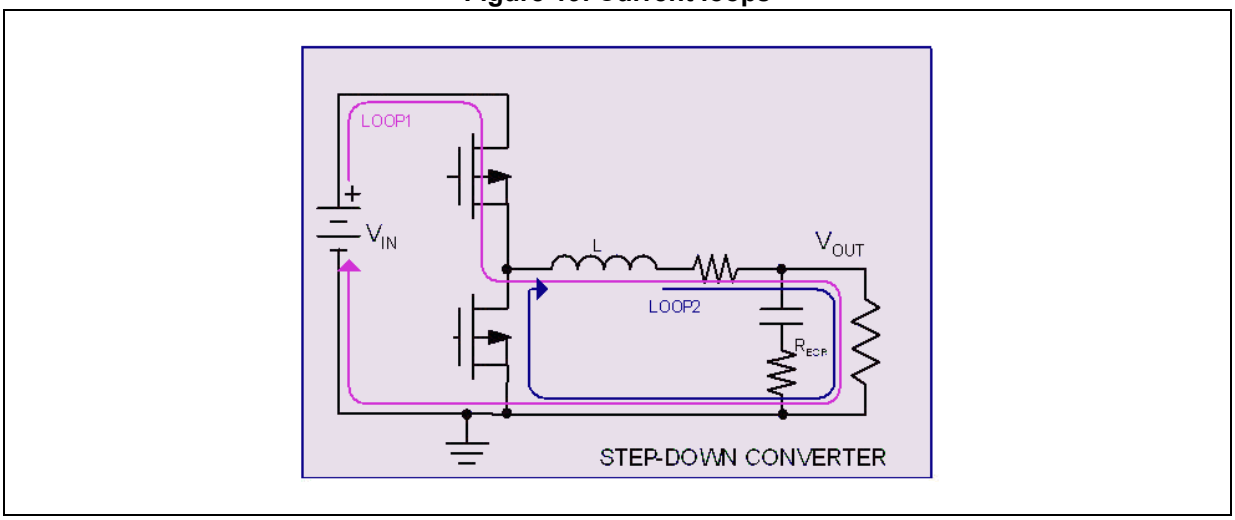
13 PCB design rules guideline

13.1 Basic principles

A step-down converter reduces an incoming voltage to a lower output voltage. A switching element, typically a bipolar or a MOSFET is switched on and off. When the switch is on, the input supply charges the inductor and capacitor and delivers power to the load. During this time, the magnitude of the inductor current ramps up as it flows through the loop 1.

When the MOSFET turns off, the input is disconnected from the output, and the inductor and output capacitor support the load. The magnitude of the inductor current ramps down as it flows through the recirculating element, following the direction indicated in the loop 2. The recirculating element can be a diode, but recently a more efficient synchronous rectification system is used where a second switching element takes over the function of the diode.

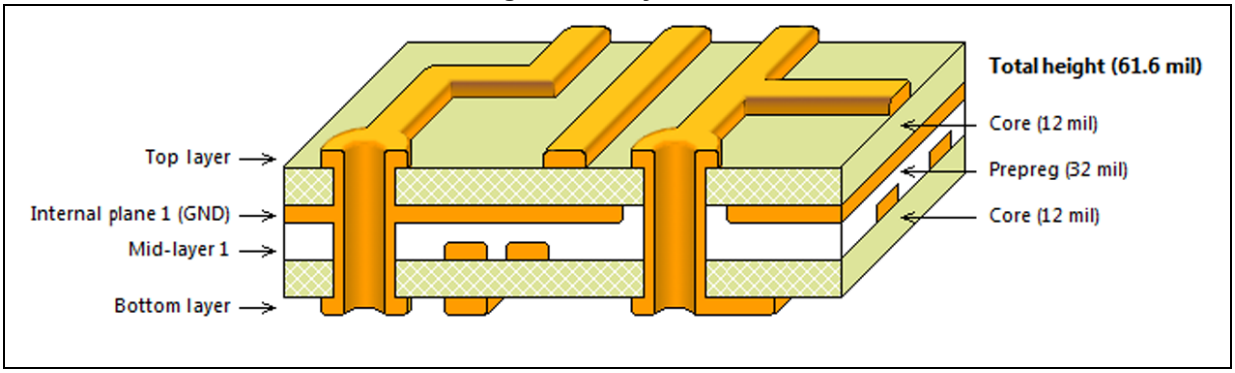
Figure 19. Current loops



13.2 Layout rules

A multilayer board is preferred using the top layer to contain all power routing for the devices, and inner layer 1 as a ground return plane.

Figure 20. Layer stack



13.2.1 Supplies

An incoming supply per switcher should be adequately buffered using an input capacitor. Refer to the device specification for suggested values. This capacitor needs to be placed as close as possible to the VIN pin to minimize the loop area.

13.2.2 Switch node

The switch node is the pin feeding the inductor. Keep the switch node as short as possible to avoid power losses. Do not make it wider than necessary to avoid capacitive loading of the switch node.

13.2.3 Feedback node

The feedback node is a high impedance input and thus sensitive to noise and current injection through the capacitive and magnetic coupling. Keep the feedback lines away from large switching surfaces or magnetic fields. Remember that magnetic fields are not stopped by copper!

Feedback components should be connected to a clean return pathway and never share return paths with the main switching elements.

13.2.4 Output capacitors

Multiple output capacitors are preferred over a single one. Each capacitor should have its own return via.

13.3 PCB layout recommendation

Figure 21. All layers (top view)

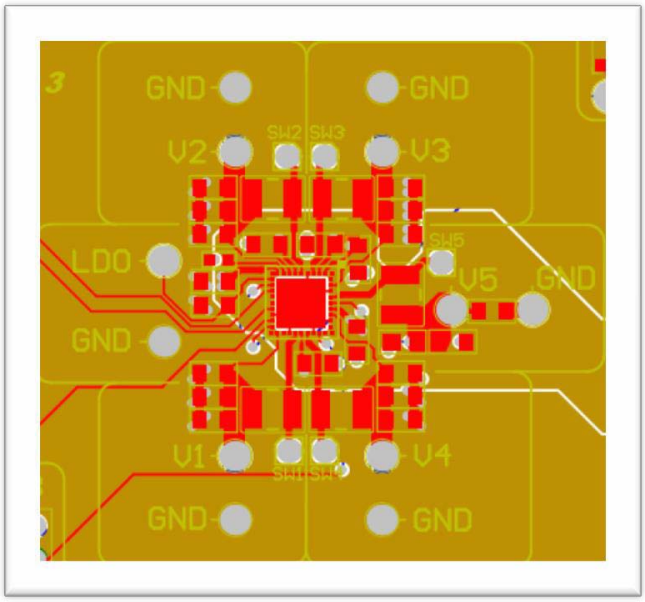


Figure 22. All layers (through view)

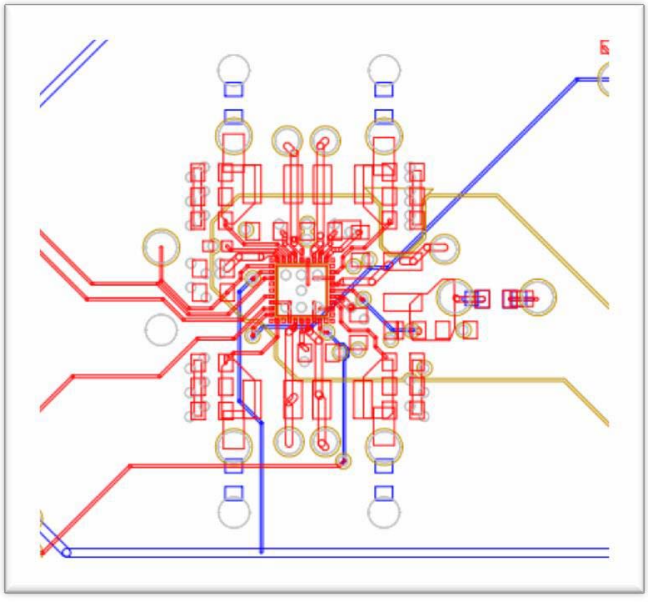


Figure 23. Top layer

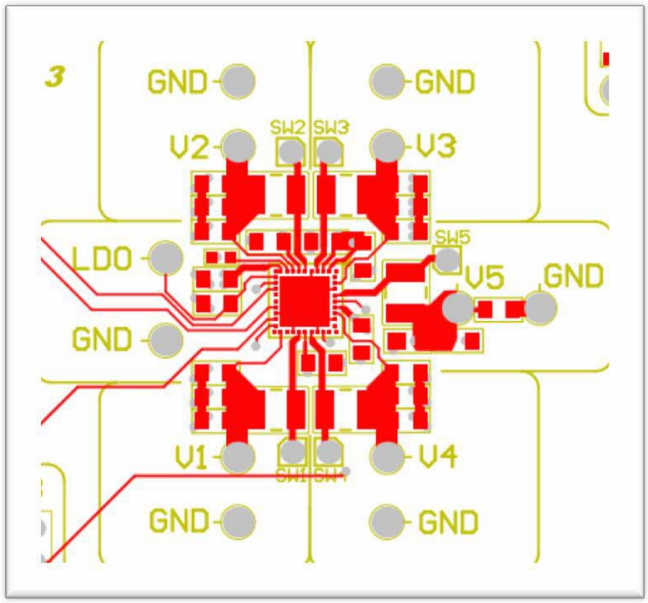


Figure 24. Bottom layer

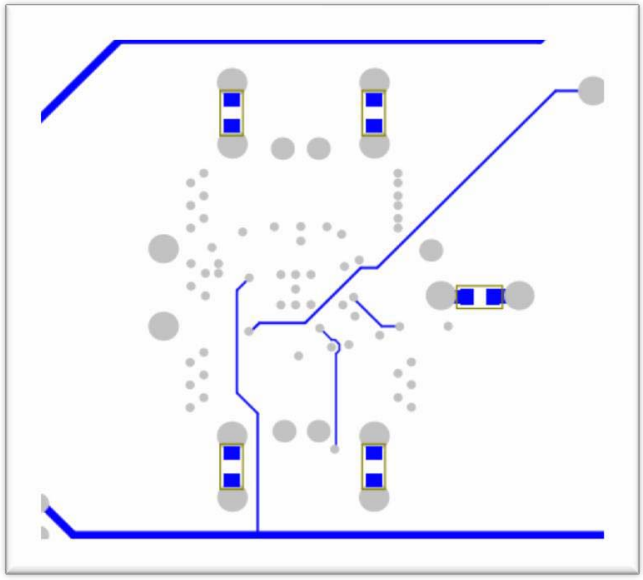


Figure 25. Middle layer 1 (ground)

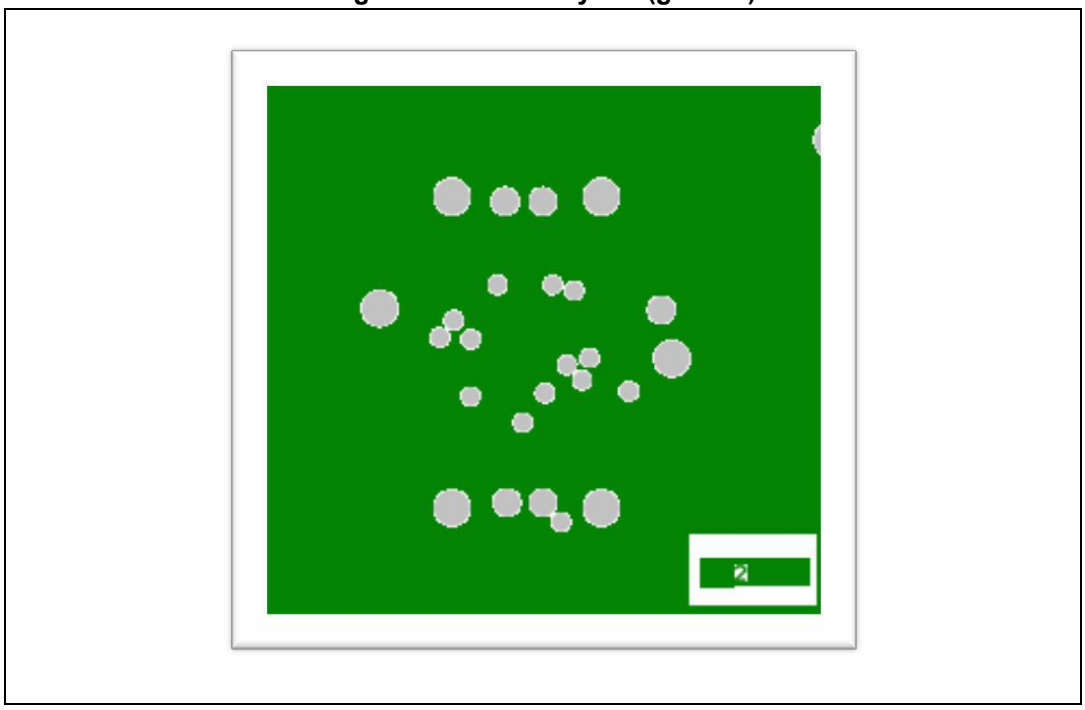
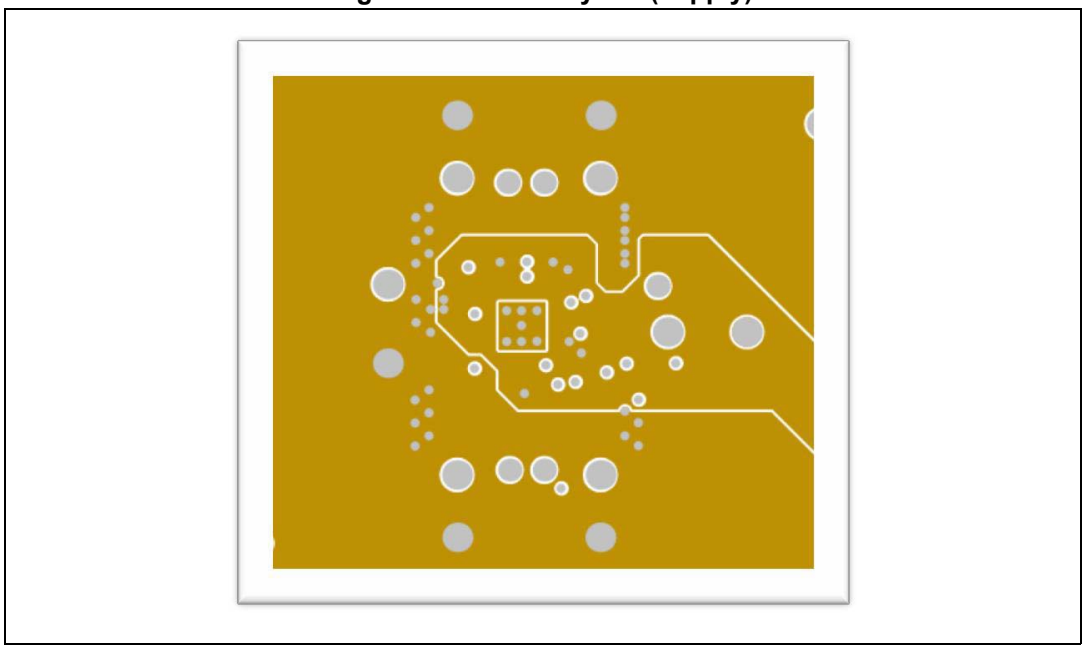


Figure 26. Middle layer 2 (supply)



13.4 General rules

- Do not share vias. Every component connecting to the power or the reference plane needs its own via.
- For large currents multiple vias are to be preferred.
- Vias shall be placed as close as possible to the component pin.
- Feedback nodes are sensitive. Keep them away from magnetic fields and nodes that may capacitive couple energy into them.

13.5 Thermal aspects

The device package uses the center pad as a thermal conduit. This pad should be connected to an adequate spread of copper. When following the suggested layer stack the internal ground plane may be sufficient. If lots of other heat generating components are close by it may be necessary to create an exposed copper area on the backside of the board. The pad should be connected using multiple vias.

14 Evaluation tool

THE ST L7292 evaluation kit consists of a serial port exerciser and a device dedicated daughter board. The system allows the device full performance evaluation as well as debug.

Figure 27. Serial port exerciser

Figure 28. L7292 daughter board

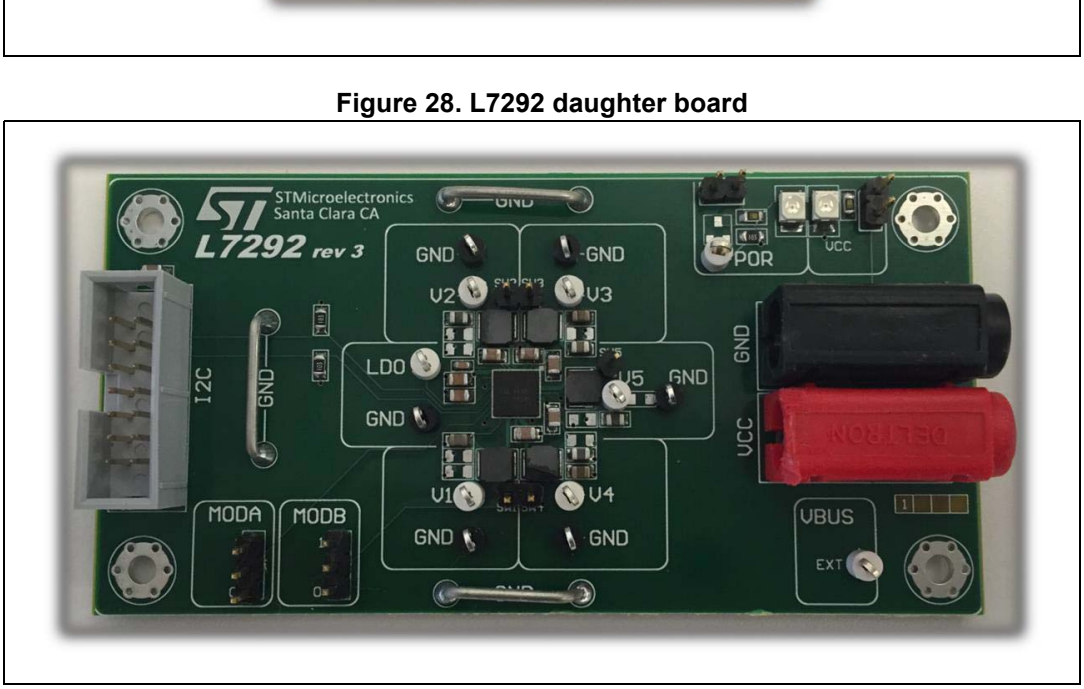


Figure 29. L7292 evaluation system - hardware

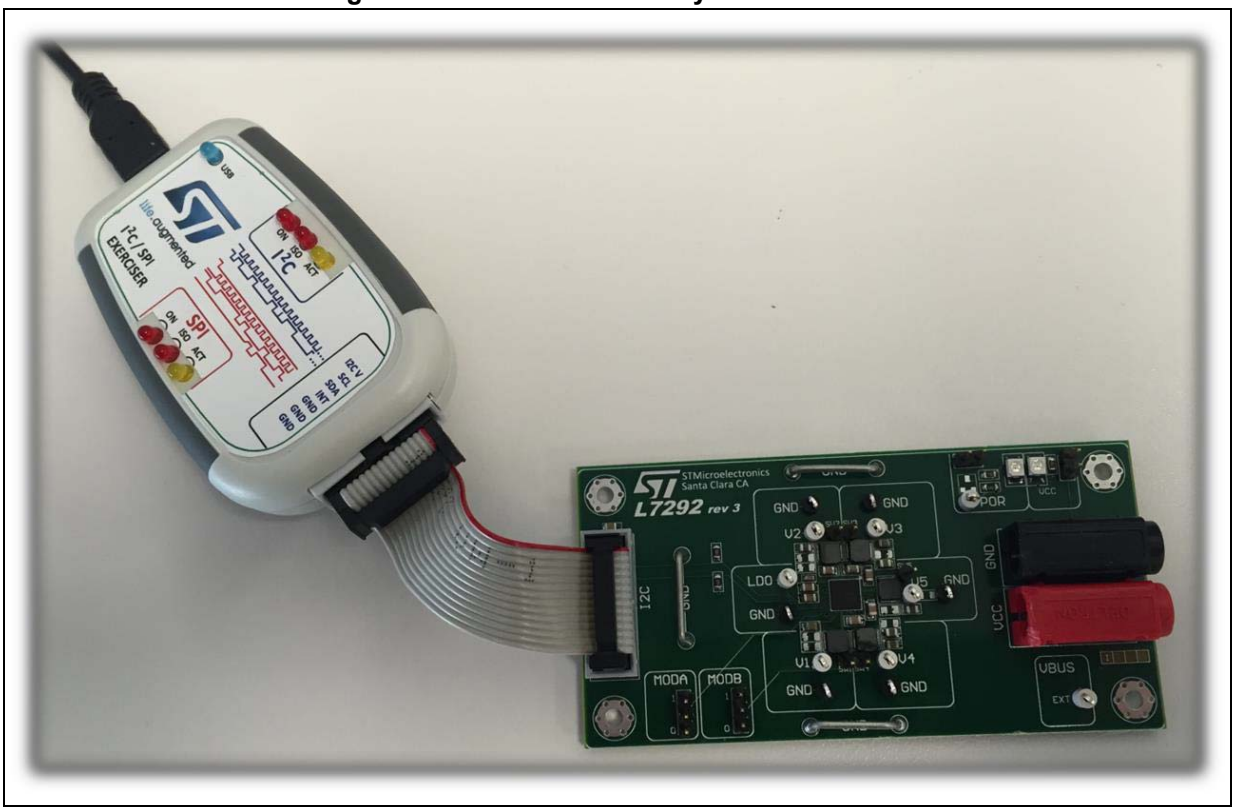
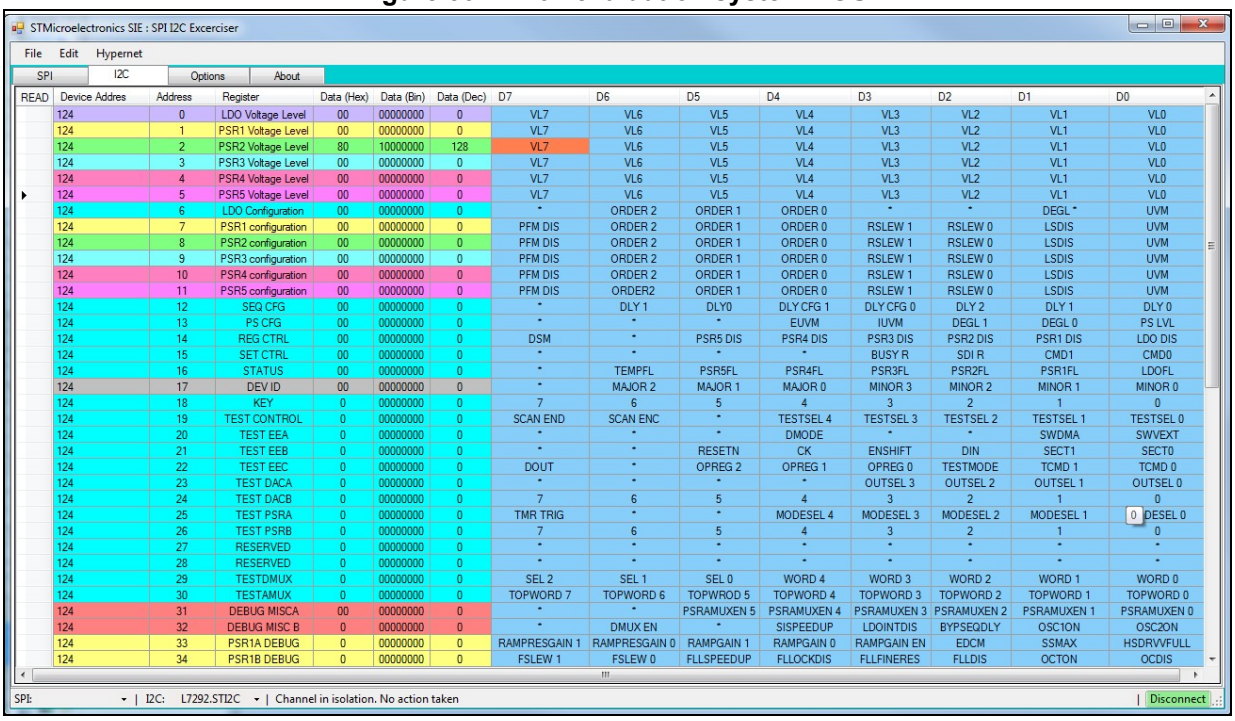


Figure 30. L7292 evaluation system - GUI



15 Order codes

Table 28. Order codes

Order code	Package	Packing
L7292D	VQFN_sr 5 x 5	Tape and reel
L7292DT	VQFN_sr 5 x 5	Tray

16 Revision history

Table 29. Document revision history

Date	Revision	Changes
05-Nov-2015	1	Initial release.
19-May-2016	2	Added *Section 11.15 on page 48*.

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