TPS6206x-Q1 采用 2 × 2 SON 封装的 3MHz 2A 降压转换器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：–40°C 至 125°C 工作结温范围
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件充电器件模型 (CDM) ESD 分类等级 C4B
- 3MHz 开关频率
- V_{IN} 范围：2.9V 至 6V
- 效率高达 97%
- 节能模式和 3MHz 固定脉宽调制 (PWM) 模式
- 电源正常输出
- PWM 模式下的输出电压精度为 ±1.5%
- 输出放电功能
- 典型值为 18μA 的静态电流
- 针对最低压降的 100% 占空比
- 电压定位
- 时钟抖动
- 支持最高 1mm 的解决方案
- 采用 2 × 2 × 0.75mm 晶圆级小外形无引线 (WSON) 封装

2 应用

- 负载点稳压器
- 汽车负载点 (POL)
- 汽车摄像机模块
- 汽车信息娱乐和导航系统
- 高级驾驶员辅助系统 (ADAS) 应用

3 说明

TPS62065-Q1 和 TPS62067-Q1 器件是一款高效同步降压 DC-DC 转换器。 该器件可提供高达 2A 的输出电流。

该器件的输入电压范围为 2.9V 至 6V，非常适合对 5V 或
3.3V 系统电源轨进行电源转换。 TPS62065-Q1 和 TPS62067-Q1 工作在 3MHz 固定频率下，并且在轻负载电流条件下会进入节能模式，从而在整个负载电流范围内保持高效率。 该节能模式针对低输出电压纹波进行了优化。 对于低噪声应用，可通过将 MODE 引脚拉为高电平来强制 TPS62065-Q1 器件进入固定频率 PWM 模式。 TPS62067-Q1 提供了开漏电源正常输出。 在关断模式下，电流消耗降至 5μA，同时内部电路将使输出电容放电。 TPS62065-Q1 和 TPS62067-Q1 器件经过了优化，可与微型 1μH 电感以及小型 10μF 输出电容搭配工作，从而实现了最小解决方案尺寸以及高稳压性能。

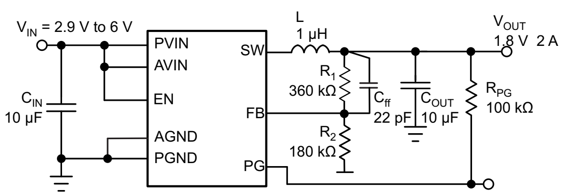
TPS62065-Q1 和 TPS62067-Q1 器件采用小型 2 × 2 × 0.75mm 8 引脚 WSON 封装。

器件信息(1)

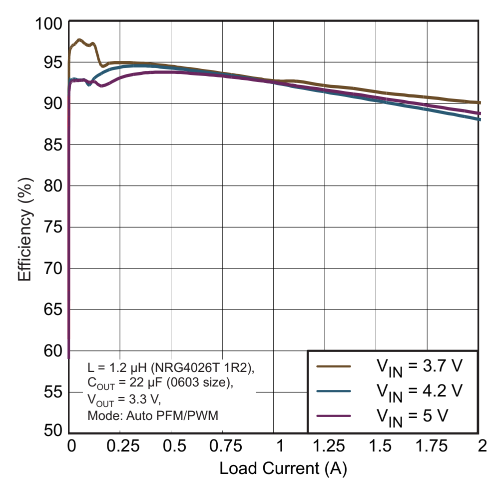
器件型号	封装	封装尺寸
TPS62065-Q1	WSON (8)	2.00mm x 2.00mm
TPS62067-Q1		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 典型应用电路



效率与负载电流间的关系



目录

5 修订历史记录

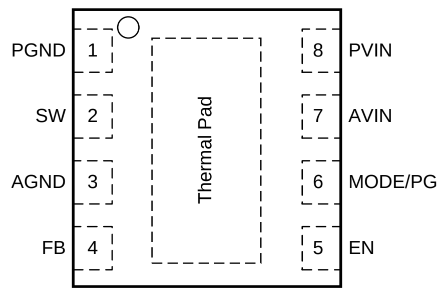
日期	修订版本	注释
2015 年 1 月	*	最初发布。

6 Device Comparison Table

PART NUMBER	MODE/PG FUNCTION
TPS62065Q1	MODE = selectable; Power Good = no
TPS62067Q1	Automatic PWM/PFM transition; Power Good = yes

7 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	PGND	—	GND supply pin for the output stage.
2	SW	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
3	AGND	—	Analog GND supply pin for the control circuit.
4	FB	IN	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
5	EN	IN	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated
6	MODE/PG	IN	**MODE**: MODE pin = high forces the device to operate in fixed frequency PWM mode. MODE pin = low enables the power save mode with automatic transition from PFM mode to fixed frequency PWM mode. This pin must be terminated. (TPS62065-Q1)
		Open Drain	**PG**: Power Good open-drain output. Connect an external pullup resistor to a rail which is below or equal AVIN. (TPS62067-Q1)
7	AVIN	IN	Analog V_{IN} power supply for the control circuit must be connected to PVIN and input capacitor.
8	PVIN	PWR	V_{IN} power supply pin for the output stage.
—	Thermal Pad	—	For good thermal performance, this pad must be soldered to the land pattern on the PCB. This pad should be used as device GND.

8 Specifications

8.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage [2]	AVIN, PVIN	–0.3	7	V
	EN, MODE/PG, FB	–0.3	V_{IN} + 0.3 < 7	
	SW	–0.3	7	
Current (sink)	into PG		1	mA
Current (source)	Peak output	Internally limited		A
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2500	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
AV_{IN} , PV_{IN}	Supply voltage	2.9		6	V
	Output current capability			2000	mA
	Output voltage range for adjustable voltage	0.8		VIN	V
L	Effective Inductance Range	0.7	1	1.6	µH
C_{OUT}	Effective Output Capacitance Range	4.5	10	22	µF
T_J	Operating junction temperature	–40		125	°C

8.4 Thermal Information

THERMAL METRIC[1]		DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.78	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.60	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.63	
ψ_{JT}	Junction-to-top characterization parameter	1.65	
ψ_{JB}	Junction-to-board characterization parameter	35.02	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.61	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to 125°C), typical values are at T_J = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 10 µF 0603, C_{OUT} = 10 µF 0603, L = 1 µH.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.9		6	V
I_Q	Operating quiescent current	I_{OUT} = 0 mA, device operating in PFM mode and not device not switching		18		µA
I_{SD}	Shutdown current	EN = GND, current into AVIN and PVIN combined		0.1	5	µA
V_{UVLO}	Undervoltage lockout threshold	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.99	
ENABLE, MODE						
V_{IH}	High level input voltage	2.9 V ≤ V_{IN} ≤ 6 V	1		6	V
V_{IL}	Low level input voltage	2.9 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_{IN}	Input bias current	EN, Mode tied to GND or AVIN		0.01	1	µA
POWER GOOD OPEN DRAIN OUTPUT						
V_{THPG}	Power good threshold voltage	Rising feedback voltage	93%	95%	98%	
		Falling feedback voltage	87%	90%	92%	
V_{OL}	Output low voltage	I_{OUT} = –1 mA; must be limited by external pullup resistor (1)			0.3	V
I_{LKG}	Leakage current into PG pin	$V_{(PG)}$ = 3.6 V			100	nA
t_{PGDL}	Internal power good delay time			5		µs
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 3.6 V (1)		120	180	mΩ
		V_{IN} = 5 V(1)		95	150	
$R_{DS(on)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6 V(1)		90	130	mΩ
		V_{IN} = 5 V(1)		75	100	
I_{LIMF}	Forward current limit MOSFET high-side and low-side	2.9 V ≤ V_{IN} ≤ 6 V	2300	2750	3300	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		10		
OSCILLATOR						
f_{SW}	Oscillator frequency	2.9 V ≤ V_{IN} ≤ 6 V	2.6	3	3.4	MHz
OUTPUT						
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage PWM Mode	PWM operation, MODE = V_{IN}, 2.9 V ≤ V_{IN} ≤ 6 V, 0-mA load	–1.5%	0%	1.5%	
$V_{FB(PFM)}$	Feedback voltage PFM mode, Voltage Positioning	device in PFM mode, voltage positioning active(2)		1%		
V_{FB}	Load regulation			–0.5		%/A
	Line regulation			0		%/V
$R_{(Discharge)}$	Internal discharge resistor	Activated with EN = GND, 2.9 V ≤ V_{IN} ≤ 6 V, 0.8 ≤ V_{OUT} ≤ 3.6 V	75	200	1450	Ω
t_{START}	Start-up time	Time from active EN to reach 95% of V_{OUT}		500		µs

(1) Maximum value applies for T_J = 85°C
(2) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the parameter measurement information.

8.6 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Shutdown Current	Input Voltage and Ambient Temperature	Figure 1
Quiescent Current	Input Voltage	Figure 2
Oscillator Frequency	Input Voltage	Figure 3
Static Drain-Source On-State Resistance	Input Voltage, Low-Side Switch	Figure 4
	Input Voltage, High-Side Switch	Figure 5
$R_{DISCHARGE}$	Input Voltage vs. V_{OUT}	Figure 6

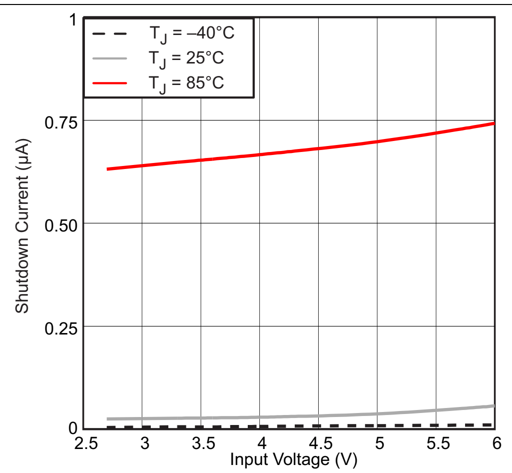


Figure 1. Shutdown Current vs Input Voltage and Ambient Temperature

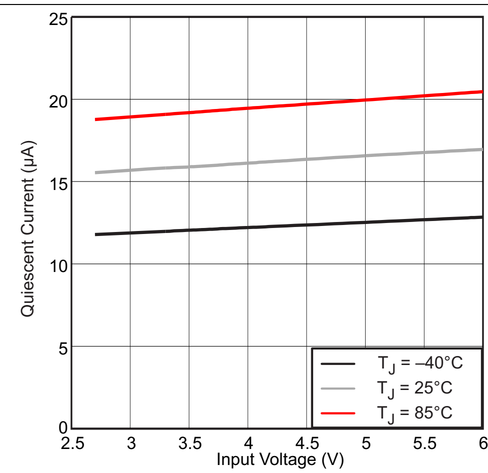


Figure 2. Quiescent Current vs Input Voltage

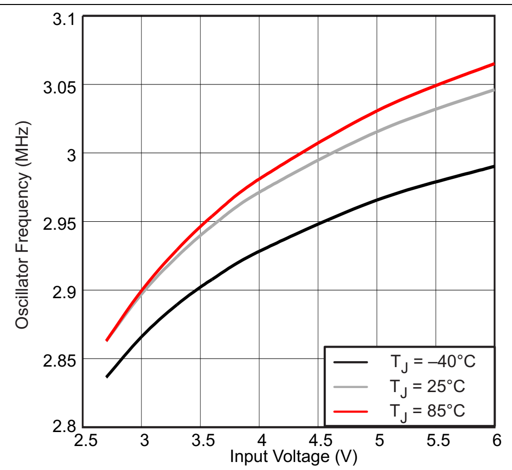
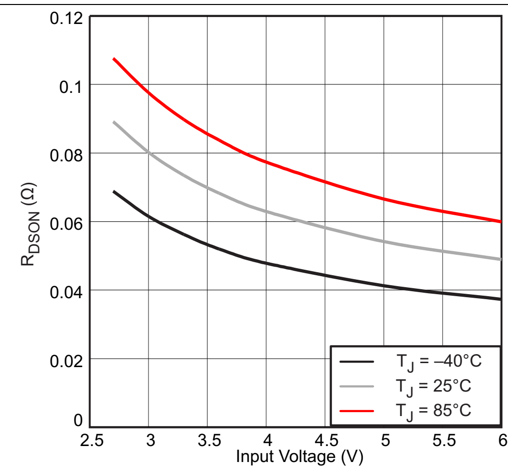
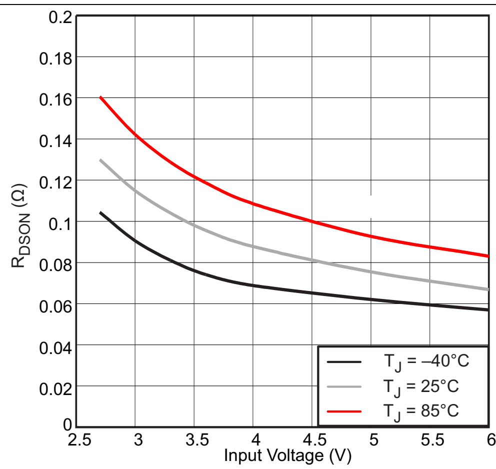


Figure 3. Oscillator Frequency vs Input Voltage



Low-Side Switch

Figure 4. Static Drain-Source On-State Resistance vs Input Voltage



High-Side Switch

Figure 5. Static Drain-Source On-State Resistance vs Input Voltage

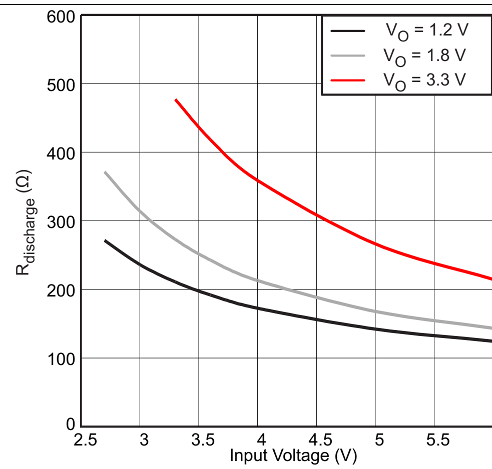
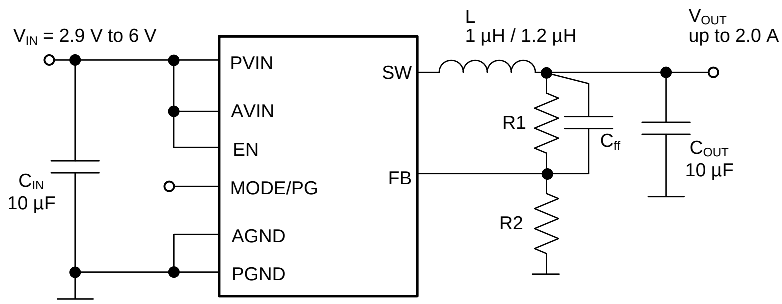


Figure 6. $R_{DISCHARGE}$ vs Input Voltage

9 Parameter Measurement Information



L: LQH44PN1R0NP0, L = 1 µH,Murata, NRG4026T1R2, L = 1.2 µH, Taiyo Yuden

C_{IN}/C_{OUT}: GRM188R60J106U, Murata 0603 size

10 Detailed Description

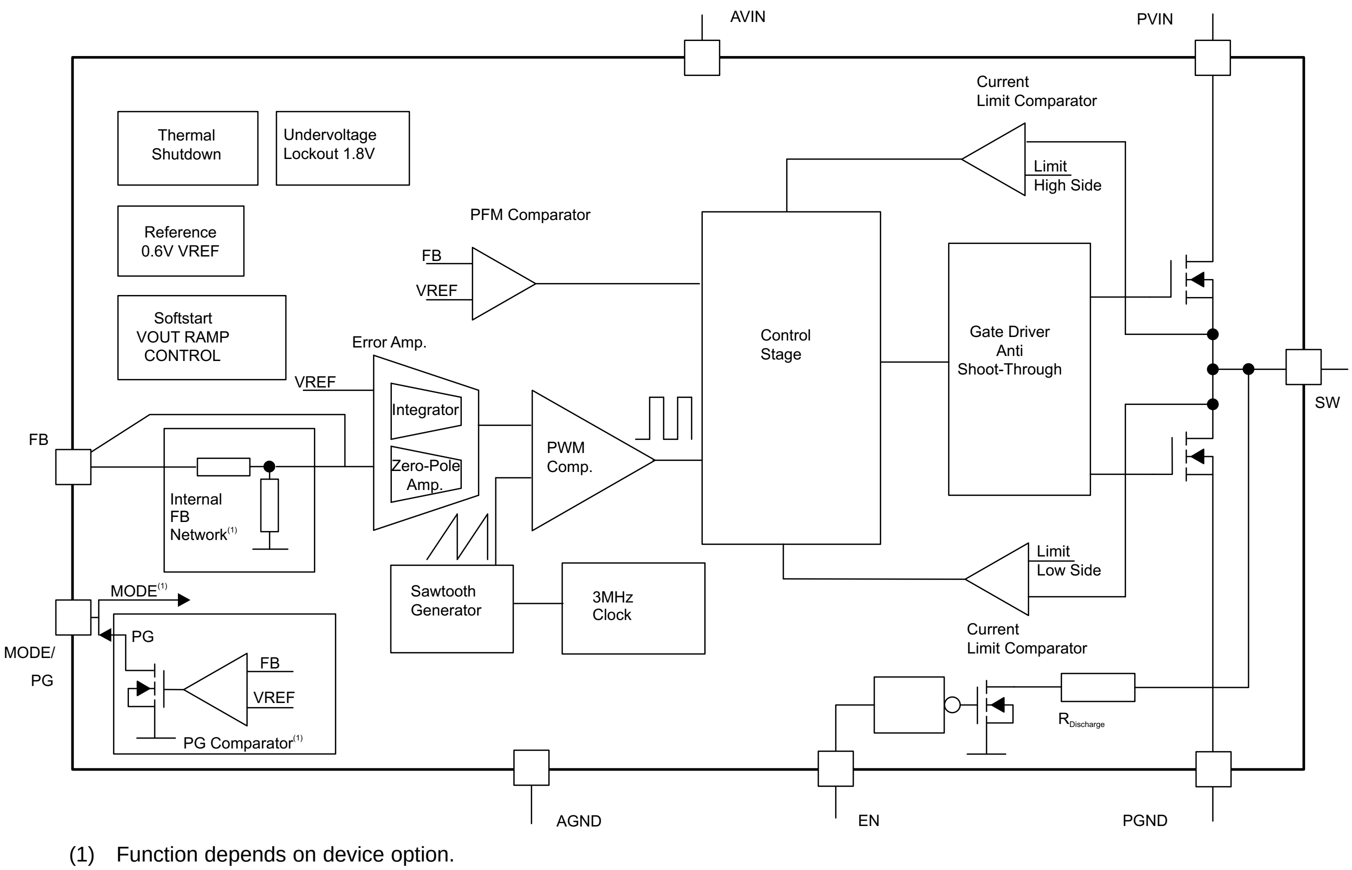
10.1 Overview

The TPS62065-Q1 and TPS62067-Q1 step-down converter operates with 3-MHz (typical) fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents the converter can automatically enter power save mode and then operate in pulse-frequency mode (PFM).

During PWM operation the converter uses an unique fast-response voltage-mode controller scheme with input-voltage feed-forward to achieve good line and load regulation which allows the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows from the input capacitor through the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch in case the current-limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. The current returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

10.2 Functional Block Diagram



(1) Function depends on device option.

10.3 Feature Description

10.3.1 Mode Selection (TPS62065-Q1)

The MODE pin allows mode selection between forced PWM mode and power save mode.

Connecting this pin to GND enables the power save mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed frequency PWM mode even at light load currents which allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to when the device is in power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

For the TPS62067-Q1 where the MODE pin is replaced with power good output, the power save mode is enabled per default.

10.3.2 Power-Good (PG) Output (TPS62067-Q1)

This function is available in the TPS62067-Q1 device only. The PG output is an open-drain output and requires an external pullup resistor. The circuit is active once the device is enabled and AVIN is above the UVLO threshold V_{UVLO}. The PG output provides a high level once the feedback voltage exceeds 95% (typical) of the nominal value. The PG output is driven to a low level when the feedback voltage falls below 90% (typical) of the nominal value. The PG output is activated with an internal delay of 5 µs.

The PG open-drain output transistor turns on immediately with the EN pin meets the low level and pulls the output low. The external pullup resistor can be connected to any voltage rail lower or equal the voltage applied to AVIN pin of the device. The value of the pullup resistor must be carefully selected in order to limit the current into the PG pin to 1 mA maximum. The external pullup resistor can be connected to VOUT or another voltage rail which does not exceed the VIN level. The current flowing through the pullup resistor impacts the current consumption of the application circuit in shutdown mode.

The shut down current of the device does not include the current through the external pullup and internal open-drain stage. The PG signal can be used for sequencing various converters or to reset a microcontroller.

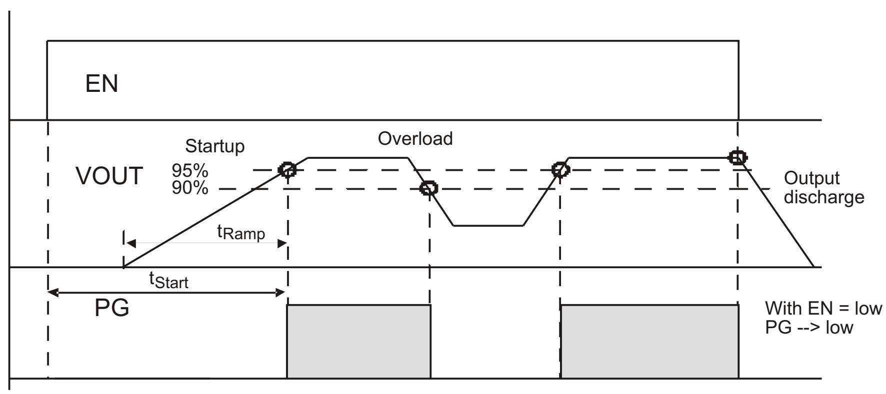


Figure 7. Power Good Output PG

10.3.3 Enable

Setting the EN pin high enables the device. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches 95% of the nominal value within t_{START} which is 500 µs (typical) after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can connect to the output of another converter in order to drive the EN pin high and get a sequencing of supply rails. When EN is pulled low the device enters shutdown mode. In this mode, all circuits are disabled and the SW pin is connected to PGND through an internal resistor to discharge the output.

Feature Description (continued)

10.3.4 Soft Start

The TPS62065-Q1 and TPS62067-Q1 device has an internal soft-start circuit that controls the ramp up of the output voltage. When the converter is enabled and the input voltage is above the UVLO threshold, V_{UVLO}, the output voltage ramps up from 5% to 95% of the nominal value with t_{Ramp} of 250 µs (typical). The ramp time limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used.

During soft start, the switch current-limit is reduced to 1/3 of the nominal value, I_{LIMF}, until the output voltage reaches 1/3 of the nominal value. When the output voltage trips this threshold, the device operates with the nominal current limit, I_{LIMF}.

10.3.5 Internal Current-Limit and Foldback Current-Limit For Short-Circuit Protection

During normal operation the high-side and low-side MOSFET switches are protected by the current-limit I_{LIMF}. When the high-side MOSFET switch reaches the current-limit, it turns off and the low-side MOSFET switch turns on. The high-side MOSFET switch can only turn on again when the current in the low-side MOSFET switch decreases below I_{LIMF}. The device is capable to provide peak-inductor currents up to the internal current limit, ILIMF..

As soon as the switch current-limits are met and the output voltage falls below 1/3 of the nominal output voltage because of overload or short circuit condition, the foldback current-limit is enabled. In this case the switch current-limit is reduced to 1/3 of the nominal value I_{LIMF}.

Because the short-circuit protection is enabled during start-up, the device does not deliver more than 1/3 of the nominal current-limit, I_{LIMF}, until the output voltage exceeds 1/3 of the nominal output voltage. This protection must be considered when a load is connected to the output of the converter, which acts as a current sink.

10.3.6 Clock Dithering

In order to reduce the noise level of switch-frequency harmonics in the higher RF bands, the TPS62065-Q1 and TPS62067-Q1 device has a built-in clock-dithering circuit. The oscillator frequency is slightly modulated with a sub clock causing a clock dither of 6 ns (typical).

10.3.7 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device enters thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues operation with a soft start once the junction temperature falls below the thermal shutdown hysteresis.

10.4 Device Functional Modes

10.4.1 Power Save Mode

At TPS62065-Q1 pulling the MODE pin low enables power save mode. In TPS62067-Q1 power-save mode is enabled per default. If the load current decreases, the converter enters power save mode operation automatically. During power save mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage 1% (typical) above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs when the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power save mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of $V_{OUTnominal}$ +1%, the device starts a PFM current pulse. For this the high-side MOSFET switch turns on and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current the output voltage rises. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with a typical 18-µA current consumption.

Device Functional Modes (continued)

In case the output voltage is still below the PFM comparator threshold, further PFM current pulses are generated until the PFM comparator reaches its threshold. The converter starts switching again once the output voltage drops below the PFM comparator threshold due to the load current.

In case the output current can no longer be supported in PFM mode, the device exits PFM mode and enters PWM mode.

10.4.1.1 Dynamic Voltage Positioning

This feature reduces the voltage under or overshoots at load steps from light to heavy load and vice versa. It is active in power save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

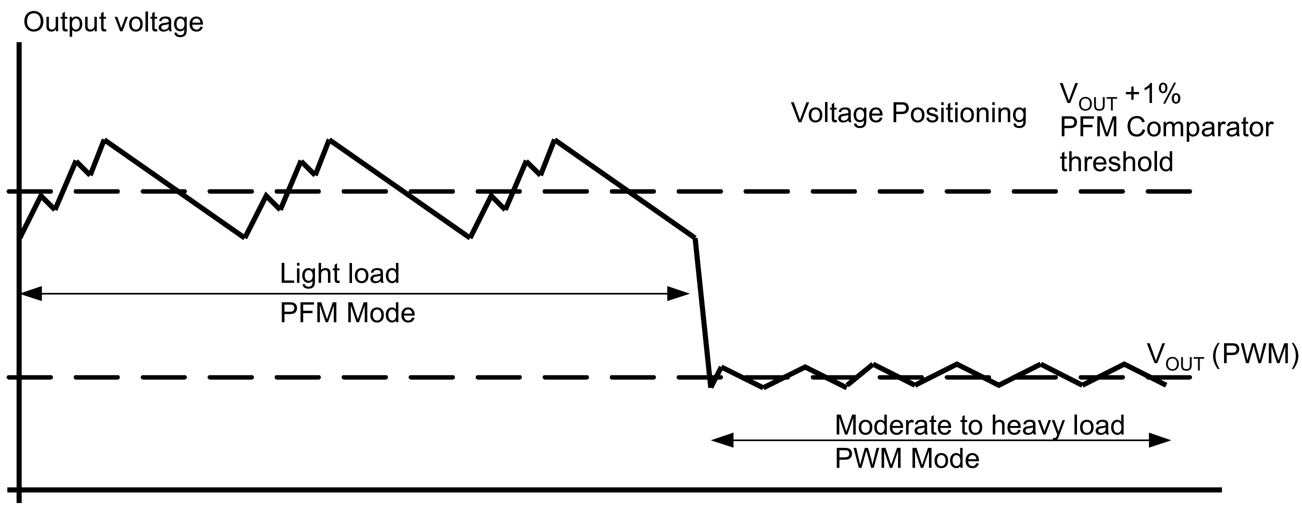


Figure 8. Power Save Mode Operation with automatic Mode transition

10.4.1.2 100% Duty-Cycle Low-Dropout Operation

The device starts to enter 100% duty cycle mode as the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing VIN the high-side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{O}max + I_{O}max \times (R_{DS(on)}max + R_{L})$$

where

- $I_O$max = maximum output current
- $R_{DS(on)}$max = maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_O$max = nominal output voltage plus maximum output voltage tolerance (1)

10.4.1.3 Undervoltage Lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling VIN trips the UVLO threshold V_{UVLO}. The UVLO threshold V_{UVLO} for falling V_{IN} is typically 1.78 V. The device starts operation once the rising V_{IN} trips UVLO threshold V_{UVLO} again at typically 1.95 V.

Device Functional Modes (continued)

10.4.1.4 Output Capacitor Discharge

With EN pulled low, the device enters shutdown mode and all internal circuits are disabled. The SW pin is connected to PGND through an internal resistor to discharge the output capacitor. This feature ensures a startup in a discharged output capacitor once the converter is enabled again and prevents a floating charge on the output capacitor. The output voltage ramps up monotonic starting from 0 V.

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The TPS62065-Q1 and TPS62067-Q1 is a highly efficient synchronous 2-A step down DC-DC converter.

11.2 Typical Application

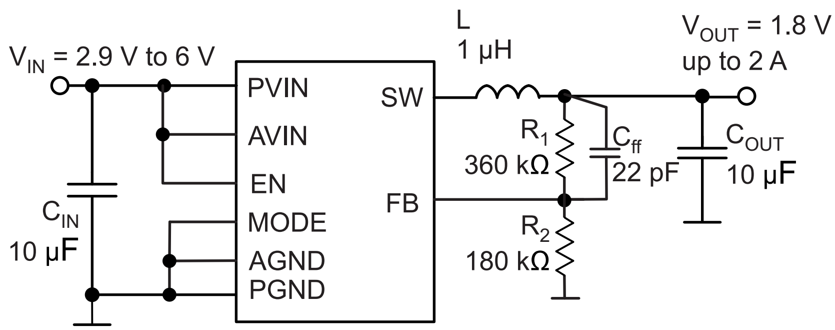


Figure 9. TPS62065-Q1 Adjustable 1.8-V Output-Voltage Configuration

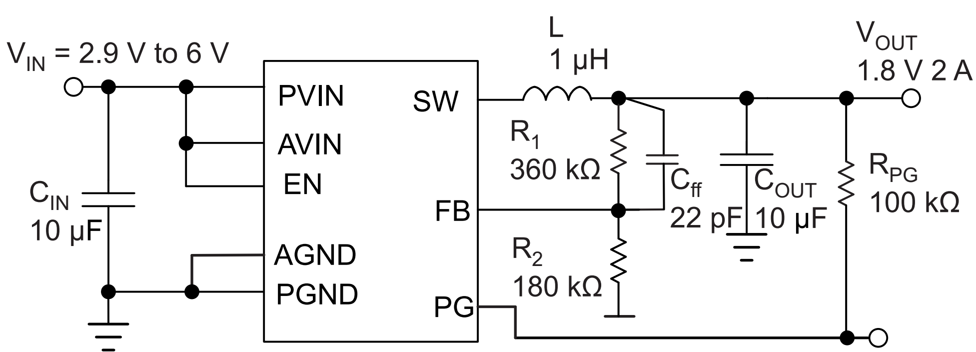


Figure 10. TPS62067-Q1 Adjustable 1.8-V Output-Voltage Configuration

11.2.1 Design Requirements

The device operates over an input voltage range from 2.9 V to 6 V. The output voltage is adjustable using an external feedback divider.

11.2.2 Detailed Design Procedure

11.2.2.1 Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \qquad R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \tag{2}$$

with an internal reference voltage V_{REF} typically 0.6 V.

Typical Application (continued)

To minimize the current through the feedback divider network, R_2 should be within the range of 120 kΩ to 360 kΩ. The sum of R_1 and R_2 should not exceed ~1 MΩ, to keep the network robust against noise. An external feed-forward capacitor C_{ff} is required for optimum regulation performance. Lower resistor values can be used. R_1 and C_{ff} places a zero in the loop. The right value for C_{ff} can be calculated as:

$$f_z = \frac{1}{2 \times \pi \times R_1 \times C_{ff}} = 25\ \text{kHz} \tag{3}$$

$$C_{ff} = \frac{1}{2 \times \pi \times R_1 \times 25\ \text{kHz}} \tag{4}$$

11.2.2.2 Output Filter Design (inductor And Output Capacitor)

The internal compensation network of TPS62065-Q1 and TPS62067-Q1 is optimized for a LC output filter with a corner frequency of:

$$f_C = \frac{1}{2 \times \pi \times \left(\sqrt{1\ \mu\text{H} \times 10\ \mu\text{F}}\right)} = 50\ \text{kHz} \tag{5}$$

The part operates with nominal inductors of 1 µH to 1.2 µH and with 10-µF to 22-µF small X5R and X7R ceramic capacitors. Please refer to the lists of inductors and capacitors. The part is optimized for a 1-µH inductor and 10-µF output capacitor.

11.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

Equation 6 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 7. This is recommended because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f}$$

where

- ΔI_L = Peak-to-peak inductor ripple current
- L = Inductor value
- f = Switching frequency (3-MHz typical) (6)

$$I_{L\,max} = I_{OUT\,max} + \frac{\Delta I_L}{2}$$

where

- I_{Lmax} = Maximum inductor current (7)

A more conservative approach is to select the inductor current rating just for the switch current limit I_{LIMF} of the converter.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the DC resistance $R_{(DC)}$ and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

Table 2. List of Inductors

DIMENSIONS [mm^3]	INDUCTANCE µH	INDUCTOR TYPE	SUPPLIER
3,2 × 2,5 × 1 max	1	LQM32PN (MLCC)	Murata
3,7 × 4 × 1,8 max	1	LQH44 (wire wound)	Murata
4 × 4 × 2,6 max	1.2	NRG4026T (wire wound)	Taiyo Yuden
3,5 × 3,7 × 1,8 max	1.2	DE3518 (wire wound)	TOKO

11.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS62065-Q1 and TPS62067-Q1 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and may not be used. For most applications a nominal 10-µF or 22-µF capacitor is suitable. At small ceramic capacitors, the DC-bias effect decreases the effective capacitance. Therefore a 22-µF capacitor can be used for output voltages higher than 2 V, see list of capacitors.

In case additional ceramic capacitors in the supplied system are connected to the output of the DC/DC converter, the output capacitor C_{OUT} must be decreased in order not to exceed the recommended effective capacitance range. In this case a loop stability analysis must be performed as described later.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

11.2.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a 10-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 3. List of Capacitors

CAPACITANCE	TYPE	SIZE [mm^3]	SUPPLIER
10 µF	GRM188R60J106M	0603: 1,6 × 0,8 × 0,8	Murata
22 µF	GRM188R60G226M	0603: 1,6 × 0,8 × 0,8	Murata
22 µF	CL10A226MQ8NRNC	0603: 1,6 × 0,8 × 0,8	Samsung
10 µF	CL10A106MQ8NRNC	0603: 1,6 × 0,8 × 0,8	Samsung

11.2.2.3 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signal

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

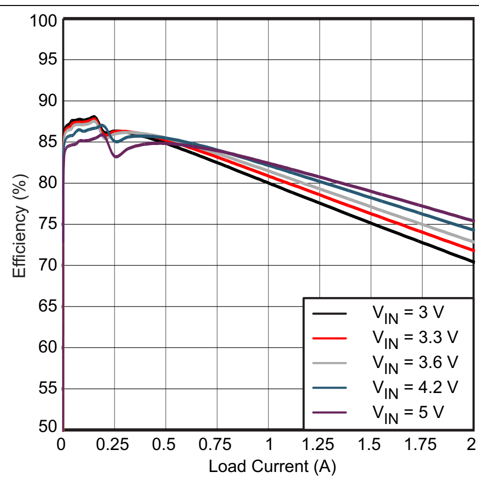
These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or wrong L-C output filter combinations. As a next step in the evaluation of the regulation loop, test the load transient response. The results are most easily interpreted when the device operates in PWM mode at medium to high load currents.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing; that helps evaluate stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin.

11.2.3 Application Curves

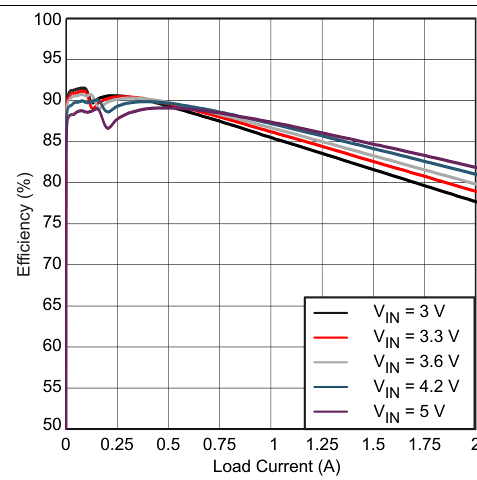
Table 4. Table of Graphs

			FIGURE
η	Efficiency	Load Current, V_{OUT} = 1.2 V, Auto PFM and PWM Mode, Linear Scale	Figure 11
		Load Current, V_{OUT} = 1.8 V, Auto PFM and PWM Mode, Linear Scale	Figure 12
		Load Current, V_{OUT} = 3.3 V, PFM and PWM Mode, Linear Scale	Figure 13
		Load Current, V_{OUT} = 1.8 V, Auto PFM and PWM Mode vs. Forced PWM Mode, Logarithmic Scale	Figure 14
	Output Voltage Accuracy	Load Current, V_{OUT} = 1.8 V, Auto PFM and PWM Mode	Figure 15
		Load Current, V_{OUT} = 1.8 V, Forced PWM Mode	Figure 16
	Typical Operation	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 500 mA, L = 1.2 µH, C_{OUT} = 10 µF	Figure 17
		PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 20 mA, L = 1.2 µH, C_{OUT} = 10 µF	Figure 18
	Load Transient	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 0.2 mA to 1 A	Figure 19
		PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 20 mA to 250 mA	Figure 20
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 200 mA to 1500 mA	Figure 21
	Line Transient	PWM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	Figure 22
		PFM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	Figure 23
	Startup into Load	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, Load = 2.2 Ω	Figure 24
	Startup TPS62067-Q1	Into 2.2-Ω Load with Power Good	Figure 25
	Output Discharge	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, No Load	Figure 26
	Shutdown TPS62067-Q1	V_{IN} = 4.2 V, V_{OUT} = 3.3 V, No Load, PG Pullup Resistor 10 kΩ	Figure 27



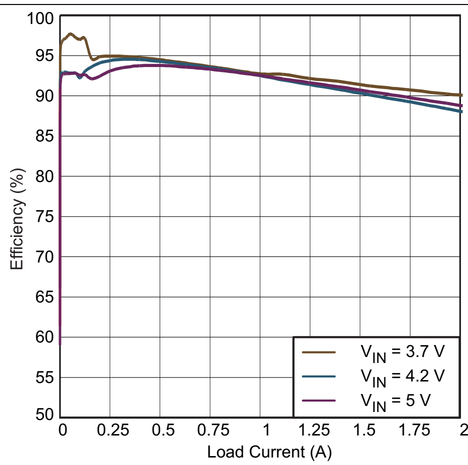
V_{OUT} = 1.2 V Linear Scale
L = 1.2 µH (NRG4026T 1R2) C_{OUT} = 10 µF (0603 size)

Figure 11. Efficiency vs Load Current Auto PFM and PWM MODE



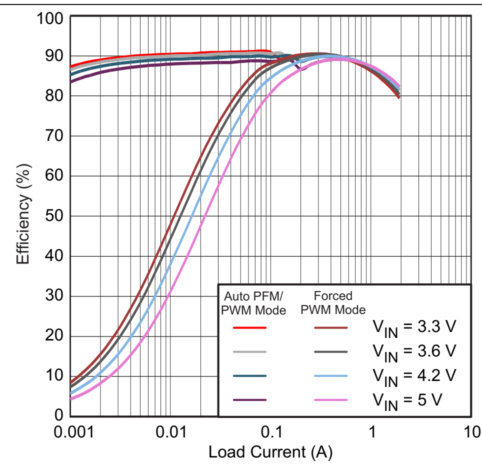
V_{OUT} = 1.8 V Linear Scale
L = 1.2 µH (NRG4026T 1R2) C_{OUT} = 10 µF (0603 size)

Figure 12. Efficiency vs Load Current PFM and PWM MODE



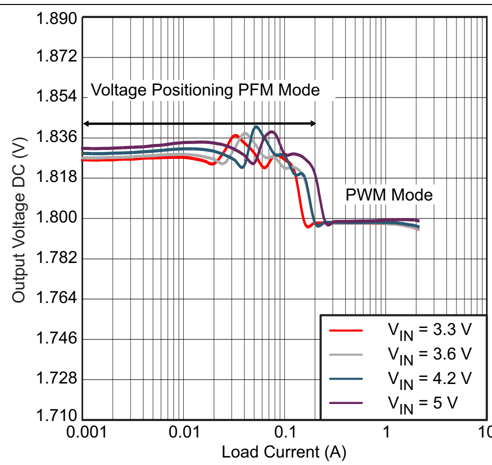
V_{OUT} = 3.3 V Linear Scale
L = 1.2 µH (NRG4026T 1R2) C_{OUT} = 22 µF (0603 size)

Figure 13. Efficiency vs Load Current Auto PFM and PWM MODE



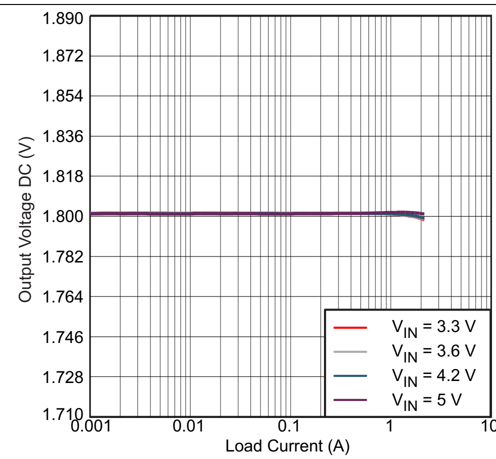
V_{OUT} = 1.8 V Logarithmic Scale
C_{OUT} = 10 µF (0603 size) L = 1.2 µH (NRG4026T 1R2)

Figure 14. Efficiency vs Load Current Auto PFM and PWM Mode vs. Forced PWM Mode



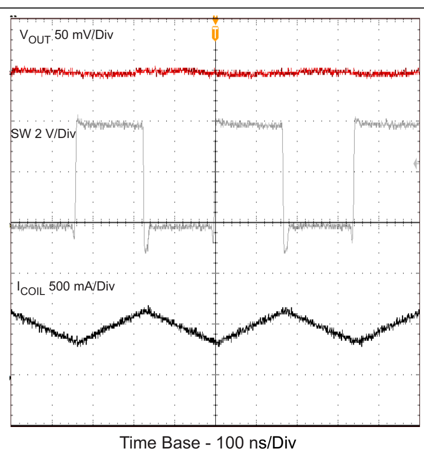
L = 1 µH V_{OUT} = 1.8 V C_{OUT} = 10 µF

Figure 15. Output Voltage Accuracy vs Load Current Auto PFM and PWM MODE



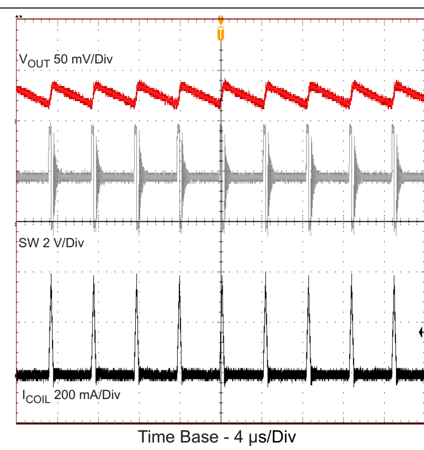
L = 1 µH V_{OUT} = 1.8 V C_{OUT} = 10 µF

Figure 16. Output Voltage Accuracy vs Load Current Forced PWM MODE



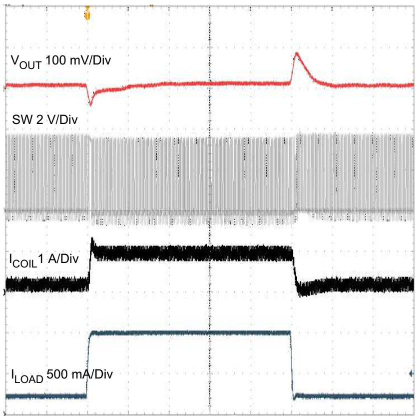
V_{IN} = 3.6 V V_{OUT} = 1.8 V MODE = GND
C_{OUT} = 10 µF L = 1.2 µH I_{OUT} = 500 mA

Figure 17. Typical Operation (PWM Mode)



V_{IN} = 3.6 V V_{OUT} = 1.8 V MODE = GND
C_{OUT} = 10 µF L = 1.2 µH I_{OUT} = 20 mA

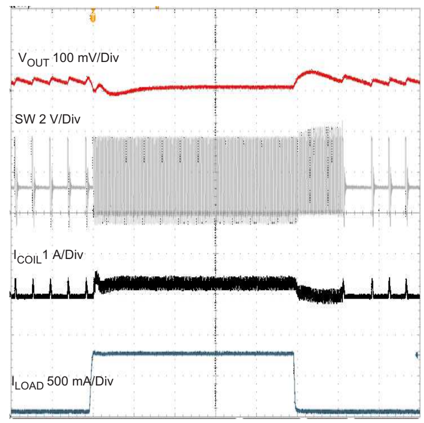
Figure 18. Typical Operation (PFM Mode)



Time Base - 10 µs/Div

V_{IN} = 3.6 V V_{OUT} = 1.2 V I_{OUT} = 0.2 to 1 A

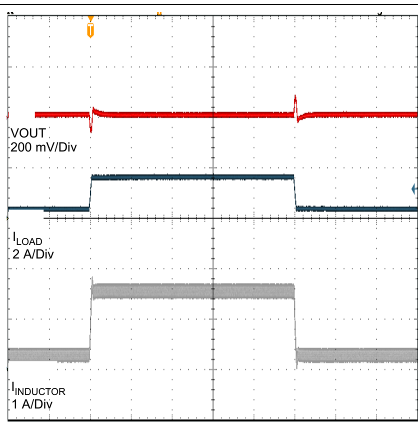
Figure 19. Load Transient Response, MODE = V_{IN} PWM Mode 0.2 A to 1 A



Time Base - 10 µs/Div

V_{IN} = 3.6 V V_{OUT} = 1.8 V I_{OUT} = 20 to 2500 mA

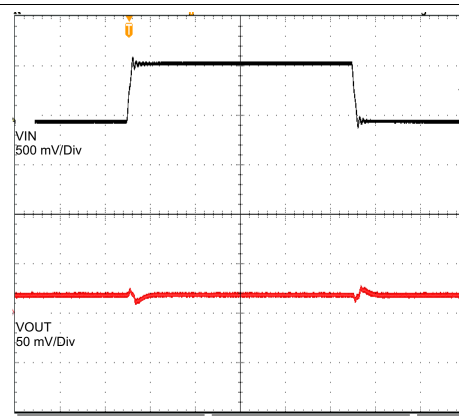
Figure 20. Load Transient PFM Mode 20 mA to 250 mA



Time Base - 100 µs/Div

V_{IN} = 3.6 V V_{OUT} = 1.8 V L = 1.2 µH
C_{OUT} = 10 µF

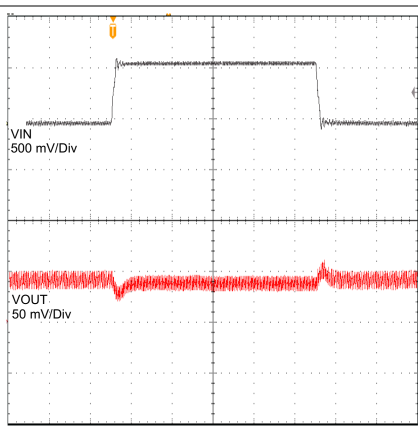
Figure 21. Load Transient Response 200 mA To 1500 mA



Time Base - 100 µs/Div

V_{IN} = 3.6 to 4.2 V V_{OUT} = 1.8 V I_{OUT} = 500 mA
C_{OUT} = 10 µF L = 1.2 µH

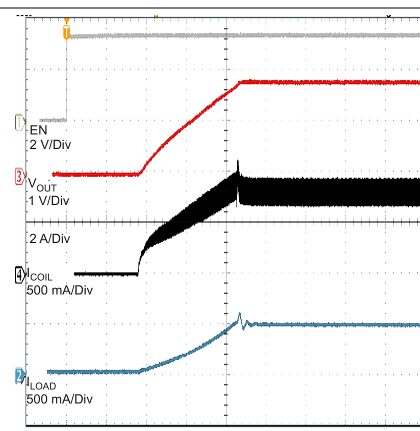
Figure 22. Line Transient Response PWM Mode



Time Base - 100 µs/Div

V_{IN} = 3.6 to 4.2 V V_{OUT} = 1.8 V I_{OUT} = 50 mA
C_{OUT} = 10 µF L = 1.2 µH

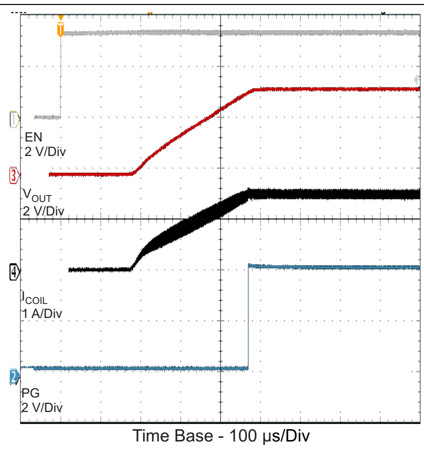
Figure 23. Line Transient PFM Mode



Time Base - 100 µs/Div

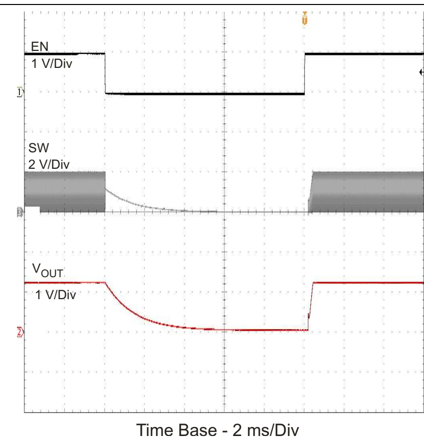
V_{IN} = 3.6 V V_{OUT} = 1.8 V Load = 2R2
C_{OUT} = 10 µF L = 1.2 µH

Figure 24. Startup Into Load



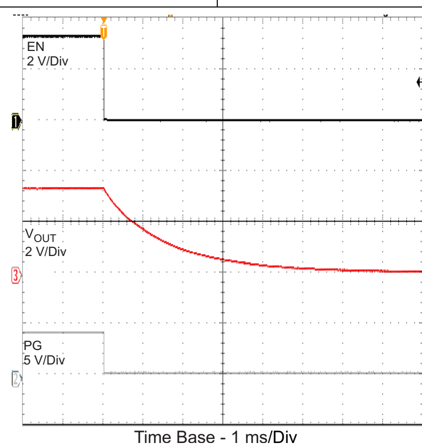
V_{IN} = 4.2 V V_{OUT} = 3.3 V Load = 2R2
PG Pullup resistor 10 kΩ

Figure 25. Startup TPS62067-Q1 into 2.2-Ω Load With Power Good



V_{IN} = 3.6 V V_{OUT} = 1.8 V No load
C_{OUT} = 1.8 µF

Figure 26. Output Discharge



V_{IN} = 4.2 V V_{OUT} = 3.3 V No load
PG pullup resistor, 10 kΩ

Figure 27. Shutdown TPS62067-Q1

12 Power Supply Recommendations

The power supply to the TPS62065-Q1 and TPS62067-Q1 must have a current rating according to the supply voltage, output voltage, and output current of the TPS62065-Q1 and TPS62067-Q1.

13 Layout

13.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. The input capacitor needs to be placed as close as possible to the IC pins.

It is critical to provide a low inductance, impedance ground and supply path. Therefore, use wide and short traces for the main current paths. Connect the AGND and PGND pins of the device to the thermal pad land of the PCB and use this pad as a star point. Use a common power PGND node and a different node for the signal AGND to minimize the effects of ground noise. The FB divider network should be connected right to the output capacitor and the FB line must be routed away from noisy components and traces (for example, SW line).

Due to the small package of this converter and the overall small solution size the thermal performance of the PCB layout is important. To get a good thermal performance a four or more layer PCB design is recommended. The PowerPAD of the IC must be soldered on the thermal pad area on the PCB to get a proper thermal connection. For good thermal performance the exposed pad on the PCB must be connected to an inner GND plane with sufficient via connections. Please refer to the documentation of the evaluation kit.

13.2 Layout Example

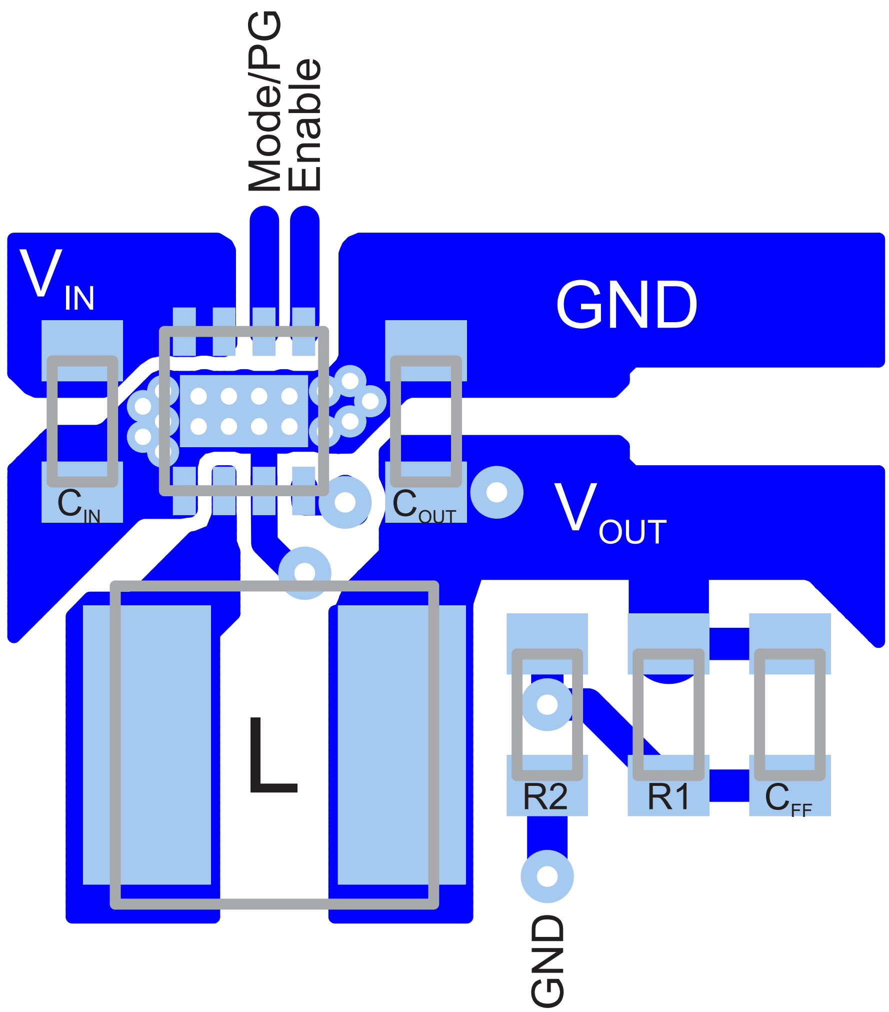


Figure 28. PCB Layout

14 器件和文档支持

14.1 器件支持

14.1.1 第三方产品免责声明

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14.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **5.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS62065-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62067-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

14.3 商标

14.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

14.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

15 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62065QDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJF	Samples
TPS62067QDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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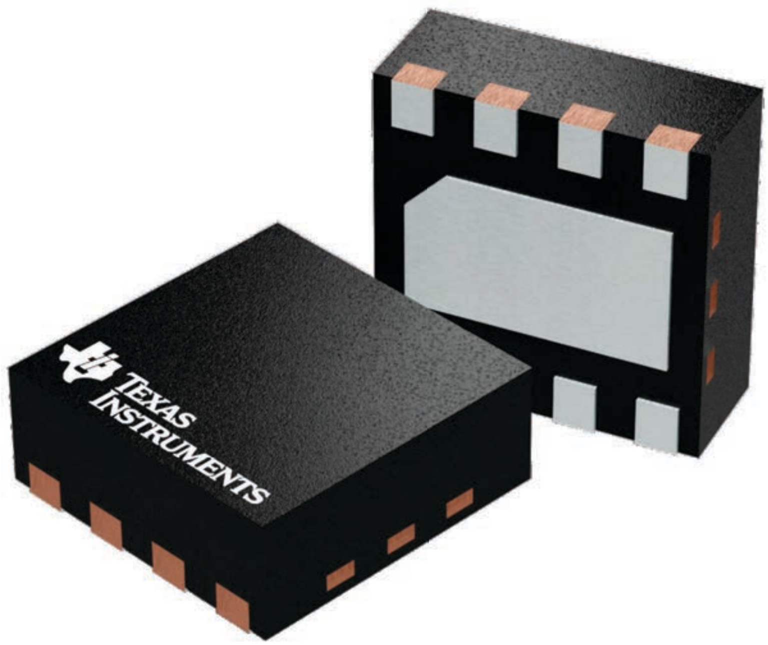
DSG 8

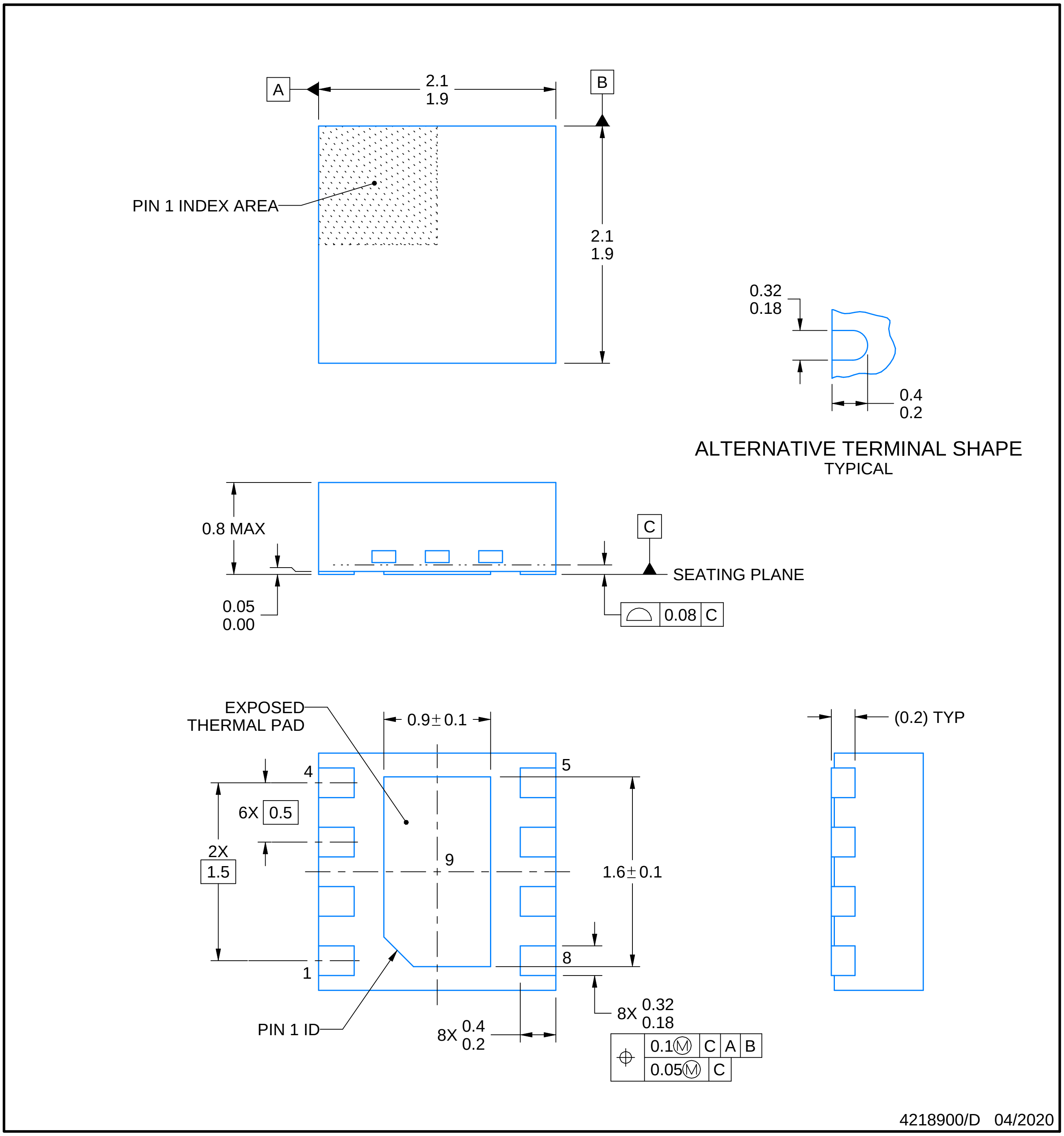
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

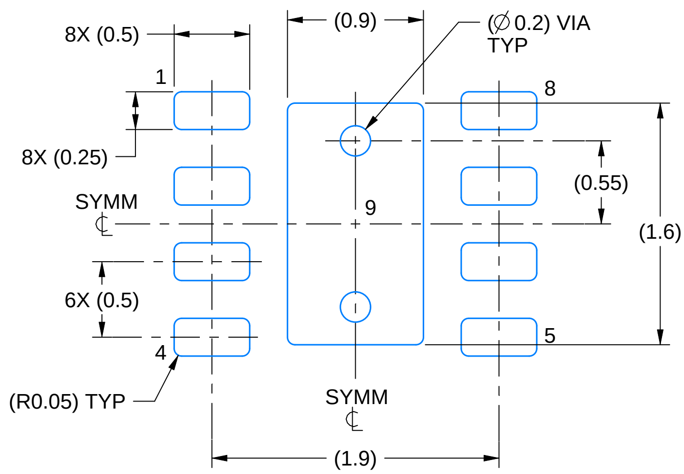
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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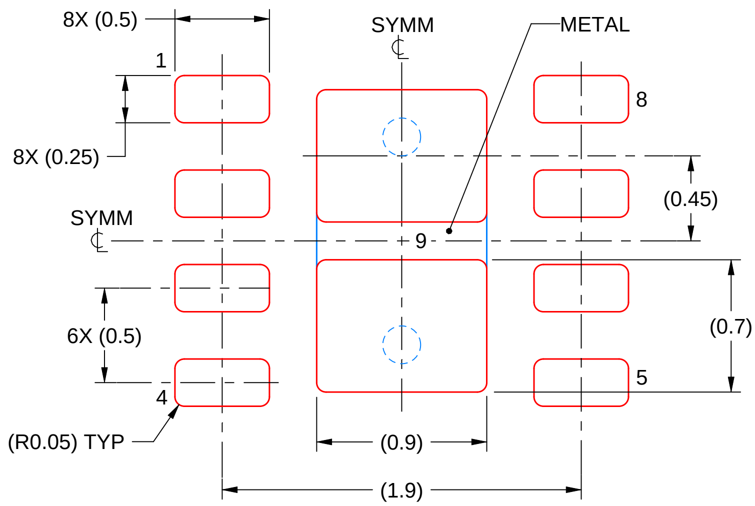
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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