

LMR33610 SIMPLE SWITCHER® 3.8V 至 36V、1A 同步降压转换器

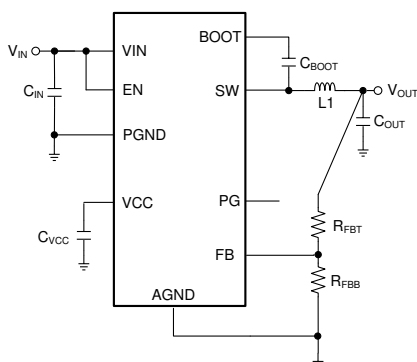
1 特性

- 专用于条件严苛的工业应用
 - 输入电压范围：3.8V 至 36V
 - 输出电压范围：1V 至 24V
 - 峰值电流模式控制
 - 结温范围为 -40°C 至 +125°C
 - 易于使用的 SOIC 封装
- 非常适合可扩展的工业电源
 - 与以下器件引脚兼容：
 - LMR33620、LMR33630 和 LMR33640 (36V、2A、3A 或 4A)
 - LMR36510 和 LMR36520 (65V、1A 或 2A)
 - 400kHz 和 1.4MHz 频率
 - 集成式补偿有助于减小解决方案尺寸、降低成本和设计复杂性
- 高效解决方案
 - 峰值效率 > 95%
 - 低至 5μA 的关断静态电流
 - 低至 25μA 的工作静态电流
- 灵活的系统接口
 - 电源正常状态标志和精密使能端
- 使用 LMR33610 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 电机驱动系统：无人机、交流逆变器、变频驱动器、伺服系统
- 工厂和楼宇自动化系统：PLC、HMI、HVAC 系统、电梯主控板
- 宽输入电压直流/直流电源

简化原理图



3 说明

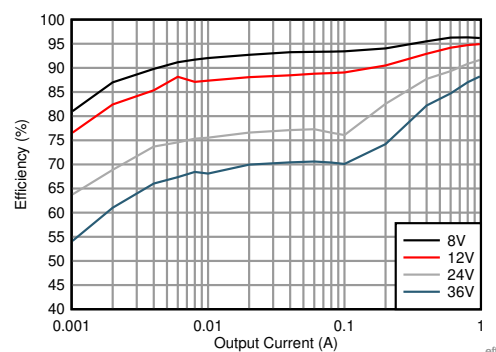
LMR33610 SIMPLE SWITCHER® 稳压器是一款简单易用的同步降压直流/直流转换器，可提供一流的效率，适用于条件严苛的工业应用。LMR33610 能够使用高达 36V 的输入电压驱动高达 1A 的负载电流。LMR33610 可提供出色的轻负载效率和输出精度。诸如电源正常状态标志和精密使能端等特性有助于实现灵活而又易用的解决方案 - 适用于广泛的应用。LMR33640 在轻负载条件下自动折返频率以提高效率。保护功能包括热关断、输入欠压锁定、逐周期电流限制和断续短路保护。通过集成和内部补偿，该器件减少了很多外部组件，并提供专为实现简单 PCB 布局而设计的引脚排列方式。该器件的功能集旨在简化各种终端设备的实施。LMR33610 与 LMR33620、LMR33630、LMR33640 (36V、2A/3A/4A) 和 LMR36510 (65V、1A) 和 LMR36520 (65V、2A) 引脚对引脚兼容，完善了可扩展的 SIMPLE SWITCHER 电源系列。降低了成本并减少了电路板布局修改的工作量。LMR33610 采用 8 引脚 HSOIC 封装。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
LMR33610	HSOIC (8)	5.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

效率与输出电流间的关系
V_{OUT} = 5V, 400kHz



目录

1	特性	1	8.4	Device Functional Modes	14
2	应用	1	9	Application and Implementation	17
3	说明	1	9.1	Application Information	17
4	修订历史记录	2	9.2	Typical Application	17
5	Device Comparison Table	3	9.3	What to Do and What Not to Do	27
6	Pin Configuration and Functions	4	10	Power Supply Recommendations	28
7	Specifications	5	11	Layout	29
7.1	Absolute Maximum Ratings	5	11.1	Layout Guidelines	29
7.2	ESD Ratings	5	11.2	Layout Example	31
7.3	Recommended Operating Conditions	5	12	器件和文档支持	32
7.4	Thermal Information	6	12.1	器件支持	32
7.5	Electrical Characteristics	6	12.2	文档支持	32
7.6	Timing Characteristics	7	12.3	接收文档更新通知	32
7.7	System Characteristics	7	12.4	支持资源	32
7.8	Typical Characteristics	9	12.5	商标	33
8	Detailed Description	10	12.6	静电放电警告	33
8.1	Overview	10	12.7	Glossary	33
8.2	Functional Block Diagram	10	13	机械、封装和可订购信息	33
8.3	Feature Description	11			

4 修订历史记录

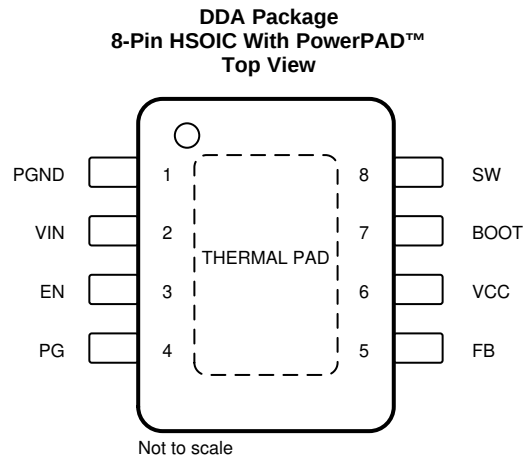
注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 10 月	*	初始发行版

5 Device Comparison Table

DEVICE OPTION	PACKAGE	FREQUENCY	RATED CURRENT	OUTPUT VOLTAGE
LMR33610ADDAR	DDA (8-pin HSOIC) 5 × 4 mm	400 kHz	1 A	Adjustable
LMR33610BDDAR		1400 kHz	1 A	

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	PGND	G	Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces.
2	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and PGND.
3	EN	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; <i>Do not float.</i>
4	PG	A	Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Flag pulls low when EN = Low. Can be left open when not used.
5	FB	A	Feedback input to regulator. Connect to tap point of feedback voltage divider. <i>Do not float. Do not ground.</i>
6	VCC	P	Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-μF capacitor from this pin to GND.
7	BOOT	P	Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. This simplifies the connection from the C _{BOOT} capacitor to the SW pin.
8	SW	P	Regulator switch node. Connect to power inductor. This simplifies the connection from the C _{BOOT} capacitor to the SW pin.
THERMAL PAD	AGND	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB. For the HSOIC package, the pad on the bottom of the device serves as both the AGND connection and a thermal connection to the heat sink ground plane. This pad must be soldered to a ground plane to achieve good electrical and thermal performance.

A = Analog, P = Power, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range⁽¹⁾

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to PGND	−0.3	38	V
	EN to AGND ⁽²⁾	−0.3	V _{IN} + 0.3	
	FB to AGND	−0.3	5.5	
	PG to AGND ⁽²⁾	0	22	
	AGND to PGND	−0.3	0.3	
	SW to PGND	−0.3	V _{IN} + 0.3	V
	SW to PGND less than 100-ns transients	−3.5	38	
	BOOT to SW	−0.3	5.5	
	VCC to AGND ⁽³⁾	−0.3	5.5	
	VCC to AGND ⁽³⁾	−0.3	5.5	
T _J	Junction temperature ⁽⁴⁾	−40	150	°C
T _{stg}	Storage temperature	−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
- (3) Under some operating conditions the VCC LDO voltage may increase beyond 5.5 V.
- (4) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM) ⁽¹⁾	±2500	V
		Charged-device model (CDM) ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of −40°C to 125°C (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN to PGND	3.8	36	V
	EN ⁽²⁾	0	V _{IN}	
	PG ⁽²⁾	0	18	
Adjustable output voltage	V _{OUT} ⁽³⁾	1	24	V
Output current	I _{OUT}	0	1	A
Temperature	Operating junction temperature, T _J ⁽⁴⁾	−40	125	°C

- (1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see [Electrical Characteristics](#).
- (2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
- (3) The maximum output voltage can be extended to 95% of V_{IN}; contact TI for details. Under no conditions should the output voltage be allowed to fall below zero volts.
- (4) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾⁽²⁾		LMR33610	UNIT
		DDA (HSOIC)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	72.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	35.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	23.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	23.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics Application Report](#).
- (2) The value of R_{θJA} given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information please see the [Maximum Ambient Temperature](#) section.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{IN}	Minimum operating input voltage				3.8	V
I _Q	Non-switching input current; measured at VIN pin ⁽¹⁾	V _{FB} = 1.2 V		24	34	μA
I _{SD}	Shutdown quiescent current; measured at VIN pin	EN = 0		5	10	μA
ENABLE						
V _{EN-VCC-H}	EN input level required to turn on internal LDO	Rising threshold			1	V
V _{EN-VCC-L}	EN input level required to turn off internal LDO	Falling threshold	0.3			V
V _{EN-H}	EN input level required to start switching	Rising threshold	1.2	1.231	1.26	V
V _{EN-HYS}	Hysteresis below V _{EN-H}	Hysteresis below V _{EN-H} ; falling		100		mV
I _{LKG-EN}	Enable input leakage current	V _{EN} = 3.3 V		0.2		nA
INTERNAL SUPPLIES						
V _{CC}	Internal LDO output voltage appearing at the VCC pin	6 V ≤ V _{IN} ≤ 36 V	4.75	5	5.25	V
V _{BOOT-UVLO}	Bootstrap voltage undervoltage lock-out threshold ⁽²⁾			2.2		V
VOLTAGE REFERENCE (FB PIN)						
V _{FB}	Feedback voltage		0.985	1	1.015	V
I _{FB}	Current into FB pin	FB = 1 V		0.2	50	nA
CURRENT LIMITS ⁽³⁾						
I _{ZC}	Zero current detector threshold			0.01		A
SOFT START						
t _{SS}	Internal soft-start time		2.9	4	6	ms
POWER GOOD (PG PIN)						
V _{PG-HIGH-UP}	Power-good upper threshold - rising	% of FB voltage	105%	107%	110%	

- (1) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
- (2) When the voltage across the C_{BOOT} capacitor falls below this voltage, the low side MOSFET is turned on to recharge C_{BOOT}.
- (3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to $+125^{\circ}\text{C}$, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^{\circ}\text{C}$, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{IN} = 12\text{ V}$, $V_{EN} = 4\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{PG-HIGH-DN}	Power-good upper threshold - falling	% of FB voltage	103%	105%	108%	
V _{PG-LOW-UP}	Power-good lower threshold - rising	% of FB voltage	92%	94%	97%	
V _{PG-LOW-DN}	Power-good lower threshold - falling	% of FB voltage	90%	92%	95%	
t _{PG}	Power-good glitch filter delay ⁽⁴⁾		60		170	μs
R _{PG}	Power-good flag R _{DS(on)}	V _{IN} = 12 V, V _{EN} = 4 V		76	150	Ω
		V _{EN} = 0 V		35	60	
V _{IN-PG}	Minimum input voltage for proper PG function	50-μA, EN = 0 V			2	V
V _{PG}	PG logic low output	50-μA, EN = 0 V, V _{IN} = 2V			0.2	V
OSCILLATOR						
f _{SW}	Switching frequency	"A" Version	340	400	460	kHz
f _{SW}	Switching frequency	"B" Version	1.2	1.4	1.6	MHz
MOSFETS						

(4) See [Power-Good Flag Output](#) for details.

7.6 Timing Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to $+125^{\circ}\text{C}$, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^{\circ}\text{C}$, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{IN} = 12\text{ V}$, $V_{EN} = 4\text{ V}$.

		MIN	NOM	MAX	UNIT
t_{ON-MAX}	Maximum switch on-time		7	9	μs

7.7 System Characteristics

The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to $T_J = 25^{\circ}\text{C}$ only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of $T_J = -40^{\circ}\text{C}$ to 125°C . *These specifications are not ensured by production testing.*

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range	$V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 0\text{ A}$	3.8	36	V
V_{OUT}	Output voltage regulation for $V_{OUT} = 5\text{ V}$ ⁽¹⁾	$V_{OUT} = 5\text{ V}$, $V_{IN} = 7\text{ V}$ to 36 V , $I_{OUT} = 0\text{ A}$ to max. load	-1.5%	2.5%	
		$V_{OUT} = 5\text{ V}$, $V_{IN} = 7\text{ V}$ to 36 V , $I_{OUT} = 1\text{ A}$ to max. load	-1.5%	1.5%	
	Output voltage regulation for $V_{OUT} = 3.3\text{ V}$ ⁽¹⁾	$V_{OUT} = 3.3\text{ V}$, $V_{IN} = 3.8\text{ V}$ to 36 V , $I_{OUT} = 0\text{ A}$ to max. load	-1.5%	2.5%	
		$V_{OUT} = 3.3\text{ V}$, $V_{IN} = 3.8\text{ V}$ to 36 V , $I_{OUT} = 1\text{ A}$ to max. load	-1.5%	1.5%	
I_{SUPPLY}	Input supply current when in regulation	$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 0\text{ A}$, $R_{FBT} = 1\text{ M}\Omega$	25		μA
V_{DROP}	Dropout voltage; ($V_{IN} - V_{OUT}$)	$V_{OUT} = 5\text{ V}$, $I_{OUT} = 1\text{ A}$ Dropout at -1% of regulation, $f_{SW} = 140\text{ kHz}$	150		mV
D_{MAX}	Maximum switch duty cycle ⁽²⁾	$V_{IN} = V_{OUT} = 12\text{ V}$, $I_{OUT} = 1\text{ A}$	98%		

(1) Deviation is with respect to $V_{IN} = 12\text{ V}$, $I_{OUT} = 1\text{ A}$.

(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: $f_{MIN} = 1 / (t_{ON-MAX} + t_{OFF-MIN})$. $D_{MAX} = t_{ON-MAX} / (t_{ON-MAX} + t_{OFF-MIN})$.

System Characteristics (continued)

The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to $T_J = 25^{\circ}\text{C}$ only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of $T_J = -40^{\circ}\text{C}$ to 125°C . *These specifications are not ensured by production testing.*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
t_D	Switch voltage dead time			2		ns
T_{SD}	Thermal shutdown temperature	Shutdown temperature		165		$^{\circ}\text{C}$
		Recovery temperature		148		$^{\circ}\text{C}$

7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: $T_A = 25^\circ\text{C}$ and $V_{IN} = 12\text{ V}$

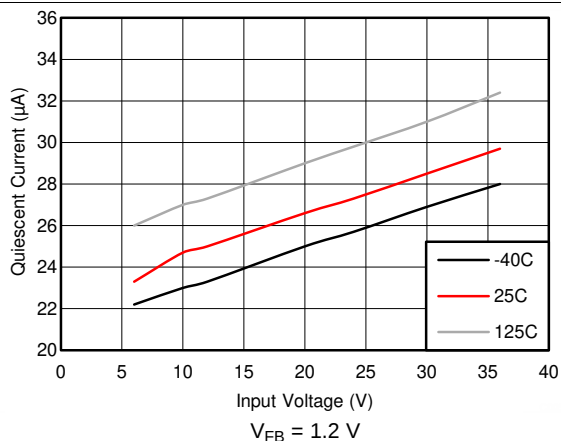


图 1. Non-Switching Input Supply Current

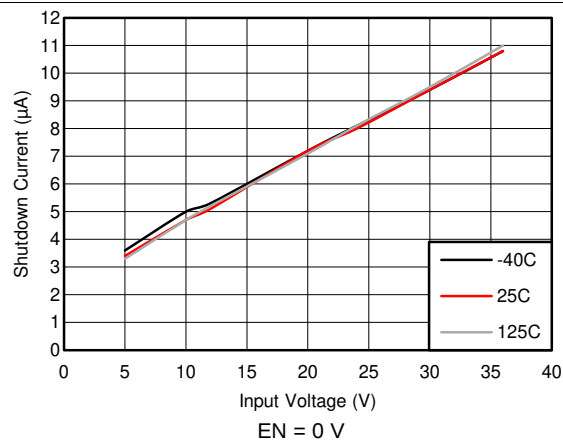


图 2. Shutdown Supply Current

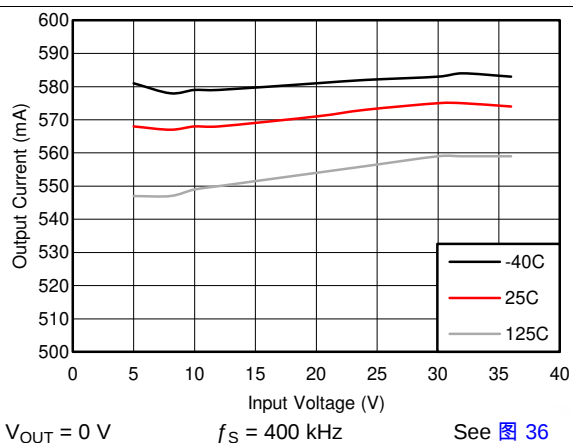


图 3. Short-Circuit Output Current

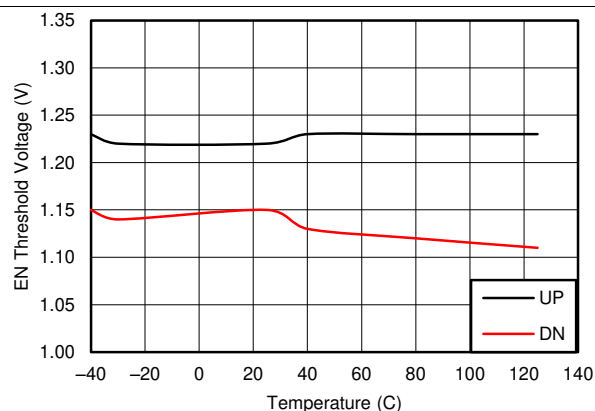


图 4. Precision Enable Thresholds

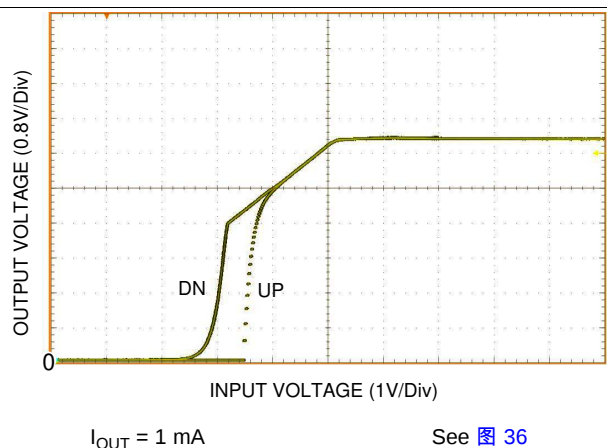


图 5. UVLO Thresholds

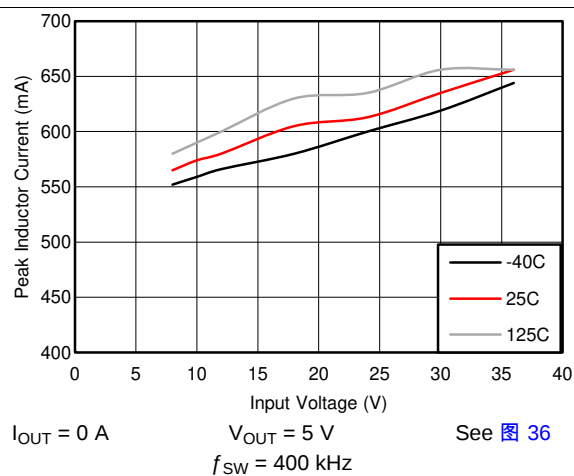


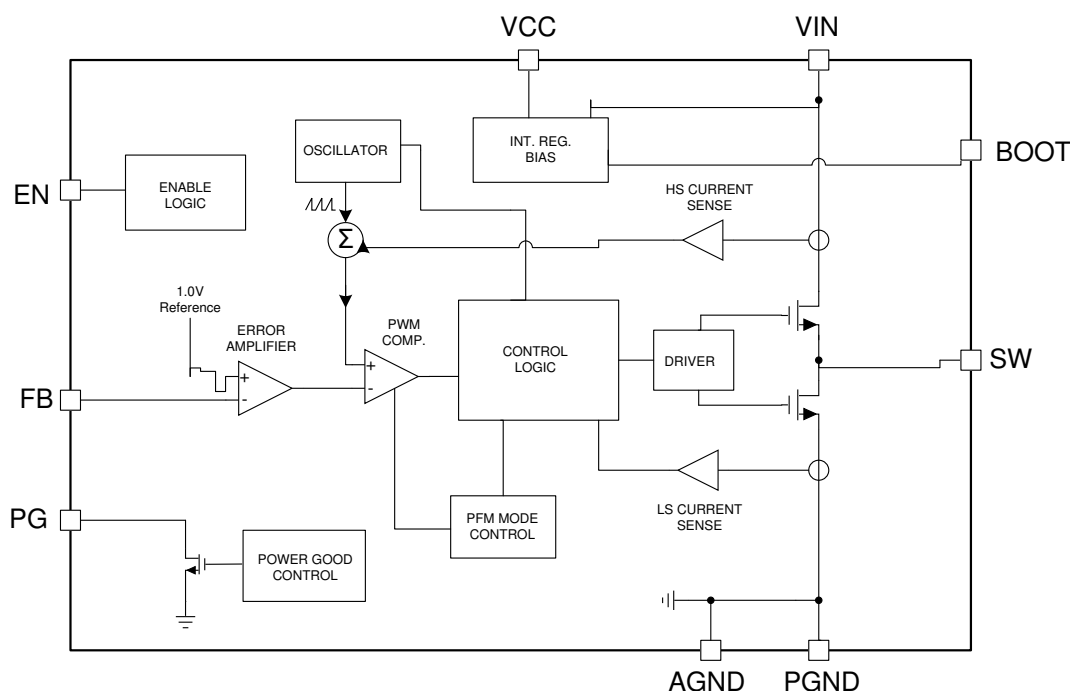
图 6. $I_{PEAK-MIN}$

8 Detailed Description

8.1 Overview

The LMR33610 is a synchronous peak-current-mode buck regulator designed for a wide variety of industrial applications. Advanced high speed circuitry allows the device to regulate from an input voltage of 20 V, while providing an output voltage of 3.3 V at a switching frequency of 1.4 MHz. The innovative architecture allows the device to regulate a 3.3 V output from an input of only 3.8 V. The regulator automatically switches modes between PFM and PWM, depending on load. At heavy loads, the device operates in PWM at a constant switching frequency. At light loads, the mode changes to PFM with diode emulation allowing DCM. This reduces the input supply current and keeps efficiency high. The device features internal loop compensation which reduces design time and requires fewer external components than externally compensated regulators.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR33610 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. The timing parameters of the glitch filter are found in the [Electrical Characteristics](#) table. Output voltage excursions lasting less than t_{PG} do not trip the power-good flag. Power-good operation can best be understood by reference to [图 7](#) and [图 8](#). Note that during initial power-up a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

The power-good output consists of an open drain NMOS, requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT} through a 100-k Ω resistor, as desired. If this function is not needed, the PG pin must be left floating. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 2 V (typical). Limit the current into the power-good flag pin to less than 5 mA D.C. The maximum current is internally limited to about 35 mA when the device is enabled and about 65 mA when the device is disabled. The internal current limit protects the device from any transient currents that can occur when discharging a filter capacitor connected to this output.

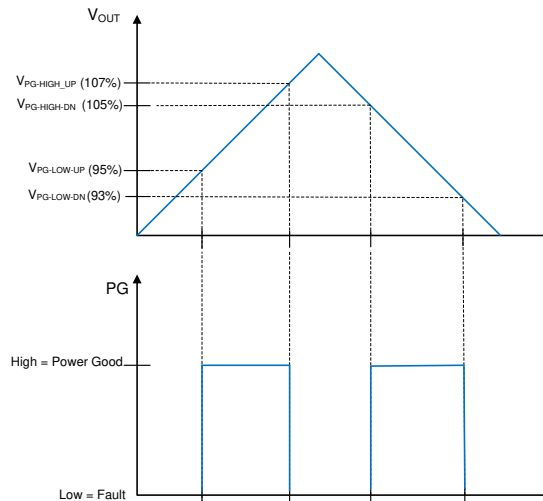


图 7. Static Power-Good Operation

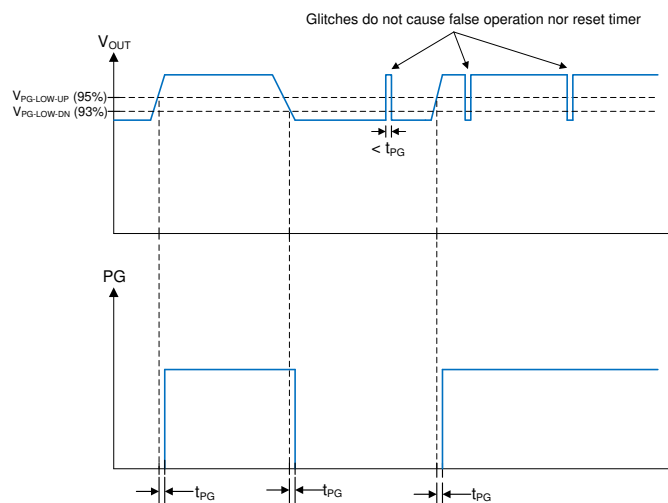


图 8. Power-Good-Timing Behavior

Feature Description (接下页)

8.3.2 Enable and Start-up

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see the [External UVLO](#) section). Applying a voltage of $\geq V_{EN-VCC_H}$ causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to V_{EN-H} fully enables the device, allowing it to enter start-up mode and begin the soft-start period. When the EN input is brought below V_{EN-H} by V_{EN-HYS} , the regulator stops running and enters standby mode. Further decrease in the EN voltage to below V_{EN-VCC_L} completely shuts down the device. 图 9 shows this behavior. The EN input can be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in the [Electrical Characteristics](#) table.

The uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. 图 10 shows a typical start-up waveform, indicating typical timings. The rise time of the output voltage is about 4 ms (see the [Electrical Characteristics](#) section).

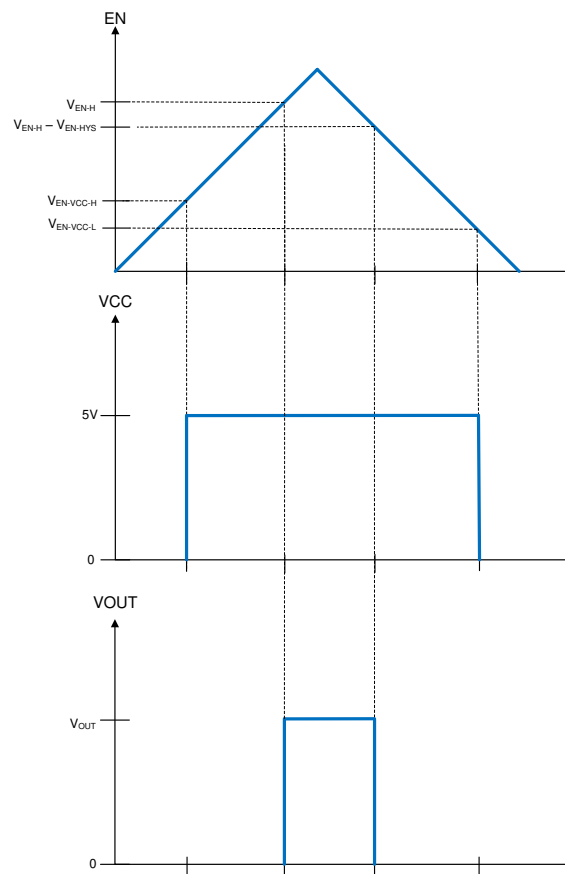


图 9. Precision Enable Behavior

Feature Description (接下页)

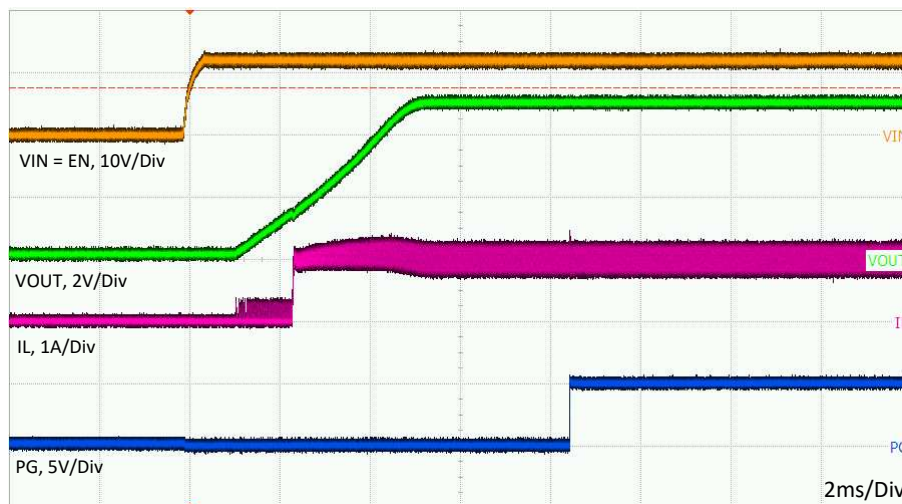


图 10. Typical Start-up Behavior
 $V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{OUT} = 1\text{ A}$

8.3.3 Current Limit and Short Circuit

The LMR33610 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement DEM at light loads (see the [Glossary](#)). The typical value of this current limit is found under I_{ZC} in the section.

When the device is overloaded, the valley of the inductor current may not reach below I_{LIMIT} , (see the [Electrical Characteristics](#) table) before the next clock cycle. When this occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, and the inductor ripple current to increase. When the peak of the inductor current reaches the high-side current limit, I_{SC} (see the [Electrical Characteristics](#) table), the switch duty cycle is reduced and the output voltage falls out of regulation. This represents the maximum output current from the converter and is given approximately by [公式 1](#).

$$I_{OUT}|_{max} = \frac{I_{LIMIT} + I_{SC}}{2} \quad (1)$$

If, during current limit, the voltage on the FB input falls below about 0.4 V, due to a short circuit, the device enters hiccup mode. In this mode, the device stops switching for t_{HC} (see the [System Characteristics](#) section), or about 94 ms, and then goes through a normal restart with soft start. If the short-circuit condition remains, the device runs in current limit for about 20 ms (typical) and then shuts down again. This cycle repeats, as shown in [图 11](#), as long as the short-circuit-condition persists. This mode of operation reduces the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode (see the [Typical Characteristics](#) section). Once the output short is removed and the hiccup delay is passed, the output voltage recovers normally as shown in [图 12](#).

Feature Description (接下页)

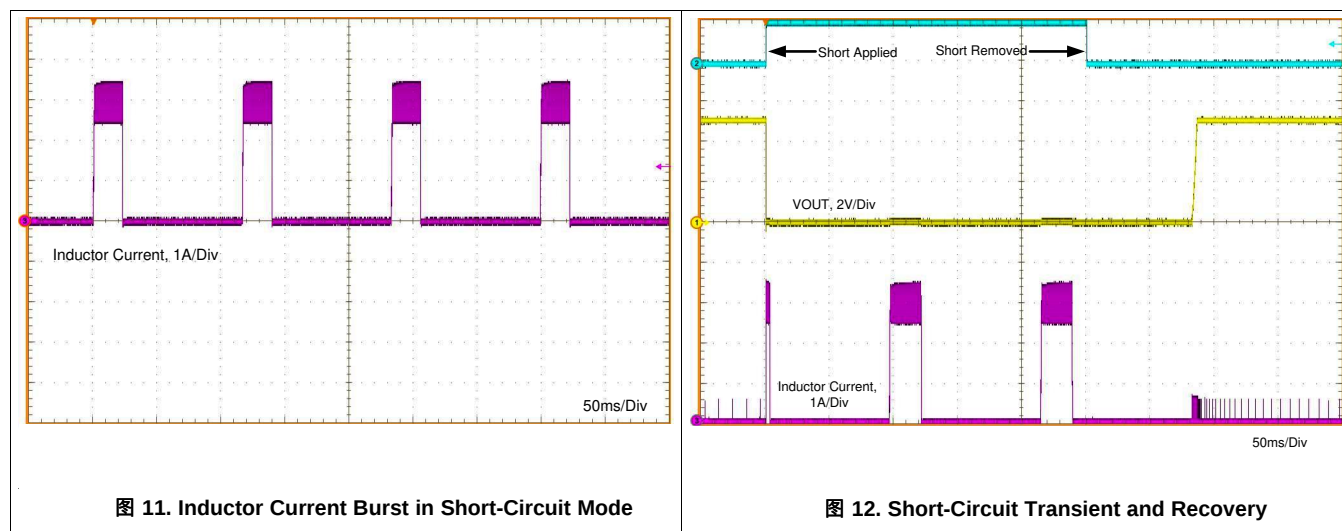


图 11. Inductor Current Burst in Short-Circuit Mode

图 12. Short-Circuit Transient and Recovery

8.3.4 Undervoltage Lockout and Thermal Shutdown

The LMR33610 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When VCC reaches about 3.7 V, the device is ready to receive an EN signal and start up. When VCC falls below about 3 V, the device shuts down, regardless of EN status. Since the LDO is in dropout during these transitions, the above values roughly represent the input voltage levels during the transitions.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 165°C, the device shuts down. Restart occurs when the temperature falls to about 148°C.

8.4 Device Functional Modes

8.4.1 Auto Mode

In auto mode, the device moves between PWM and PFM as the load changes. At light loads, the regulator operates in PFM. At higher loads, the mode changes to PWM. The load current for which the device moves from PFM to PWM can be found in the [Application Curves](#) section. The output current at which the device changes modes depends on the input voltage, inductor value, and the nominal switching frequency. The device is in PWM mode for output currents above the curve. The device is in PFM for currents below the curve. The curves apply for a nominal switching frequency of 400 kHz and the BOM shown in the [Application Curves](#). At higher switching frequencies, the load at which the mode change occurs is greater. For applications where the switching frequency must be known for a given condition, the transition between PFM and PWM must be carefully tested before the design is finalized.

In PWM mode, the regulator operates as a constant frequency converter, using PWM to regulate the output voltage. While operating in this mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach $I_{PEAK-MIN}$. The periodicity of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see the [Glossary](#)). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at light loads. PFM results in very good light-load efficiency, but also yields larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depends on the input voltage, output voltage, and load. 图 13 and 图 14 show typical switching waveforms in PFM and PWM. See the [Application Curves](#) section for output voltage variation with load in auto mode.

Device Functional Modes (接下页)

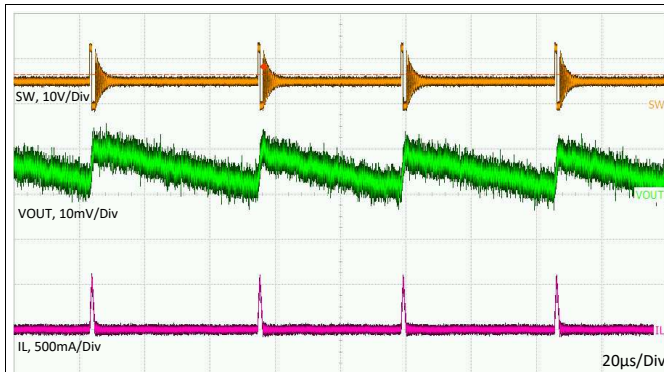


图 13. Typical PFM Switching Waveforms
 $V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{OUT} = 10\text{ mA}$

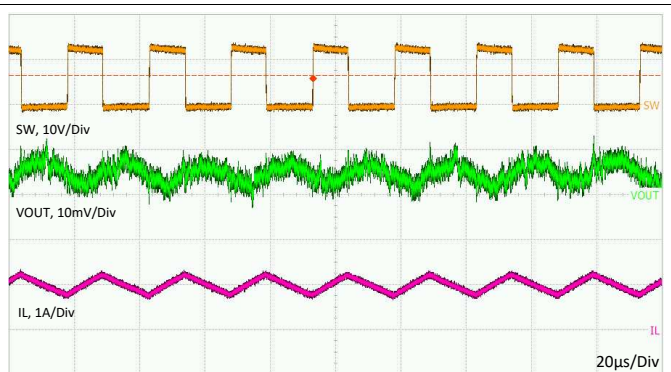


图 14. Typical PWM Switching Waveforms
 $V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{OUT} = 1\text{ A}$, $f_s = 400\text{ kHz}$

8.4.2 Dropout

The dropout performance of any buck regulator is affected by the $R_{DS(on)}$ of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off-time of the high side MOSFET starts to approach the minimum value (see the [Timing Characteristics](#) section). Beyond this point, the switching can become erratic and the output voltage falls out of regulation. To avoid this problem, the LMR33610 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet, the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of its nominal value. Under this condition, the switching frequency has dropped to its minimum value of about 140 kHz. Note that the 0.4 V short circuit detection threshold is not activated when in dropout mode. Typical dropout characteristics can be found in [图 15](#) and [图 16](#).

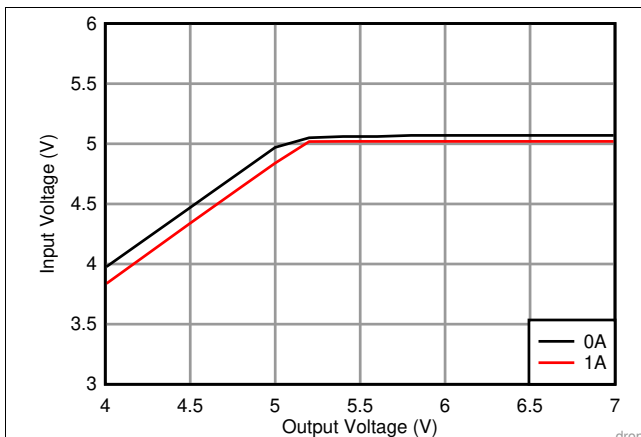


图 15. Overall Dropout Characteristic
 $V_{OUT} = 5\text{ V}$

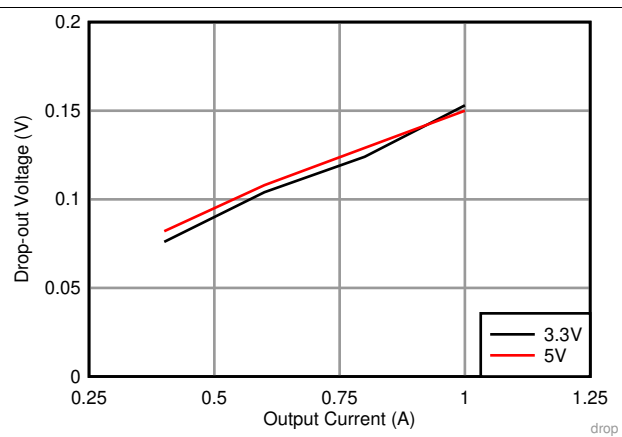


图 16. Typical Dropout Voltage versus Output Current in Frequency Foldback
 $f_{sw} = 140\text{ kHz}$

Device Functional Modes (接下页)

8.4.3 Minimum Switch On-Time

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LMR33610 automatically reduces the switching frequency when the minimum on-time limit is reached. This way, the converter can regulate the lowest programmable output voltage at the maximum input voltage. Use [公式 2](#) to estimate the approximate input voltage for a given output voltage before frequency foldback occurs. The values of t_{ON} and f_{SW} can be found in the [Electrical Characteristics](#) table. As the input voltage is increased, the switch on-time (duty-cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops while the on-time remains fixed.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \cdot f_{SW}} \quad (2)$$

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMR33610 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the LMR33610. Alternately, the WEBENCH Design Tool can be used to generate a complete design. This tool uses an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

注

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

9.2 Typical Application

图 17 shows a typical application circuit for the LMR33610. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, 表 2 provides typical component values for a range of the most common output voltages. The values given in the table are typical. Other values can be used to enhance certain performance criterion as required by the application.

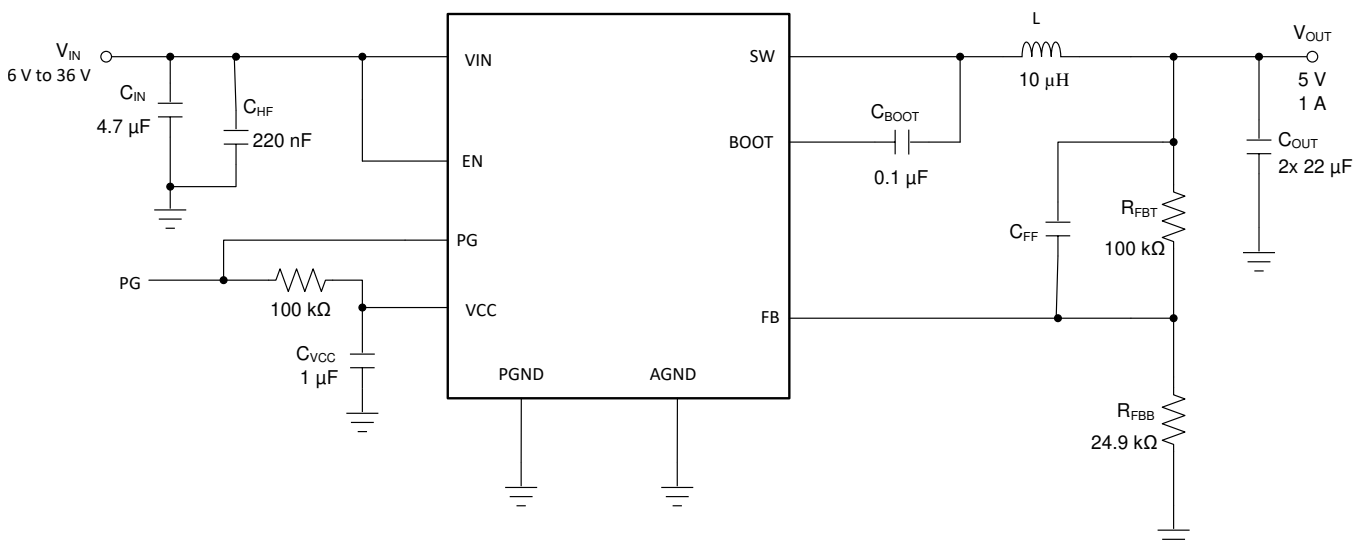


图 17. Example Application Circuit (400 kHz)

Typical Application (接下页)

9.2.1 Design Requirements

表 1 provides the parameters for the detailed design procedure example.

表 1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V (6 V to 36 V)
Output voltage	5 V
Maximum output current	0 A to 1 A
Switching frequency	400 kHz

表 2. Typical External Component Values

f_{sw} (kHz)	V_{OUT} (V)	L (μ H)	C_{OUT} (RATED CAPACITANCE)	R_{FBT} (Ω)	R_{FBB} (Ω)	$C_{IN} + C_{HF}$	C_{BOOT}	C_{VCC}	C_{FF}
400	3.3	10	$2 \times 22 \mu F$	100 k	43.2 k	$4.7 \mu F + 220 nF$	100 nF	1 μF	Open
1400	3.3	2.2	$1 \times 22 \mu F$	100 k	43.2 k	$4.7 \mu F + 220 nF$	100 nF	1 μF	Open
400	5	10	$2 \times 22 \mu F$	100 k	24.9 k	$4.7 \mu F + 220 nF$	100 nF	1 μF	Open
1400	5	2.2	$1 \times 22 \mu F$	100 k	24.9 k	$4.7 \mu F + 220 nF$	100 nF	1 μF	Open
400	12	15	$2 \times 22 \mu F$	100 k	9.09 k	$4.7 \mu F + 220 nF$	100 nF	1 μF	Open
1400	12	4.7	$2 \times 10 \mu F$	100 k	9.09 k	$4.7 \mu F + 220 nF$	100 nF	1 μF	Open

9.2.2 Detailed Design Procedure

The following design procedure applies to 图 17 and 表 1.

9.2.2.1 Custom Design With WEBENCH® Tools

Click [here](#) to create a custom design using the LMR33610 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WBENCH.

9.2.2.2 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors hence, a more compact design. 400 kHz was chosen for this example.

9.2.2.3 Setting the Output Voltage

The output voltage of LMR33610 is externally adjustable using a resistor divider network. The range of recommended output voltage is found in the table. The divider network is comprised of R_{FBT} and R_{FBB} and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF} . The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 k Ω with a maximum value of 1 M Ω . If a 1 M Ω is selected for R_{FBT} , then a feedforward capacitor must be used across this resistor to provide adequate loop phase margin (see the [C_{FF} Selection](#) section). Once R_{FBT} is selected, use [公式 3](#) to select R_{FBB} . V_{REF} is nominally 1 V (see the section for limits).

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1 \right]} \quad (3)$$

For this 5-V example, $R_{FBT} = 100$ k Ω and $R_{FBB} = 24.9$ k Ω are chosen.

9.2.2.4 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Use the maximum device current when selecting the ripple current for application with a much smaller maximum load than the maximum available from the device. Use [公式 4](#) to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, $K = 0.3$ and an inductance of was found. The next standard value of was selected.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUTmax}} \cdot \frac{V_{OUT}}{V_{IN}} \quad (4)$$

Ideally, the saturation current rating of the inductor must be at least as large as the high-side switch current limit, I_{SC} (see the [Electrical Characteristics](#) section). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT} , is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powdered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1 MHz. In any case, the inductor saturation current must not be less than the device low-side current limit, I_{LIMIT} (see the [Electrical Characteristics](#) section). To avoid subharmonic oscillation, the inductance value must not be less than that given in [公式 5](#). The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L_{MIN} \geq 0.36 \cdot \frac{V_{OUT}}{f_{SW}} \quad (5)$$

9.2.2.5 Output Capacitor Selection

The value of the output capacitor and its ESR determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements rather than the output voltage ripple. Use [公式 6](#) to estimate a lower bound on the total output capacitance and an upper bound on the ESR, which is required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[1+K + \frac{K^2}{12} \cdot \left(1 + \frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = ripple factor from [Inductor Selection](#)

(6)

Once the output capacitor and ESR have been calculated, use [公式 7](#) to check the peak-to-peak output voltage ripple, V_r .

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}}$$

(7)

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

This example requires a $\Delta V_{OUT} \leq 250$ mV for an output current step of $\Delta I_{OUT} = 1$ A. [公式 6](#) gives a minimum value of 25 μ F and a maximum ESR of 0.21 Ω . Assuming a 20% tolerance and a 10% bias de-rating, there is a minimum capacitance of 35 μ F. This can be achieved with a bank of 2 $\times$ 22- μ F, 16-V, ceramic capacitors in the 1210 case size. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases, an aluminum electrolytic capacitor can be placed in parallel with the ceramics to help build up the required value of capacitance. In general, use a capacitor of at least 10 V for output voltages of 3.3 V or less, while a capacitor of 16 V or more must be used for output voltages of 5 V and above.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing voltage spikes on the output caused by inductor and board parasitics.

The maximum value of total output capacitance must be limited to about 10 times the design value, or 1000 μ F, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

9.2.2.6 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 4.7 μ F of ceramic capacitance is required on the input of the LMR33610. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 220-nF ceramic capacitor must be used at the input as close as possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example, a 4.7- μ F, 50-V, X7R (or better) ceramic capacitor is chosen. The 220 nF must also be rated at 50 V with an X7R dielectric.

Many times, it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate worst case RMS value of this current can be calculated from 公式 8 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \quad (8)$$

9.2.2.7 C_{BOOT}

The LMR33610 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 10 V is required.

9.2.2.8 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-μF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see the [Power-Good Flag Output](#) section). A value of 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V; see the [Electrical Characteristics](#) section for limits. Do not short this output to ground or any other external voltage.

9.2.2.9 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of $R_{FBT} > 100 \text{ k}\Omega$ are used. Large values of R_{FBT} , in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A C_{FF} can help mitigate this effect. Use 公式 9 to estimate the value of C_{FF} . The value found with 公式 9 is a starting point; use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The [Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor Application Report](#) is helpful when experimenting with a feedforward capacitor.

$$C_{FF} < \frac{V_{OUT} \cdot C_{OUT}}{120 \cdot R_{FBT} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (9)$$

9.2.2.10 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 图 18. The input voltage at which the device turns on is designated V_{ON} while the turnoff voltage is V_{OFF} . First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ and then 公式 10 is used to calculate R_{ENT} and V_{OFF} .

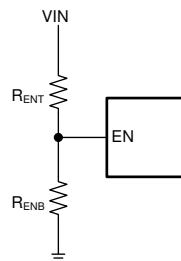


图 18. Set-Up for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left(1 - \frac{V_{EN-HYS}}{V_{EN-H}} \right)$$

where

- $V_{ON} = V_{IN}$ turnon voltage
- $V_{OFF} = V_{IN}$ turnoff voltage

(10)

9.2.2.11 Maximum Ambient Temperature

As with any power conversion device, the LMR33610 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device and PCB combination. The maximum internal die temperature for the LMR33610 must be limited to 125°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 公式 11 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the [Semiconductor and IC Package Thermal Metrics Application Report](#), the value of $R_{\theta JA}$ given in the table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1 - \eta)} \cdot \frac{1}{V_{OUT}}$$

where

- η = efficiency

(11)

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The HSOIC (DDA) package uses a die attach paddle or thermal pad (PAD) to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Typical examples of $R_{\theta JA}$ versus copper board area can be found in 图 19. The copper area given in the graph is for each layer; the top and bottom layers are 2 ounce copper each, while the inner layers are 1 ounce.

图 20 and 图 21 shows the typical curves of maximum output current versus ambient temperature. This data was taken with a device and PCB combination, giving an $R_{\theta JA}$ as noted in the graph. It must be remembered that the data given in these graphs are for illustration purposes only and the actual performance in any given application depends on all of the previously mentioned factors.

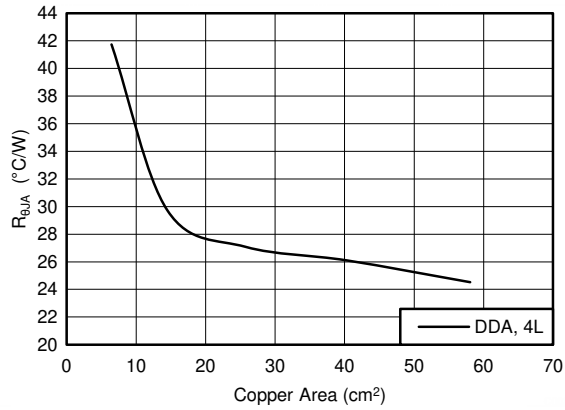


图 19. Typical $R_{\theta JA}$ versus Copper Area for a Four-Layer Board and the HSOIC (DDA) Package

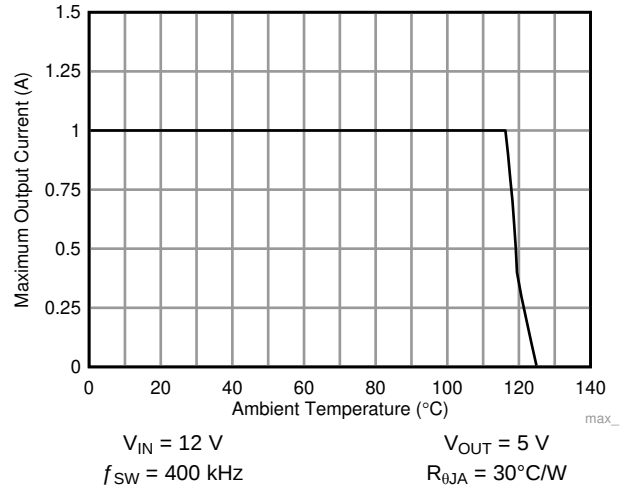


图 20. Maximum Output Current versus Ambient Temperature

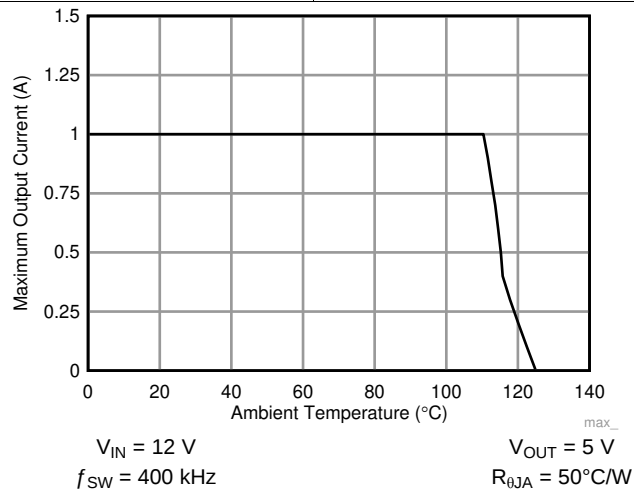


图 21. Maximum Output Current versus Ambient Temperature

Use the following resources as a guide to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- [*Thermal Design by Insight not Hindsight Application Report*](#)
- [*A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*](#)
- [*Semiconductor and IC Package Thermal Metrics Application Report*](#)
- [*Thermal Design Made Simple with LM43603 and LM43602 Application Report*](#)
- [*PowerPAD™ Thermally Enhanced Package Application Report*](#)
- [*PowerPAD™ Made Easy Application Report*](#)
- [*Using New Thermal Metrics Application Report*](#)

9.2.3 Application Curves

Unless otherwise specified the following conditions apply: $V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$. 图 36 shows the circuit with the appropriate BOM from 表 3.

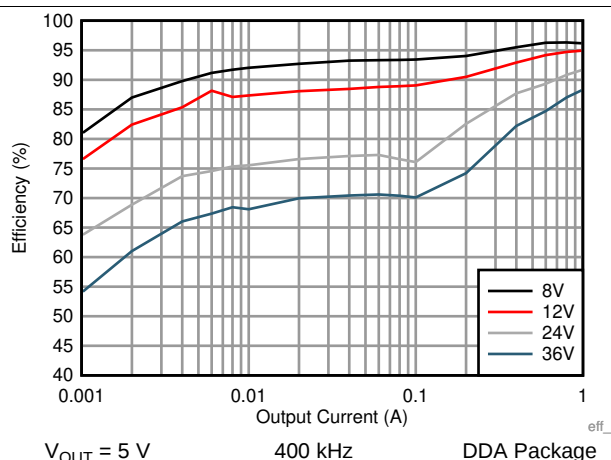


图 22. Efficiency

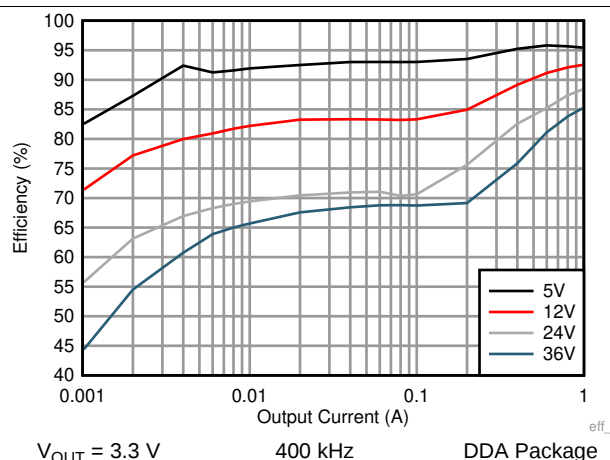


图 23. Efficiency

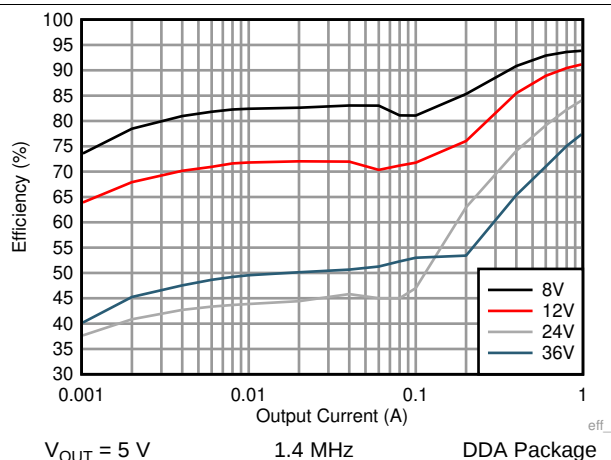


图 24. Efficiency

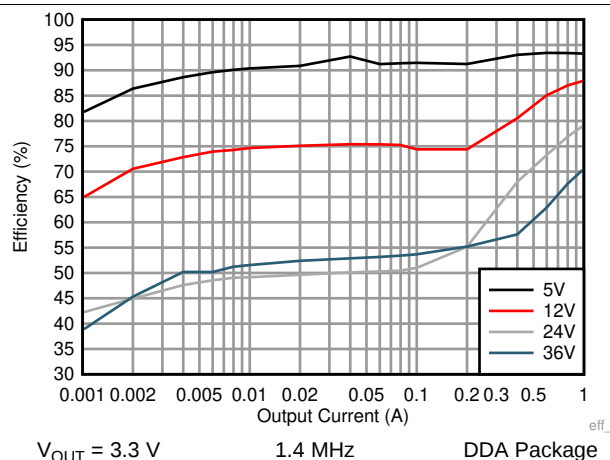


图 25. Efficiency

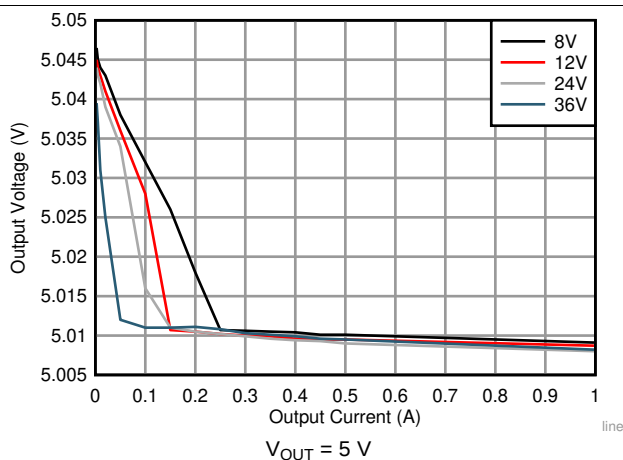


图 26. Line and Load Regulation

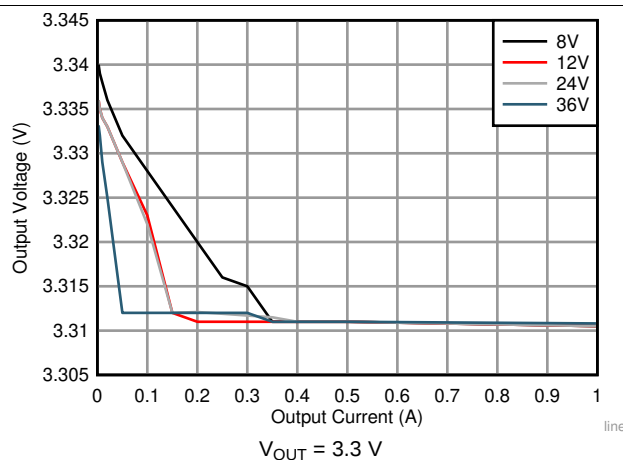


图 27. Line and Load Regulation

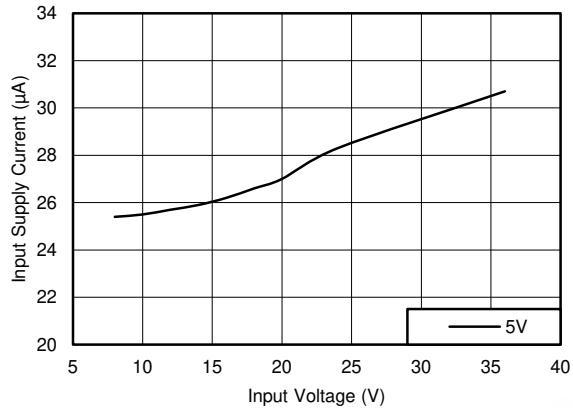


图 28. Input Supply Current

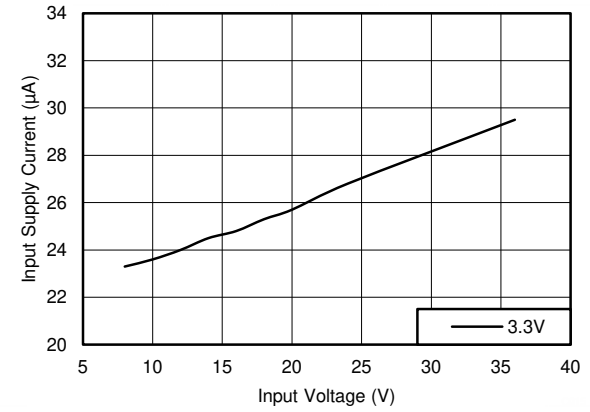


图 29. Input Supply Current

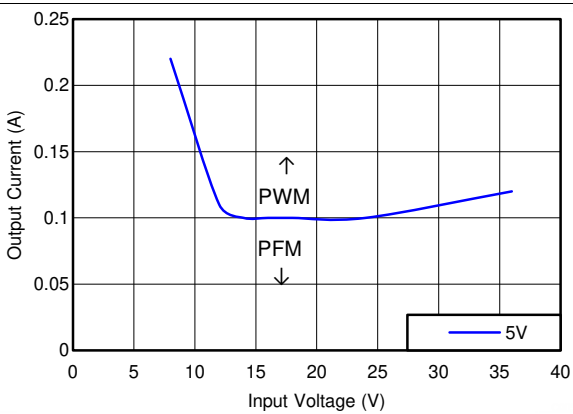


图 30. Mode Change Thresholds

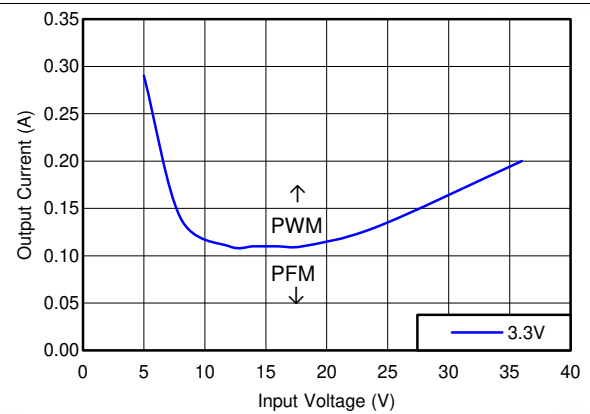


图 31. Mode Change Thresholds

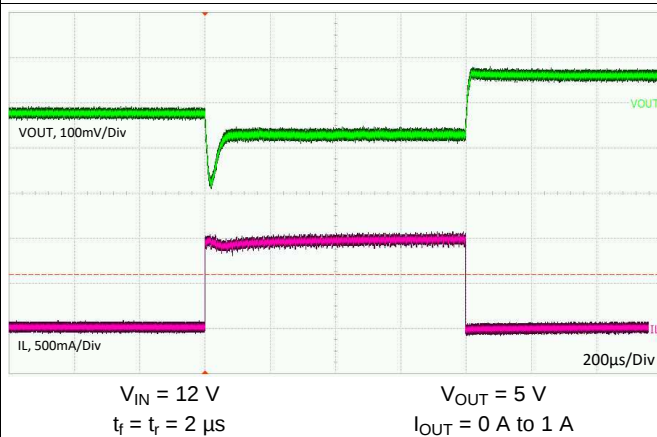


图 32. Load Transient

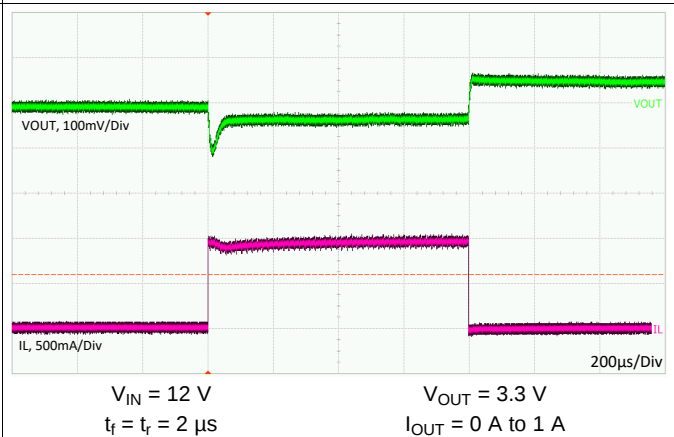


图 33. Load Transient

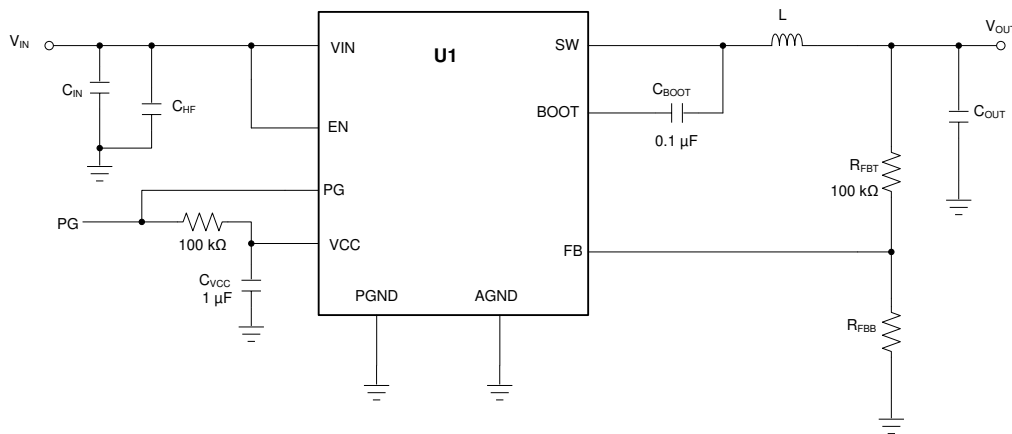
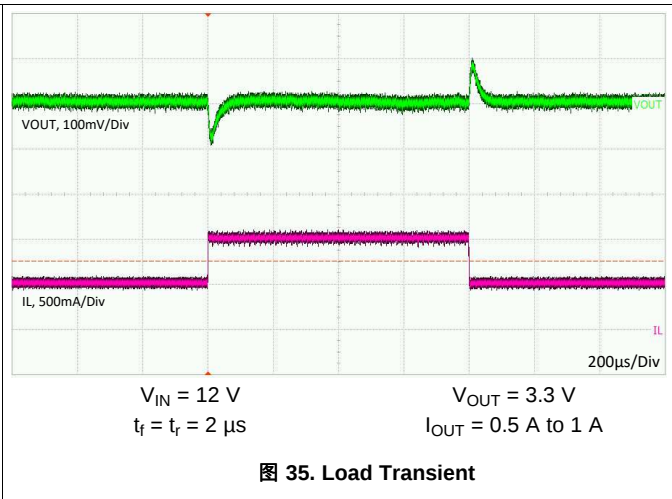
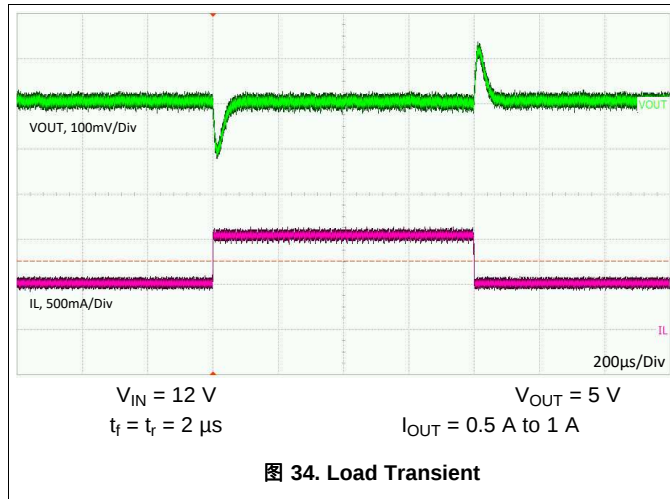


表 3. BOM for Typical Application Curves DDA Package⁽¹⁾

V _{OUT}	FREQUENCY	R _{FBB}	C _{OUT}	C _{IN} + C _{FB}	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 μF	1 × 10 μF + 1 × 220 nF	6.8 μH, 14 mΩ	LMR33610ADDA
3.3 V	1400 KHz	43.3 kΩ	4 × 22 μF	1 × 10 μF + 1 × 220 nF	2.2 μH, 11.4 mΩ	LMR33610BDDBA
5 V	400 kHz	24.9 kΩ	4 × 22 μF	1 × 10 μF + 1 × 220 nF	8.2 μH, 14 mΩ	LMR33610ADDA
5 V	1400 KHz	24.9 kΩ	4 × 22 μF	1 × 10 μF + 1 × 220 nF	2.2 μH, 11.4 mΩ	LMR33610BDDBA

(1) The values in this table were selected to enhance certain performance criteria and may not represent typical values.

9.3 What to Do and What Not to Do

- Do not exceed the [Absolute Maximum Ratings](#).
- Do not exceed the [ESD Ratings](#).
- Do not exceed the [Recommended Operating Conditions](#).
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Do not use the value of R_{θJA} given in the [Thermal Information](#) table to design your application. Use the information in the [Maximum Ambient Temperature](#) section.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success (see the [支持资源](#)).

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the and found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. Use [公式 12](#) to estimate the average input current.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta}$$

where

- η is the efficiency (12)

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help damp the input resonant circuit and reduce any overshoots. A value in the range of 20 μ F to 100 μ F is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The [AN-2162 Simple Success With Conducted EMI From DCDC Converters User's Guide](#) provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharges through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output must be used.

11 Layout

11.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in [Figure 37](#). This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. [Figure 38](#) and show recommended layouts for the critical components of the LMR33610.

1. *Place the input capacitor or capacitors as close as possible to the VIN and GND terminals.* VIN and GND pins are adjacent, simplifying the input capacitor placement. A wide VIN plane must be used on a lower layer to connect both of the VIN pairs together to the input supply.
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short, wide traces to the BOOT and SW pins.
4. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and a heat dissipation path.
6. *Connect the thermal pad to the ground plane.* The SOIC package has a thermal pad (PAD) connection that must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection and an electrical ground connection for the regulator. The integrity of this solder connection has a direct bearing on the total effective R_{θJA} of the application.
7. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. *Provide enough PCB area for proper heat sinking.* As stated in the [Maximum Ambient Temperature](#) section, enough copper area must be used to ensure a low R_{θJA}, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. With the SOIC package, use an array of heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
9. *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- [Layout Guidelines for Switching Power Supplies Application Report](#)
- [Simple Switcher PCB Layout Guidelines Application Report](#)
- [Construction Your Power Supply- Layout Considerations Seminar](#)
- [Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report](#)

Layout Guidelines (接下页)

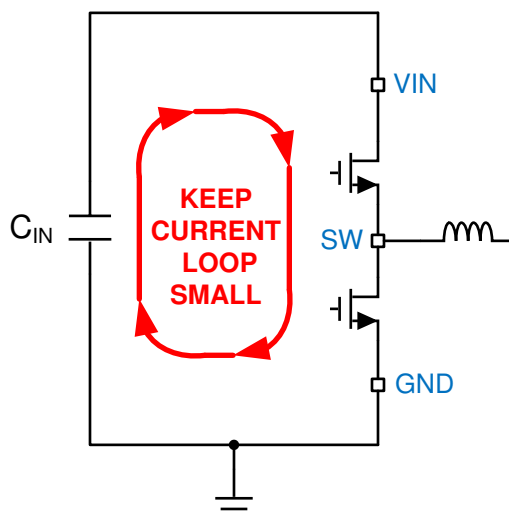


图 37. Current Loops with Fast Edges

11.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by using the thermal pad (PAD) of the device as the primary thermal path. Use a minimum 4×3 array of 10 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible. For system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.

11.2 Layout Example

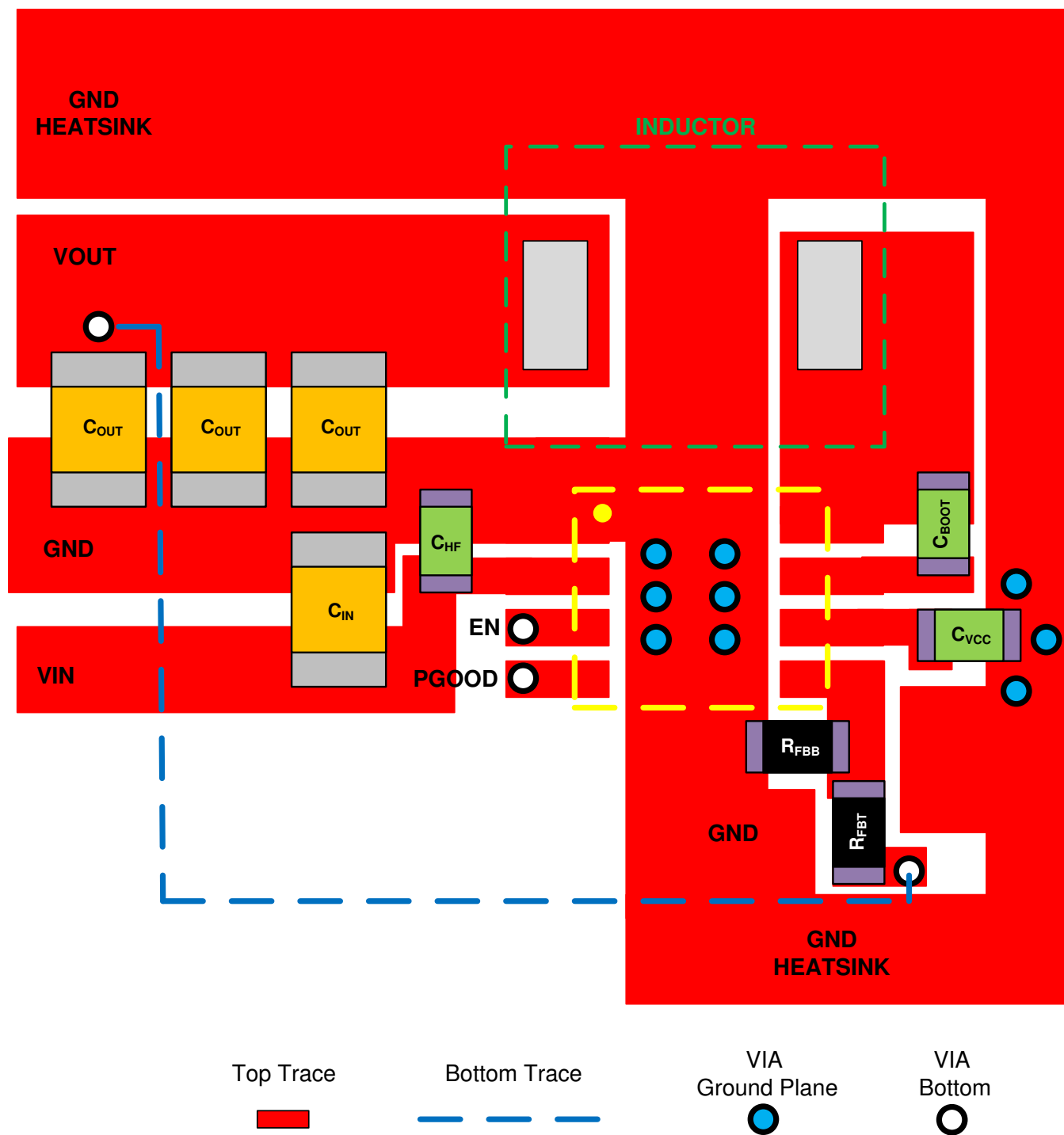


图 38. Example Layout for HSOIC (DDA) Package

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 使用 WEBENCH® 工具创建定制设计

单击[此处](#)，使用 LMR33610 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WBENCH。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，《[热设计：学会洞察先机，不做事后诸葛](#)》应用报告
- 德州仪器 (TI)，《[外露焊盘封装实现最佳热阻性的电路板布局指南](#)》应用报告
- 德州仪器 (TI)，《[半导体和 IC 封装热指标](#)》应用报告
- 德州仪器 (TI)，《[通过 LM43603 和 LM43602 简化热设计](#)》应用报告
- 德州仪器 (TI)，《[PowerPAD™ 热增强型封装](#)》应用报告
- 德州仪器 (TI)，《[PowerPAD™ 速成](#)》应用报告
- 德州仪器 (TI)，《[使用新的热指标应用报告](#)》
- 德州仪器 (TI)，《[开关电源布局指南](#)》应用报告
- 德州仪器 (TI)，《[Simple Switcher PCB 布局指南](#)》应用报告
- 德州仪器 (TI)，《[构建电源 - 布局注意事项](#)》
- 德州仪器 (TI)，《[使用 LM4360x 与 LM4600x 简化低辐射 EMI 布局](#)》应用报告

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 商标

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12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR33610ADDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33610A	Samples
LMR33610BDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33610B	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

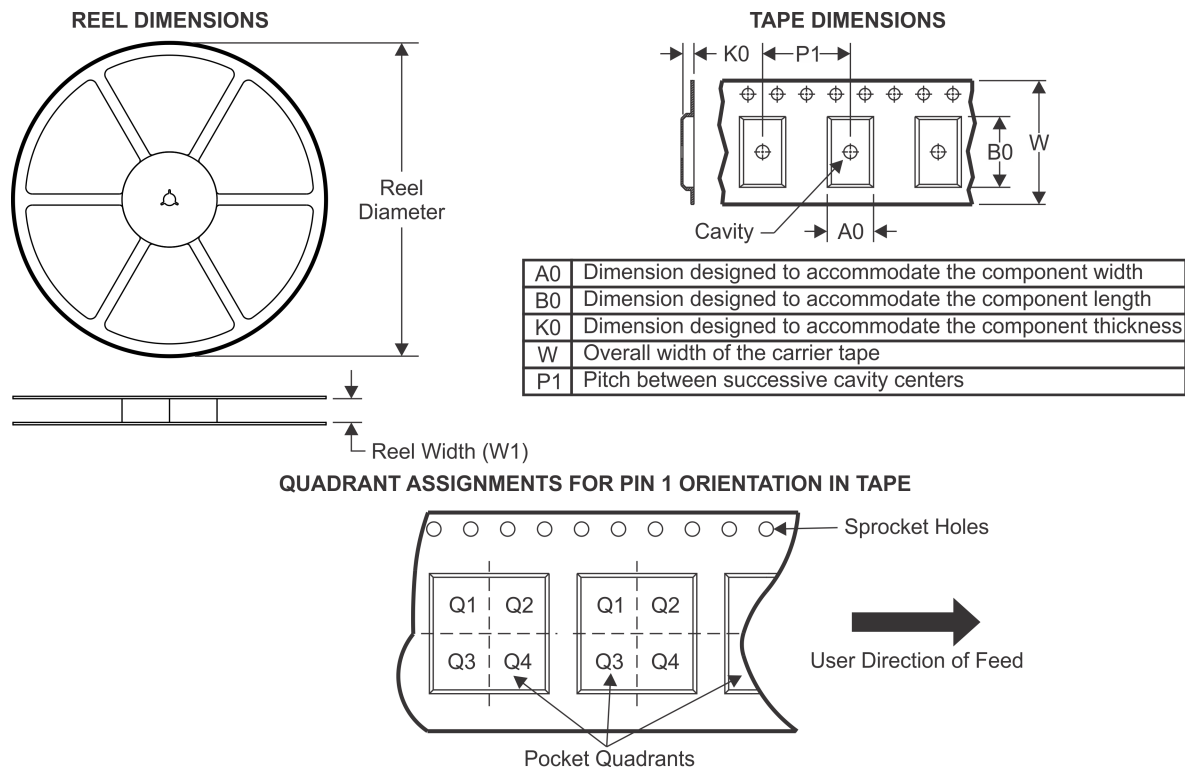
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

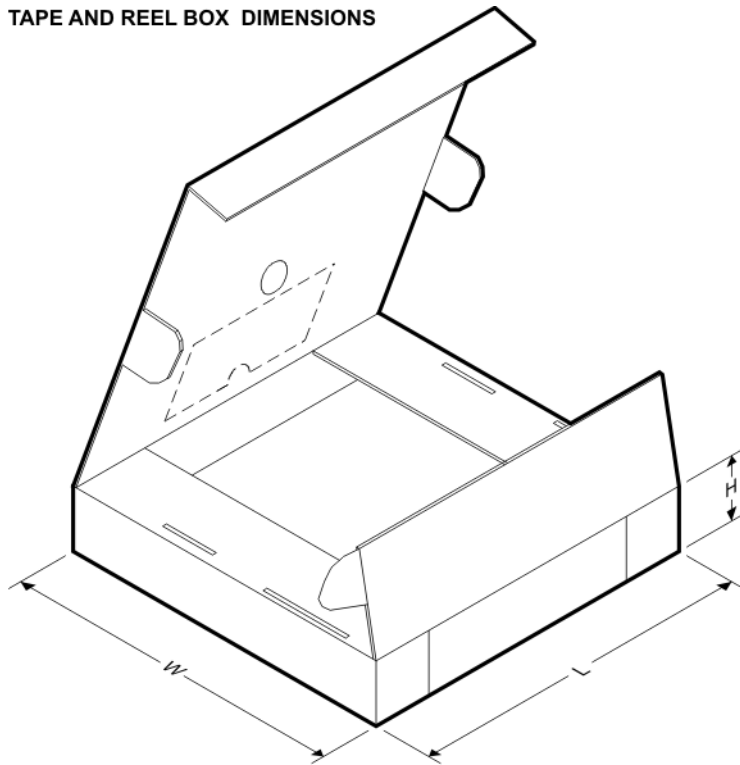
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

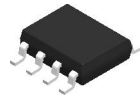
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR33610ADDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR33610BDDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

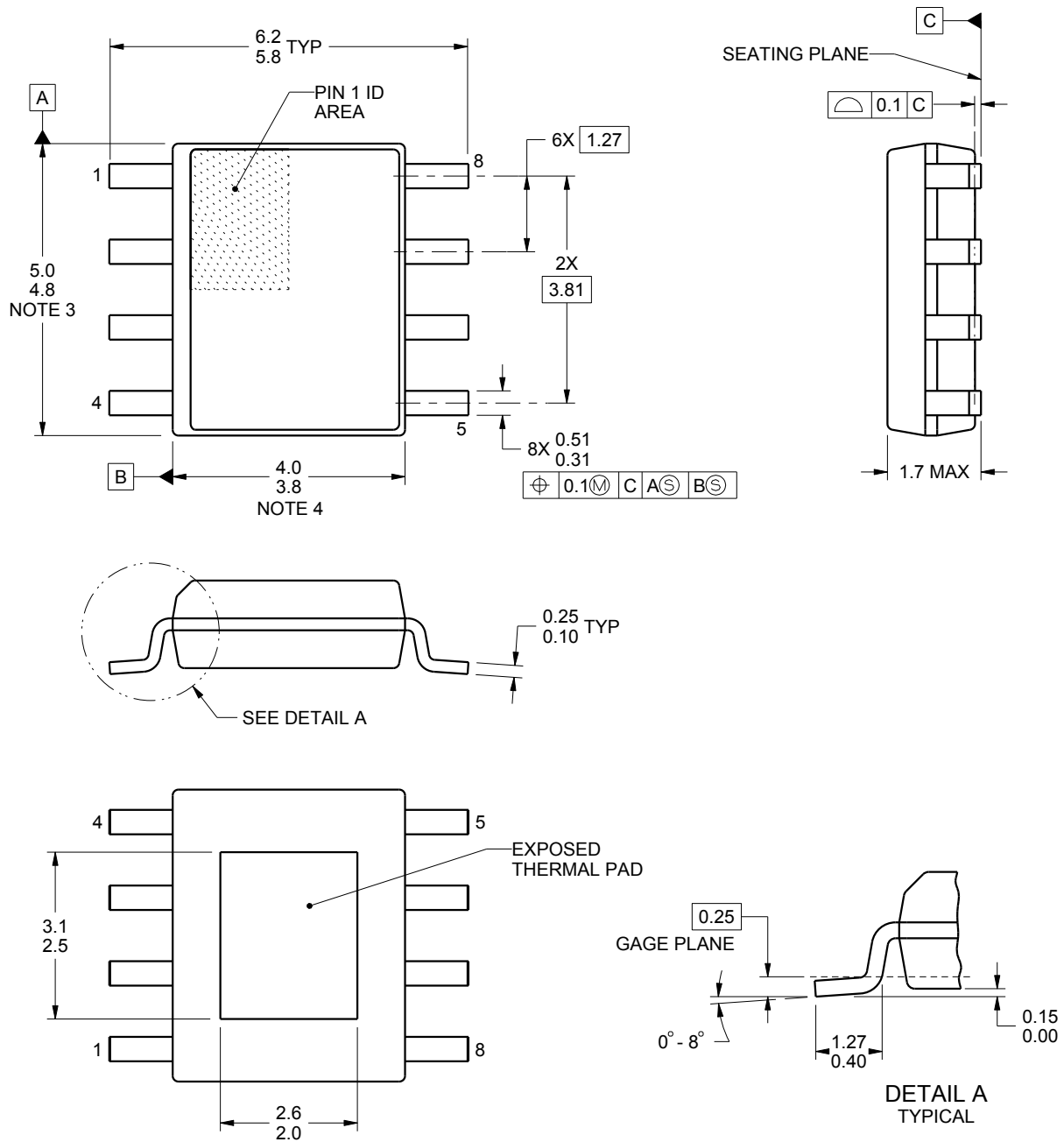
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR33610ADDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR33610BDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA0008J

PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4221637/B 03/2016

PowerPAD is a trademark of Texas Instruments.

NOTES:

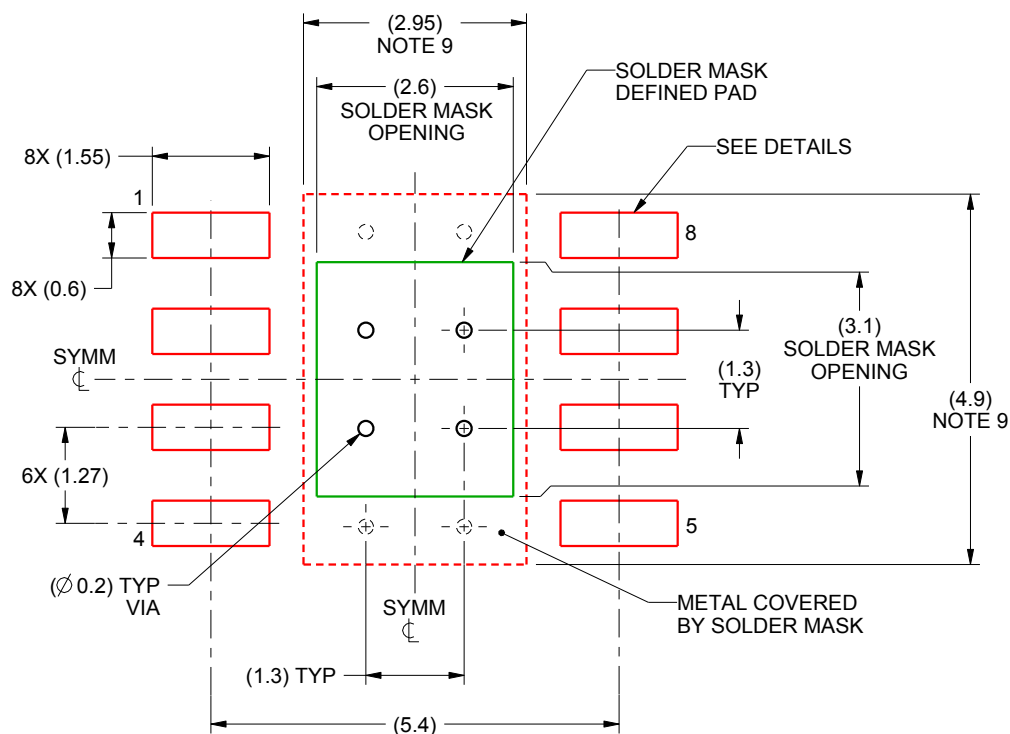
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

EXAMPLE BOARD LAYOUT

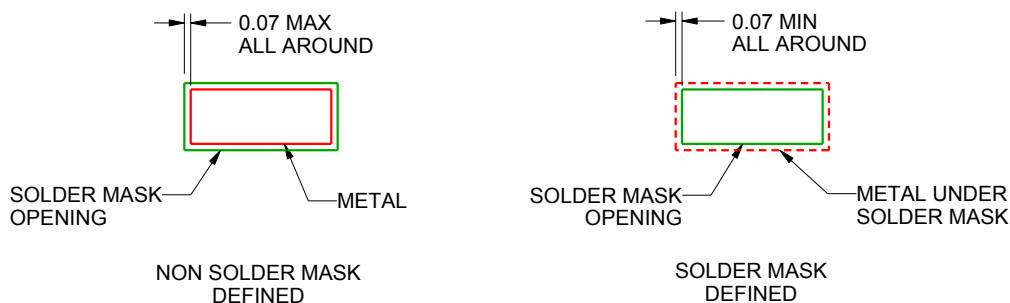
DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

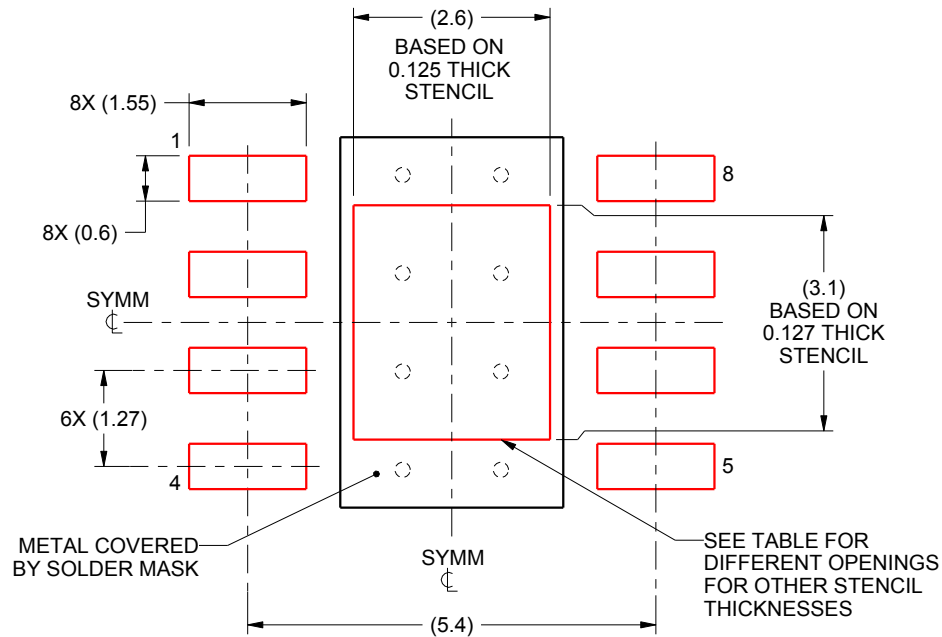
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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