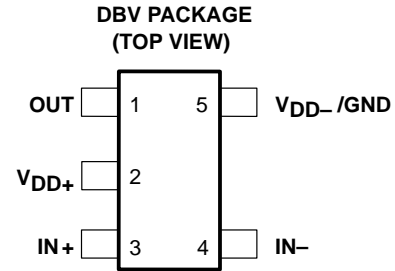


- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 15 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Single-Supply 3-V and 5-V Operation**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High Gain Bandwidth . . . 2 MHz at V_{DD} = 5 V with 600 Ω Load**
- **High Slew Rate . . . 1.6 V/μs at V_{DD} = 5 V**
- **Wide Supply Voltage Range 2.7 V to 10 V**
- **Macromodel Included**



description

The TLV2731 is a single low-voltage operational amplifier available in the SOT-23 package. It offers 2 MHz of bandwidth and 1.6 V/μs of slew rate for applications requiring good ac performance. The device exhibits rail-to-rail output performance for increased dynamic range in single or split supply applications. The TLV2731 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2731, exhibiting high input impedance and low noise, is excellent for small-signal conditioning of high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). The device can also drive 600-Ω loads for telecom applications.

With a total area of 5.6mm², the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES	SYMBOL	CHIP FORM‡ (Y)
		SOT-23 (DBV)†		
0°C to 70°C	3 mV	TLV2731CDBV	VALC	TLV2731Y
–40°C to 85°C	3 mV	TLV2731IDBV	VALI	

† The DBV package available in tape and reel only.

‡ Chip forms are tested at T_A = 25°C only.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.


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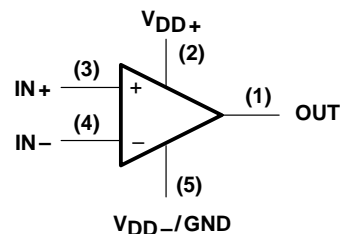
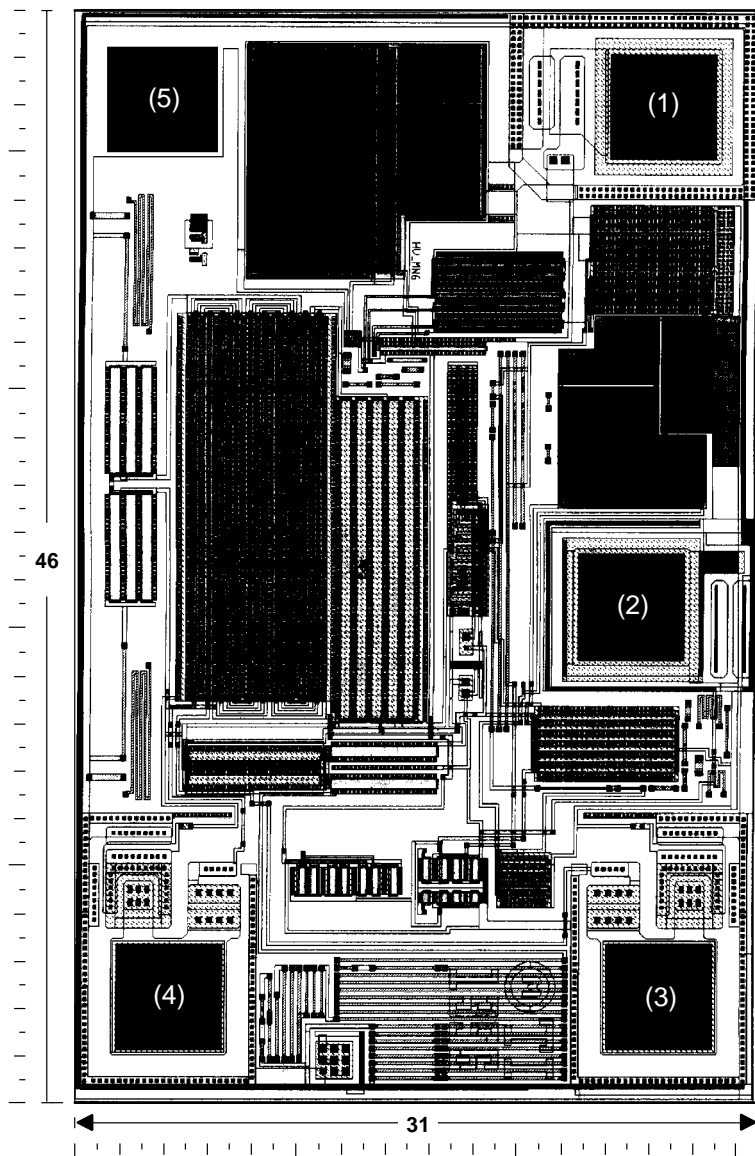
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TLV2731Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2731C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4×4 MILS MINIMUM

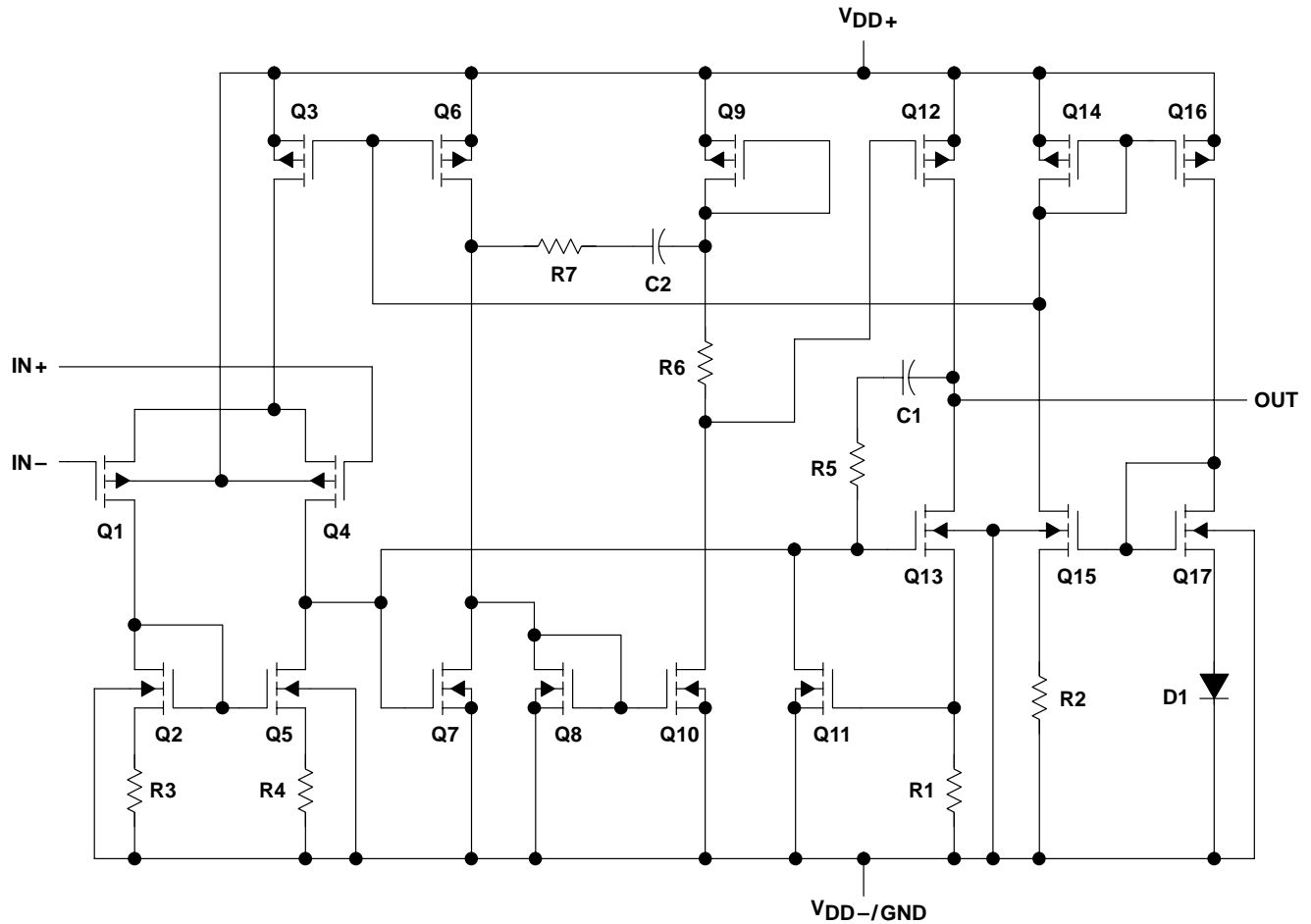
$T_{jmax} = 150^{\circ}\text{C}$

TOLERANCES ARE $\pm 10\%$.

ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



COMPONENT COUNT†	
Transistors	23
Diodes	5
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	12 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	$-0.3\text{ V to }V_{DD}$
Input current, I_I (each input)	$\pm 5\text{ mA}$
Output current, I_O	$\pm 50\text{ mA}$
Total current into V_{DD+}	$\pm 50\text{ mA}$
Total current out of V_{DD-}	$\pm 50\text{ mA}$
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : TLV2731C	$0^\circ\text{C to }70^\circ\text{C}$
TLV2731I	$-40^\circ\text{C to }85^\circ\text{C}$
Storage temperature range, T_{stg}	$-65^\circ\text{C to }150^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-} .
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3\text{ V}$.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DBV	150 mW	1.2 mW/ $^\circ\text{C}$	96 mW	78 mW

recommended operating conditions

	TLV2731C		TLV2731I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	0	70	-40	85	$^\circ\text{C}$

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-} .

electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A †	TLV2731C			TLV2731I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD} ± = ±1.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω		Full range	0.7		3	0.7		3	mV
αV _{IO}	Temperature coefficient of input offset voltage				0.5		0.5		μV/°C		
	Input offset voltage long-term drift (see Note 4)			25°C	0.003		0.003		μV/mo		
I _{IO}	Input offset current			25°C	0.5	60	0.5	60	pA		
				Full range	150		150				
I _{IB}	Input bias current			25°C	1	60	1	60	pA		
		Full range	150		150						
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	0 to 2	−0.3 to 2.2	0 to 2	−0.3 to 2.2	V		
				Full range	0 to 1.7		0 to 1.7				
V _{OH}	High-level output voltage	I _{OH} = −1 mA		25°C	2.87		2.87		V		
		I _{OH} = −2 mA		25°C	2.74		2.74				
				Full range	2.3		2.3				
V _{OL}	Low-level output voltage	V _{IC} = 1.5 V, I _{OL} = 50 μA		25°C	10		10		mV		
		V _{IC} = 1.5 V, I _{OL} = 500 μA		25°C	100		100				
				Full range	300		300				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 1.5 V, V _O = 1 V to 2 V	R _L = 600 Ω‡	25°C	1	1.6	1	1.6	V/mV		
				Full range	0.3		0.3				
			R _L = 1 MΩ‡	25°C	250		250				
r _{id}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω		
r _{ic}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω		
c _{ic}	Common-mode input capacitance	f = 10 kHz		25°C	6		6		pF		
z _o	Closed-loop output impedance	f = 1 MHz, A _V = 1		25°C	156		156		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 1.7 V, V _O = 1.5 V, R _S = 50 Ω		25°C	60	70	60	70	dB		
				Full range	55		55				
k _{SVR}	Supply voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 2.7 V to 8 V, V _{IC} = V _{DD} /2, No load		25°C	70	96	70	96	dB		
				Full range	70		70				
I _{DD}	Supply current	V _O = 1.5 V, No load		25°C	750	1200	750	1200	μA		
				Full range	1500		1500				

† Full range for the TLV2731C is 0°C to 70°C. Full range for the TLV2731I is -40°C to 85°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER		TEST CONDITIONS	T_A †	TLV2731C			TLV2731I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.1\text{ V to }1.9\text{ V}$, $C_L = 100\text{ pF}‡$	25°C	0.75	1.25		0.75	1.25		$\text{V}/\mu\text{s}$
			Full range	0.5			0.5			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		105			105		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	25°C		16			16		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		1.4			1.4		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.5			1.5		
I_n	Equivalent input noise current		25°C		0.6			0.6		$\text{fA}/\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion plus noise	$V_O = 1\text{ V to }2\text{ V}$, $f = 20\text{ kHz}$, $R_L = 600\ \Omega‡$	25°C	$A_V = 1$		0.285%	0.285%			
				$A_V = 10$		7.2%	7.2%			
		$V_O = 1\text{ V to }2\text{ V}$, $f = 20\text{ kHz}$, $R_L = 600\ \Omega§$	25°C	$A_V = 1$		0.014%	0.014%			
				$A_V = 10$		0.098%	0.098%			
				$A_V = 100$		0.13%	0.13%			
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}‡$	25°C		1.9			1.9		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $R_L = 600\ \Omega‡$	25°C		60			60		kHz
t_s	Settling time	$A_V = -1$, Step = $1\text{ V to }2\text{ V}$, $R_L = 600\ \Omega‡$, $C_L = 100\text{ pF}‡$	25°C	To 0.1%		0.9	0.9			μs
				To 0.01%		1.5	1.5			
ϕ_m	Phase margin at unity gain	$R_L = 600\ \Omega‡$, $C_L = 100\text{ pF}‡$	25°C		50°			50°		
	Gain margin		25°C		8			8		dB

† Full range is -40°C to 85°C .

‡ Referenced to 1.5 V

§ Referenced to 0 V

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A †	TLV2731C			TLV2731I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD±} = ±2.5 V, V _{IC} = 0, V _O = 0, R _S = 50 Ω		Full range	0.7 3			0.7 3			mV
α _{VIO}	Temperature coefficient of input offset voltage				0.5			0.5			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003			μV/mo
I _{IO}	Input offset current			25°C	0.5 60			0.5 60			pA
				Full range	150			150			
I _{IB}	Input bias current			25°C	1 60			1 60			pA
		Full range	150			150					
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	0 to 4 −0.3 to 4.2		0 to 4 −0.3 to 4.2		V		
				Full range	0 to 3.7		0 to 3.7				
V _{OH}	High-level output voltage	I _{OH} = −1 mA		25°C	4.9		4.9		V		
		I _{OH} = −4 mA		25°C	4.6		4.6				
				Full range	4.3		4.3				
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 500 μA		25°C	80		80		mV		
		V _{IC} = 2.5 V, I _{OL} = 1 mA		25°C	160		160				
				Full range	500		500				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 600 Ω‡	25°C	1 1.5		1 1.5		V/mV		
			R _L = 1 MΩ‡	Full range	0.3		0.3				
				25°C	400		400				
r _{id}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω		
r _{ic}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω		
c _{ic}	Common-mode input capacitance	f = 10 kHz		25°C	6		6		pF		
z _o	Closed-loop output impedance	f = 1 MHz, A _V = 1		25°C	138		138		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 50 Ω		25°C	60 70		60 70		dB		
				Full range	55		55				
KSVR	Supply voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 8 V, V _{IC} = V _{DD} /2, No load		25°C	70 96		70 96		dB		
				Full range	70		70				
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	850 1300		850 1300		μA		
				Full range	1600		1600				

† Full range for the TLV2731C is 0°C to 70°C. Full range for the TLV2731I is –40°C to 85°C.

‡ Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS	T_A †	TLV2731C			TLV2731I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V}$, $R_L = 600\ \Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	1	1.6		1	1.6		V/μs
			Full range	0.7			0.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		100			100		nV/√Hz
		$f = 1\text{ kHz}$	25°C		15			15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		1.4			1.4		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.5			1.5		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	$V_O = 1.5\text{ V to }3.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 600\ \Omega$ ‡	25°C	$A_V = 1$		0.409%	0.409%			
				$A_V = 10$		3.68%	3.68%			
		$V_O = 1.5\text{ V to }3.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 600\ \Omega$ §	25°C	$A_V = 1$		0.018%	0.018%			
				$A_V = 10$		0.045%	0.045%			
				$A_V = 100$		0.116%	0.116%			
	Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 600\ \Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		2			2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $R_L = 600\ \Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C		300			300		kHz
t_s	Settling time	$A_V = -1$, Step = 1.5 V to 3.5 V, $R_L = 600\ \Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	To 0.1%		0.95	0.95			μs
				To 0.01%		2.4	2.4			
ϕ_m	Phase margin at unity gain	$R_L = 600\ \Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		48°			48°		
	Gain margin		25°C		8			8		dB

† Full range is –40°C to 85°C.

‡ Referenced to 2.5 V

§ Referenced to 0 V



electrical characteristics at $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV2731Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		750		μV
I_{IO} Input offset current			0.5	60	pA
I_{IB} Input bias current			1	60	pA
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$		–0.3 to 2.2		V
V_{OH} High-level output voltage	$I_{OH} = -1\text{ mA}$		2.87		V
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$		10		mV
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$		100		
A_{VD} Large-signal differential voltage amplification	$V_O = 1\text{ V to }2\text{ V}$		$R_L = 600\ \Omega^\dagger$	1.6	V/mV
			$R_L = 1\text{ M}\Omega^\dagger$	250	
r_{id} Differential input resistance			10^{12}		Ω
r_{ic} Common-mode input resistance			10^{12}		Ω
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$		6		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}$, $A_V = 1$		156		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$		70		dB
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V}$, $V_{IC} = 0$, No load		96		dB
I_{DD} Supply current	$V_O = 0$, No load		750		μA

† Referenced to 1.5 V

electrical characteristics at $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV2731Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		710		μV
I_{IO} Input offset current			0.5	60	pA
I_{IB} Input bias current			1	60	pA
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$		–0.3 to 4.2		V
V_{OH} High-level output voltage	$I_{OH} = -1\text{ mA}$		4.9		V
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$		80		mV
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 1\text{ mA}$		160		
A_{VD} Large-signal differential voltage amplification	$V_O = 1\text{ V to }2\text{ V}$		$R_L = 600\ \Omega^\dagger$	15	V/mV
			$R_L = 1\text{ M}\Omega^\dagger$	400	
r_{id} Differential input resistance			10^{12}		Ω
r_{ic} Common-mode input resistance			10^{12}		Ω
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$		6		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}$, $A_V = 1$		138		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$		70		dB
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V}$, $V_{IC} = 0$, No load		96		dB
I_{DD} Supply current	$V_O = 0$, No load		850		μA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

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CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	27 28
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	29, 30 31
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THD + N	Total harmonic distortion plus noise	vs Frequency	46
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	47 48
	Gain margin	vs Load capacitance	49, 50
ϕ_m	Phase margin	vs Frequency vs Load capacitance	21, 22 51, 52
B_1	Unity-gain bandwidth	vs Load capacitance	53, 54

TYPICAL CHARACTERISTICS

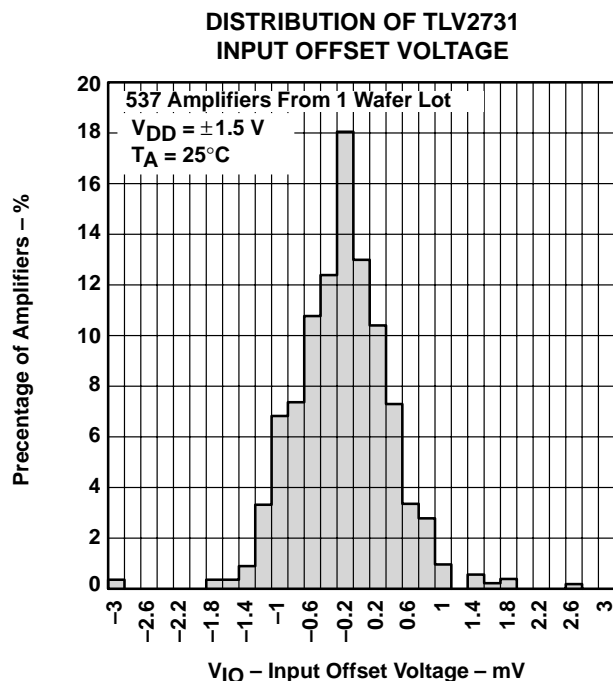


Figure 1

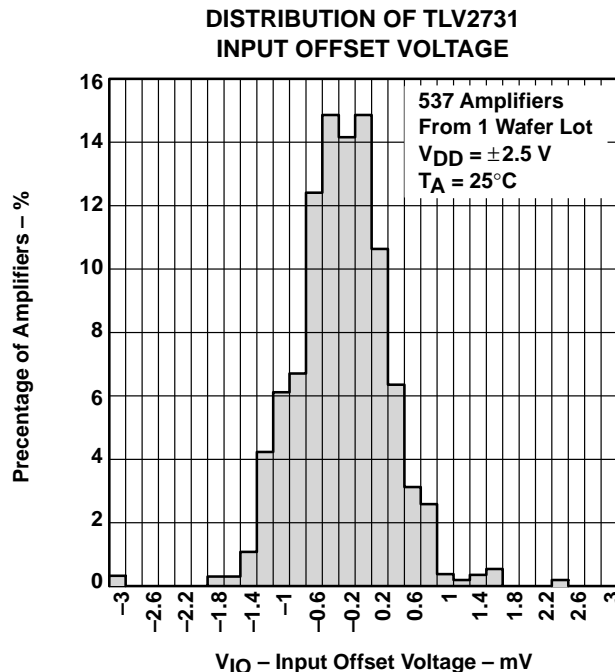


Figure 2

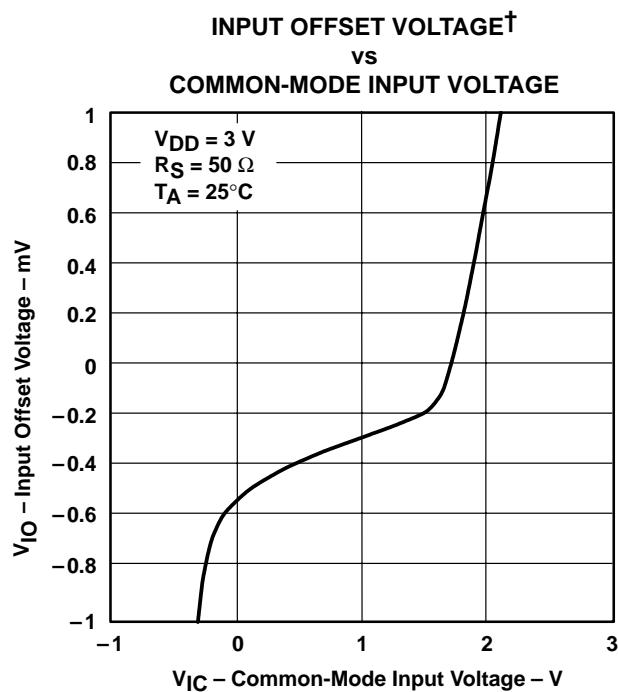


Figure 3

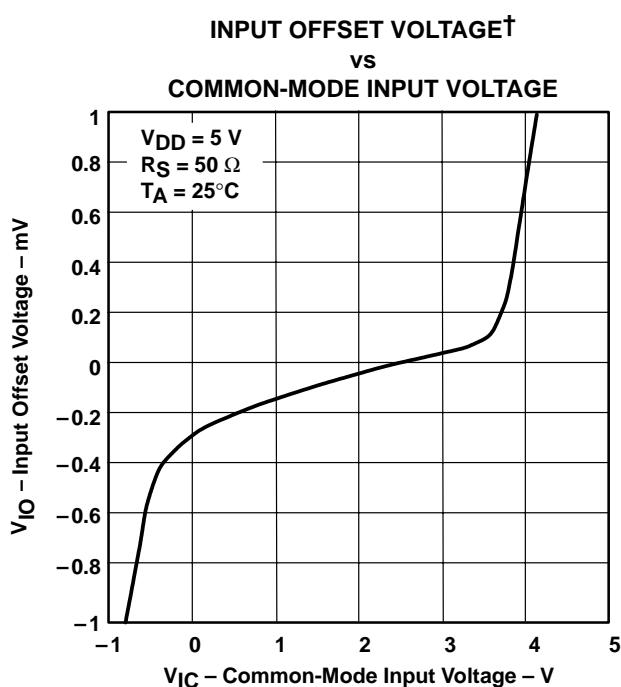


Figure 4

† For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

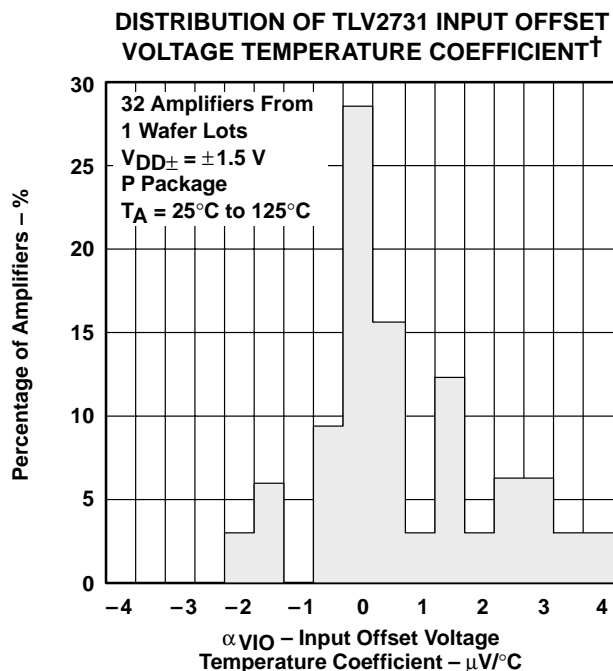


Figure 5

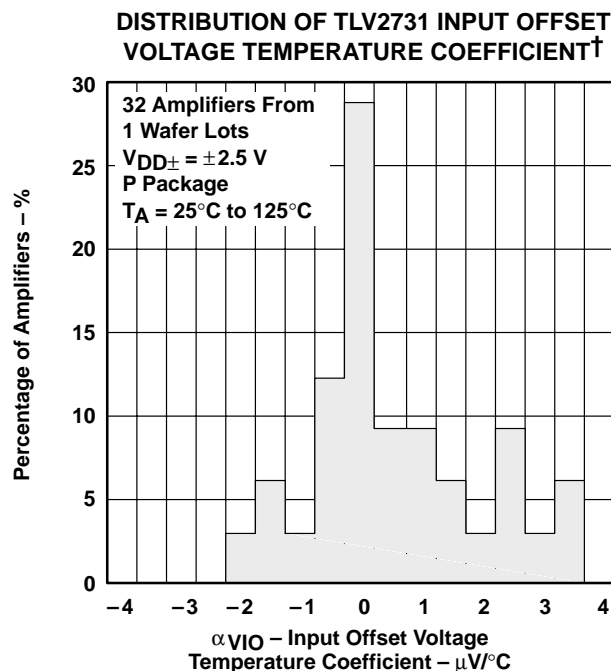


Figure 6

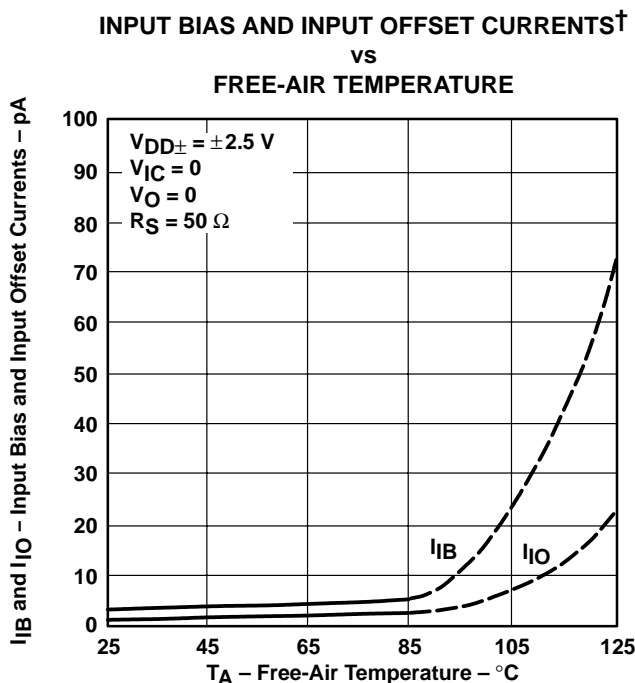


Figure 7

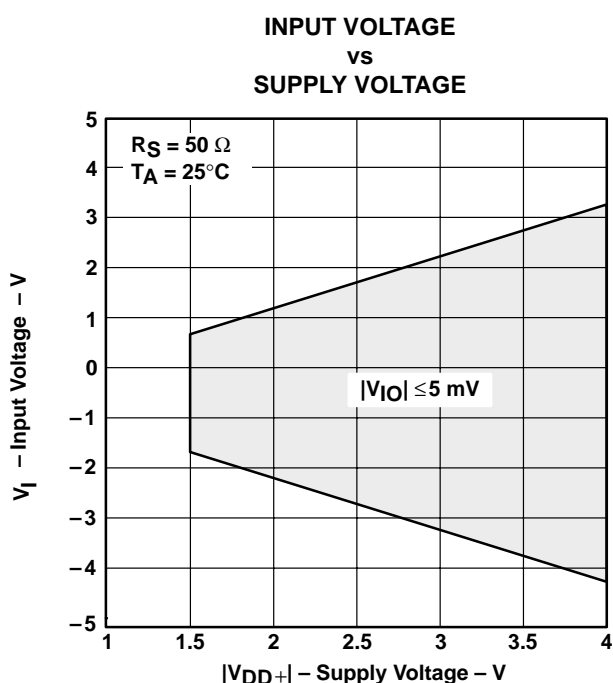


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

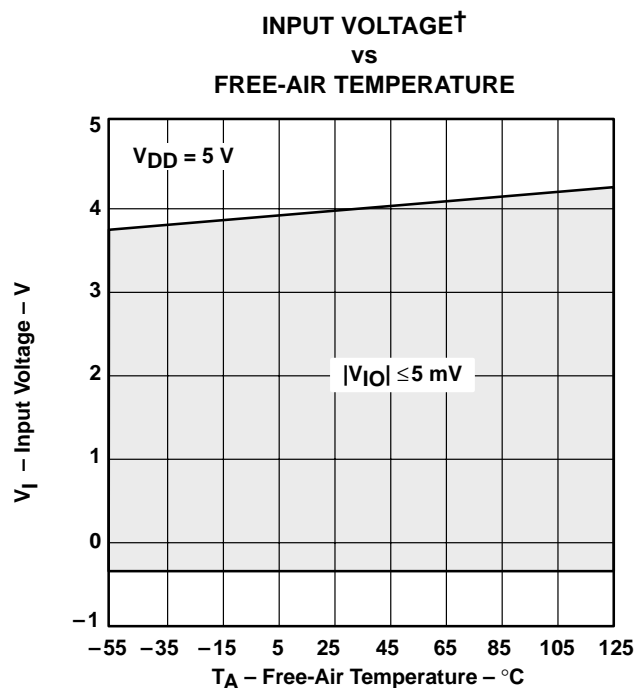


Figure 9

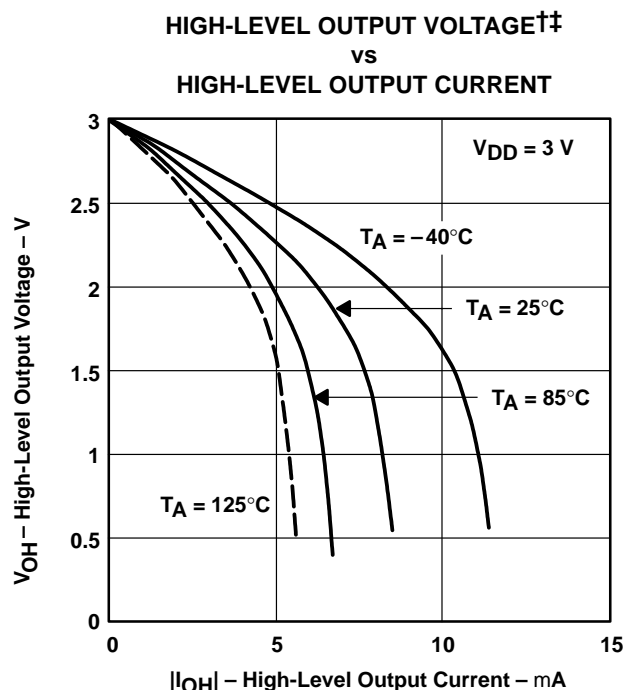


Figure 10

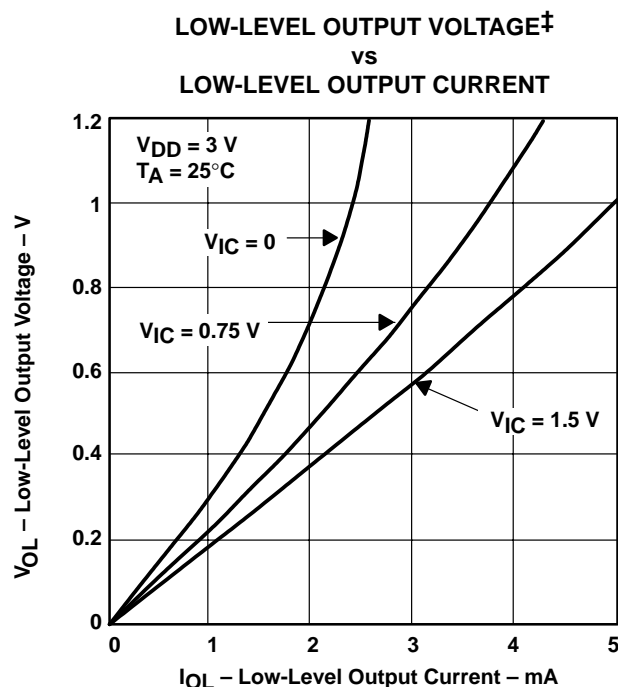


Figure 11

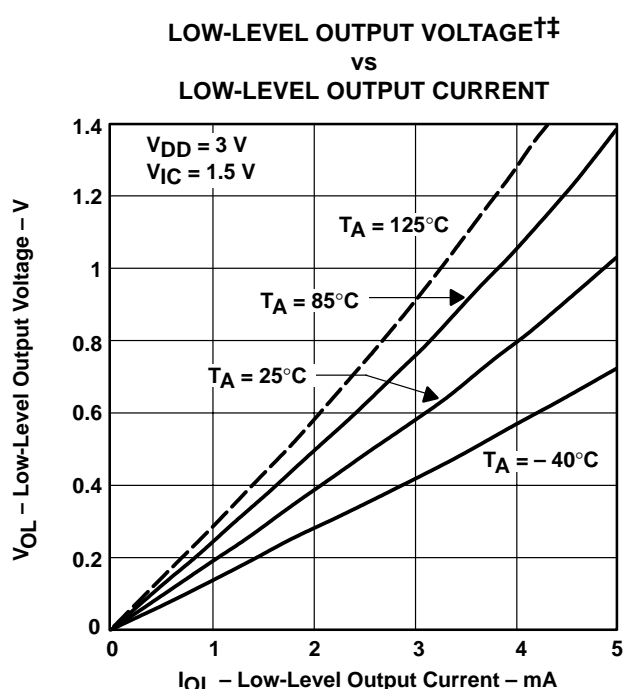


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

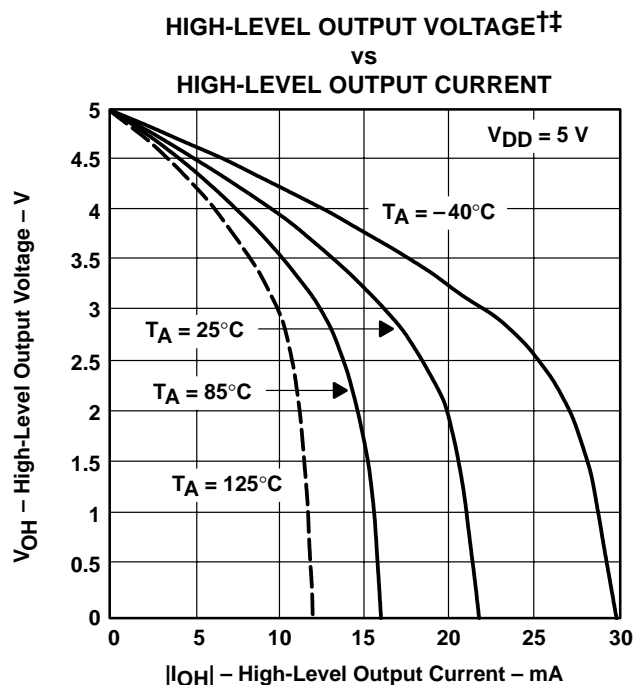


Figure 13

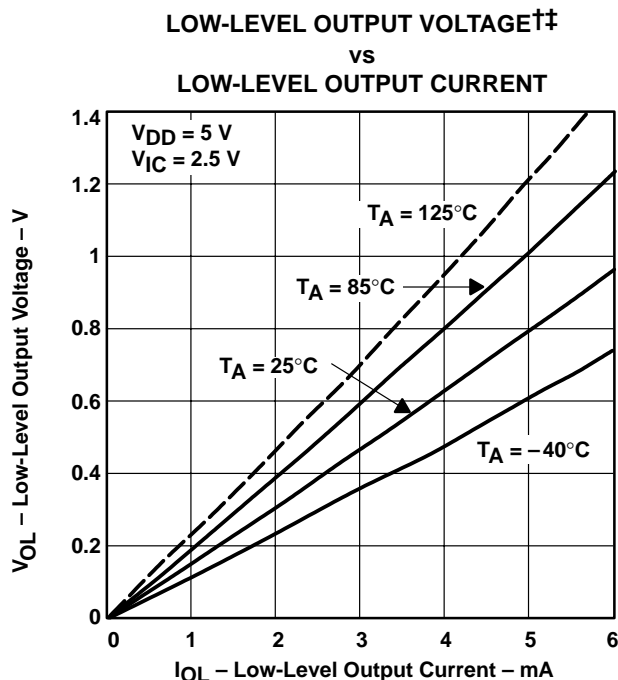


Figure 14

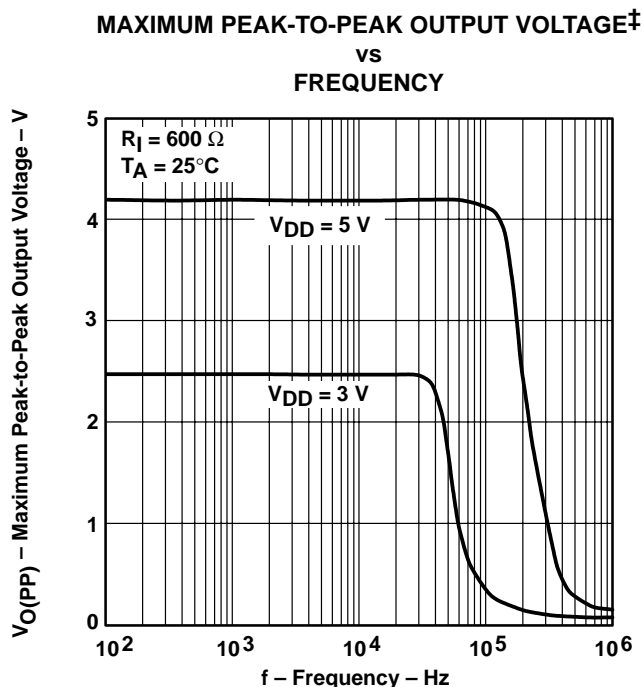


Figure 15

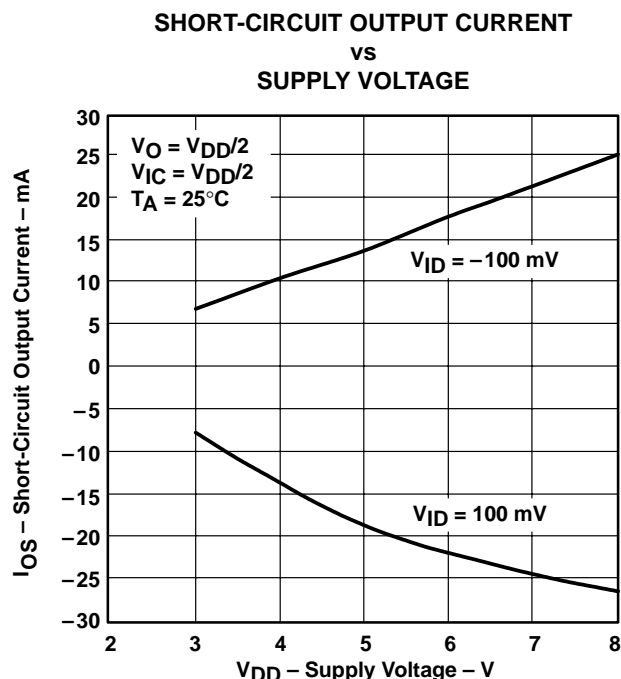
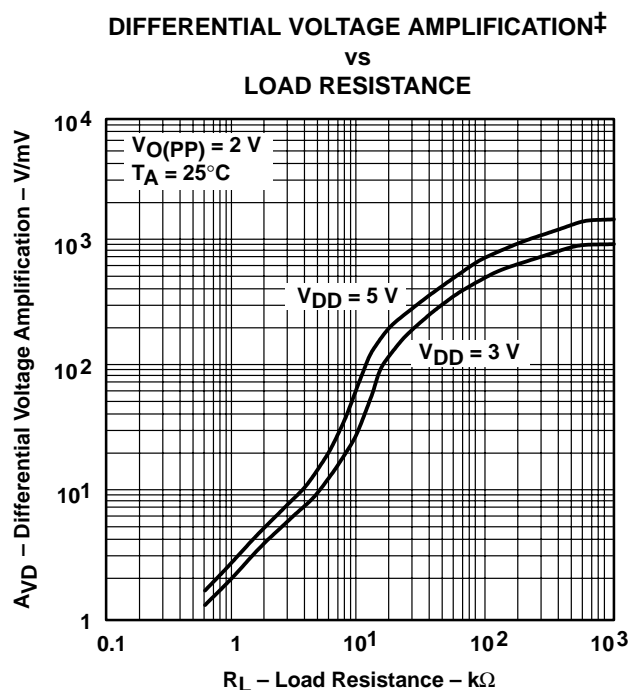
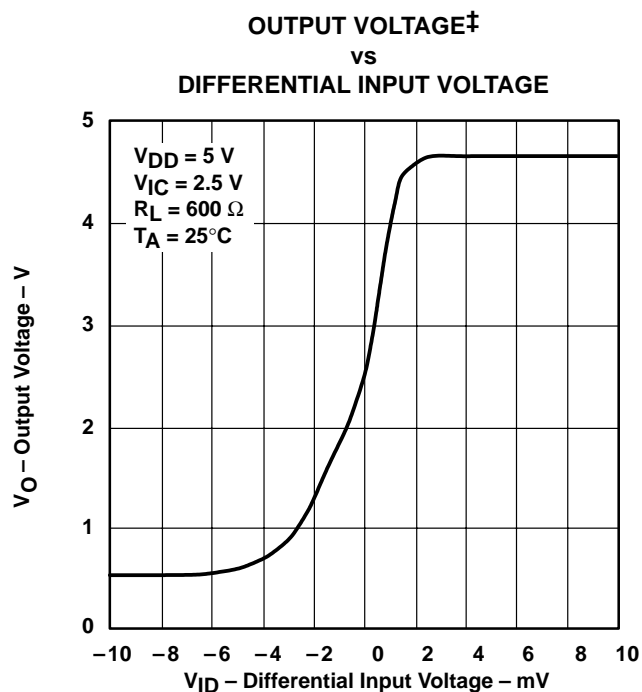
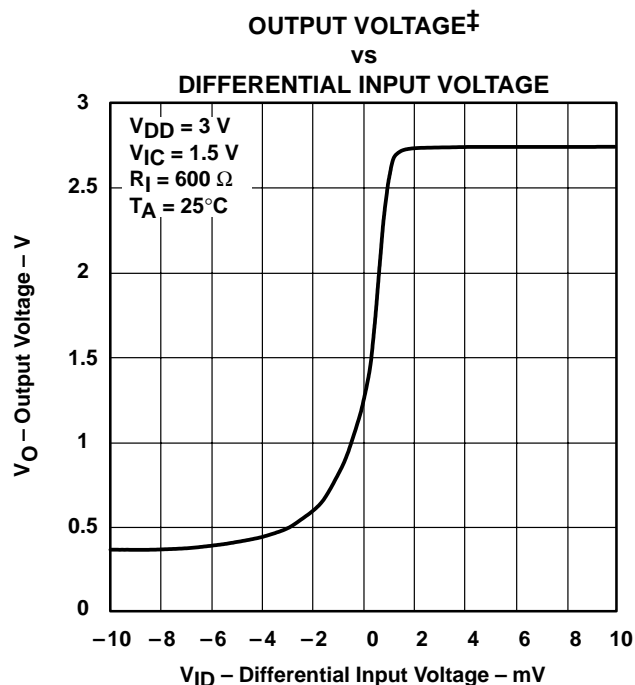
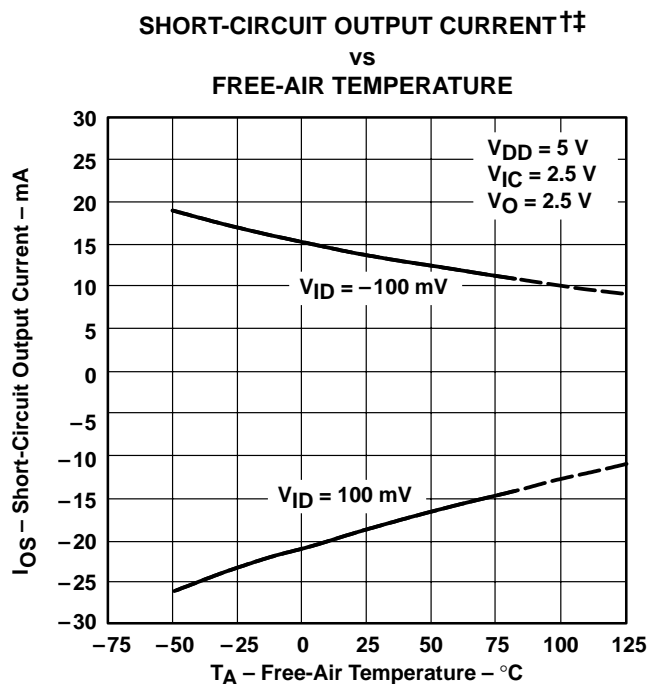


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†

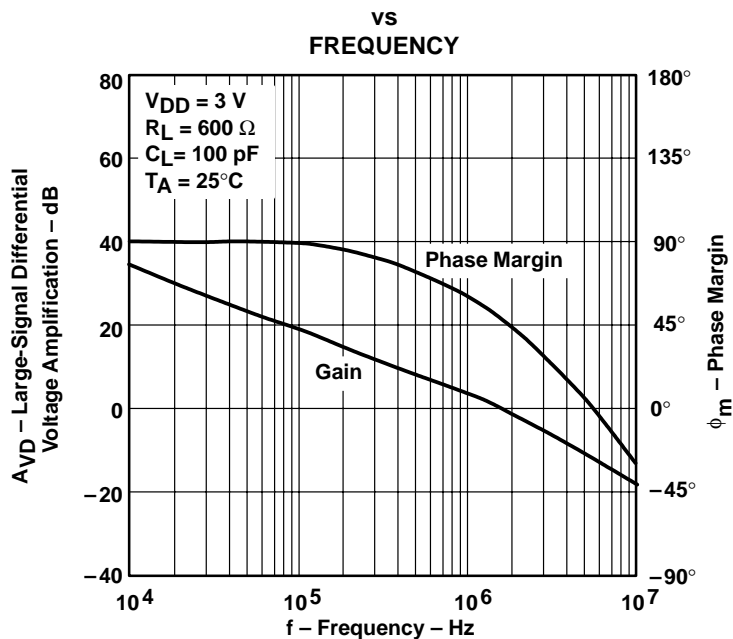


Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†

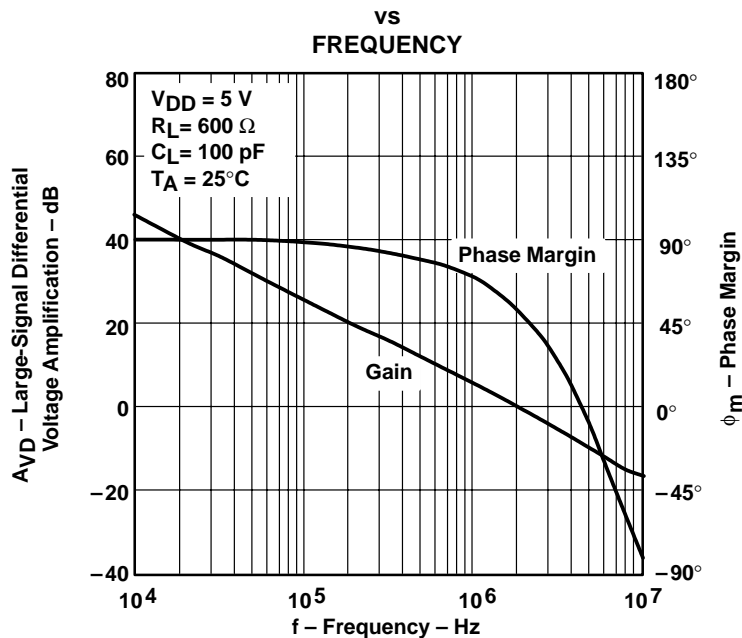


Figure 22

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

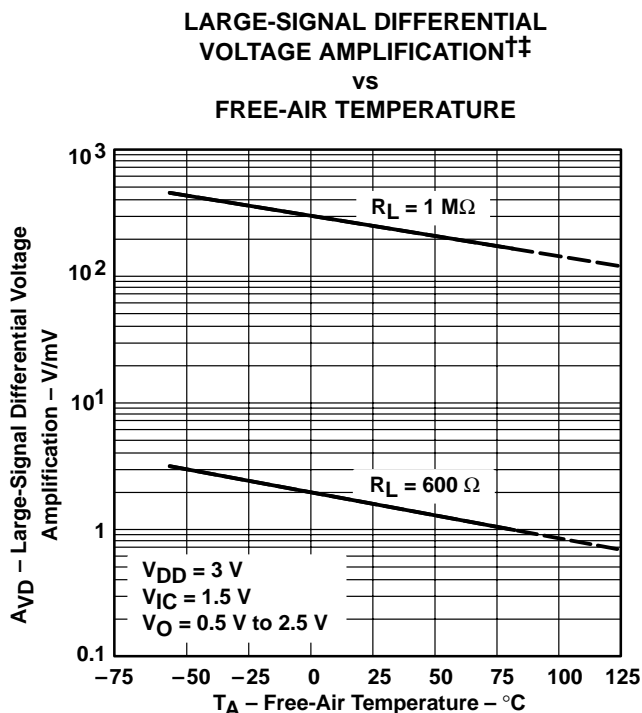


Figure 23

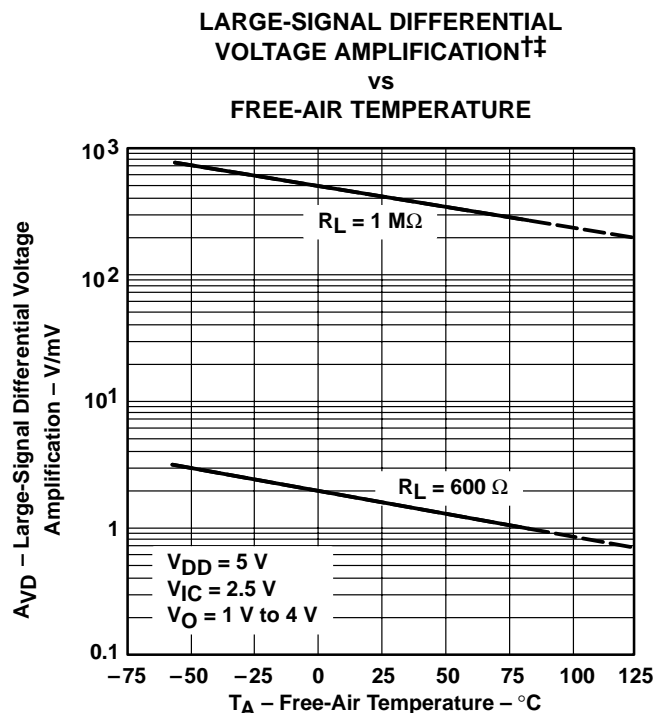


Figure 24

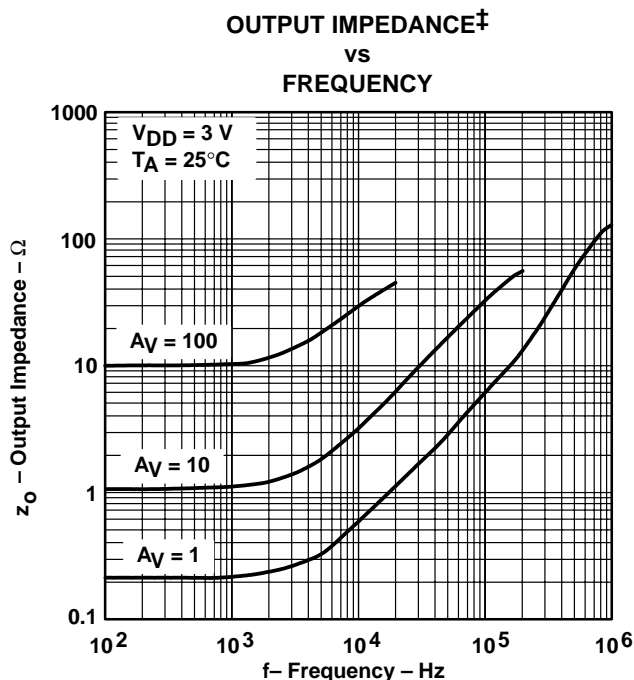


Figure 25

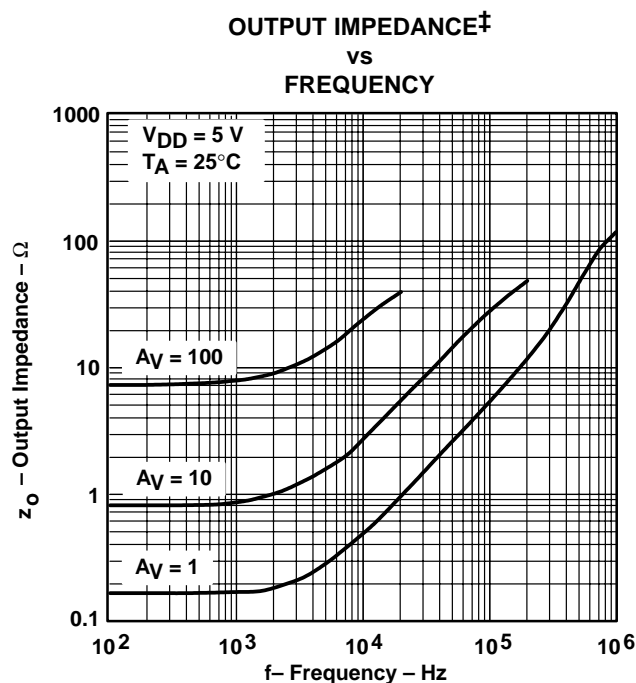


Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

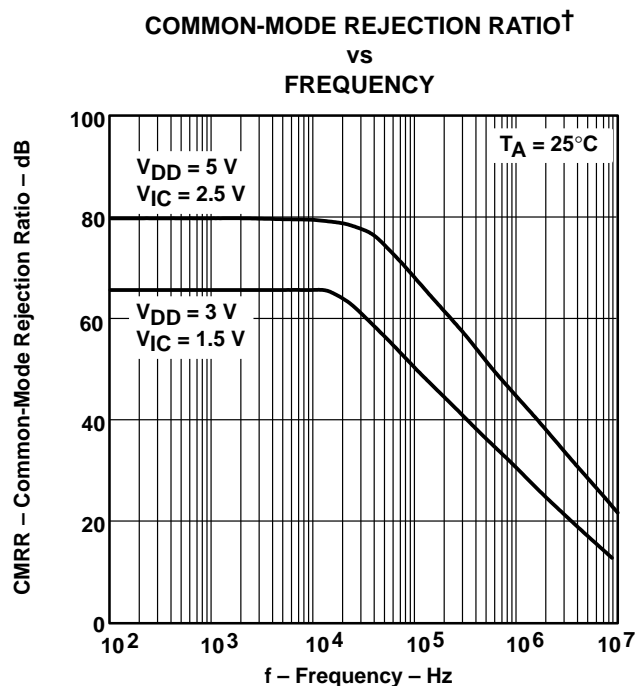


Figure 27

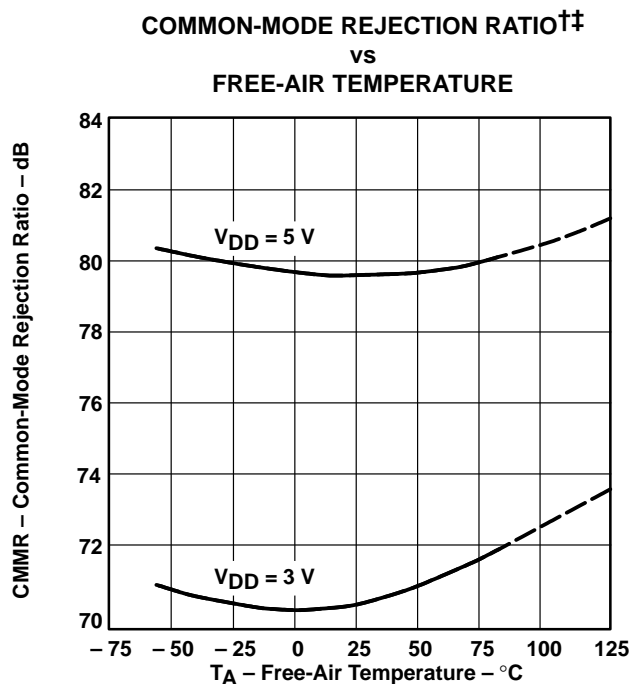


Figure 28

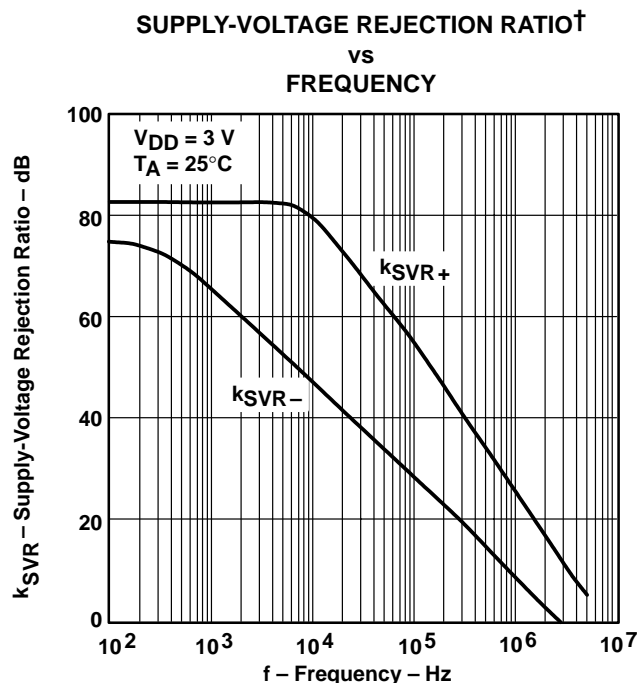


Figure 29

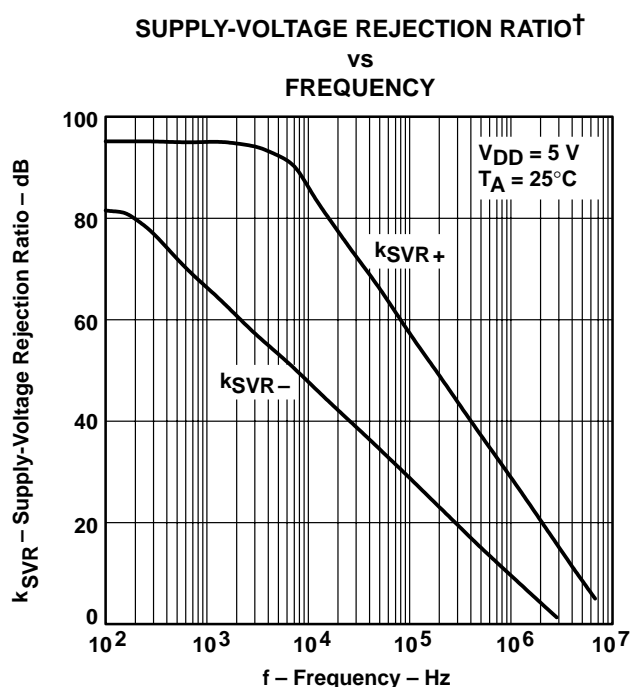


Figure 30

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

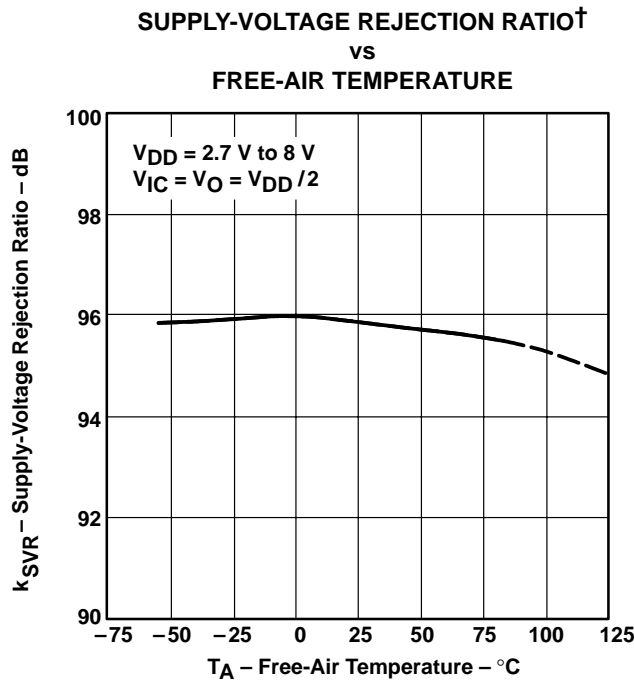


Figure 31

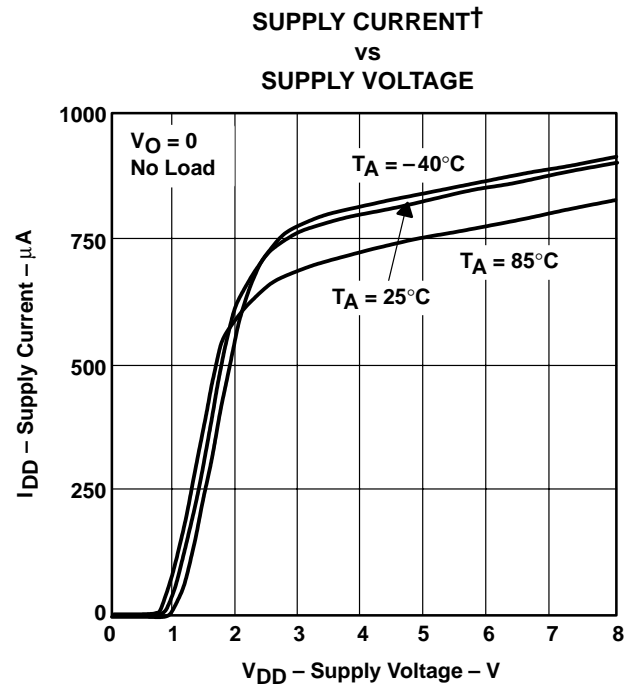


Figure 32

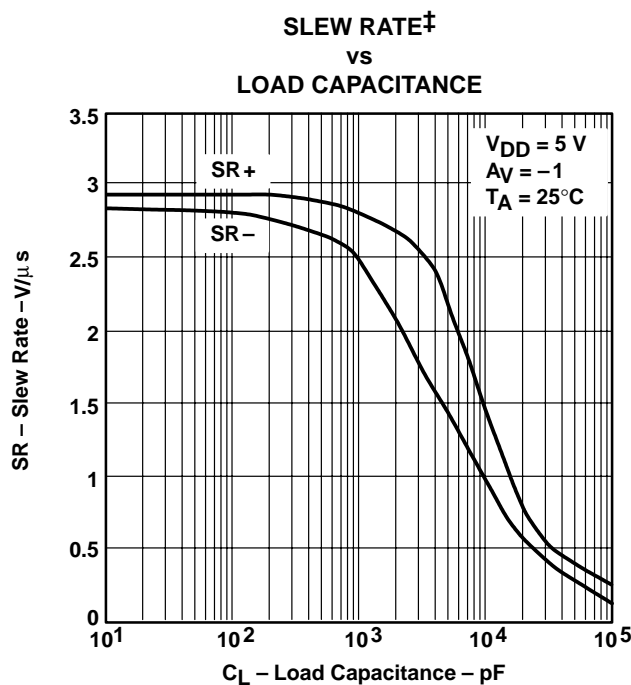


Figure 33

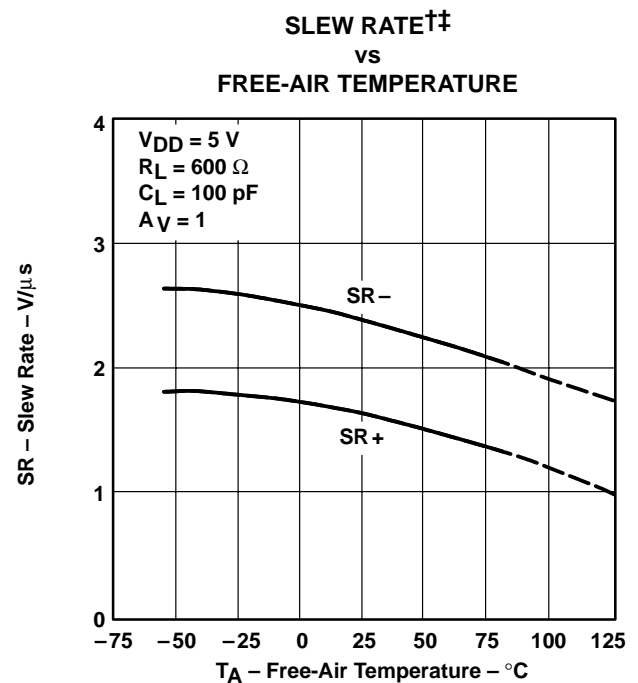


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

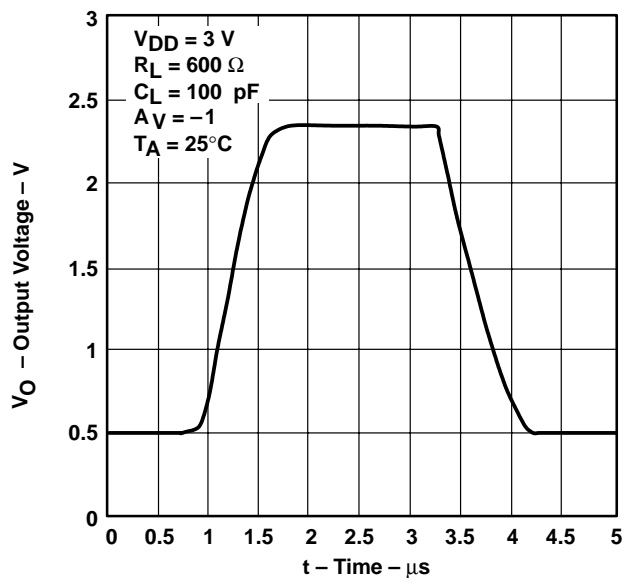


Figure 35

INVERTING LARGE-SIGNAL PULSE RESPONSE†

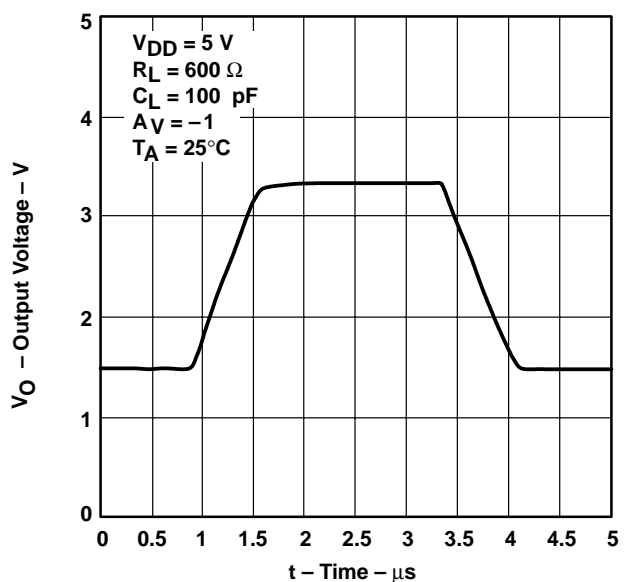


Figure 36

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

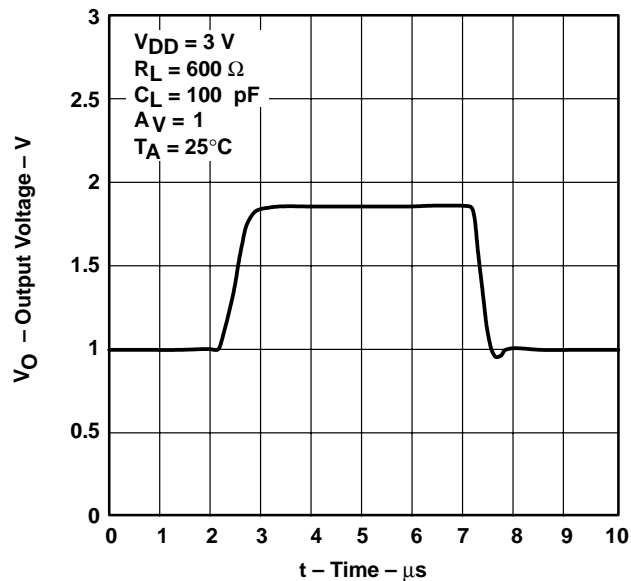


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

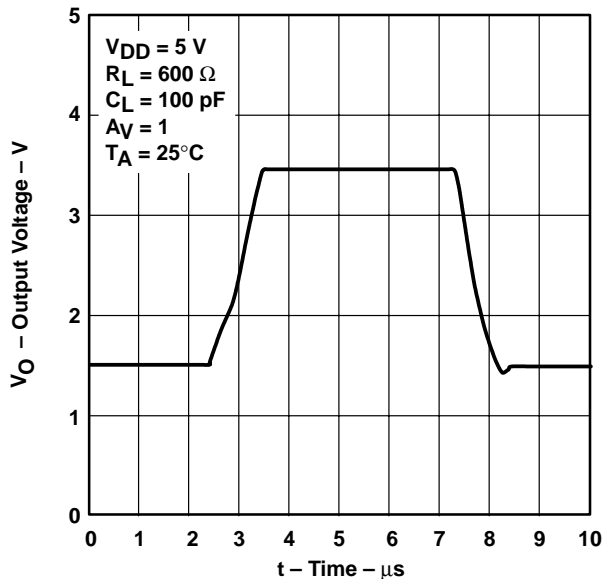


Figure 38

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

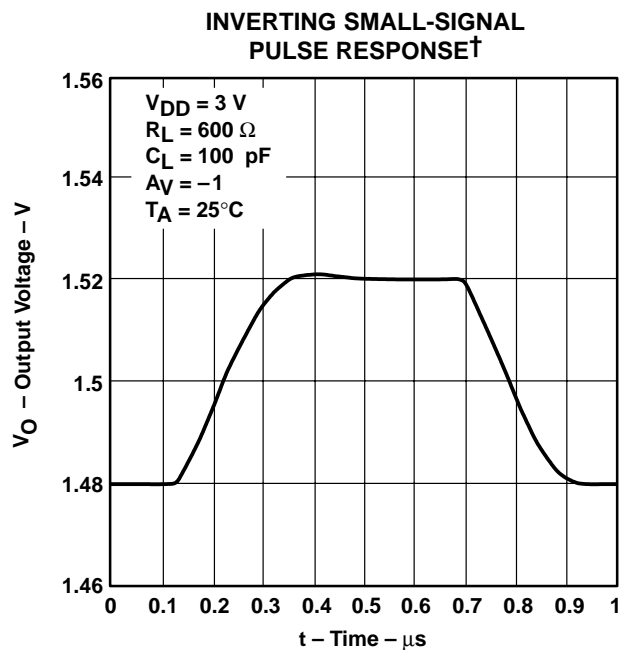


Figure 39

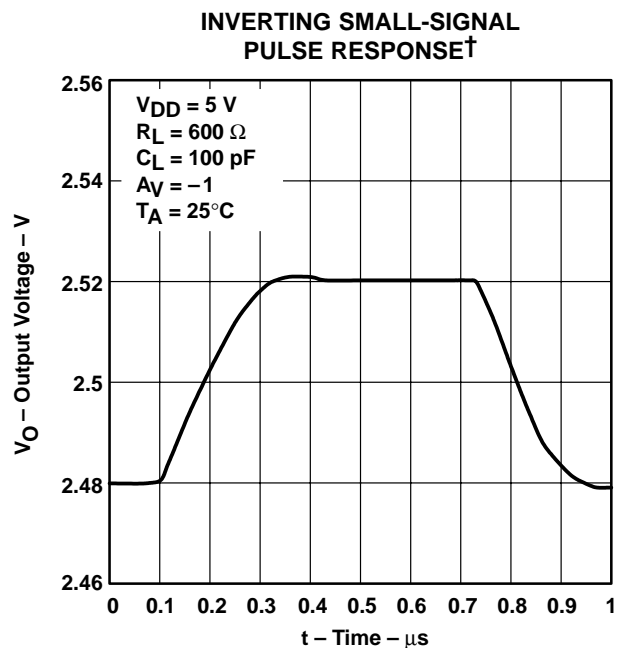


Figure 40

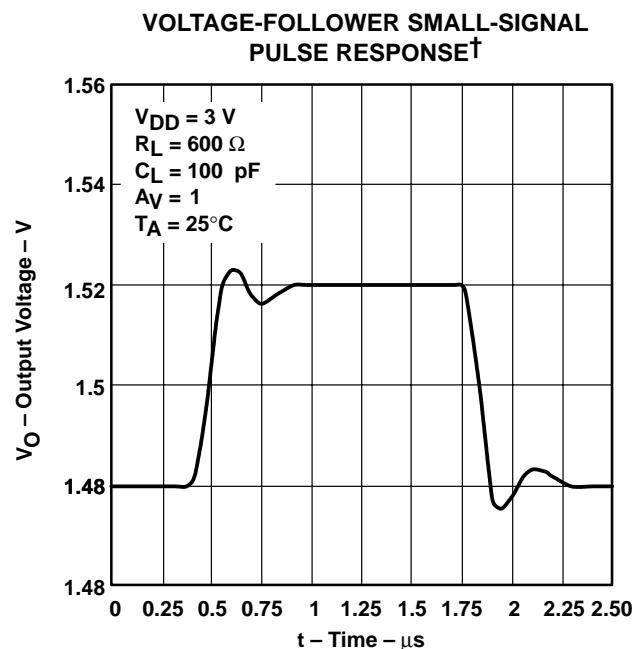


Figure 41

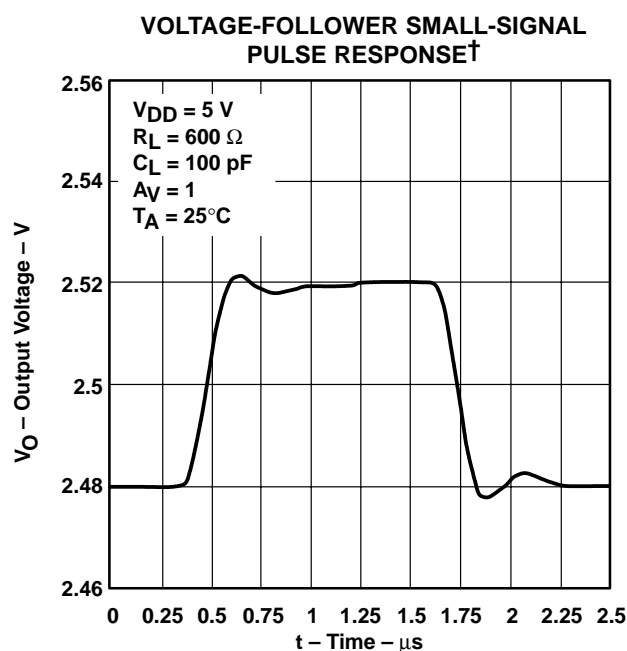


Figure 42

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

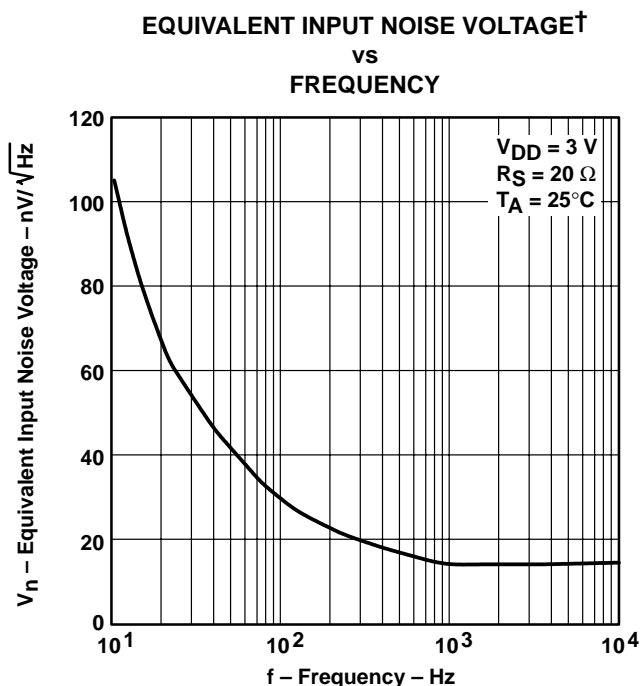


Figure 43

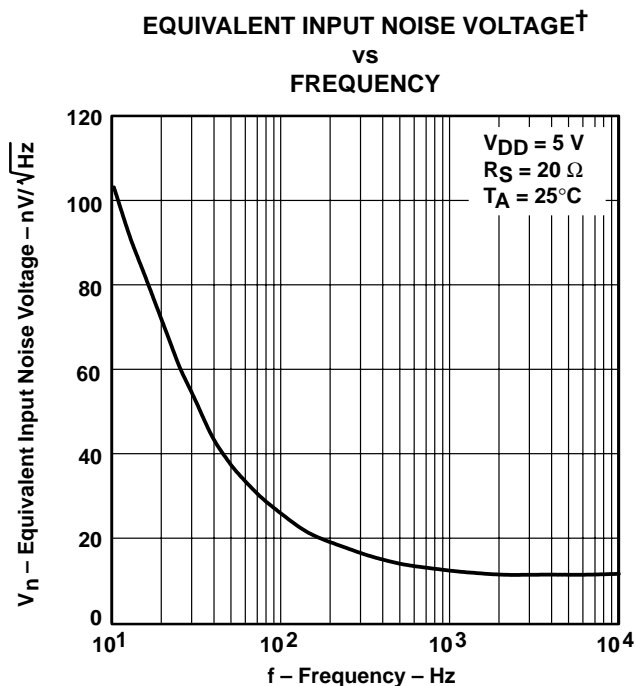


Figure 44

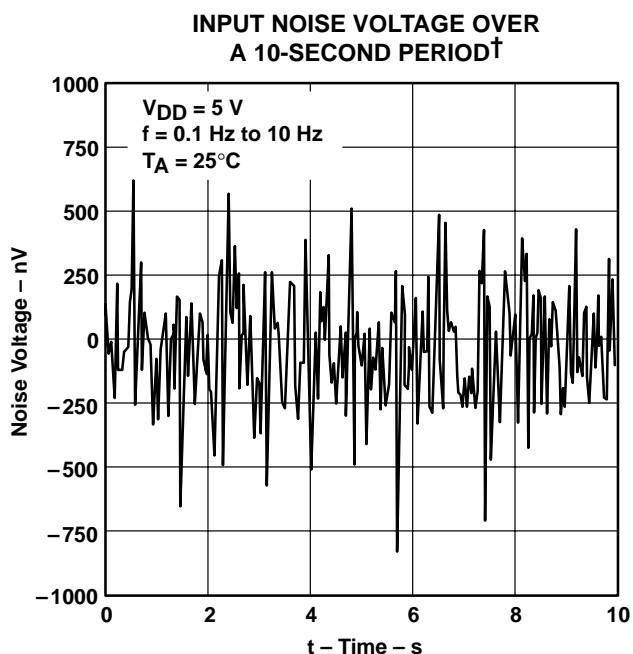


Figure 45

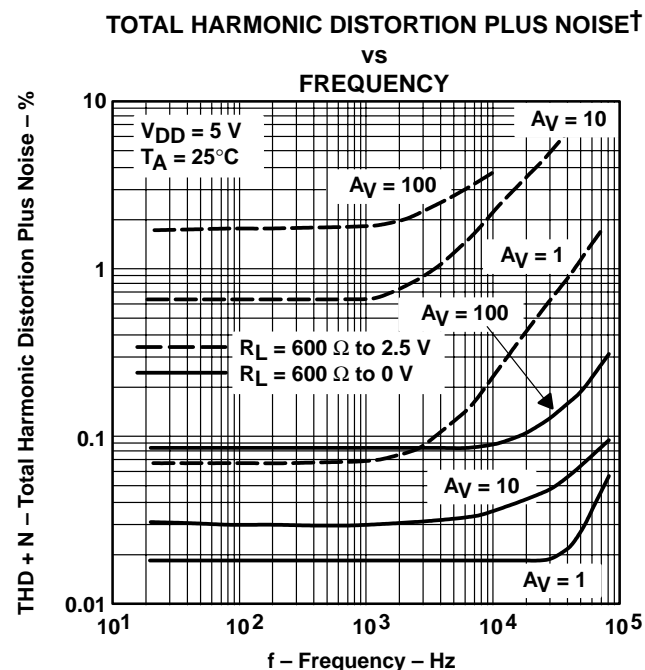


Figure 46

† For all curves where $V_{DD} = 5V$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3V$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

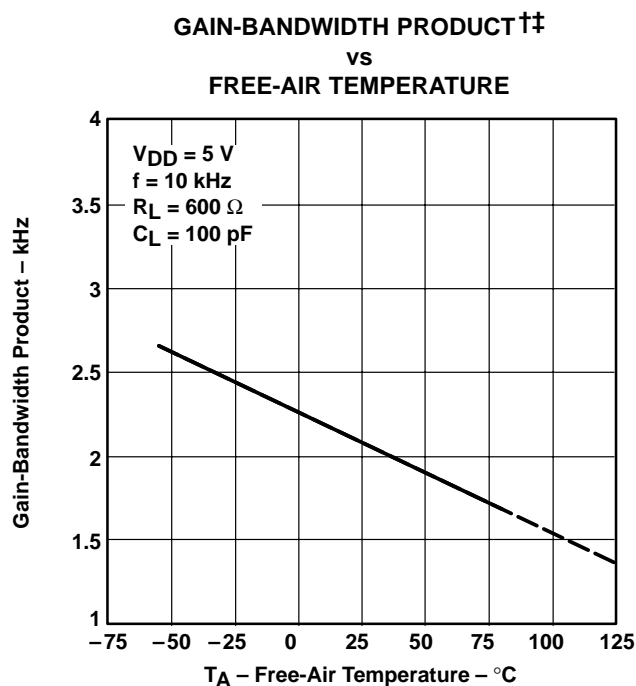


Figure 47

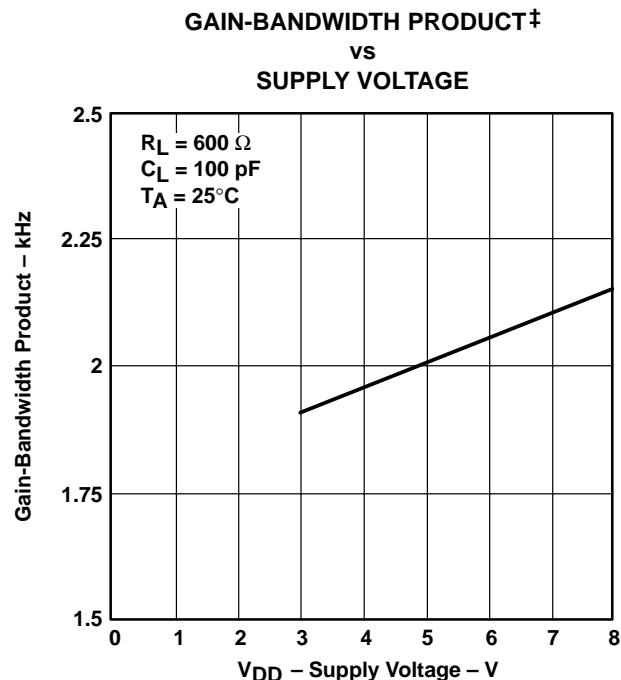


Figure 48

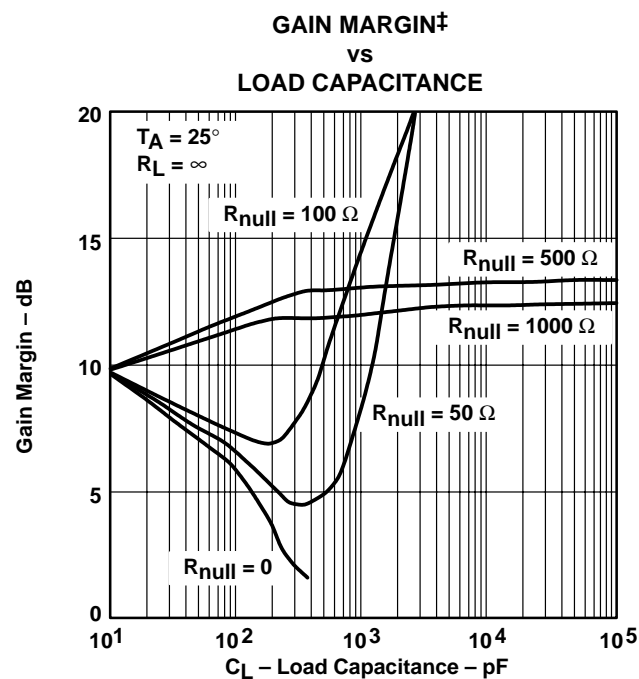


Figure 49

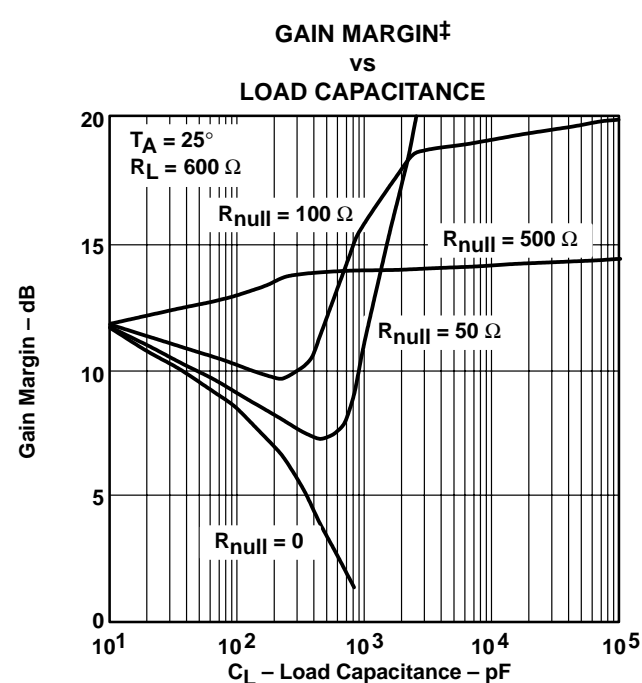


Figure 50

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

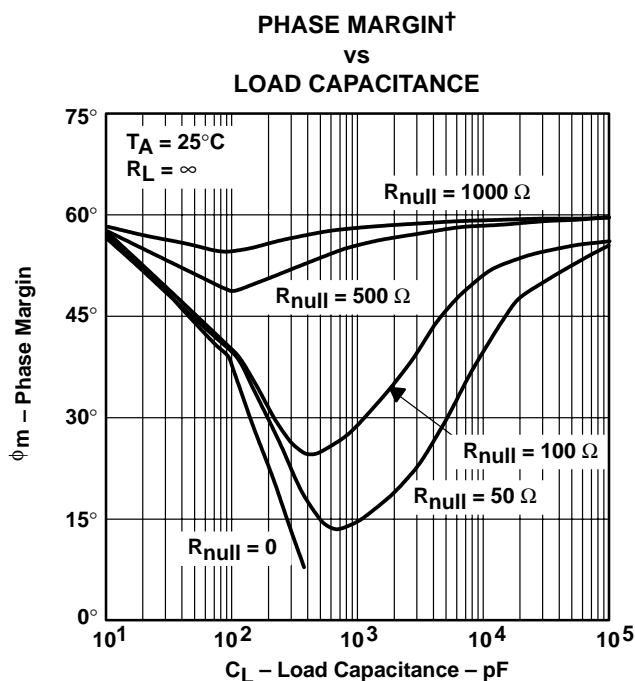


Figure 51

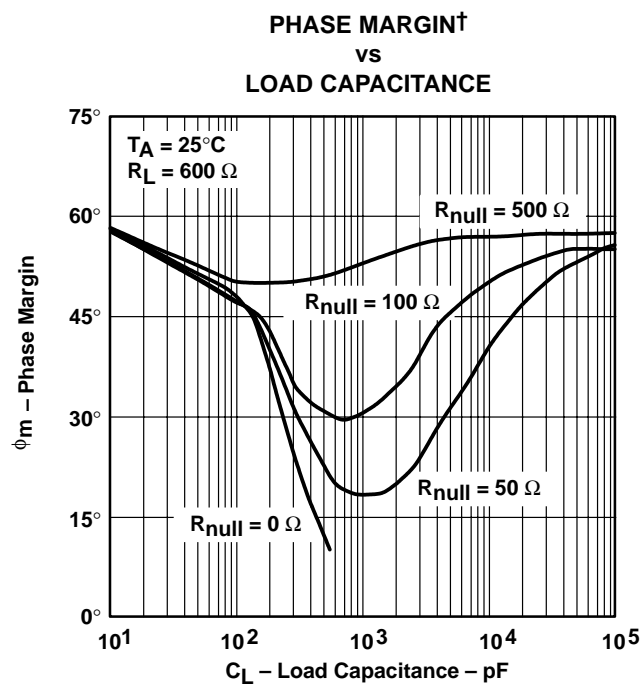


Figure 52

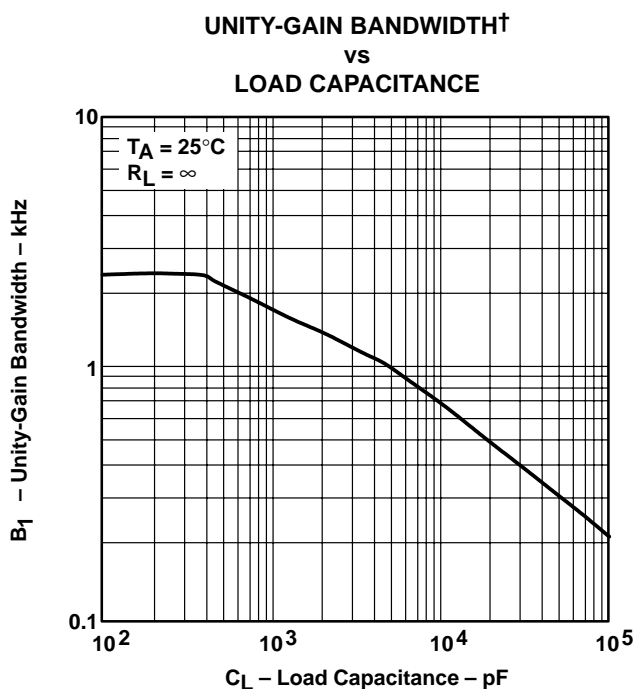


Figure 53

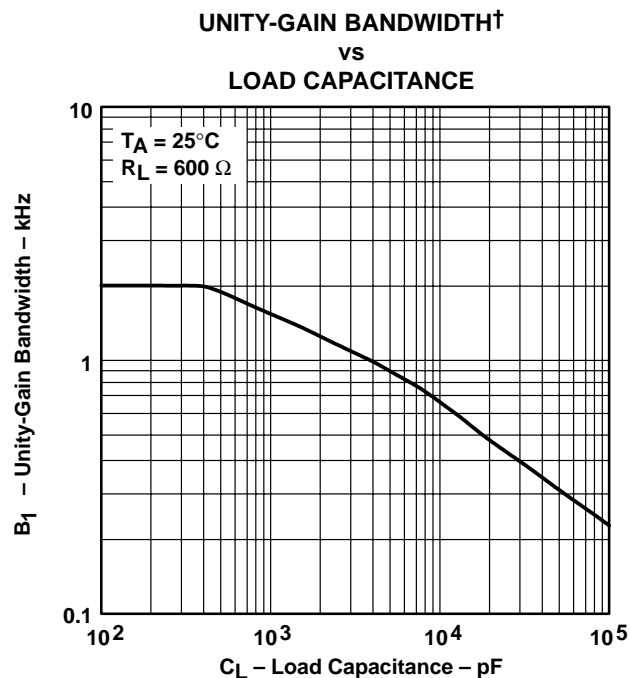


Figure 54

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

APPLICATION INFORMATION

driving large capacitive loads

The TLV2731 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 49 through Figure 54 illustrate its ability to drive loads greater than 100 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A small series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 49 through Figure 52 show the effects of adding series resistances of 50 Ω , 100 Ω , 500 Ω , and 1000 Ω . The addition of this series resistor has two effects: the first effect is that it adds a zero to the transfer function and the second effect is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} (2 \times \pi \times \text{UGBW} \times R_{null} \times C_L) \quad (1)$$

Where :

$\Delta\phi_{m1}$ = Improvement in phase margin

UGBW = Unity-gain bandwidth frequency

R_{null} = Output series resistance

C_L = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53 and Figure 54). To use equation 1, UGBW must be approximated from Figure 53 and Figure 54.

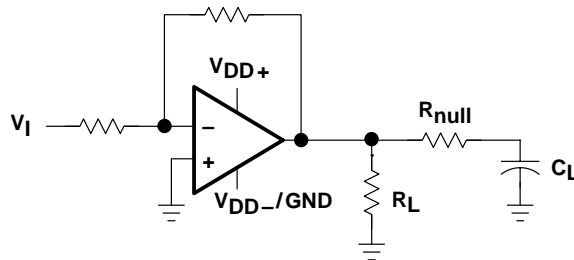


Figure 55. Series-Resistance Circuit

SLOS198A – AUGUST 1997 – REVISED MARCH 2001

macromodel information

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

```

RD1      60      11      3.183E3
RD2      60      12      3.183E3
R01       8       5       25
R02       7      99       25
RP        3       4      6.553E3
RSS       10     99      2.500E6
VAD       60      4       -.5
VB        9       0       DC 0
VC        3      53      DC .795
VE       54      4       DC .795
VLIM      7       8       DC 0
VLP       91      0      DC 12.4
VLN       0      92      DC 17.4
.MODEL DX D (IS=800.0E-18)
.MODEL JX PJF (IS=500.0E-15 BETA=2.939E-3
+ VTO=--.065)
.ENDS

```

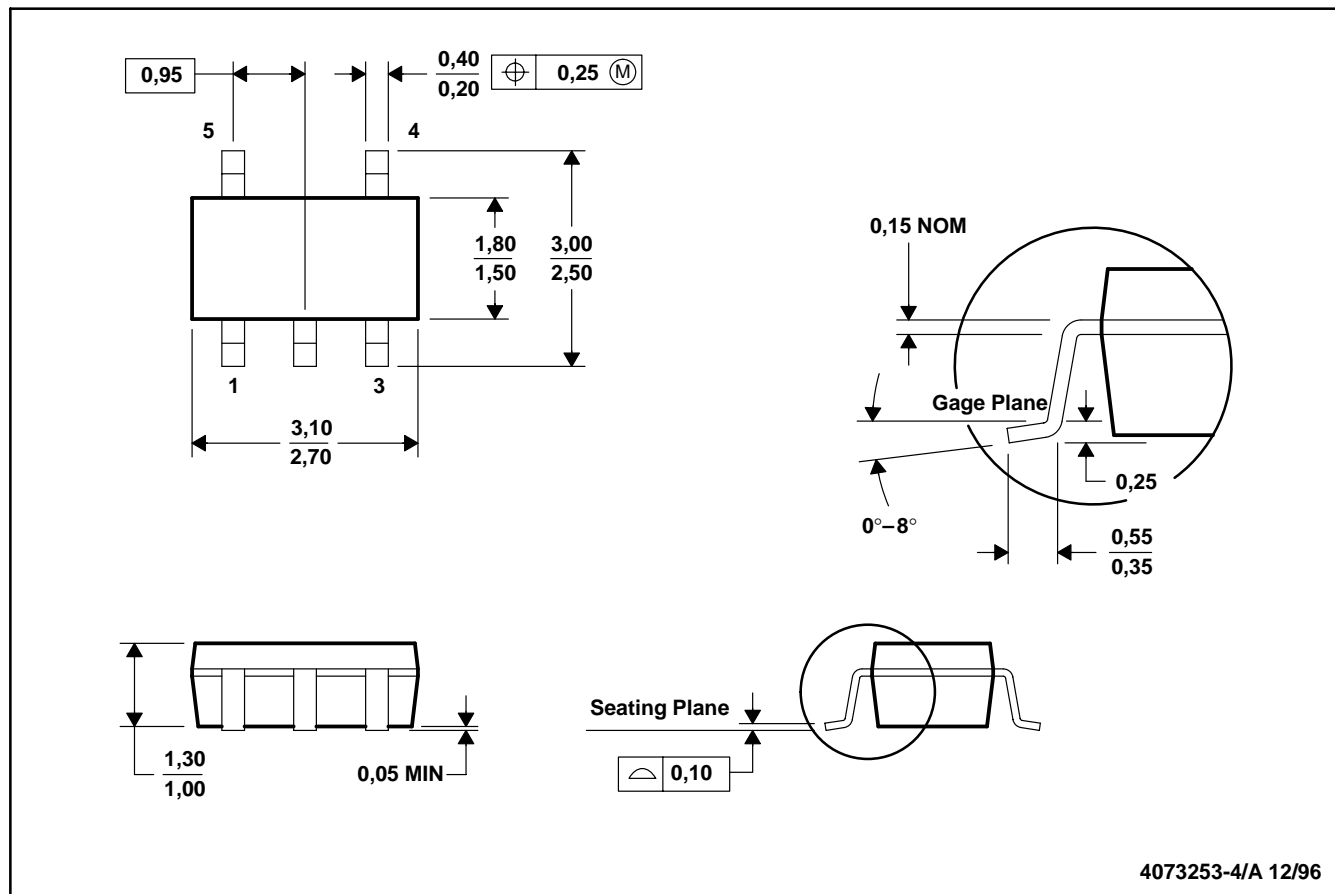
*P*Spice and *P*arts are trademark of MicroSim Corporation.



MECHANICAL INFORMATION

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions include mold flash or protrusion.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2731CDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VALC	Samples
TLV2731CDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		VALC	Samples
TLV2731IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VALI	Samples
TLV2731IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		VALI	Samples
TLV2731IDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		VALI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2731CDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2731CDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2731IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2731IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2731CDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2731CDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2731IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2731IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0

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