AMC1300 精密、±250mV 输入、增强型隔离放大器

1 特性

- ±250mV 输入电压范围，针对使用分流电阻器测量电流进行了优化
- 低失调电压误差和温漂：
  - AMC1300B：±0.2mV（最大值），±3μV/°C（最大值）
  - AMC1300：±2mV（最大值），±4μV/°C（最大值）
- 固定增益：8.2
- 超低增益误差和温漂：
  - AMC1300B：±0.3%（最大值），±50ppm/°C（最大值）
  - AMC1300：±1%（最大值），±50ppm/°C（典型值）
- 低非线性度和温漂：0.03%，1ppm/°C（典型值）
- 高侧 3.3V 工作电压 (AMC1300B)
- 系统级诊断 功能
- 安全相关认证：
  - 符合 DIN VDE V 0884-11: 2017-01 标准的 $7071V_{PK}$ 增强型隔离
  - 符合 UL1577 标准且长达 1 分钟的 $5000V_{RMS}$ 隔离
- AMC1300B 具有高 CMTI：140kV/μs（典型值）

2 应用

- 基于分流电阻器的电流感应，可用于：
  - 电机驱动器
  - 变频器
  - 不间断电源

3 说明

AMC1300 是一款隔离式精密放大器，此放大器的输出与输入电路由抗电磁干扰性能极强的隔离栅隔开。根据 VDE V 0884-11 和 UL1577 标准，该隔离栅经认证可提供高达 $5kV_{RMS}$ 的增强型电隔离。与隔离式电源结合使用时，该隔离放大器可将以不同共模电压电平运行的系统的各器件隔开，并防止较低电压器件损坏。

AMC1300 的输入经过优化，可直接连接至分流电阻器或其他低电压电平信号源。该器件性能出色，支持精确电流控制，从而可降低系统级功耗，尤其是在。AMC1300 的集成共模过压和高侧电源电压缺失检测器件 AMC1300 的集成共模过压和高侧电源电压缺失检测功能可简化系统级设计和诊断。

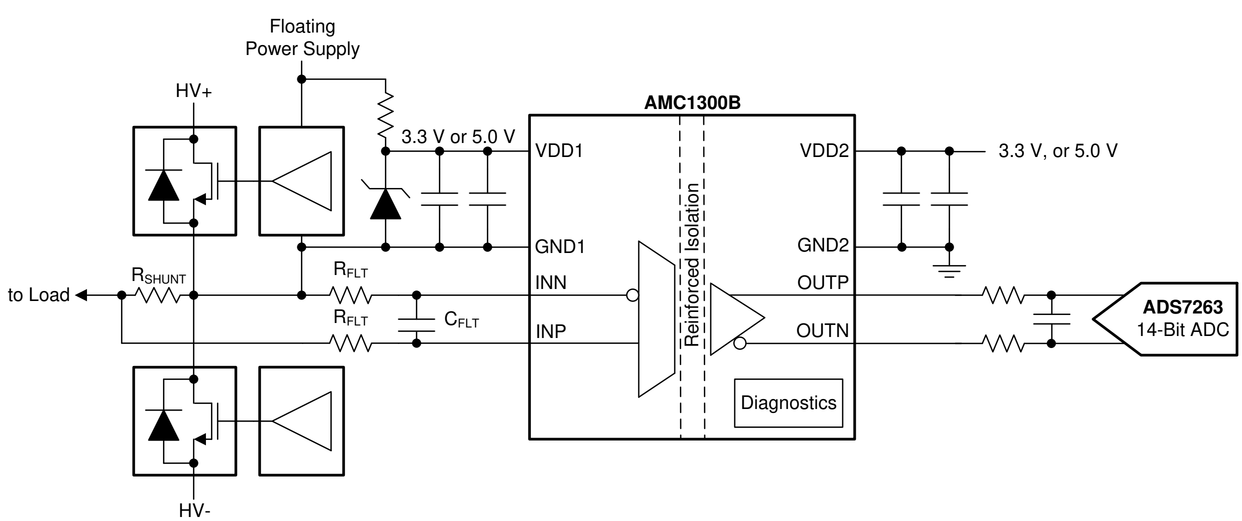
AMC1300 提供两种性能级别选项：AMC1300B 和 AMC1300，两者的额定扩展工业温度范围分别为 –55°C 至 +125°C 和 –40°C 至 +125°C。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
AMC1300	SOIC (8)	5.85mm × 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (June 2018) to Revision B	Page
• 已更改 将 *DIN V VDE V* 更改为 *DIN VDE V*（位于*安全相关认证* “特性” 项目符号	1
• Changed CLR and CPG parameter values from 9 mm to 8.5 mm in *Insulation Specifications* table	7
• Changed *Insulation Specifications* table per ISO standard	7
• Changed *Safety-Related Certification* table per ISO standard	8
• Changed P_S equation details in *Safety Limiting Values* table	8
• 已添加 *Input Offset Voltage vs Temperature* figure	13
• 已添加 *Common-Mode Rejection Ratio vs Input Frequency* figure	14
• 已添加 *Gain Error vs Temperature* figure	15
• 已添加 *Gain Error Drift Histogram* figure	15
• 已更改 *Do's and Don'ts* section title to *What to Do and What Not to Do*	25

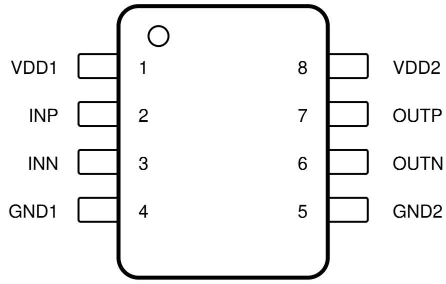
Changes from Original (May 2018) to Revision A	Page
• 已更改 *Reinforced Isolation Capacitor Lifetime Projection* figure	12

5 器件比较表

<table>
<tr><th colspan="2">参数</th><th>AMC1300B</th><th>AMC1300</th></tr>
<tr><td colspan="2">高侧电源电压，VDD1</td><td>3.0V 至 5.5V</td><td>4.5V 至 5.5V</td></tr>
<tr><td colspan="2">额定环境温度，T_A</td><td>–55°C 至 +125°C</td><td>–40°C 至 125°C</td></tr>
<tr><td rowspan="2">输入偏移电压，V_{OS}</td><td>4.5V ≤ VDD1 ≤ 5.5V</td><td rowspan="2">±0.2mV</td><td>±2mV</td></tr>
<tr><td>3.0V ≤ VDD1 ≤ 4.5V</td><td>不适用</td></tr>
<tr><td colspan="2">输入温漂 TCV_{OS}</td><td>±3µV/°C（最大值）</td><td>±4µV/°C（最大值）</td></tr>
<tr><td colspan="2">增益误差，E_G</td><td>±0.3%</td><td>±1%</td></tr>
<tr><td colspan="2">增益误差漂移，TCE_G</td><td>±15ppm/°C（典型值），±50ppm/°C（最大值）</td><td>±50ppm/°C（典型值）</td></tr>
<tr><td colspan="2">共模瞬态抗扰度，CMTI</td><td>75kV/µs（最小值），140kV/µs（典型值）</td><td>15kV/µs（最小值），30kV/µs（典型值）</td></tr>
<tr><td colspan="2">输出带宽，BW</td><td>250kHz（最小值），310kHz（典型值）</td><td>170kHz（最小值），230kHz（典型值）</td></tr>
<tr><td colspan="2">INP、INN 至 OUTP、OUTN 信号延迟 (50% – 90%)</td><td>3µs（最大值）</td><td>3.4µs（最大值）</td></tr>
</table>

6 Pin Configuration and Functions

**DWV Package
8-Pin SOIC
Top View**



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	—	High-side power supply, 3.0 V to 5.5 V for the AMC1300B (4.5 V to 5.5 V for the AMC1300), relative to GND1. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
2	INP	I	Noninverting analog input
3	INN	I	Inverting analog input
4	GND1	—	High-side analog ground
5	GND2	—	Low-side analog ground
6	OUTN	O	Inverting analog output
7	OUTP	O	Noninverting analog output
8	VDD2	—	Low-side power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

7 Specifications

7.1 Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
Power-supply voltage	VDD1 to GND1	–0.3	6.5	V
	VDD2 to GND2	–0.3	6.5	
Input voltage	INP, INN	GND1 – 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1, AMC1300	4.5	5	5.5	V
		VDD1 to GND1, AMC1300B	3.0	5	5.5	
	Low-side power supply	VDD2 to GND2	3.0	3.3	5.5	V
ANALOG INPUTS						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±320		mV
V_{FSR}	Specified linear differential input full-scale	$V_{IN} = V_{INP} – V_{INN}$	–250		250	mV
	Absolute common-mode input voltage[1]	$(V_{INP} + V_{INN})$ / 2 to GND1	–2		VDD1	V
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN})$ / 2 to GND1	–0.16		VDD1 – 2.1	V
TEMPERATURE RANGE						
T_A	Specified ambient temperature	AMC1300	–40		125	°C
		AMC1300B	–55		125	

(1) Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.

7.4 Thermal Information

THERMAL METRIC[(1)]		AMC1300x DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	98.45	mW
		VDD1 = VDD2 = 3.6 V, AMC1300B only	56.52	
P_{D1}	Maximum power dissipation (high-side supply)	VDD1 = 5.5 V	53.90	mW
		VDD1 = 3.6 V, AMC1300B only	30.60	
P_{D2}	Maximum power dissipation (low-side supply)	VDD2 = 5.5 V	44.55	mW
		VDD2 = 3.6 V	25.92	

7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0105 mm)	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2121	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave); see 图 4	1500	V_{RMS}
		At DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7071	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8485	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.5\ V_{PP}$ at 1 MHz	~1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$ or 7000 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 62368-1: 2016-05, EN 62368-1: 2014, and IEC 62368-1: 2014	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 85.4°C/W, T_J = 150°C, T_A = 25°C, VDD1 = VDD2 = 5.5 V, see 图 2			266	mA
		$R_{\theta JA}$ = 85.4°C/W, T_J = 150°C, T_A = 25°C, VDD1 = VDD2 = 3.6 V, AMC1300B only, see 图 2			406	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 85.4°C/W, T_J = 150°C, T_A = 25°C, see 图 3			1463	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.

$P_S = I_S \times VDD1_{max} + I_S \times VDD2_{max}$, where $VDD1_{max}$ is the maximum high-side supply voltage and $VDD2_{max}$ is the maximum low-side supply voltage.

7.9 Electrical Characteristics

minimum and maximum specifications of the AMC1300 apply from T_A = –40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = GND1 = 0 V; minimum and maximum specifications of the AMC1300B apply from T_A = –55°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = GND1 = 0 V; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{CMov}	Common-mode overvoltage detection level		VDD1 – 2			V
	Hysteresis of common-mode overvoltage detection level			95		mV
V_{OS}	Input offset voltage(1)	AMC1300, initial, at T_A = 25°C, V_{INP} = V_{INN} = GND1	–2	±0.01	2	mV
		AMC1300B, initial, at T_A = 25°C, V_{INP} = V_{INN} = GND1	–0.2	±0.01	0.2	
TCV_{OS}	Input offset drift(1)	AMC1300	–4	±1.3	4	µV/°C
		AMC1300B	–3	±1	3	
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–100		dB
		f_{IN} = 10 kHz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–98		
C_{IN}	Single-ended input capacitance	INN = GND1, f_{IN} = 275 kHz		2		pF
C_{IND}	Differential input capacitance	f_{IN} = 275 kHz		1		pF
R_{IN}	Single-ended input resistance	INN = GND1		19		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IB}	Input bias current	INP = INN = GND1, I_{IB} = (I_{IBP} + I_{IBN}) / 2	–41	–30	–24	µA
TCI_{IB}	Input bias current drift			±1		nA/°C
I_{IO}	Input offset current			±5		nA

(1) The typical value includes one sigma statistical variation.

Electrical Characteristics (continued)

minimum and maximum specifications of the AMC1300 apply from T_A = –40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = GND1 = 0 V; minimum and maximum specifications of the AMC1300B apply from T_A = –55°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = GND1 = 0 V; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
	Nominal gain			8.2		V/V
E_G	Gain error(1)	AMC1300, initial, at T_A = 25°C	–1%	0.4%	1%	
		AMC1300B, initial, at T_A = 25°C	–0.3%	±0.05%	0.3%	
TCE_G	Gain error drift(1)	AMC1300		±50		ppm/°C
		AMC1300B	–50	±15	50	
	Nonlinearity(1)		–0.03%	±0.01%	0.03%	
	Nonlinearity drift			±1		ppm/°C
THD	Total harmonic distortion	V_{IN} = 0.5 V, f_{IN} = 10 kHz, BW = 100 kHz		–85		dB
	Output noise	V_{INP} = V_{INN} = GND1, BW = 100 kHz		230		μV_{RMS}
SNR	Signal-to-noise ratio	V_{IN} = 0.5 V, f_{IN} = 1 kHz, BW = 10 kHz	80	85		dB
		V_{IN} = 0.5 V, f_{IN} = 10 kHz, BW = 100 kHz		72		
PSRR	Power-supply rejection ratio(2)	PSRR vs VDD1, at DC		–103		dB
		PSRR vs VDD1, 100-mV and 10-kHz ripple		–96		
		PSRR vs VDD2, at DC		–106		
		PSRR vs VDD2, 100-mV and 10-kHz ripple		–86		
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{FAILSAFE}$	Failsafe differential output voltage	V_{CM} ≥ V_{CMov} or VDD1 missing		–2.6	–2.5	V
BW	Output bandwidth	AMC1300	170	230		kHz
		AMC1300B	250	310		
R_{OUT}	Output resistance	On OUTP or OUTN		< 0.2		Ω
	Output short-circuit current			±13		mA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1 kV, AMC1300	15	30		kV/µs
		|GND1 – GND2| = 1 kV, AMC1300B	75	140		
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold voltage	VDD1 falling	1.75	2.53	2.7	V
IDD1	High-side supply current	AMC1300B only, 3.0 V ≤ VDD1 ≤ 3.6 V		6.3	8.5	mA
		4.5 V ≤ VDD1 ≤ 5.5 V		7.2	9.8	
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		5.3	7.2	mA
		4.5 V ≤ VDD2 ≤ 5.5 V		5.9	8.1	

(2) This parameter is output referred.

7.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time of OUTP, OUTN	See 图 1		1.3		µs
t_f	Fall time of OUTP, OUTN	See 图 1		1.3		µs
	INP, INN to OUTP, OUTN signal delay (50% – 10%)	AMC1300, unfiltered output, see 图 1		1.5	2.2	µs
		INP, INN to OUTP, OUTN signal delay (50% – 50%)		1	1.5	
	INP, INN to OUTP, OUTN signal delay (50% – 90%)	AMC1300, unfiltered output, see 图 1		2	2.7	µs
		AMC1300B, unfiltered output, see 图 1		1.6	2.1	
	INP, INN to OUTP, OUTN signal delay (50% – 90%)	AMC1300, unfiltered output, see 图 1		2.7	3.4	µs
		AMC1300B, unfiltered output, see 图 1		2.5	3	
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling		500		µs

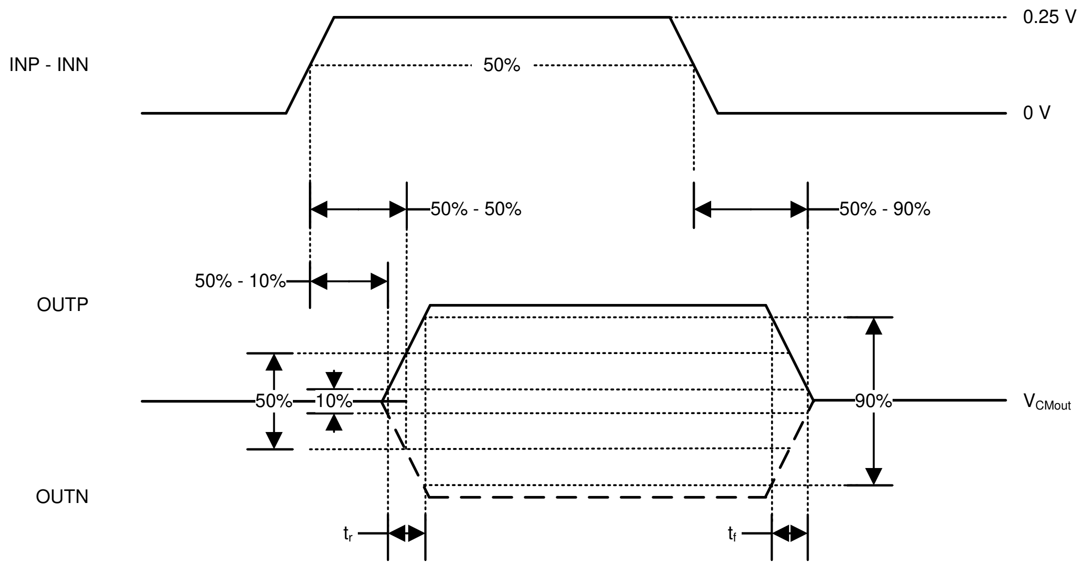


图 1. Rise, Fall, and Delay Time Waveforms

7.11 Insulation Characteristics Curves

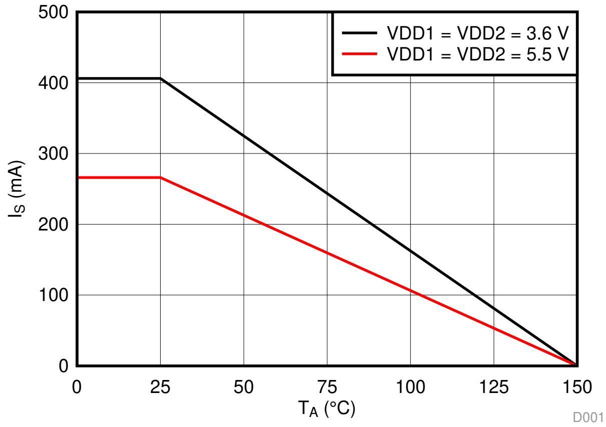


图 2. Thermal Derating Curve for Safety-Limiting Current per VDE

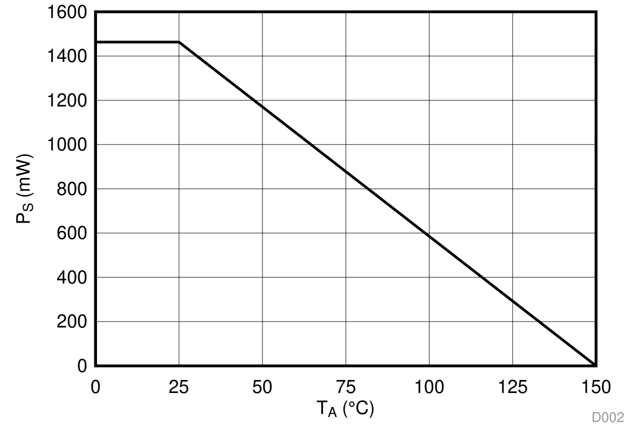
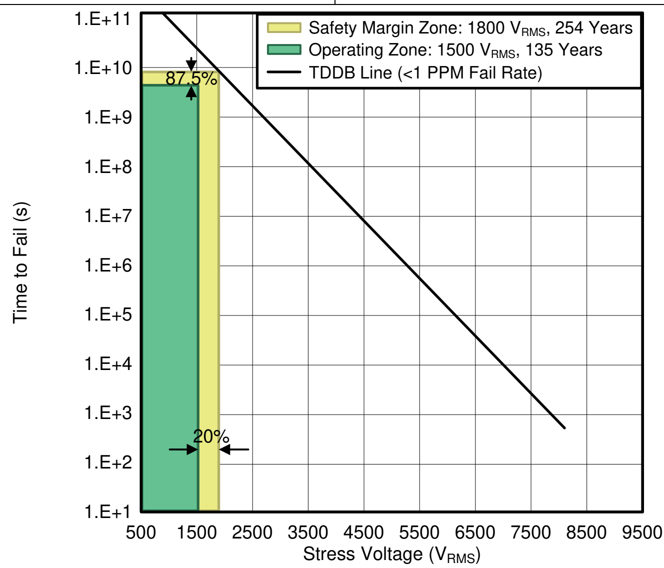


图 3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 year

图 4. Reinforced Isolation Capacitor Lifetime Projection

7.12 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

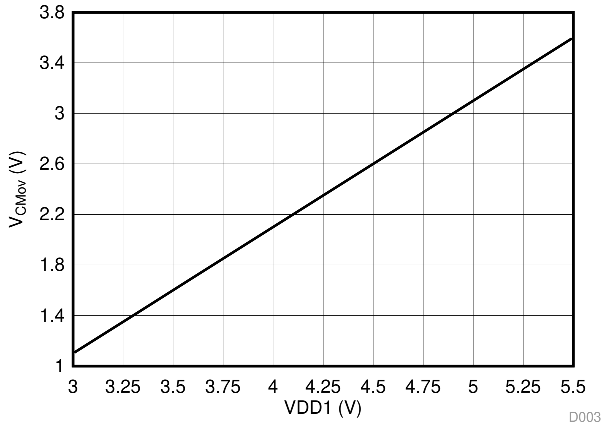
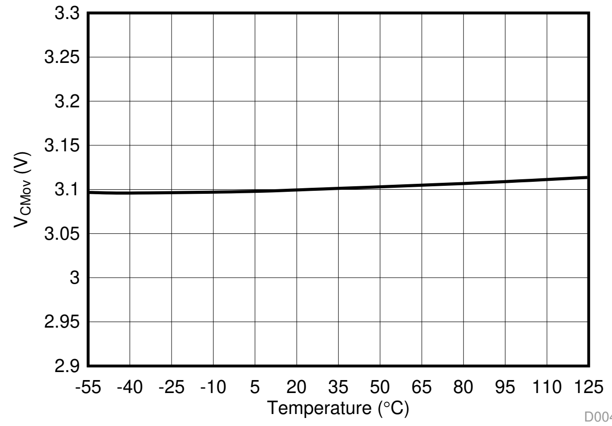
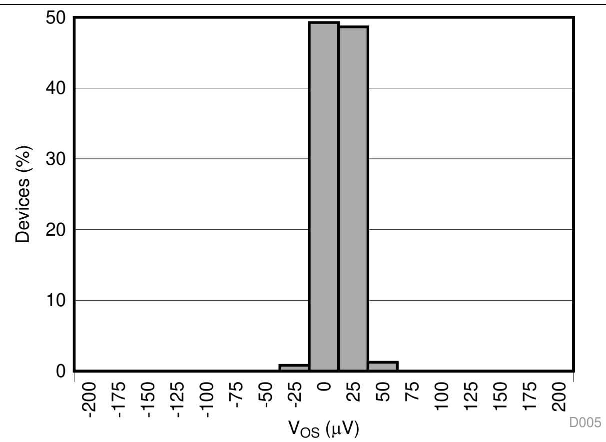


图 5. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage



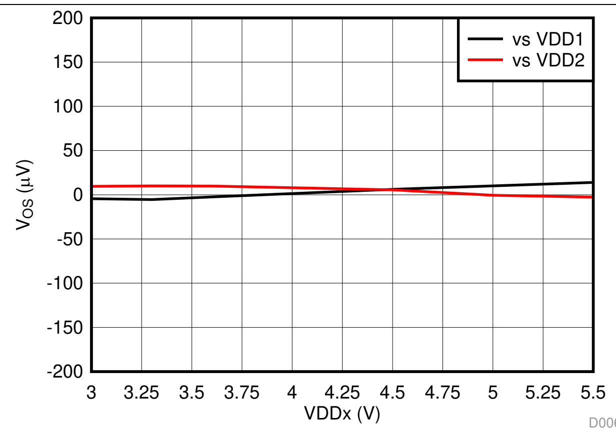
–55°C ≤ T_A < –40°C for AMC1300B only

图 6. Common-Mode Overvoltage Detection Level vs Temperature



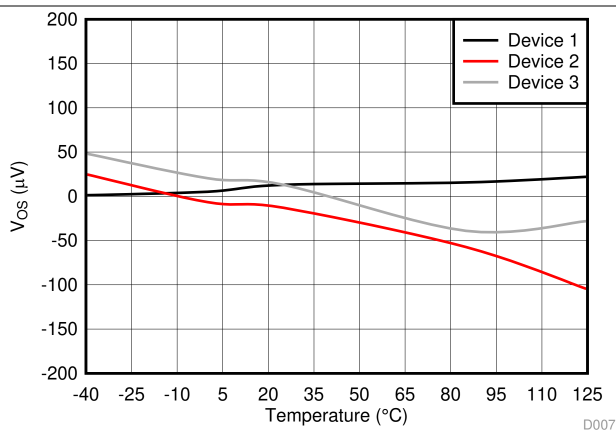
AMC1300B

图 7. Input Offset Voltage Histogram



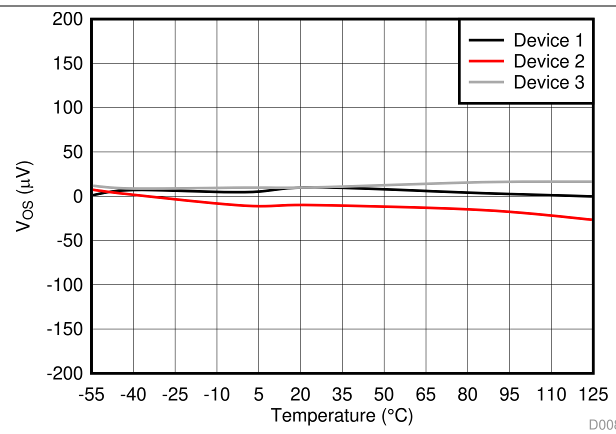
3 V ≤ VDD1 < 4.5 V for AMC1300B only

图 8. Input Offset Voltage vs Supply Voltage



AMC1300

图 9. Input Offset Voltage vs Temperature

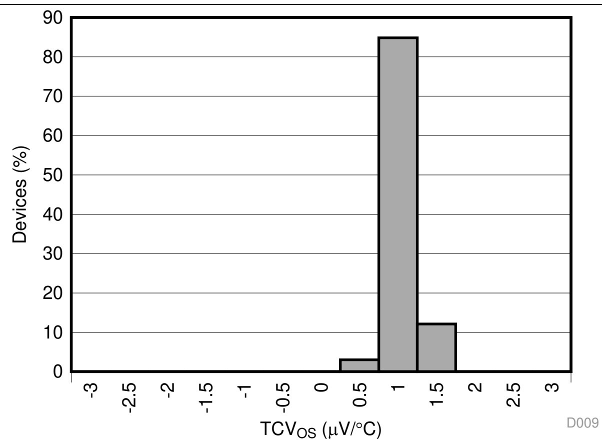


AMC1300B

图 10. Input Offset Voltage vs Temperature

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



AMC1300B

图 11. Input Offset Drift Histogram

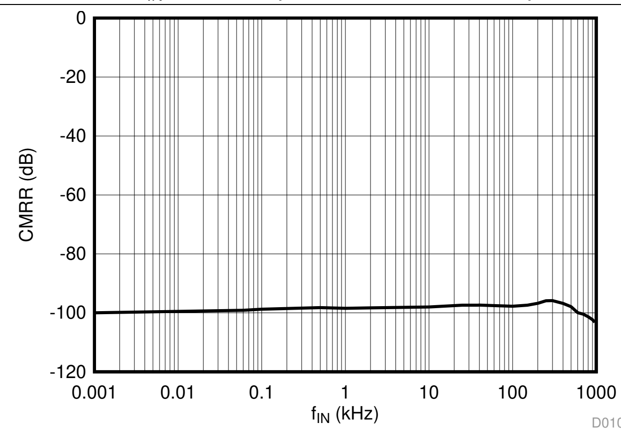
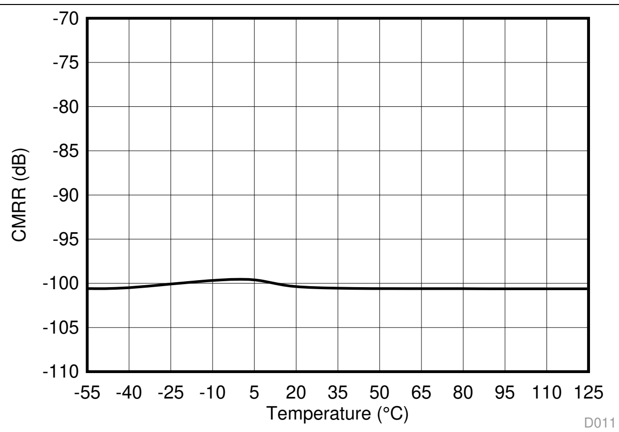


图 12. Common-Mode Rejection Ratio vs Input Frequency



–55°C ≤ T_A < –40°C for AMC1300B only

图 13. Common-Mode Rejection Ratio vs Temperature

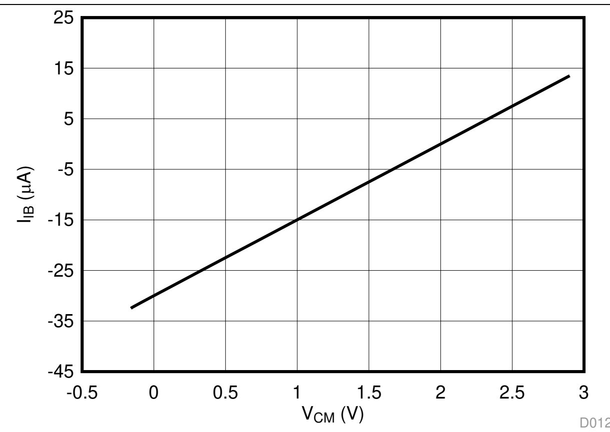


图 14. Input Bias Current vs Common-Mode Input Voltage

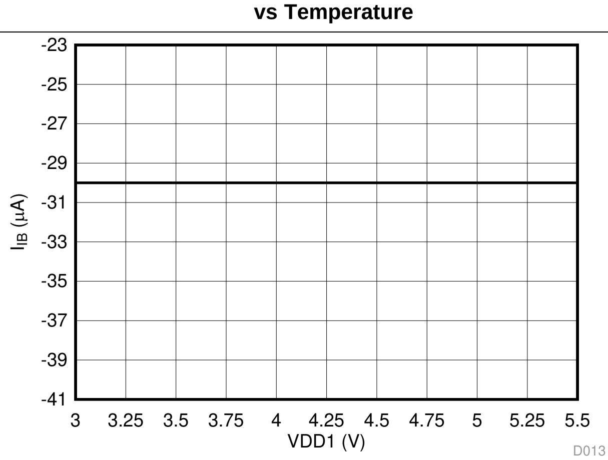
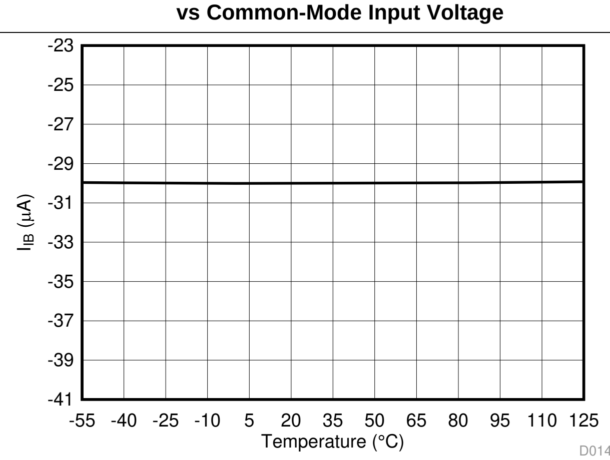


图 15. Input Bias Current vs High-Side Supply Voltage

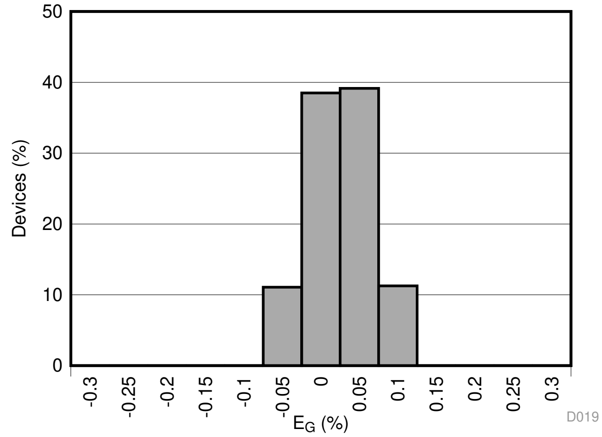


–55°C ≤ T_A < –40°C for AMC1300B only

图 16. Input Bias Current vs Temperature

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



AMC1300B

图 17. Gain Error Histogram

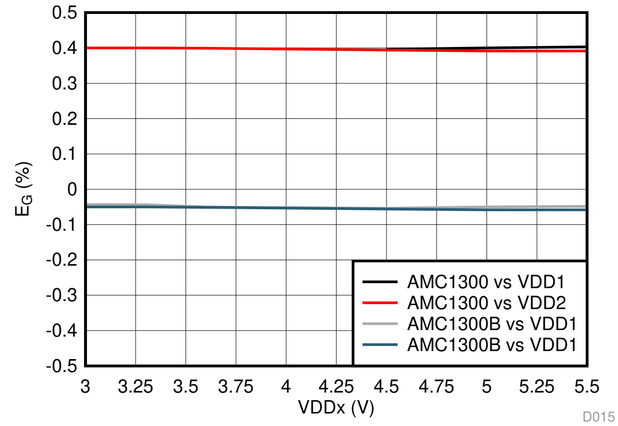
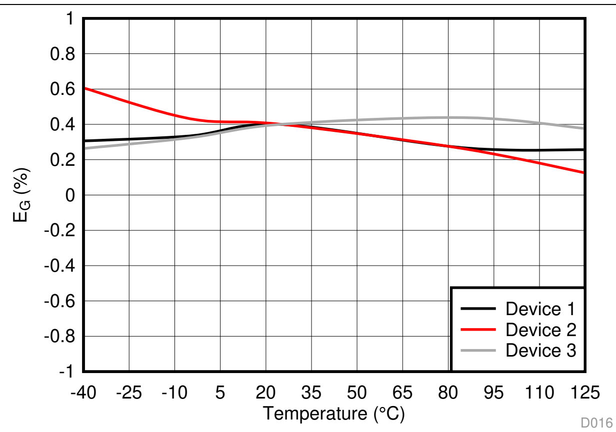
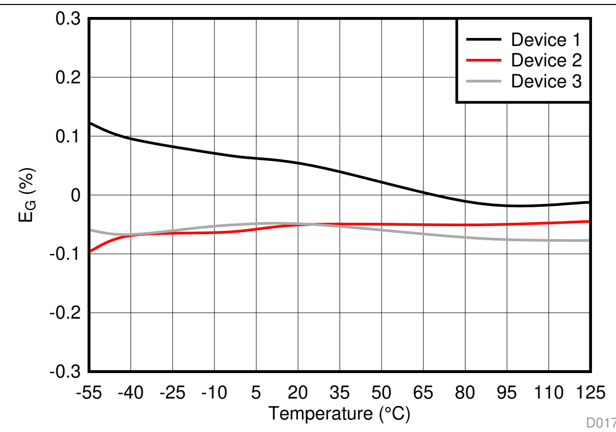


图 18. Gain Error vs Supply Voltage



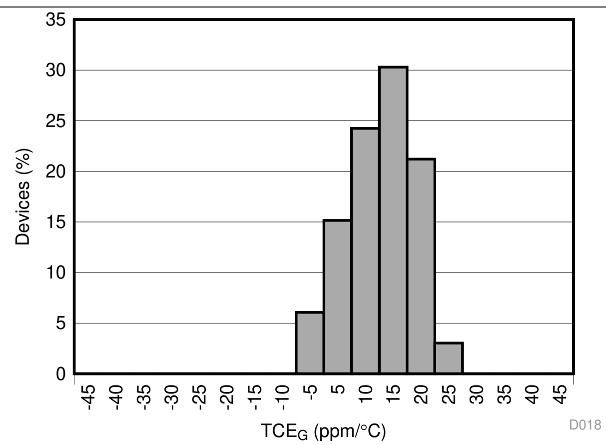
AMC1300

图 19. Gain Error vs Temperature



AMC1300B

图 20. Gain Error vs Temperature



AMC1300B

图 21. Gain Error Drift Histogram

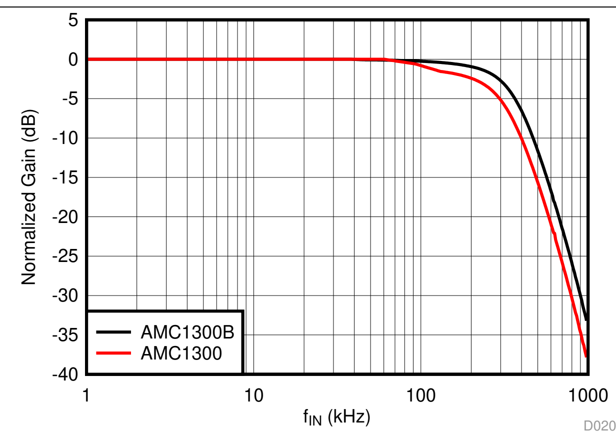


图 22. Normalized Gain vs Input Frequency

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

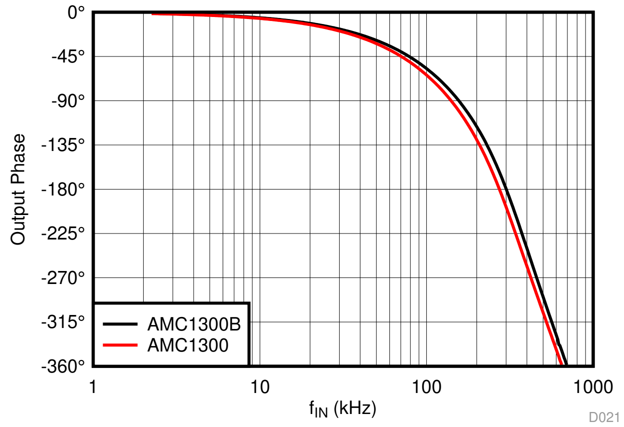


图 23. Output Phase vs Input Frequency

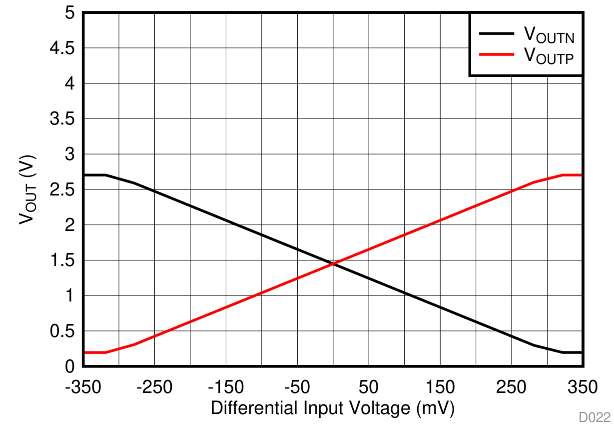


图 24. Output Voltage vs Input Voltage

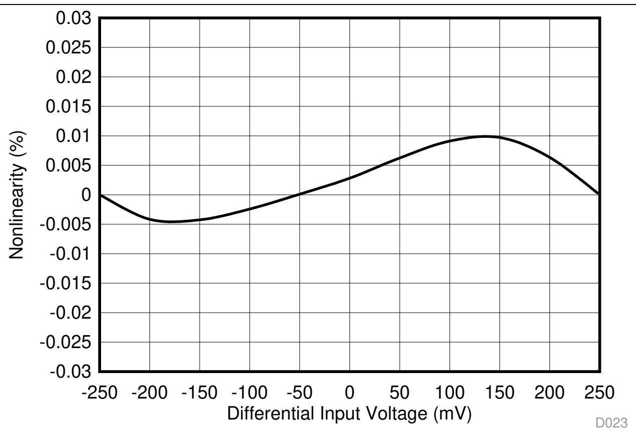


图 25. Nonlinearity vs Input Voltage

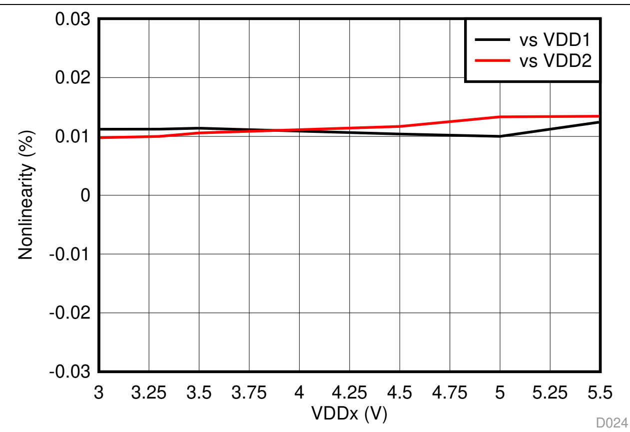
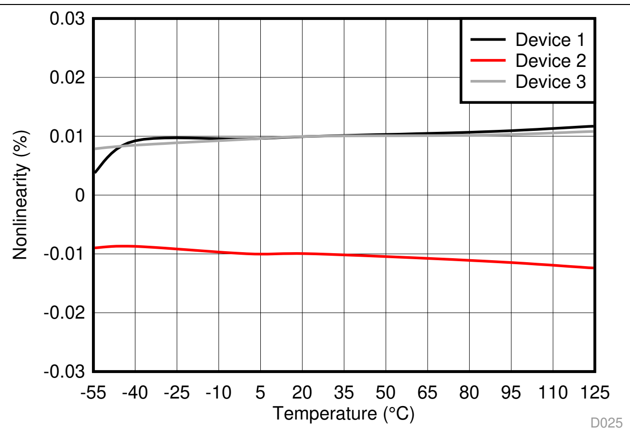
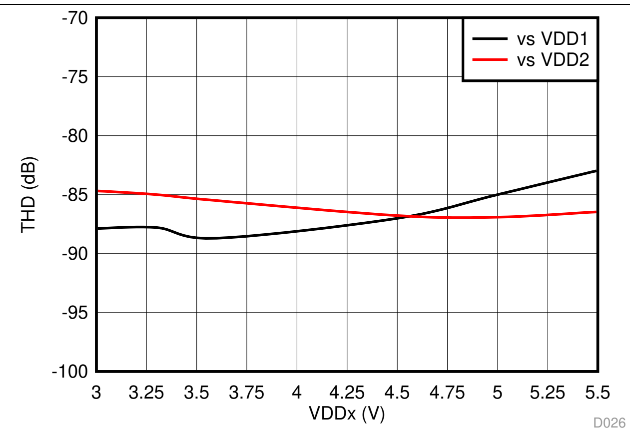


图 26. Nonlinearity vs Supply Voltage



–55°C ≤ T_A < –40°C for AMC1300B only

图 27. Nonlinearity vs Temperature

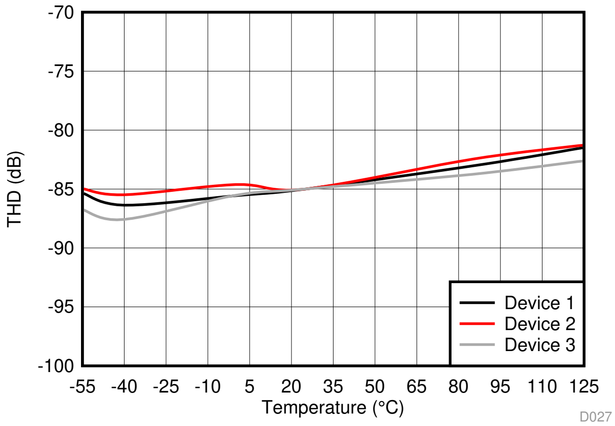


3 V ≤ VDD1 < 4.5 V for AMC1300B only

图 28. Total Harmonic Distortion vs Supply Voltage

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



–55°C ≤ T_A < –40°C for AMC1300B only

图 29. Total Harmonic Distortion vs Temperature

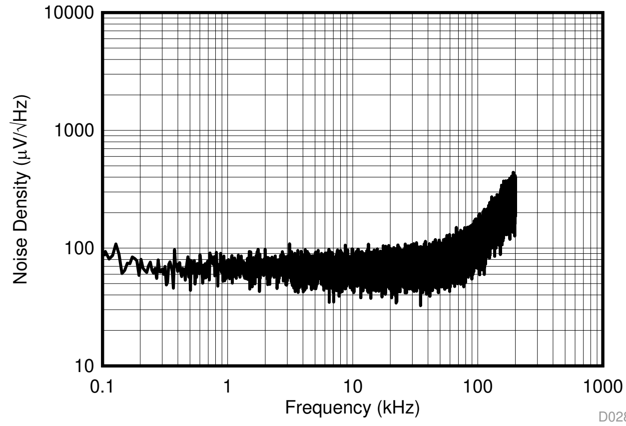


图 30. Input-Referred Noise Density vs Frequency

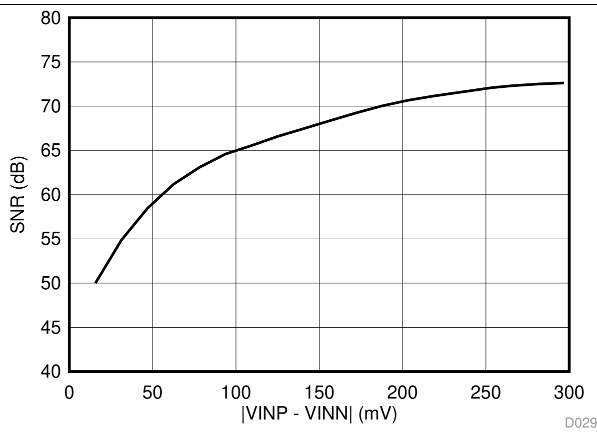
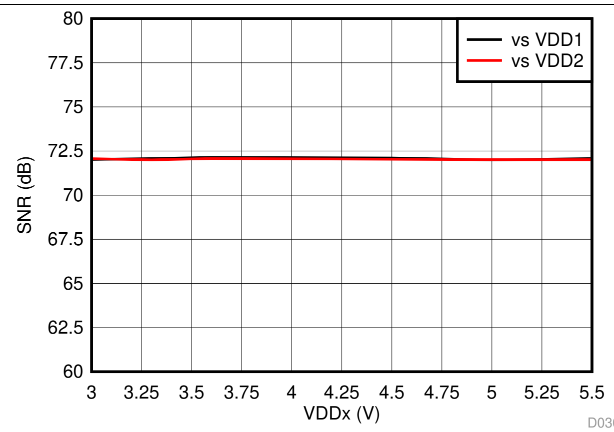
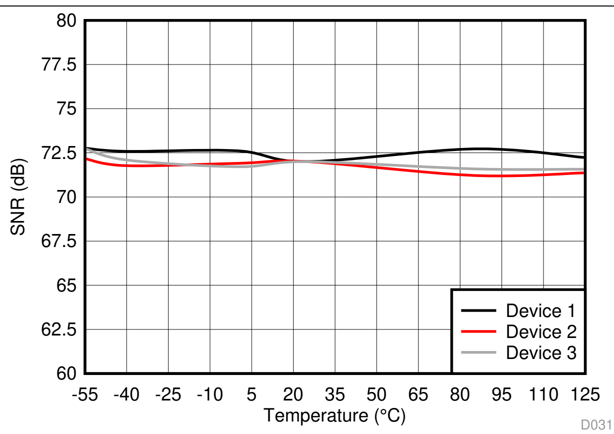


图 31. Signal-to-Noise Ratio vs Input Voltage



3 V ≤ VDD1 < 4.5 V for AMC1300B only

图 32. Signal-to-Noise Ratio vs Supply Voltage



–55°C ≤ T_A < –40°C for AMC1300B only

图 33. Signal-to-Noise Ratio vs Temperature

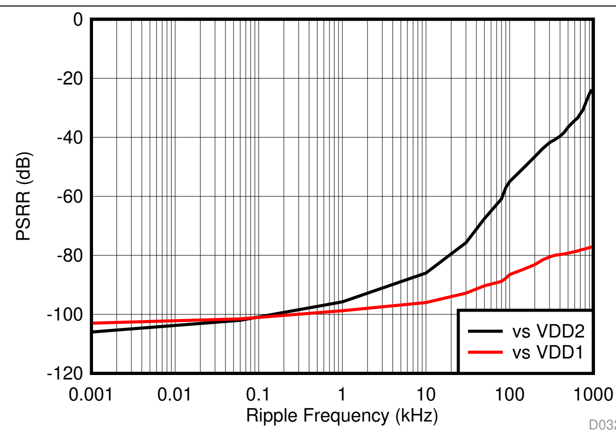


图 34. Power-Supply Rejection Ratio vs Ripple Frequency

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

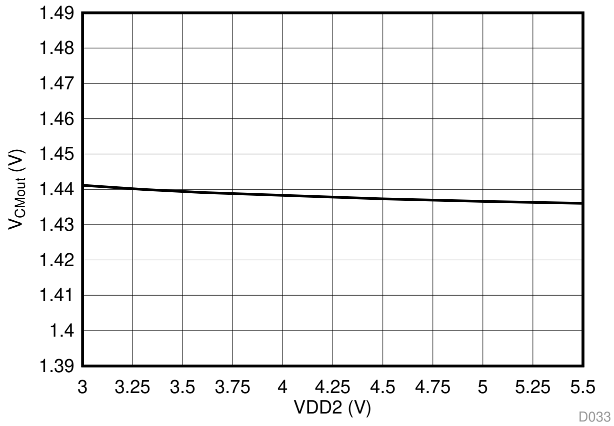
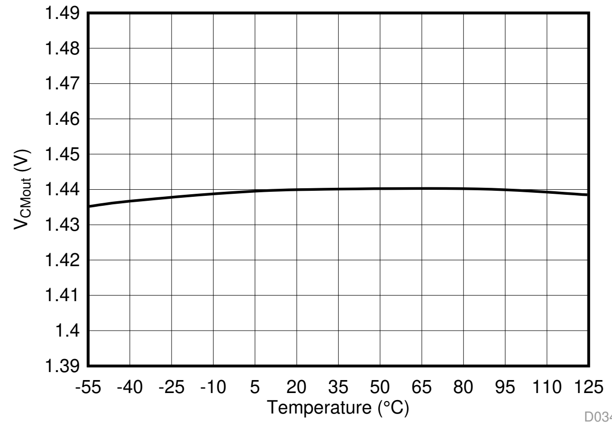


图 35. Output Common-Mode Voltage vs Low-Side Supply Voltage



–55°C ≤ T_A < –40°C for AMC1300B only

图 36. Output Common-Mode Voltage vs Temperature

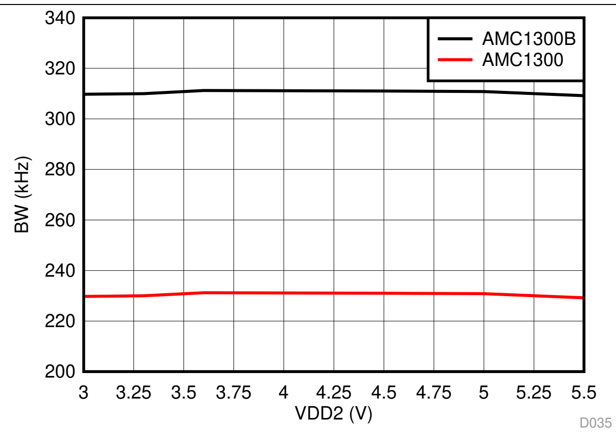


图 37. Output Bandwidth vs Low-Side Supply Voltage

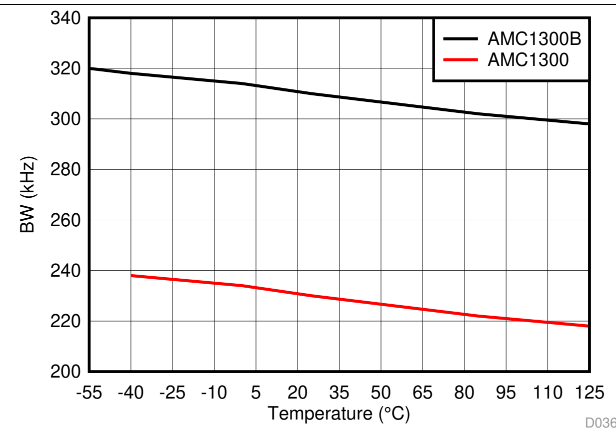
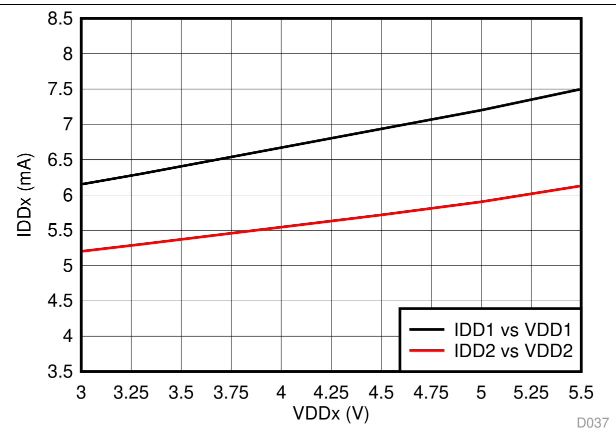
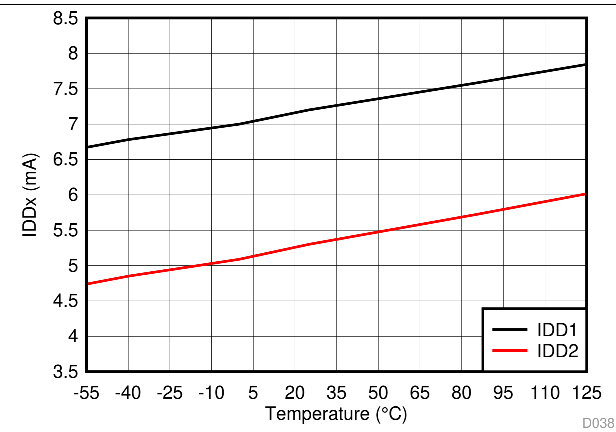


图 38. Output Bandwidth vs Temperature



3 V ≤ VDD1 < 4.5 V for AMC1300B only

图 39. Supply Current vs Supply Voltage



–55°C ≤ T_A < –40°C for AMC1300B only

图 40. Supply Current vs Temperature

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

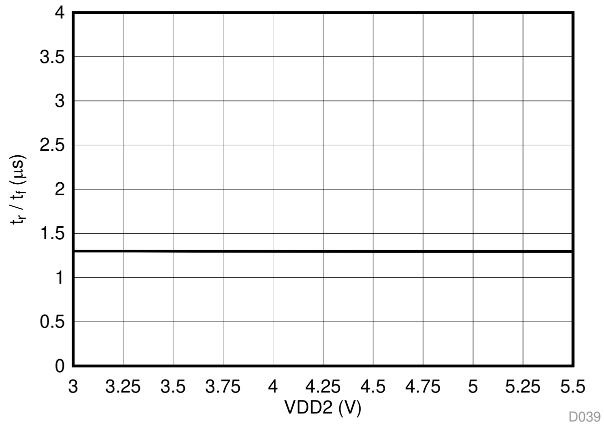
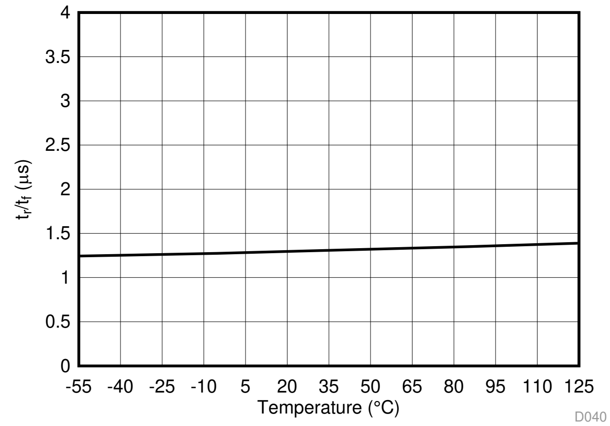
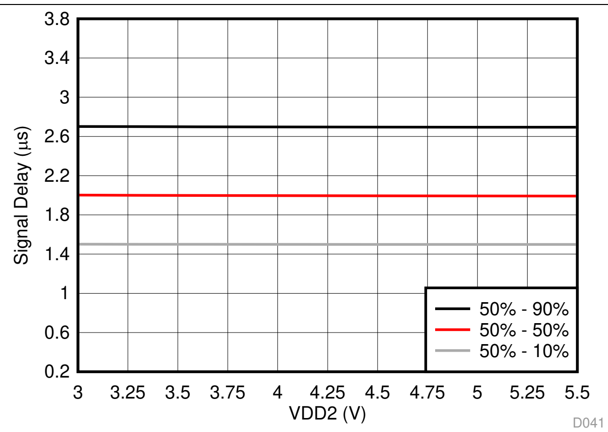


图 41. Output Rise and Fall Time vs Low-Side Supply



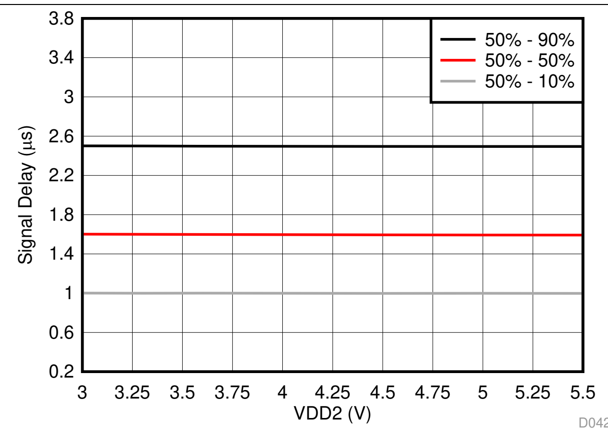
–55°C ≤ T_A < –40°C for AMC1300B only

图 42. Output Rise and Fall Time vs Temperature



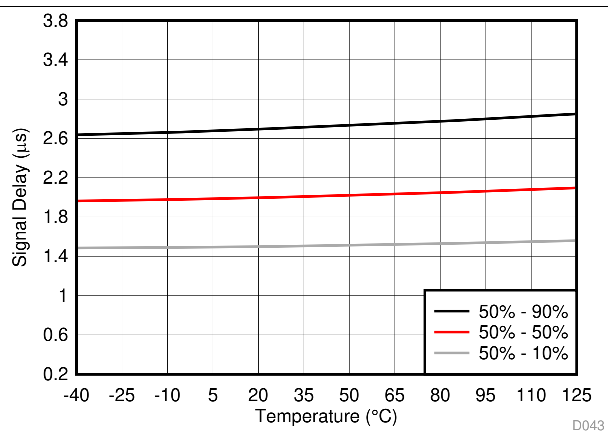
AMC1300

图 43. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage



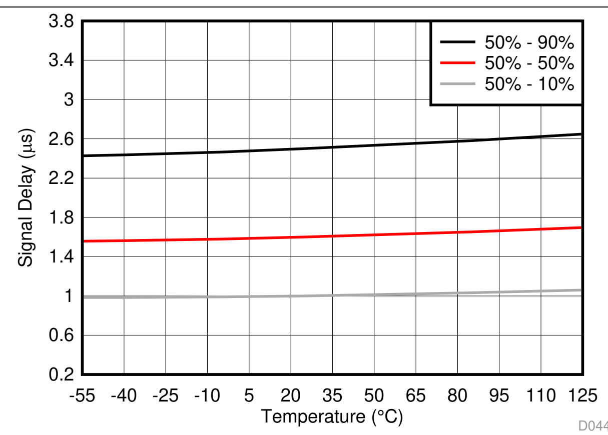
AMC1300B

图 44. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage



AMC1300

图 45. V_{IN} to V_{OUT} Signal Delay vs Temperature



AMC1300B

图 46. V_{IN} to V_{OUT} Signal Delay vs Temperature

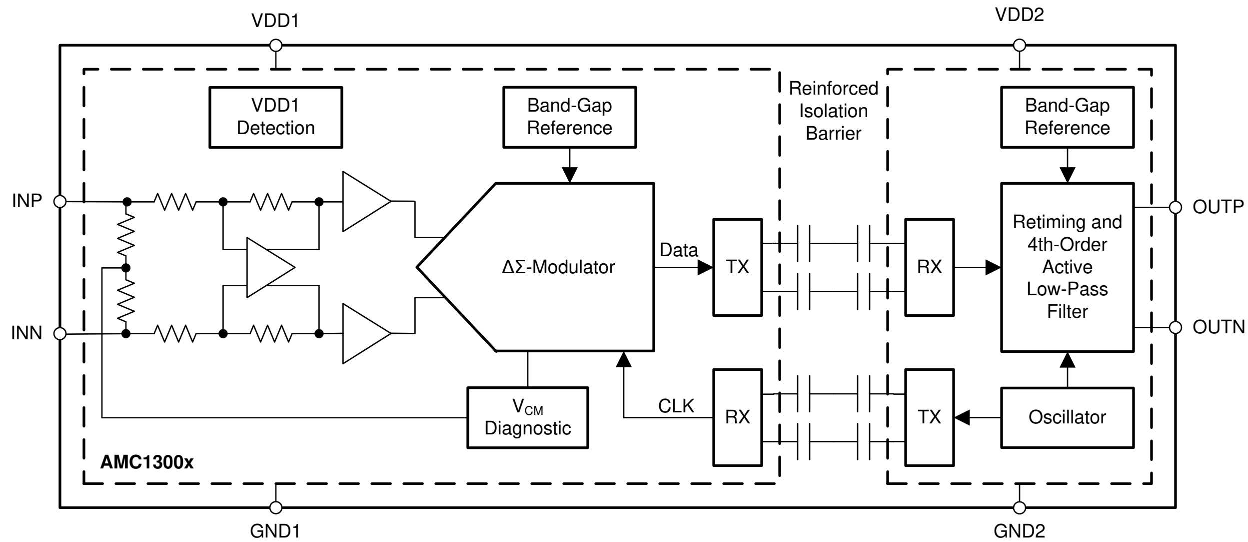
8 Detailed Description

8.1 Overview

The AMC1300 is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called *TX* in the *Functional Block Diagram*) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed, as shown in the *Functional Block Diagram*, by a fourth-order analog filter on the low-side and presented as a differential output of the device.

The SiO_2-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in *ISO72x Digital Isolator Magnetic-Field Immunity*. The digital modulation used in the AMC1300 and the isolation barrier characteristics result in high reliability and common-mode transient immunity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The differential amplifier input stage of the AMC1300 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 with a differential input impedance of 22 kΩ. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals (V_{INP} and V_{INN}). First, if the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

Feature Description (接下页)

8.3.2 Isolation Channel Signal Transmission

The AMC1300 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. As shown in 图 47, the transmitter modulates the bitstream at TX IN with an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent the digital *zero*. The nominal frequency of the carrier used inside the AMC1300 is 480 MHz.

The receiver demodulates the signal after advanced signal conditioning and produces the output. The AMC1300 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

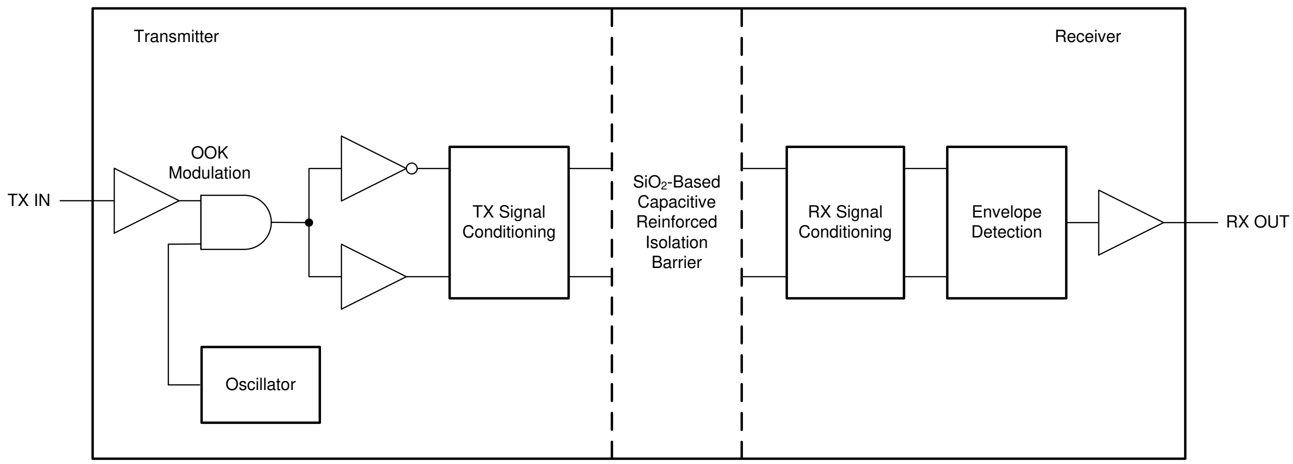


图 47. Block Diagram of an Isolation Channel

图 48 shows the concept of the OOK scheme.

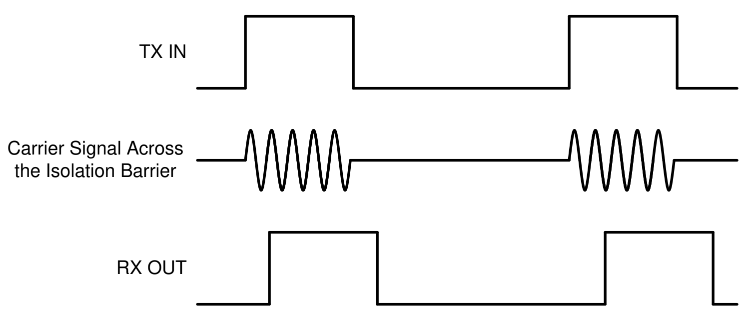


图 48. OOK-Based Modulation Scheme

Feature Description (接下页)

8.3.3 Fail-Safe Output

The AMC1300 offers a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active in two cases:

- When the high-side supply VDD1 of the AMC1300 is missing, or
- When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN}) / 2$, exceeds the minimum common-mode overvoltage detection level V_{CMov} of VDD1 – 2 V.

图 49 and 图 50 show the fail-safe output of the AMC1300 as a negative differential output voltage value that does not occur under normal device operation. Use the $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for the fail-safe detection on a system level.

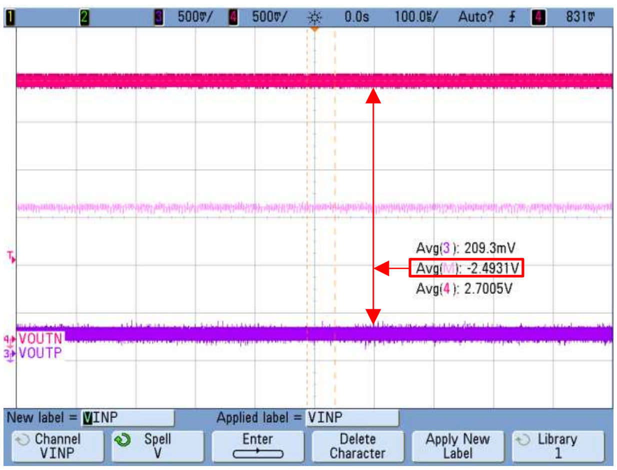


图 49. Typical Negative Clipping Output of the AMC1300

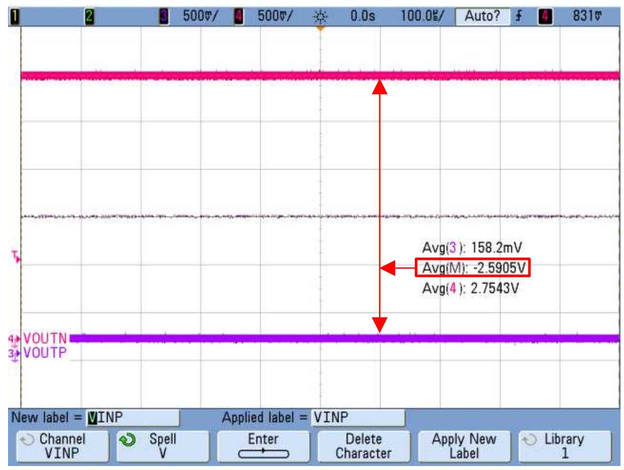


图 50. Typical Fail-Safe Output of the AMC1300

8.4 Device Functional Modes

The AMC1300 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table in the *Specifications* section.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The low input voltage range, very low nonlinearity, and temperature drift make the AMC1300 a high-performance solution for industrial applications where shunt-based current sensing with high common-mode voltage levels is required.

9.2 Typical Application

Isolated amplifiers are widely used in frequency inverters, which are critical parts of industrial motor drives, photovoltaic inverters, uninterruptible power supplies, and other industrial applications. The input structure of the AMC1300 is optimized for use with low-value shunt resistors in current sensing applications.

图 51 depicts a typical operation of the AMC1300 for current sensing in a frequency inverter application. Phase current measurement is accomplished through the shunt resistors, R_{SHUNT} (in this case, a two-pin shunt). The differential input and the high common-mode transient immunity of the AMC1300 ensure reliable and accurate operation even in high-noise environments (such as the power stage of the motor drive). The high-impedance input and wide input voltage range make the AMC1311 suitable for DC bus voltage sensing.

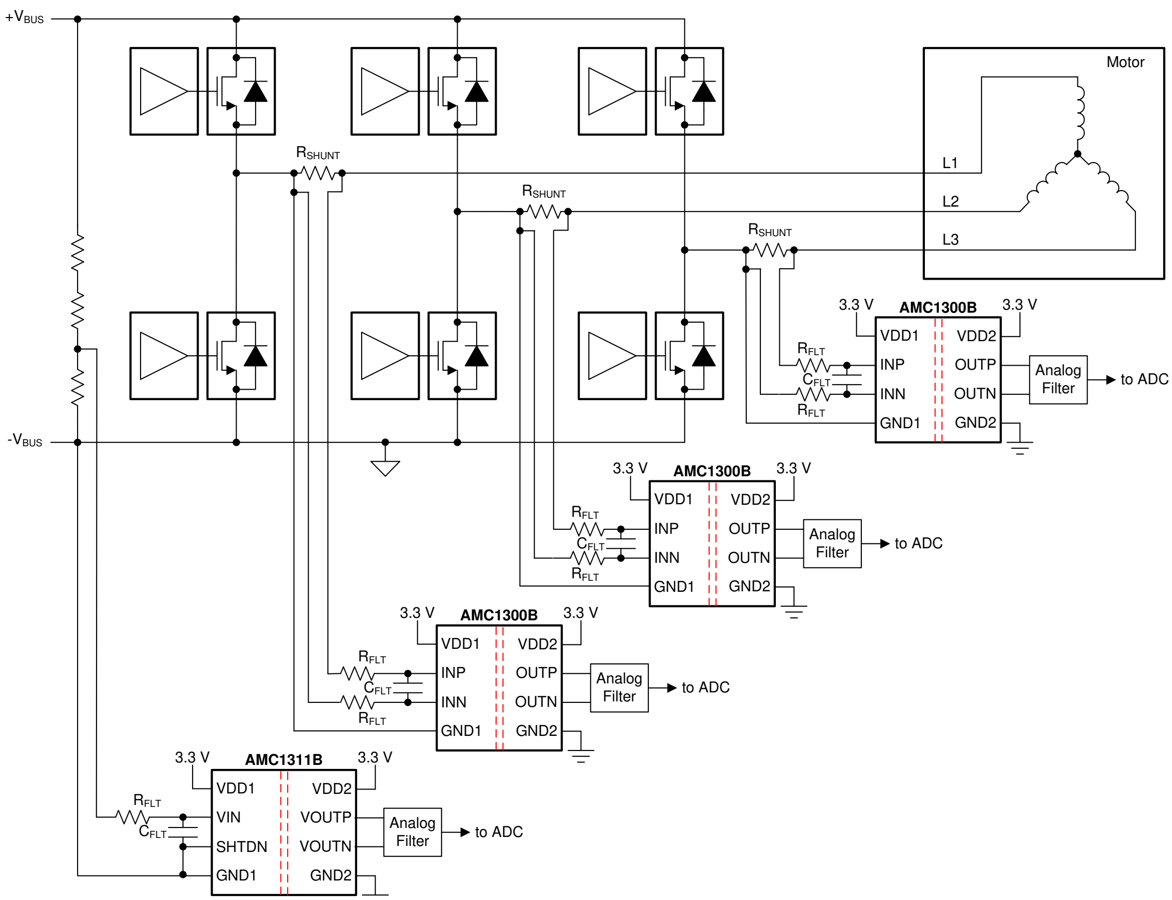


图 51. Using the AMC1300 for Current Sensing in Frequency Inverters

Typical Application (接下页)

9.2.1 Design Requirements

表 1 lists the parameters for this typical application.

表 1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response	± 250 mV (maximum)
Signal delay (50% VIN to 90% OUTP, OUTN)	3 µs (maximum)

9.2.2 Detailed Design Procedure

The high-side power supply (VDD1) for the AMC1300 is derived from the power supply of the upper gate driver. Further details are provided in the *Power Supply Recommendations* section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1300 (INN). If a four-pin shunt is used, the inputs of the AMC1300 device are connected to the inner leads and GND1 is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250$ mV
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$

For systems using single-ended input ADCs, 图 52 shows an example of a TLV6001-based signal conversion and filter circuit as used on the AMC1311EVM. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

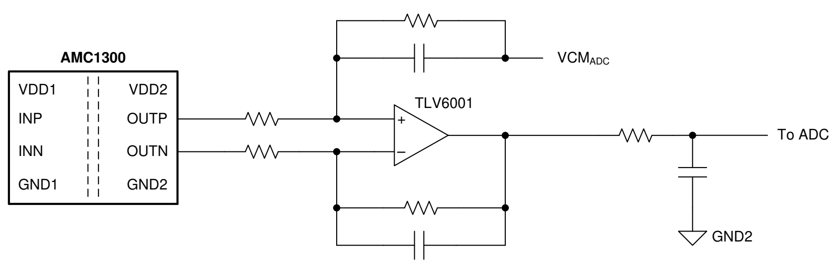


图 52. Connecting the AMC1300 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

9.2.3 Application Curves

In frequency inverter applications, the power switches must be protected in case of an overcurrent condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. 图 53 shows the typical full-scale step response of the AMC1300. Consider the delay of the required window comparator and the micro contol unit (MCU) to calculate the overall response time of the system.

图 53. Step Response of the AMC1300

The high linearity and low temperature drift of offset and gain errors of the AMC1300, as shown in 图 54, allow design of motor drives with low torque ripple.

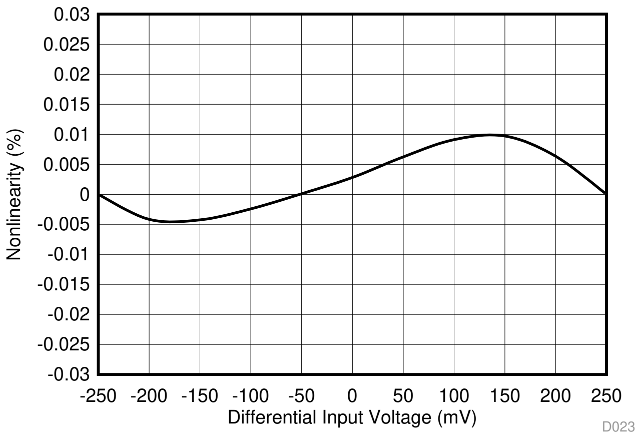


图 54. Typical Nonlinearity of the AMC1300

9.3 What to Do and What Not to Do

Do not leave the inputs of the AMC1300 unconnected (floating) when the device is powered up. If both device inputs are left floating, the input bias current drives these inputs to the output common-mode of the analog front-end of approximately 2 V. If the high-side supply voltage VDD1 is below 4 V, the internal common-mode overvoltage detector turns on and the output functions as described in the *Fail-Safe Output* section, which may lead to an undesired reaction on the system level.

10 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply (VDD1) for the device is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5 V or 3.3 V (for the AMC1300B only) ± 10%. Alternatively, a low-cost low-dropout (LDO) regulator (for example, the LM317-N) may be used to minimize noise on the power supply. TI recommends a low-ESR decoupling capacitor of 0.1 µF to filter this power-supply path. Place this capacitor (C2 in 图 55) as close as possible to the VDD1 pin of the AMC1300 for best performance. If better filtering is required, an additional 2.2-µF capacitor may be used. The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads, and GND1 is connected to one of the outer leads of the shunt.

To decouple the low-side power supply on the controller side, use a 0.1-µF capacitor placed as close to the VDD2 pin of the AMC1300 as possible, followed by an additional capacitor from 1 µF to 10 µF.

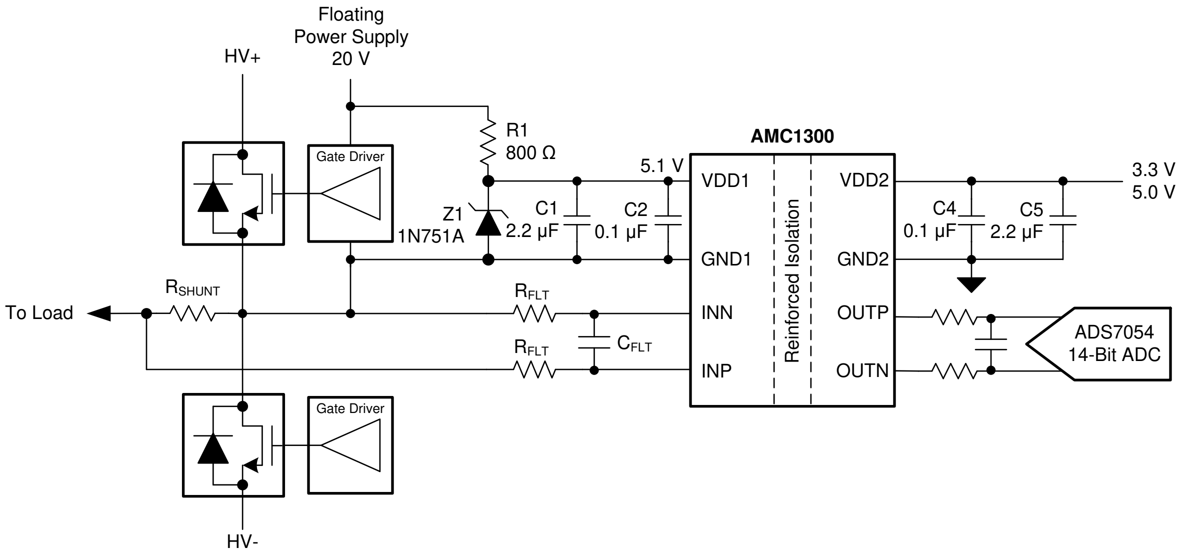


图 55. Zener-Diode-Based, High-Side Power Supply

11 Layout

11.1 Layout Guidelines

图 56 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1300 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1300 and keep the layout of both connections symmetrical.

11.2 Layout Example

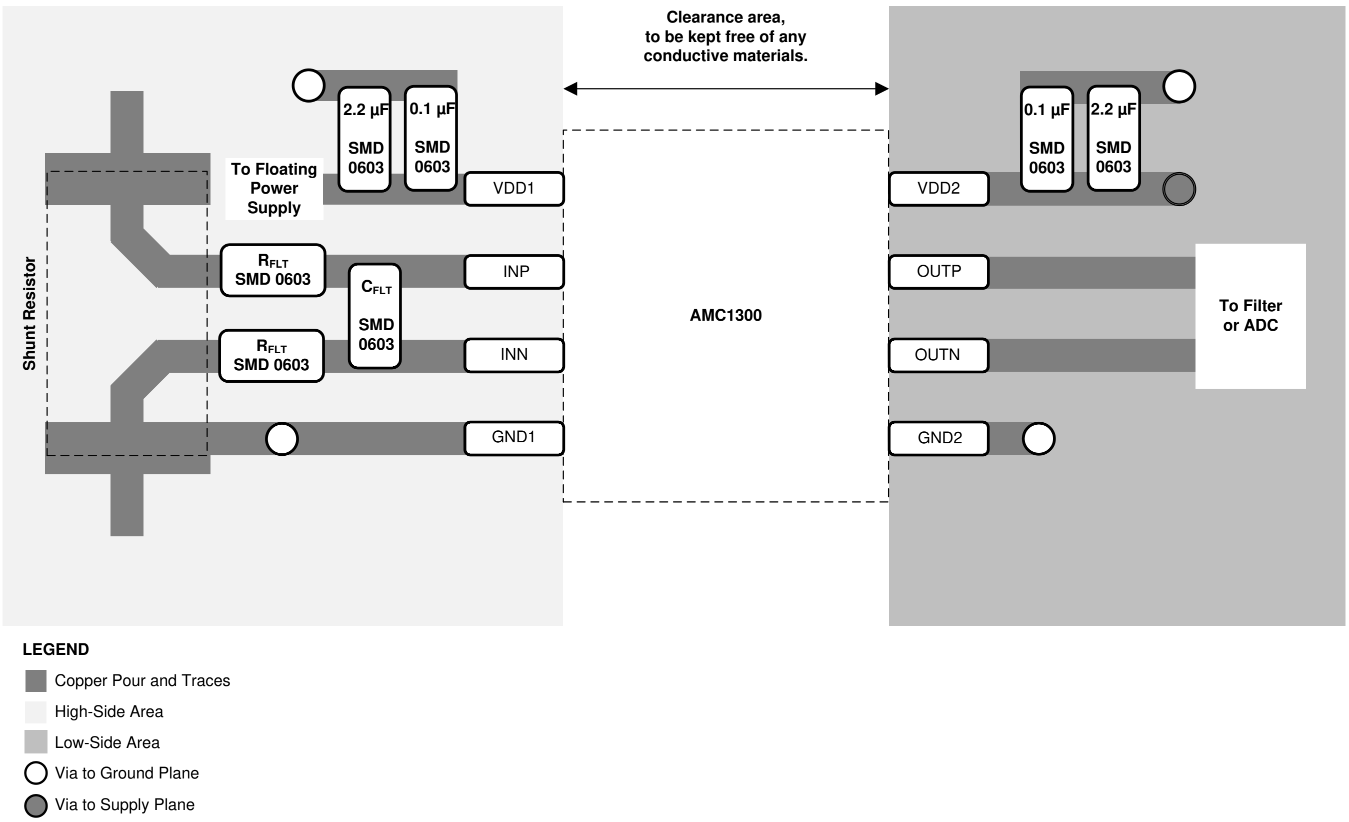


图 56. Recommended Layout of the AMC1300

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《隔离相关术语》* 应用报告
- 德州仪器 (TI)，*《ADSxxx3 双通道、1MSPS、16/14/12 位、4×2 或 2×2 通道同步采样模数转换器》* 数据表
- 德州仪器 (TI)，*《半导体和 IC 封装热指标》* 应用报告
- 德州仪器 (TI)，*《ISO72x 数字隔离器磁场抗扰度》* 应用报告
- 德州仪器 (TI)，*《AMC1311x 高阻抗 2V 输入增强型隔离式放大器》* 数据表
- 德州仪器 (TI)，*《适用于成本敏感型系统的 TLV600x 低功耗、轨至轨输入/输出、1MHz 运算放大器》* 数据表
- 德州仪器 (TI)，*《AMC1311EVM》* 用户指南
- 德州仪器 (TI)，*《经优化可实现较低失真和噪声的 18 位、1MSPS 数据采集块 (DAQ)》* 参考指南
- 德州仪器 (TI)，*《经优化可实现较低功耗的 18 位、1MSPS 数据采集块 (DAQ)》* 参考指南
- 德州仪器 (TI)，*《LM117、LM317-N 宽温度范围三引脚可调稳压器》* 数据表
- 德州仪器 (TI)，*《SN6501 用于隔离式电源的变压器驱动器》* 数据表
- 德州仪器 (TI)，*《适用于三相逆变器的高带宽相电流和直流链路电压检测参考设计》*
- 德州仪器 (TI)，*《采用具有内置死区时间插入功能的栅极驱动器的三相逆变器参考设计》*
- 德州仪器 (TI)，*《采用具有 ±10V 测量范围的 16 位 SAR ADC 的高精度模拟前端参考设计》*
- 德州仪器 (TI)，*《效率大于 93% 且适用于 UPS 的 2kW、48V 至 400V 隔离式双向直流/直流转换器参考设计》*
- 德州仪器 (TI)，*《具有电流、电压和温度保护的增强型隔离式三相逆变器参考设计》*
- 德州仪器 (TI)，*《带有增强型隔离放大器且基于分流器的峰值电流测量 (200A) 参考设计》*
- 德州仪器 (TI)，*《采用 24 位 Δ-Σ ADC 的高精度 ±0.5% 电流和隔离式电压测量参考设计》*
- 德州仪器 (TI)，*《使用隔离放大器且基于分流器的 200A 峰值电流测量参考设计》*

12.2 接收文档更新通知

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1300BDWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B	Samples
AMC1300BDWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B	Samples
AMC1300DWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1300	Samples
AMC1300DWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1300	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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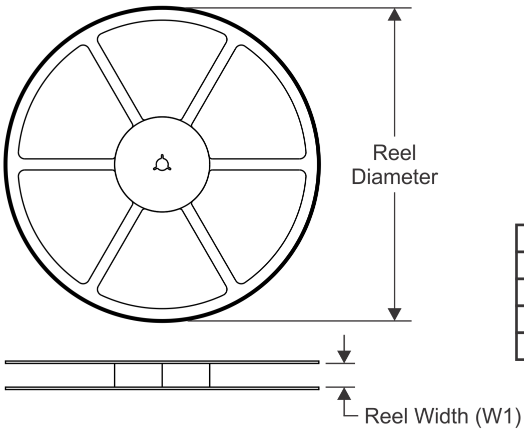
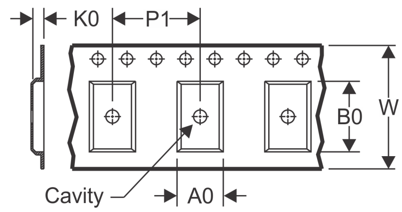
TAPE AND REEL INFORMATION

REEL DIMENSIONS

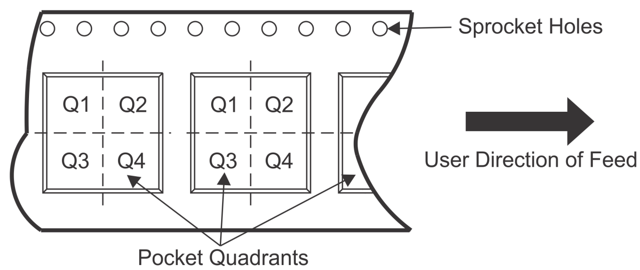


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

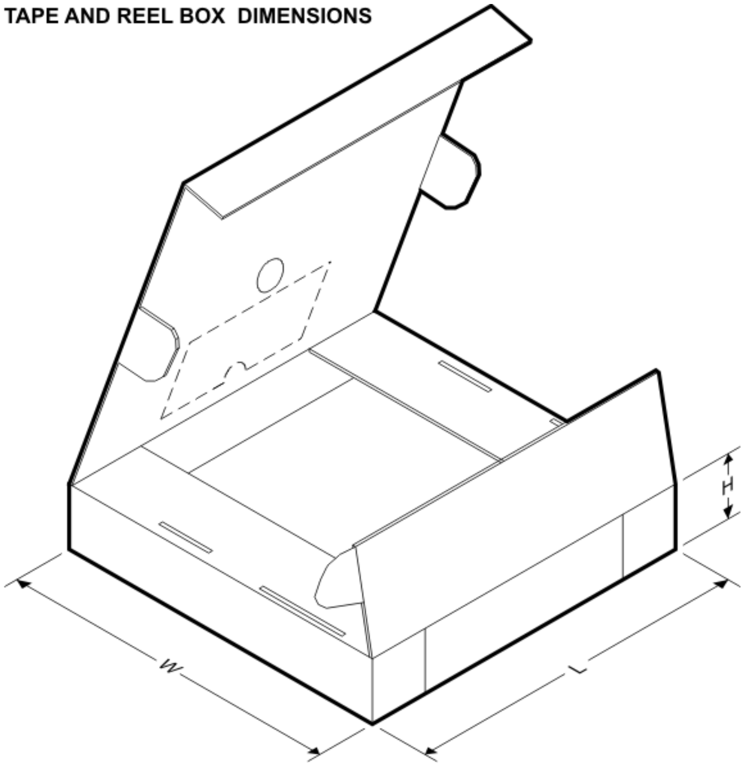
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

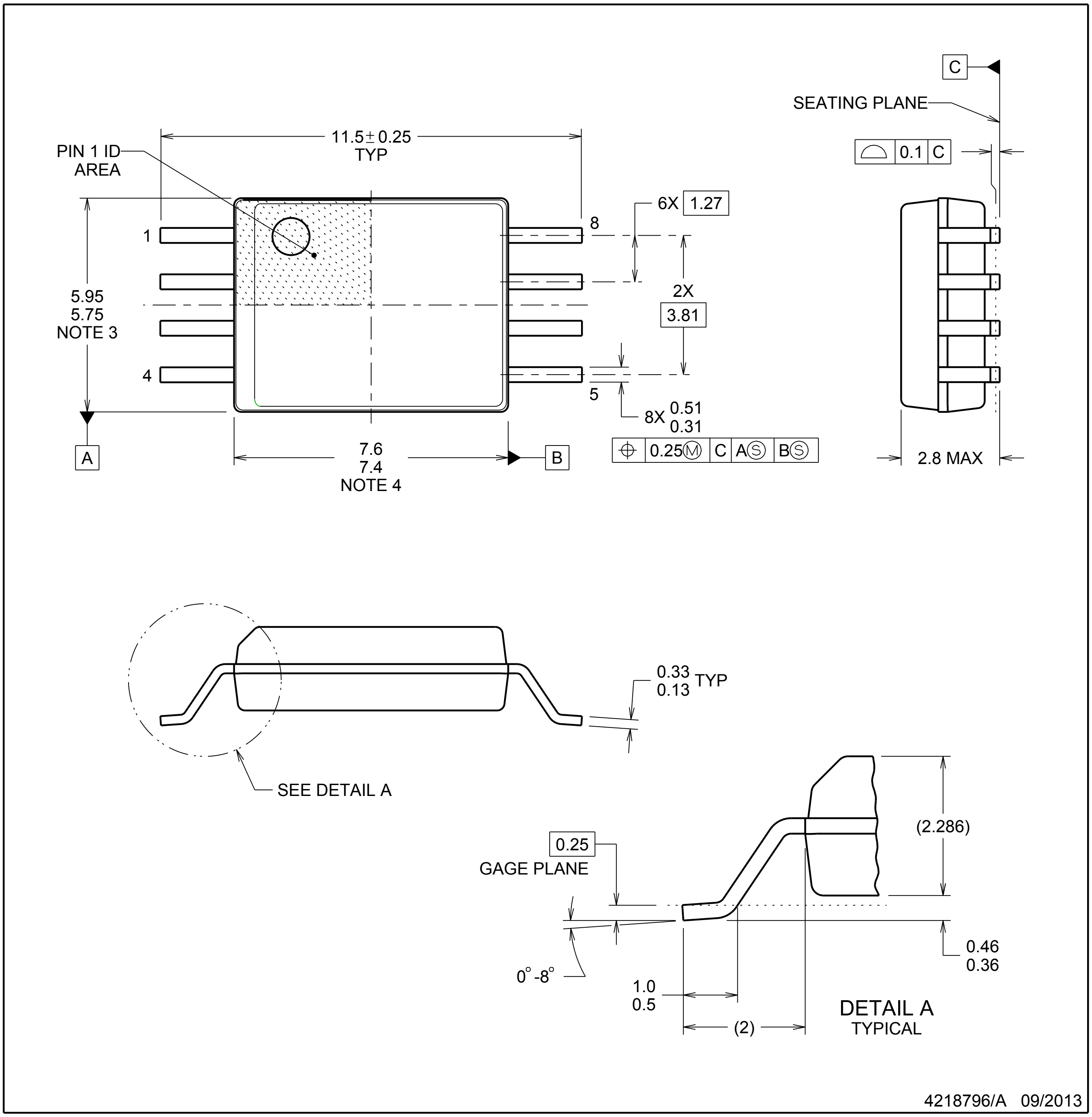
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1300BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1300DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



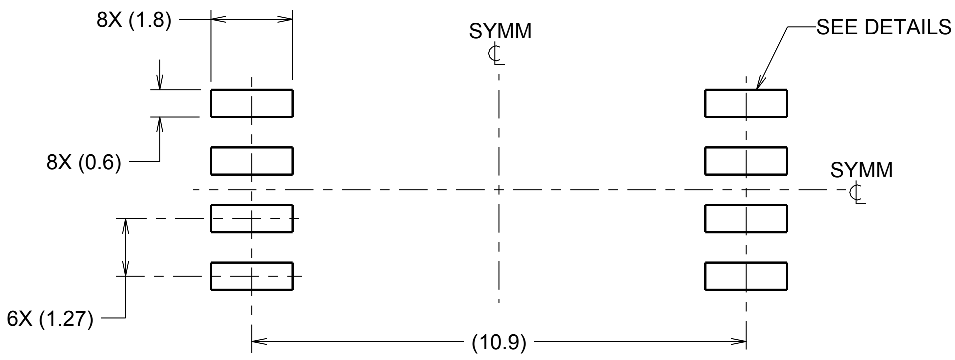
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1300BDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1300DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0

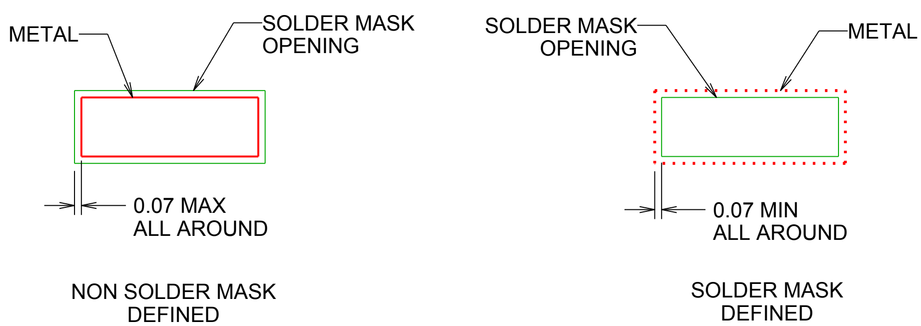


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

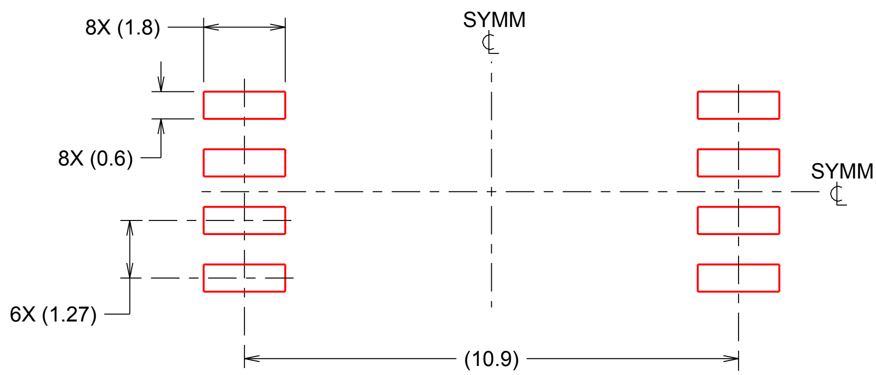


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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