AMC1311x-Q1 高阻抗 2V 输入增强型隔离放大器

1 特性

- 符合汽车类应用的 标准
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度 1 级：–40°C 至 125°C 的环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 2V 高阻抗输入电压范围，针对隔离式电压测量进行优化
- 低失调误差和温漂：
  - AMC1311B-Q1：±1.5mV（最大值），±15µV/°C（最大值）
  - AMC1311-Q1：±9.9mV（最大值），±20µV/°C（典型值）
- 固定增益：1
- 极低增益误差和温漂：
  - AMC1311B-Q1：±0.3%（最大值），±45ppm/°C（最大值）
  - AMC1311-Q1：±1%（最大值），±30ppm/°C（典型值）
- 低非线性和温漂：0.01%，1ppm/°C（典型值）
- 高侧 3.3V 运行电压 (AMC1311B-Q1)
- 高侧电源缺失指示
- 安全相关认证：
  - 符合 DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01 标准的 7000 V_{PK} 增强型隔离
  - 符合 UL1577 标准且长达 1 分钟的 5000V_{RMS} 隔离
  - CAN/CSA No. 5A 组件验收服务通知

2 应用

- 可用于以下应用的隔离式电压检测：
  - 牵引逆变器
  - 板载充电器
  - 直流/直流转换器

3 说明

AMC1311-Q1 是一款隔离式精密放大器，此放大器的输出与输入电路由抗电磁干扰性能极强的隔离栅隔开。根据 VDE V 0884-11 和 UL1577 标准，该隔离栅经认证可提供高达 7kV_{PEAK} 的增强型电隔离。与隔离式电源结合使用时，该隔离放大器可将以不同共模电压电平运行的系统的各器件隔开，并防止较低电压器件损坏。

AMC1311-Q1 的高阻抗输入针对连接高压电阻分压器或具有高输出电阻的其他电压信号源的情况进行了优化。器件性能出色，支持在闭环系统中进行精确的低温漂电压或温度检测和控制。集成的高侧电源电压缺失检测功能可简化系统级设计和诊断。

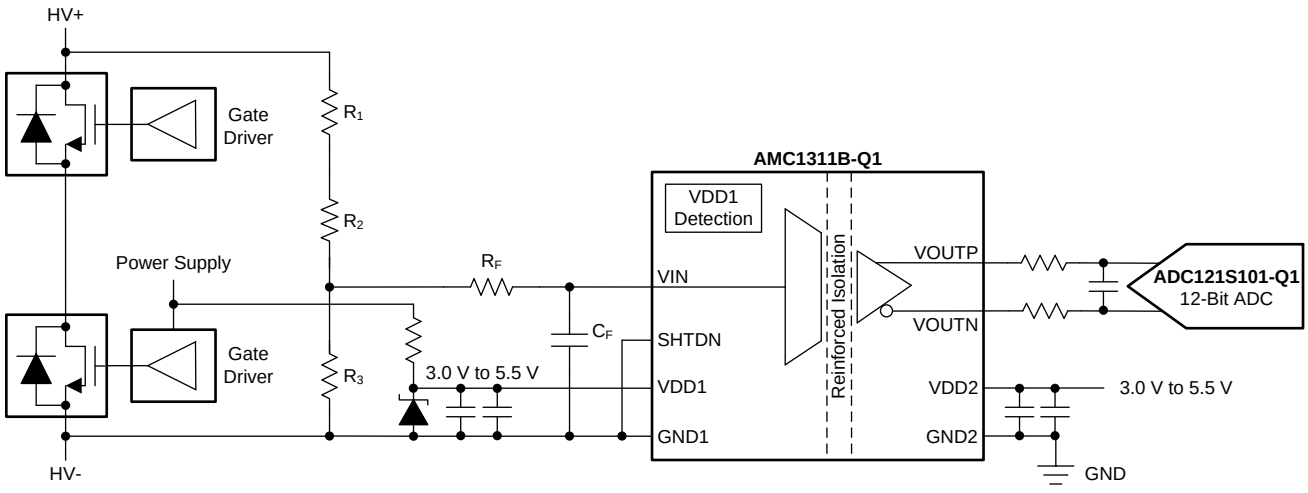
AMC1311-Q1 提供两种性能级别选项：AMC1311-Q1 和 AMC1311B-Q1。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
AMC1311x-Q1	SOIC (8)	5.85mm × 7.50mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

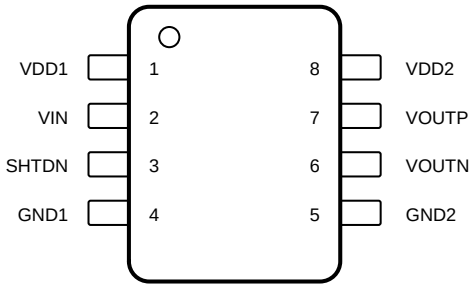
Changes from Original (March 2018) to Revision A	Page
• 已投入量产	1

5 器件比较表

参数		AMC1311B-Q1	AMC1311-Q1
高侧电源电压，VDD1		3.0V 至 5.5V	4.5V 至 5.5V
额定环境温度，T_A		–40°C 至 +125°C	-40°C 至 125°C
输入失调电压，V_{OS}	4.5V ≤ VDD1 ≤ 5.5V	±1.5mV	±9.9mV
	3.0V ≤ VDD1 ≤ 5.5V	±2.5mV	不适用
输入失调电压温漂，TCV_{OS}		±3µV/°C（典型值），±15µV/°C（最大值）	±20µV/°C（典型值）
增益误差，E_G		±0.3%	±1%
增益误差漂移，TCE_G		±5ppm/°C（典型值），±45ppm/°C（最大值）	±30ppm/°C（典型值）
共模瞬态抗扰度，CMTI		75kV/µs（最小值）	15kV/µs（最小值）

6 Pin Configuration and Functions

DWV Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	—	High-side power supply, 3.0 V to 5.5 V for the AMC1311B-Q1 (4.5 V to 5.5 V for the AMC1311-Q1), relative to GND1. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
2	VIN	I	Analog input
3	SHTDN	I	Shutdown input, active high, with internal pullup resistor (typical value: 100 kΩ)
4	GND1	—	High-side analog ground
5	GND2	—	Low-side analog ground
6	VOUTN	O	Inverting analog output
7	VOUTP	O	Noninverting analog output
8	VDD2	—	Low-side power supply, 3.0 V to 5.5 V, relative to GND2. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Power-supply voltage	VDD1 to GND1	–0.3	6.5	V
	VDD2 to GND2	–0.3	6.5	
Input voltage	VIN	GND1 – 6	VDD1 + 0.5	V
	SHTDN	GND1 – 0.5	VDD1 + 0.5	
Output voltage	VOUTP, VOUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1, AMC1311-Q1	4.5	5	5.5	V
		VDD1 to GND1, AMC1311B-Q1	3.0	5	5.5	
	Low-side power supply	VDD2 to GND2	3.0	3.3	5.5	V
ANALOG INPUT						
	Absolute input voltage	VIN to GND1	–2		VDD1	V
V_{FSR}	Specified linear input full-scale voltage	VIN to GND1	–0.1		2	V
$V_{Clipping}$	Input voltage before clipping output	VIN to GND1		2.516		V
DIGITAL INPUT						
	Input voltage	SHTDN	GND1		VDD1	V
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		AMC1311x-Q1 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	97.9	mW
		VDD1 = VDD2 = 3.6 V, AMC1311B-Q1 only	56.16	
P_{D1}	Maximum power dissipation (high-side supply)	VDD1 = 5.5 V	53.35	mW
		VDD1 = 3.6 V, AMC1311B-Q1 only	30.24	
P_{D2}	Maximum power dissipation (low-side supply)	VDD2 = 5.5 V	44.55	mW
		VDD2 = 3.6 V	25.92	

7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 9	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 9	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0105 mm)	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At ac voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At ac voltage (sine wave)	1500	V_{RMS}
		At dc voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8400	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1 MHz	~1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS} or 7000 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6000 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O may allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 84.6°C/W, T_J = 150°C, T_A = 25°C, VDD1 = VDD2 = 5.5 V, see 图 2			268	mA
		$R_{\theta JA}$ = 84.6°C/W, T_J = 150°C, T_A = 25°C, VDD1 = VDD2 = 3.6 V, AMC1311B-Q1 only, see 图 2			410	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 84.6°C/W, T_J = 150°C, T_A = 25°C, see 图 3			1477	mW
T_S	Maximum safety temperature				150	°C

(1) Input, output, or the sum of input and output power must not exceed this value.

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

7.9 Electrical Characteristics

minimum and maximum specifications of the AMC1311-Q1 apply from T_A = –40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VIN = –0.1 V to 2 V, and SHTDN = GND1 = 0 V; minimum and maximum specifications of the AMC1311B-Q1 apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VIN = –0.1 V to 2 V, and SHTDN = GND1 = 0 V; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{OS}	Input offset voltage(1)	AMC1311-Q1, initial, at T_A = 25°C, VIN = GND1	–9.9	±0.4	9.9	mV
		AMC1311B-Q1, initial, at T_A = 25°C, VIN = GND1, 4.5 V ≤ VDD1 ≤ 5.5 V	–1.5	±0.4	1.5	
		AMC1311B-Q1, initial, at T_A = 25°C, VIN = GND1, 3.0 V ≤ VDD1 ≤ 5.5 V(2)	–2.5	–1.1	2.5	
TCV_{OS}	Input offset drift(1)	AMC1311-Q1		±20		µV/°C
		AMC1311B-Q1	–15	±3	15	
C_{IN}	Input capacitance(3)	f_{IN} = 275 kHz		7		pF
R_{IN}	Input resistance(3)			1		GΩ
I_{IB}	Input bias current	VIN = GND1	–15	3.5	15	nA
TCI_{IB}	Input bias current drift			±10		pA/°C
ANALOG OUTPUT						
	Nominal gain			1		
E_G	Gain error(1)	AMC1311-Q1, initial, at T_A = 25°C	–1%	0.4%	1%	
		AMC1311B-Q1, initial, at T_A = 25°C	–0.3%	±0.05%	0.3%	
TCE_G	Gain error drift(1)	AMC1311-Q1		±30		ppm/°C
		AMC1311B-Q1	–45	±5	45	
	Nonlinearity(1)		–0.04%	±0.01%	0.04%	
	Nonlinearity drift			1		ppm/°C
THD	Total harmonic distortion	VIN = 2 V, f_{IN} = 10 kHz, BW = 100 kHz		–87		dB
	Output noise	VIN = GND1, BW = 100 kHz		220		μV_{RMS}
SNR	Signal-to-noise ratio	VIN = 2 V, f_{IN} = 1 kHz, BW = 10 kHz	79	82.6		dB
		VIN = 2 V, f_{IN} = 10 kHz, BW = 100 kHz		70.9		
PSRR	Power-supply rejection ratio(4)	PSRR vs VDD1, at dc		–65		dB
		PSRR vs VDD1, 100-mV and 10-kHz ripple		–65		
		PSRR vs VDD2, at dc		–85		
		PSRR vs VDD2, 100-mV and 10-kHz ripple		–70		
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{FAILSAFE}$	Failsafe differential output voltage	VOUTP – VOUTN, SHTDN = high, or VDD1 ≤ $VDD1_{UV}$, or VDD1 missing		–2.6	–2.5	V
BW	Output bandwidth	AMC1311-Q1	100	220		kHz
		AMC1311B-Q1	220	275		
R_{OUT}	Output resistance	On VOUTP or VOUTN		< 0.2		Ω
	Output short-circuit current			±13		mA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1 kV, AMC1311-Q1	15	30		kV/µs
		|GND1 – GND2| = 1 kV, AMC1311B-Q1	75	140		

(1) The typical value includes one sigma statistical variation.
(2) The typical value is at VDD1 = 3.3 V.
(3) See the *Analog Input* section for more details.
(4) This parameter is output referred.

Electrical Characteristics (continued)

minimum and maximum specifications of the AMC1311-Q1 apply from T_A = –40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VIN = –0.1 V to 2 V, and SHTDN = GND1 = 0 V; minimum and maximum specifications of the AMC1311B-Q1 apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VIN = –0.1 V to 2 V, and SHTDN = GND1 = 0 V; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT (SHTDN Pin: CMOS Logic Family, CMOS With Schmitt-Trigger)						
I_{IN}	Input current	GND1 ≤ V_{SHTDN} ≤ VDD1	–70		1	µA
C_{IN}	Input capacitance			5		pF
V_{IH}	High-level input voltage		0.7 × VDD1		VDD1 + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × VDD1	V
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold voltage	VDD1 falling	1.75	2.53	2.7	V
IDD1	High-side supply current	AMC1311B-Q1 only, 3.0 V ≤ VDD1 ≤ 3.6 V, SHTDN = low		6	8.4	mA
		4.5 V ≤ VDD1 ≤ 5.5 V, SHTDN = low		7.1	9.7	
		SHTDN = high		1.3		µA
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		5.3	7.2	mA
		4.5 V ≤ VDD2 ≤ 5.5 V		5.9	8.1	

7.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time of VOUTP, VOUTN	See 图 1		1.3		µs
t_f	Fall time of VOUTP, VOUTN	See 图 1		1.3		µs
	VIN to VOUTN, VOUTP signal delay (50% – 10%)	AMC1311-Q1, unfiltered output, see 图 1		1.5	2.5	µs
		AMC1311B-Q1, unfiltered output, see 图 1		1.0	1.5	
	VIN to VOUTN, VOUTP signal delay (50% – 50%)	AMC1311-Q1, unfiltered output, see 图 1		2.1	3.1	µs
		AMC1311B-Q1, unfiltered output, see 图 1		1.6	2.1	
	VIN to VOUTN, VOUTP signal delay (50% – 90%)	AMC1311-Q1, unfiltered output, see 图 1		3.0	4.0	µs
		AMC1311B-Q1, unfiltered output, see 图 1		2.5	3.0	
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to VOUTP, VOUTN valid, 0.1% settling		50	100	µs
t_{EN}	Device enable time	SHTDN high to low		50	100	µs
t_{SHTDN}	Shutdown time	SHTDN low to high		3	10	µs

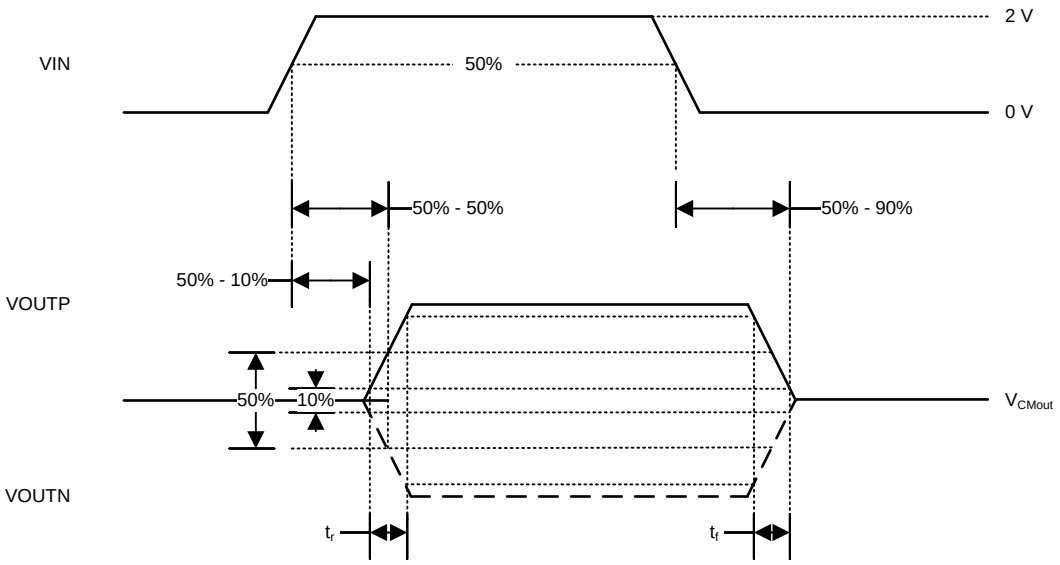


图 1. Rise, Fall, and Delay Time Waveforms

7.11 Insulation Characteristics Curves

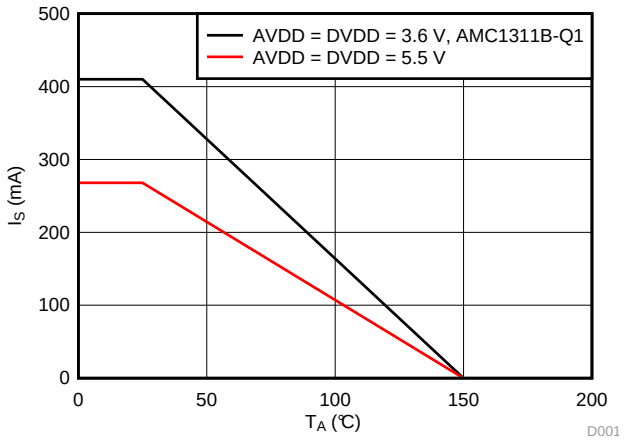


图 2. Thermal Derating Curve for Safety-Limiting Current per VDE

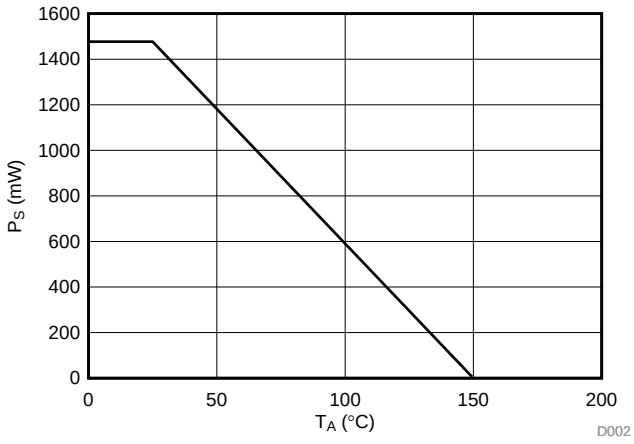
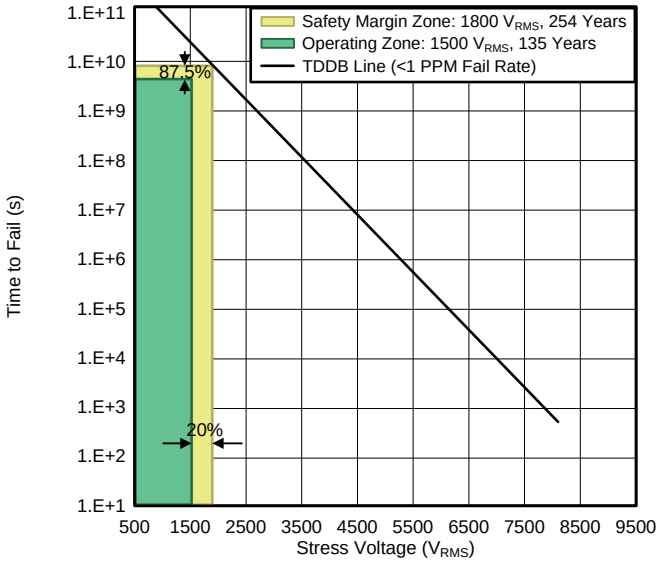


图 3. Thermal Derating Curve for Safety-Limiting Power per VDE

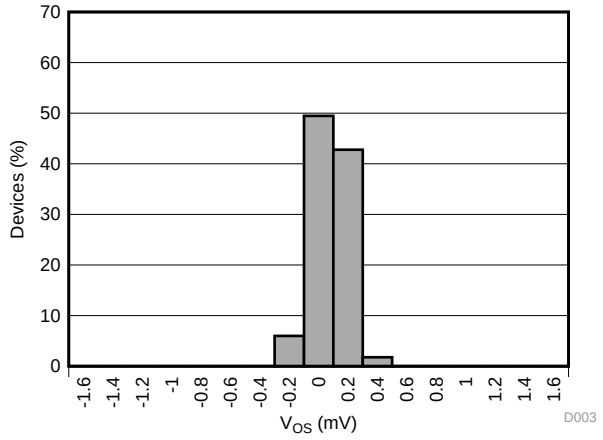


T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

图 4. Reinforced Isolation Capacitor Lifetime Projection

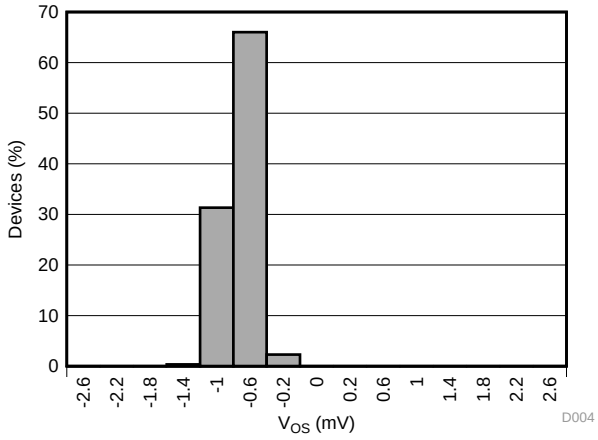
7.12 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)



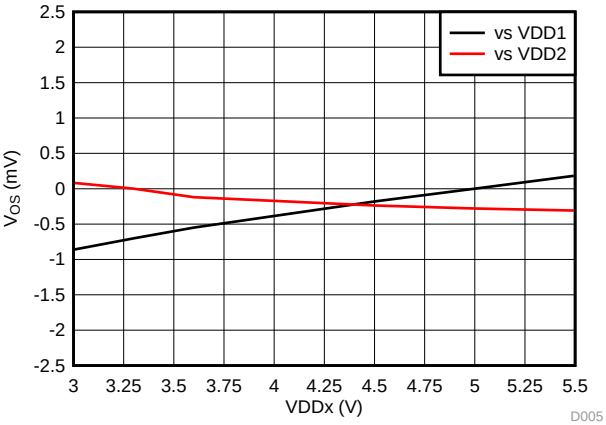
VDD1 = 5 V, AMC1311B-Q1

图 5. Input Offset Voltage Histogram



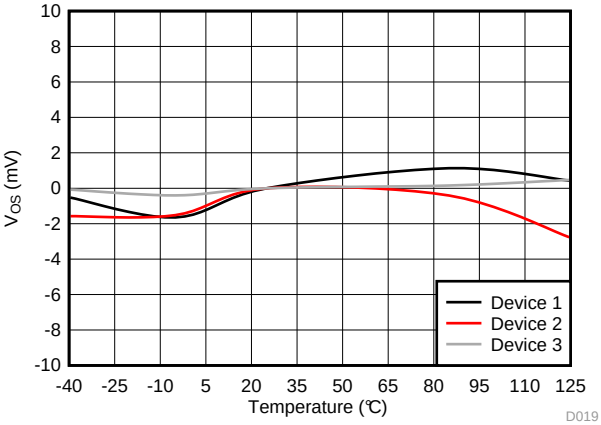
VDD1 = 3.3 V, AMC1311B-Q1

图 6. Input Offset Voltage Histogram



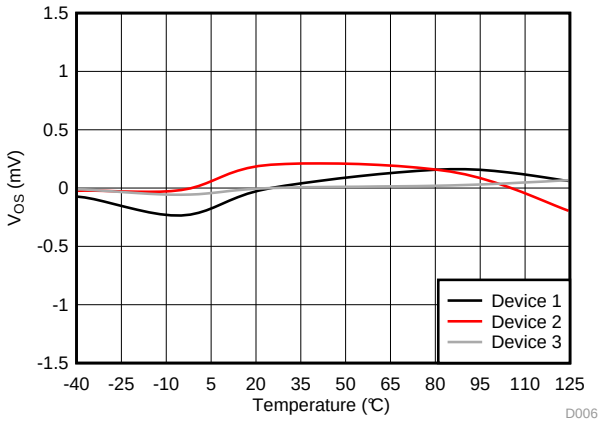
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B-Q1 only

图 7. Input Offset Voltage vs Supply Voltage



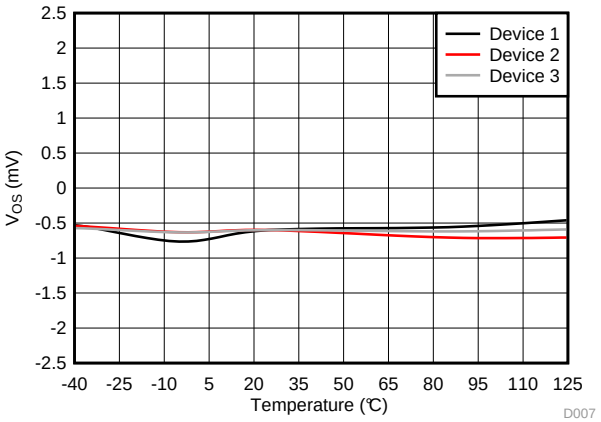
AMC1311-Q1

图 8. Input Offset Voltage vs Temperature



VDD1 = 5 V, AMC1311B-Q1

图 9. Input Offset Voltage vs Temperature

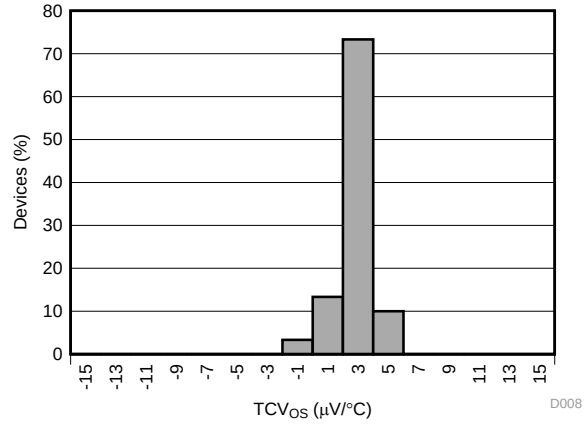


VDD1 = 3.3 V, AMC1311B-Q1

图 10. Input Offset Voltage vs Temperature

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)



AMC1311B-Q1

图 11. Input Offset Drift Histogram

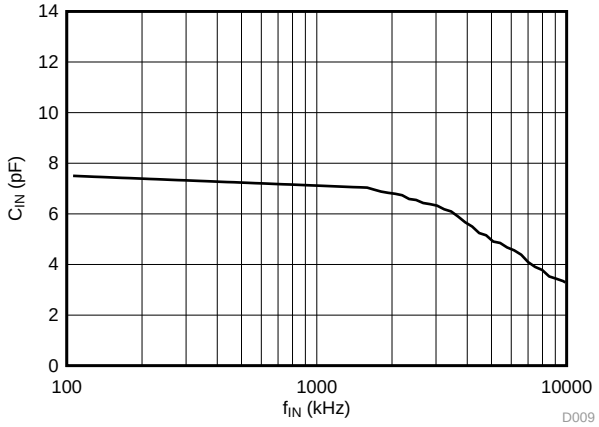
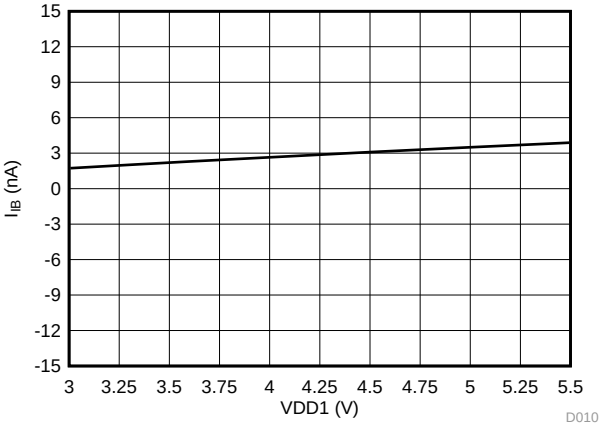


图 12. Input Capacitance vs Input Signal Frequency



3.0 V ≤ VDD1 < 4.5 V for the AMC1311B-Q1 only

图 13. Input Bias Current vs High-Side Supply Voltage

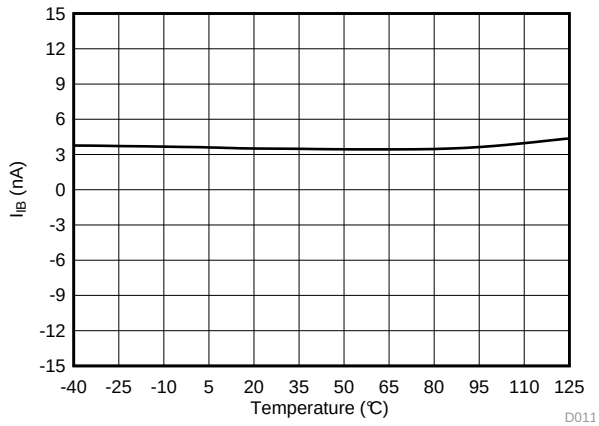
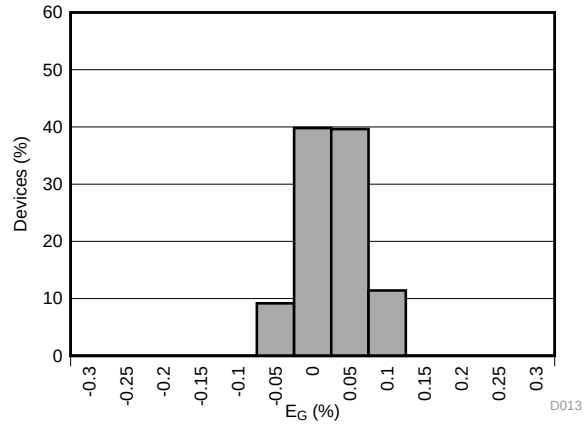
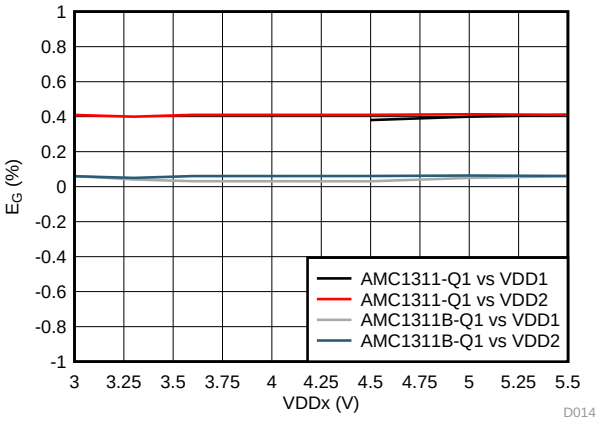


图 14. Input Bias Current vs Temperature



AMC1311B-Q1

图 15. Gain Error Histogram

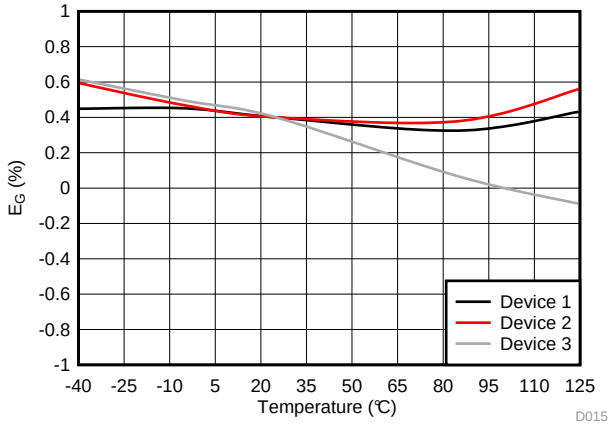


3.0 V ≤ VDD1 < 4.5 V for the AMC1311B-Q1 only

图 16. Gain Error vs Supply Voltage

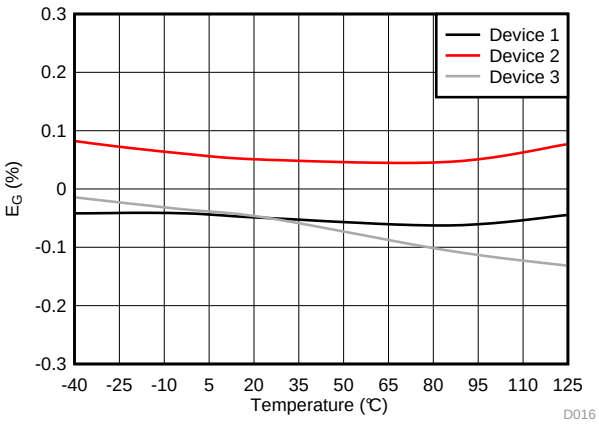
Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)



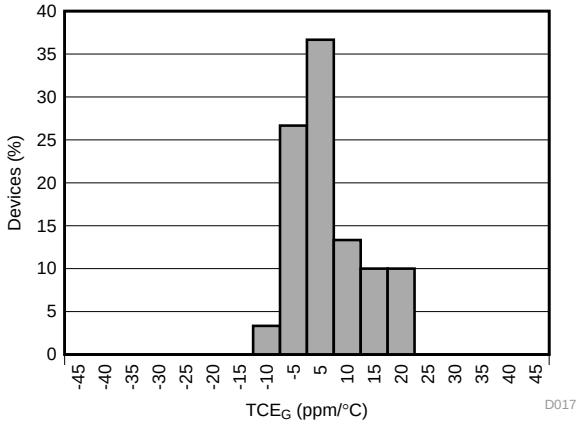
AMC1311-Q1

图 17. Gain Error vs Temperature



AMC1311B-Q1

图 18. Gain Error vs Temperature



AMC1311B-Q1

图 19. Gain Error Drift Histogram

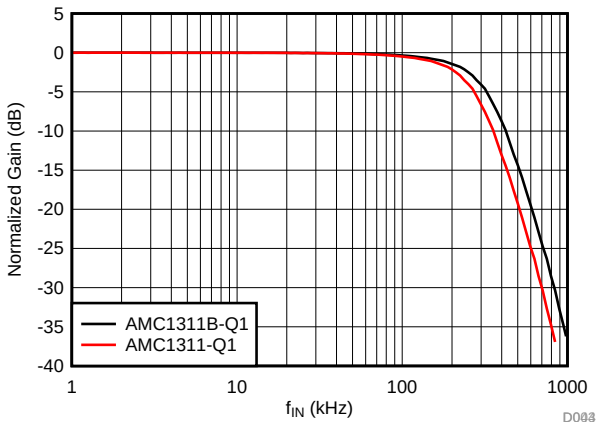


图 20. Normalized Gain vs Input Frequency

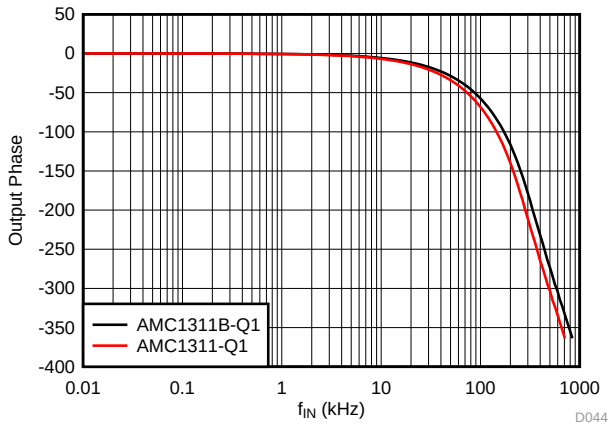


图 21. Output Phase vs Input Frequency

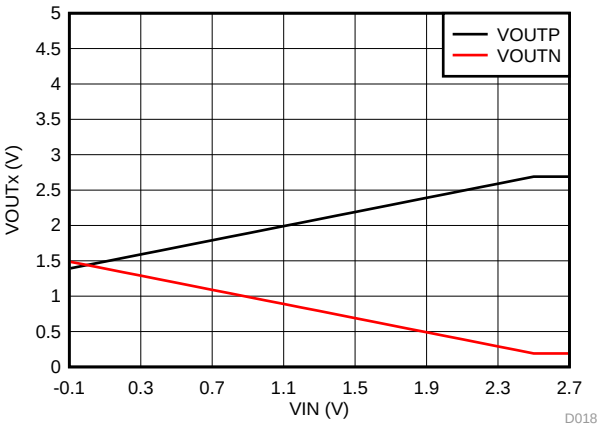


图 22. Output Voltage vs Input Voltage

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

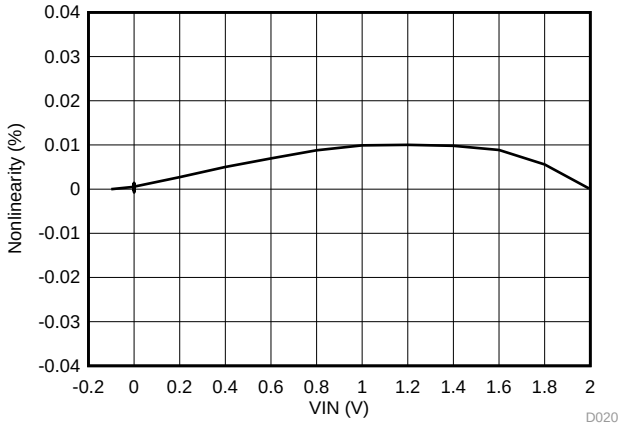
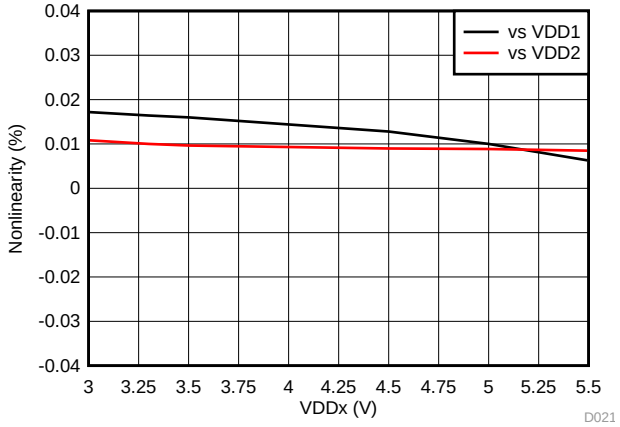


图 23. Nonlinearity vs Input Voltage



3.0 V ≤ VDD1 < 4.5 V for the AMC1311B-Q1 only

图 24. Nonlinearity vs Supply Voltage

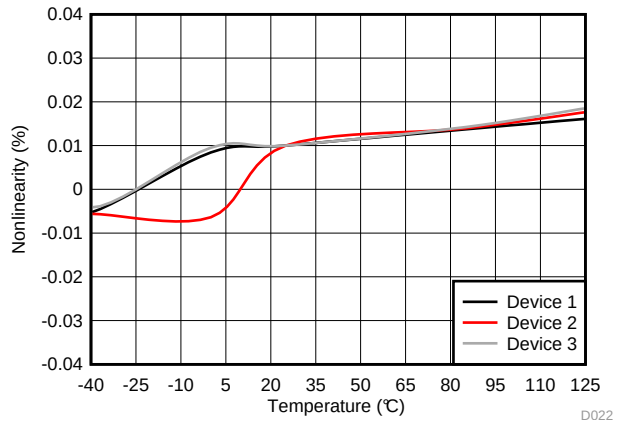
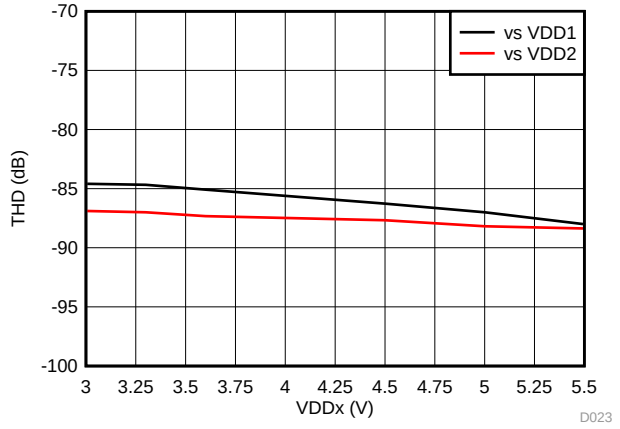


图 25. Nonlinearity vs Temperature



3.0 V ≤ VDD1 < 4.5 V for the AMC1311B-Q1 only

图 26. Total Harmonic Distortion vs Supply Voltage

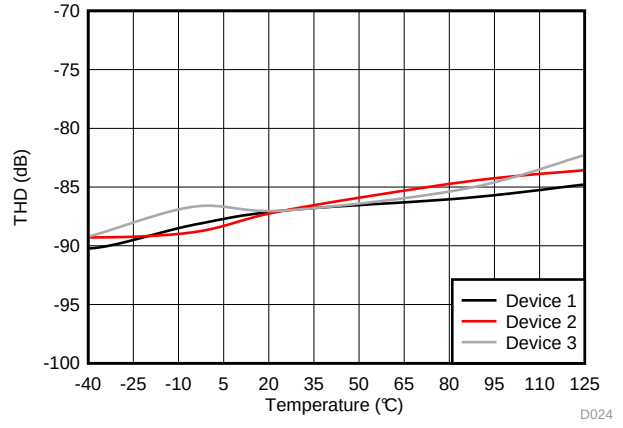


图 27. Total Harmonic Distortion vs Temperature

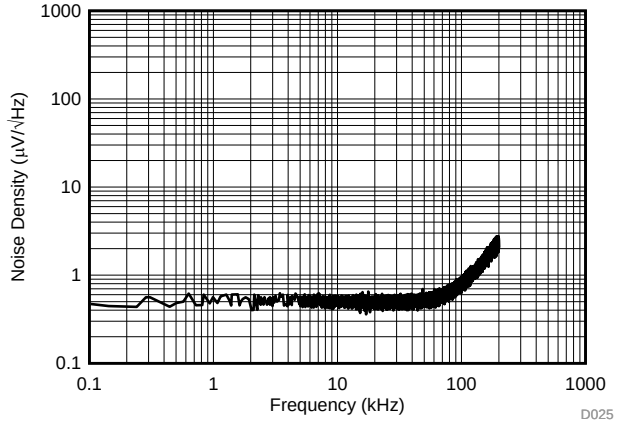


图 28. Input-Referred Noise Density vs Frequency

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

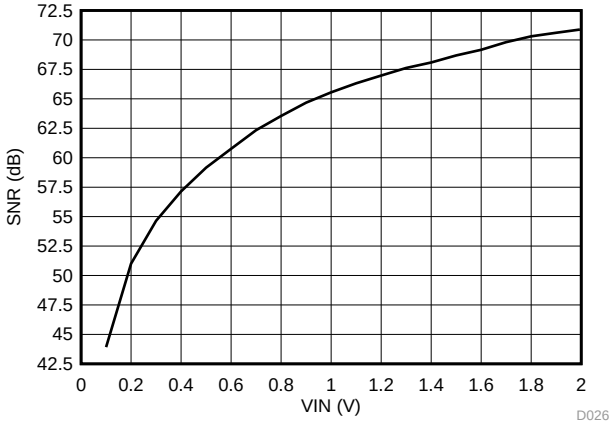
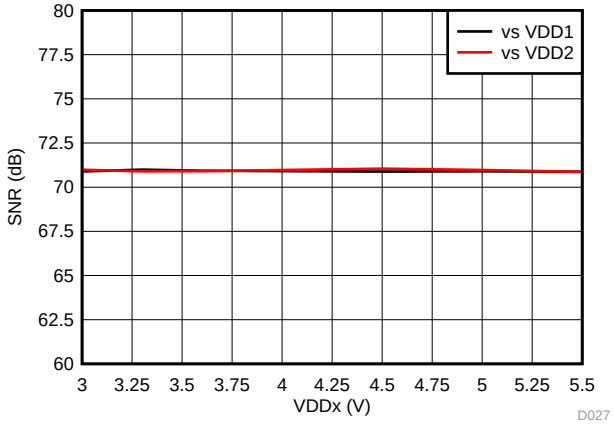


图 29. Signal-to-Noise Ratio vs Input Voltage



3.0 V ≤ VDD1 < 4.5 V for the AMC1311B-Q1 only

图 30. Signal-to-Noise Ratio vs Supply Voltage

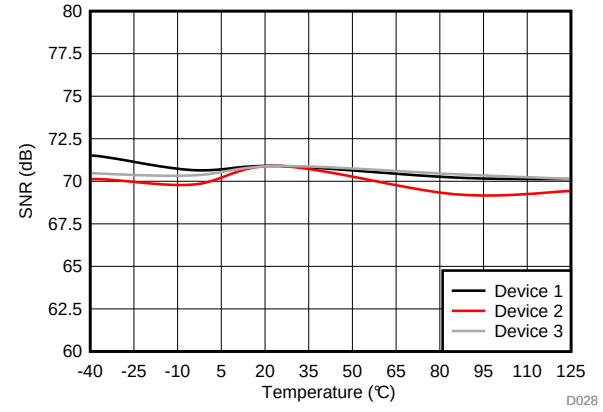
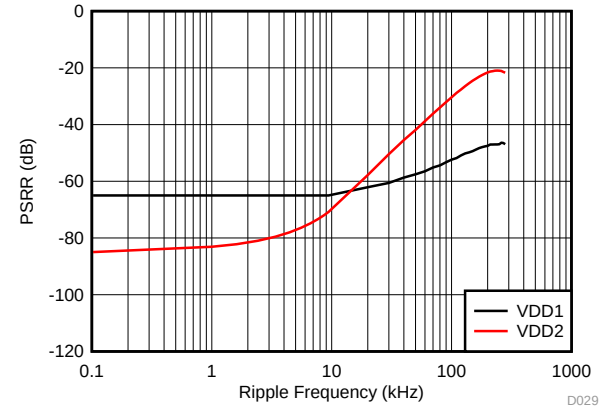


图 31. Signal-to-Noise Ratio vs Temperature



100-mV ripple

图 32. Power-Supply Rejection Ratio vs Ripple Frequency

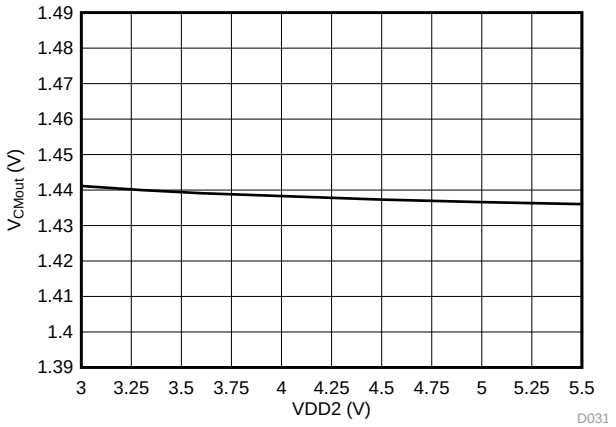


图 33. Output Common-Mode Voltage vs Low-Side Supply Voltage

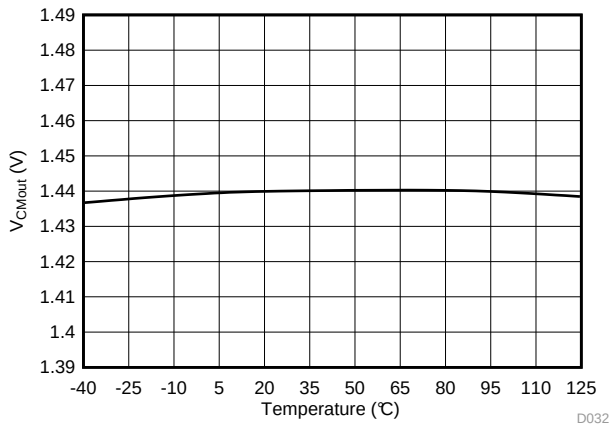


图 34. Output Common-Mode Voltage vs Temperature

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

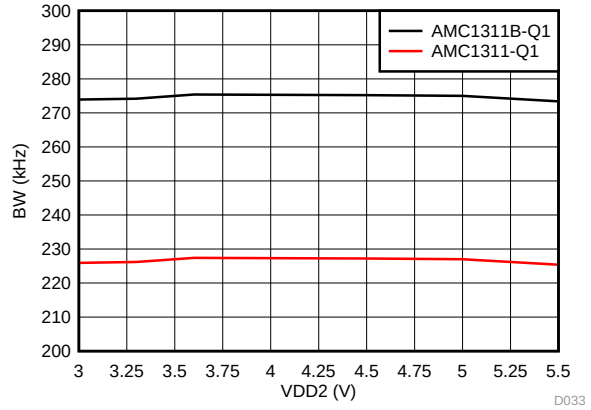


图 35. Output Bandwidth vs Low-Side Supply Voltage

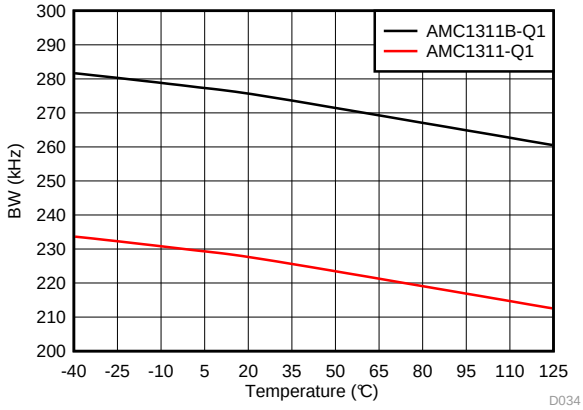
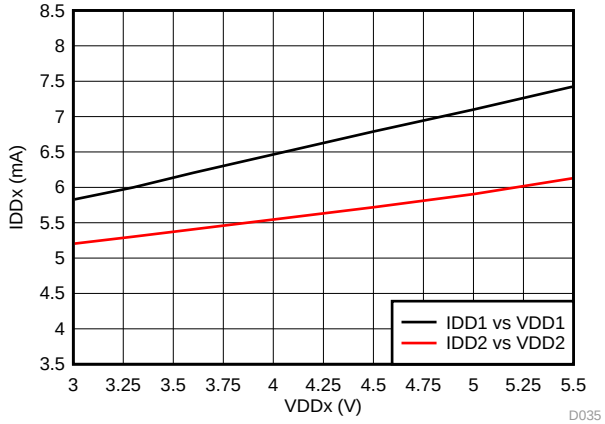


图 36. Output Bandwidth vs Temperature



3.0 V ≤ VDD1 < 4.5 V for the AMC1311B-Q1 only

图 37. Supply Current vs Supply Voltage

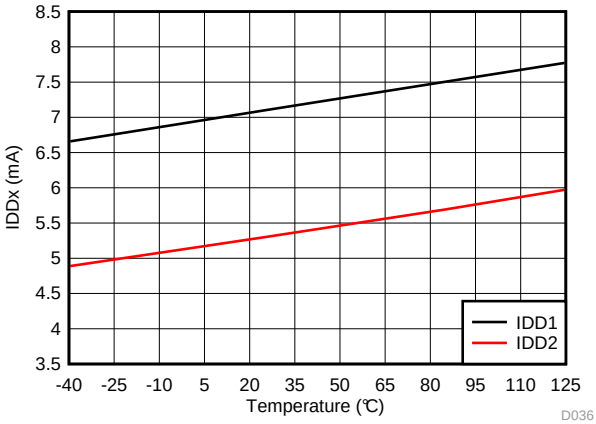


图 38. Supply Current vs Temperature

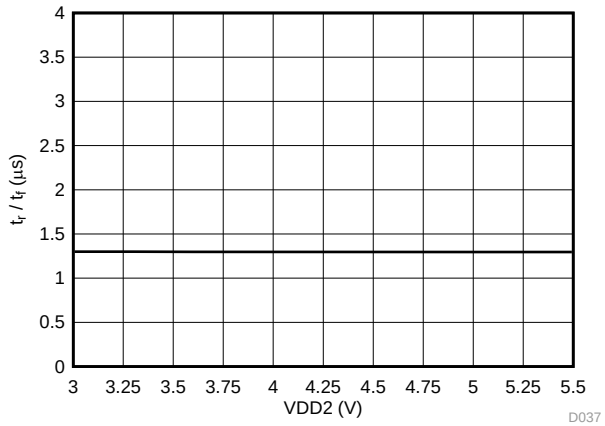


图 39. Output Rise and Fall Time vs Low-Side Supply Voltage

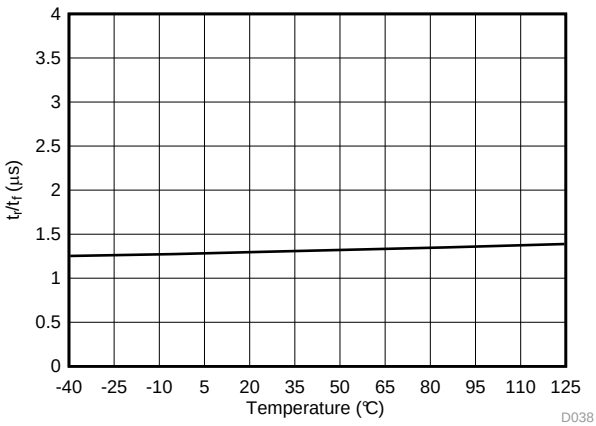
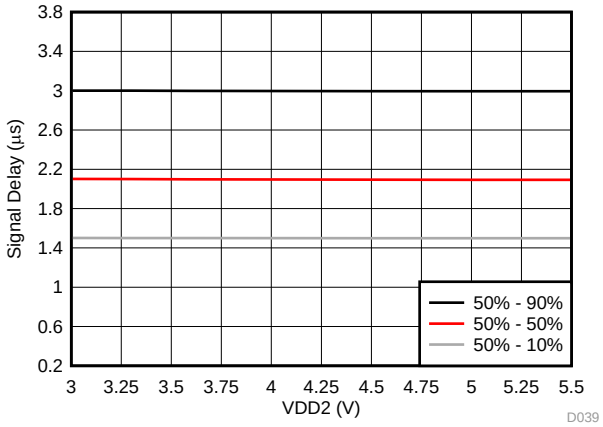


图 40. Output Rise and Fall Time vs Temperature

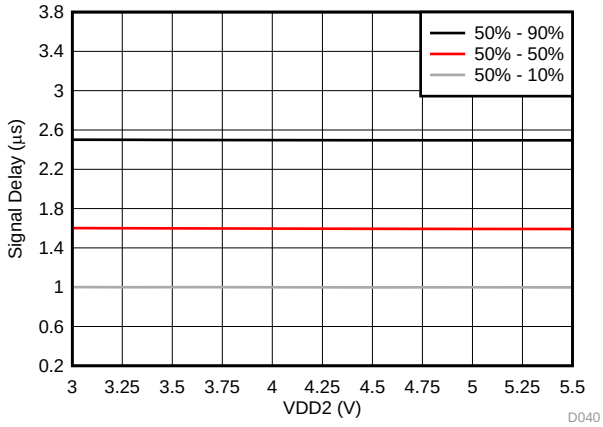
Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)



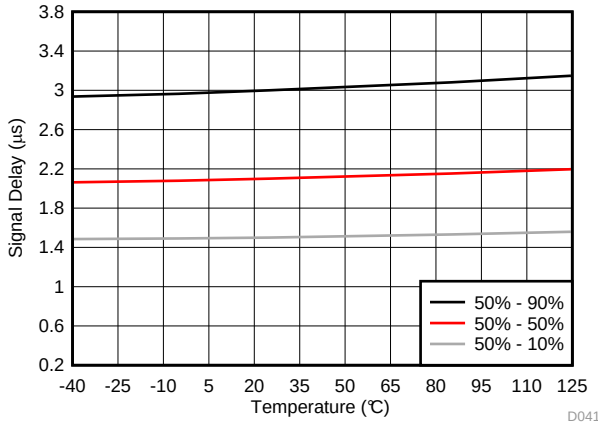
AMC1311-Q1

图 41. VIN to VOUTP, VOUTN Signal Delay vs Low-Side Supply Voltage



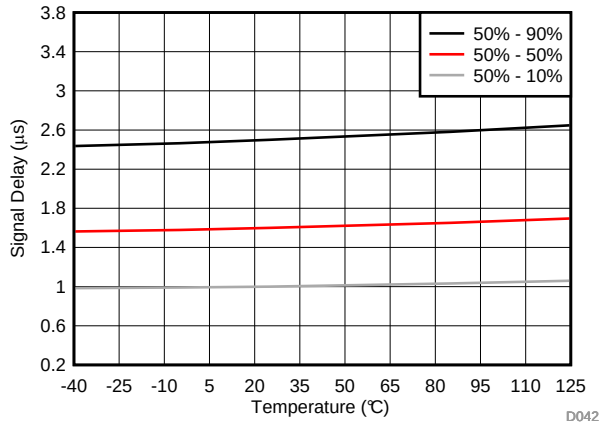
AMC1311B-Q1

图 42. VIN to VOUTP, VOUTN Signal Delay vs Low-Side Supply Voltage



AMC1311-Q1

图 43. VIN to VOUTP, VOUTN Signal Delay vs Temperature



AMC1311B-Q1

图 44. VIN to VOUTP, VOUTN Signal Delay vs Temperature

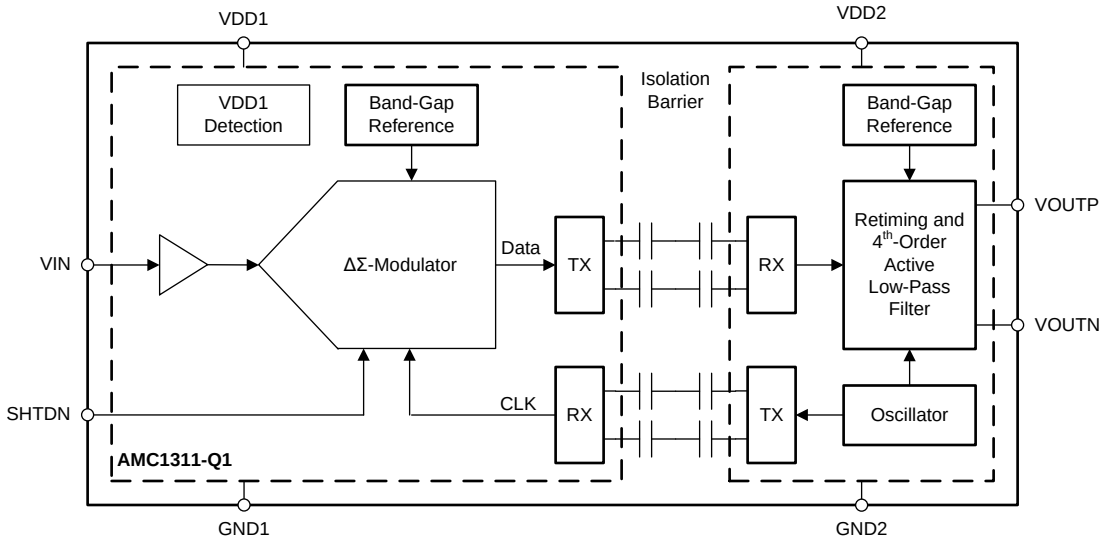
8 Detailed Description

8.1 Overview

The AMC1311-Q1 is a precision, isolated amplifier with a high input-impedance and wide input-voltage range. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (termed *TX* in the *Functional Block Diagram* section) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential analog output.

The SiO_2-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in *ISO72x Digital Isolator Magnetic-Field Immunity*. The digital modulation used in the AMC1311-Q1 and the isolation barrier characteristics result in high reliability and common-mode transient immunity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The input stage of the AMC1311-Q1 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section. The high-impedance, and low bias-current input of the AMC1311-Q1 makes the device suitable for isolated voltage sensing applications. 图 45 depicts the equivalent input structure of the AMC1311-Q1 with the relevant components.

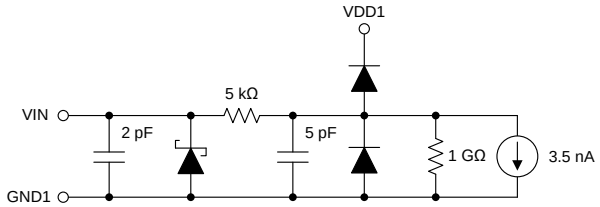


图 45. Equivalent Analog Input Circuit

Feature Description (接下页)

There are two restrictions on the analog input signal, VIN. First, if the input voltage VIN exceeds the voltage of 6.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) protection turns on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (V_{FSR}).

8.3.2 Isolation Channel Signal Transmission

The AMC1311-Q1 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. As shown in 图 46, the transmitter modulates the bitstream at TX IN with an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent the digital *zero*. The nominal frequency of the carrier used inside the AMC1311-Q1 is 480 MHz.

The receiver demodulates the signal after advanced signal conditioning and produces the output. The AMC1311-Q1 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

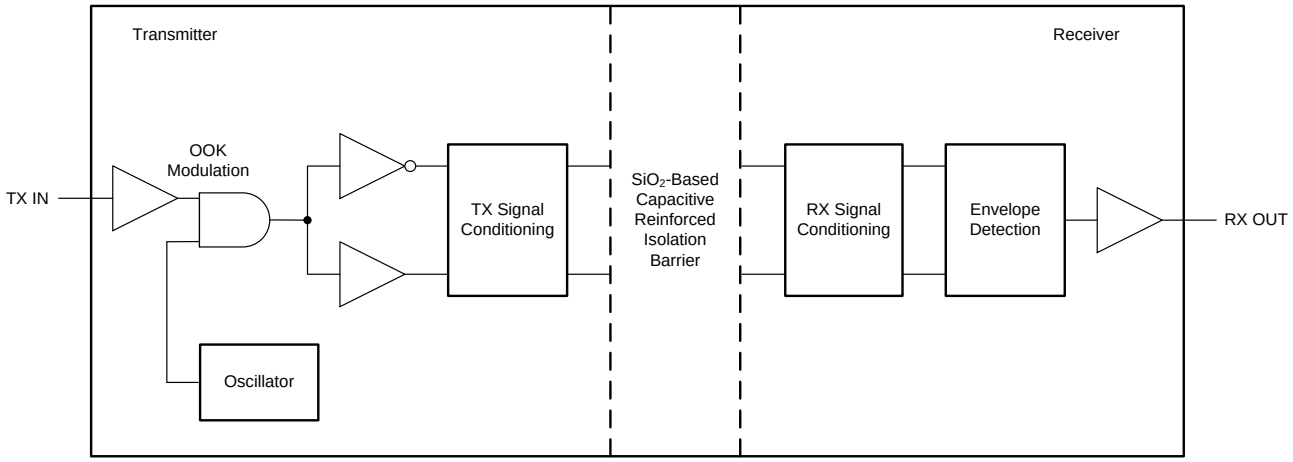


图 46. Block Diagram of an Isolation Channel

图 47 shows the concept of the OOK scheme.

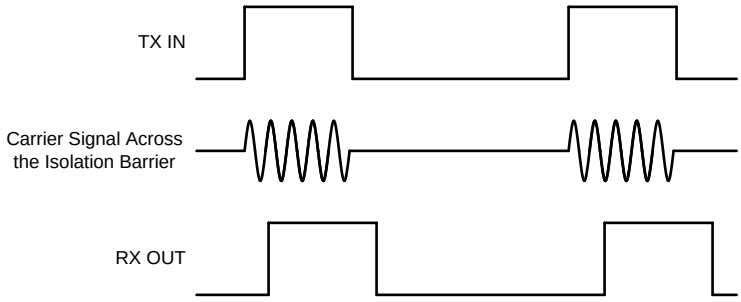


图 47. OOK-Based Modulation Scheme

Feature Description (接下页)

8.3.3 Fail-Safe Output

The AMC1311-Q1 offers a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active in three cases:

- When the high-side supply VDD1 of the AMC1311-Q1 device is missing
- When the high-side supply VDD1 falls under the $VDD1_{UV}$ undervoltage threshold level or
- When the SHTDN pin is pulled high

图 48 shows the fail-safe output of the AMC1311-Q1 that is a negative differential output voltage that does not occur under normal device operation. As a reference value for the fail-safe detection on a system level, use the $V_{FAILSAFE}$ voltage as specified in the *Electrical Characteristics* table.

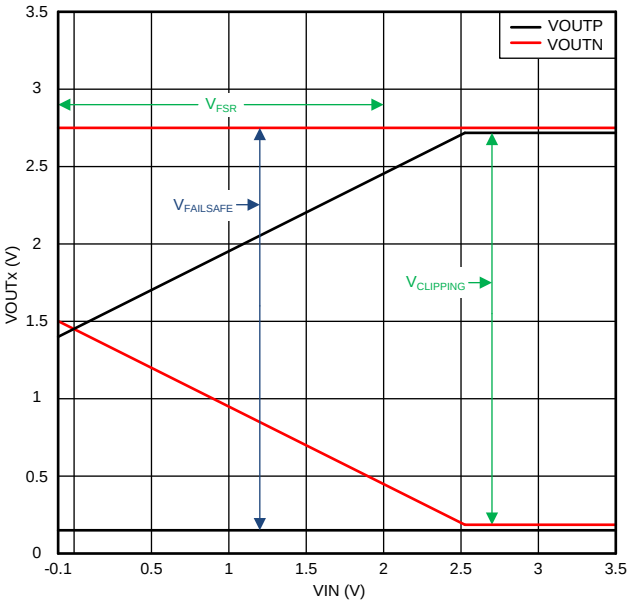


图 48. AMC1311-Q1 Output Behavior

8.4 Device Functional Modes

The AMC1311-Q1 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The very low input bias current, ac and dc errors, and temperature drift make the AMC1311-Q1 a high-performance solution for automotive applications where voltage measurement with high common-mode levels is required.

9.2 Typical Application

Isolated amplifiers are widely used in automotive applications such as traction inverters, on-board chargers, and dc/dc converters. The input structure of the AMC1311-Q1 is tailored for isolated voltage sensing using resistive dividers to reduce the high common-mode voltage.

图 49 depicts a typical use of the AMC1311-Q1 for dc bus voltage sensing in a traction inverter application. Phase current measurement is accomplished through the shunt resistors, R_{SHUNT} (in this case, two-pin shunts) and the AMC1301-Q1 isolated amplifiers that are optimized for isolated current sensing. The high-impedance input and the high common-mode transient immunity of the AMC1311-Q1 ensure reliable and accurate operation even in high-noise environments.

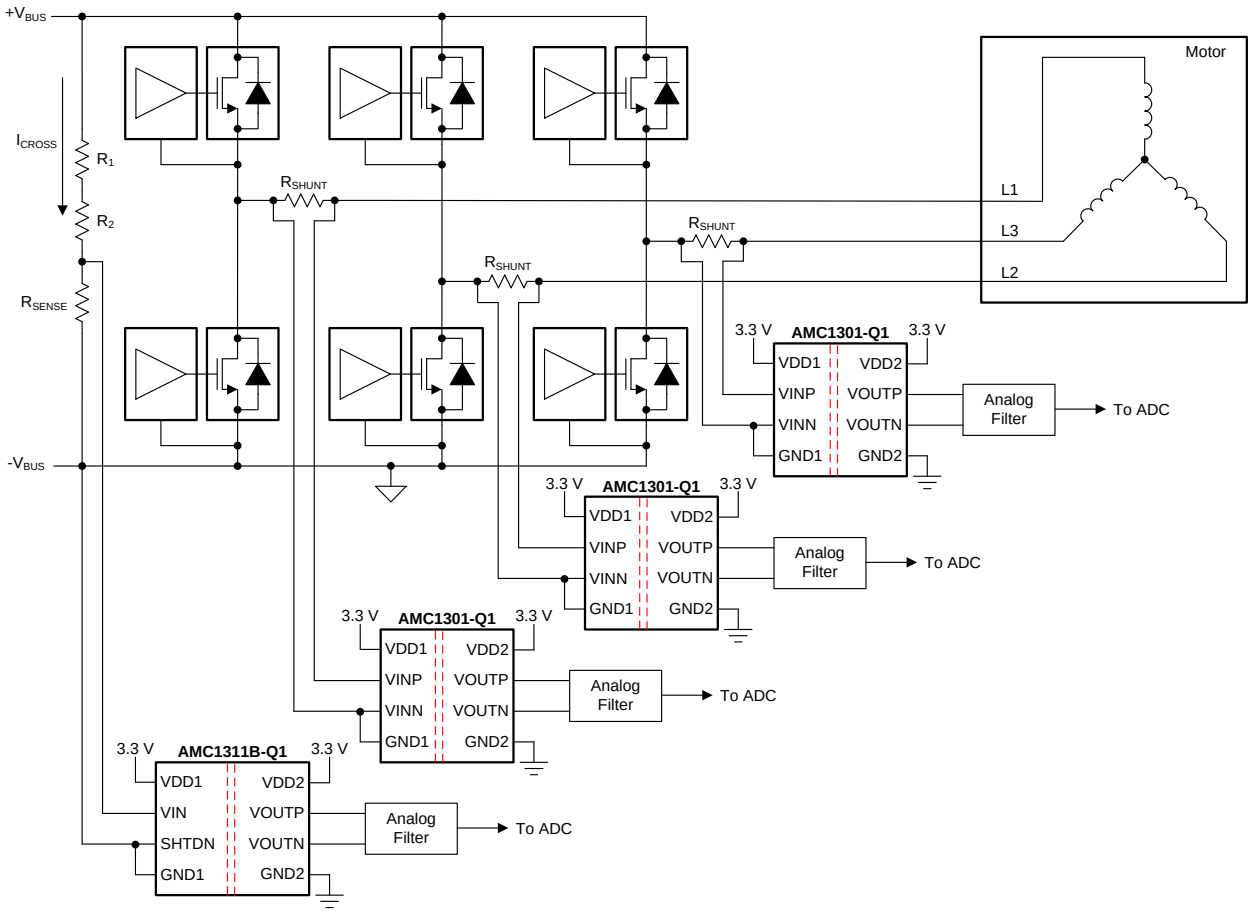


图 49. Using the AMC1311B-Q1 for DC Bus Voltage Sensing in Traction Inverters

Typical Application (接下页)

9.2.1 Design Requirements

表 1 lists the parameters for this typical application.

表 1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the sensing resistor for a linear response	2 V (maximum)
Current through the resistive divider, I_{CROSS}	0.1 mA (maximum)
Signal delay (50% VIN to 90% VOUTP, VOUTN)	3 µs (maximum)

9.2.2 Detailed Design Procedure

Use Ohm's Law to calculate the minimum total resistance of the resistive divider to limit the cross current to the desired value ($R_{TOTAL} = V_{BUS} / I_{CROSS}$) and the required sense resistor value to be connected to the AMC1311-Q1 input: $R_{SENSE} = V_{FSR} / I_{CROSS}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SENSE}:

- The voltage drop on R_{SENSE} caused by the nominal voltage range of the system must not exceed the recommended input voltage range: $V_{SENSE} \leq V_{FSR}$
- The voltage drop on R_{SENSE} caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: $V_{SENSE} \leq V_{Clipping}$

表 2 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 600 V and 800 V on the dc bus.

表 2. Resistor Value Examples

PARAMETER	600-V DC BUS	800-V DC Bus
Resistive divider resistor R_1	3.01 MΩ	4.22 MΩ
Resistive divider resistor R_2	3.01 MΩ	4.22 MΩ
Sense resistor R_{SENSE}	20 kΩ	21 kΩ
Resulting current through resistive divider I_{CROSS}	99.3 µA	94.5 µA
Resulting voltage drop on sense resistor V_{SENSE}	1.987 V	1.986 V

For systems using single-ended input ADCs, 图 50 shows an example of a TLV313-Q1-based signal conversion and filter circuit as used on the AMC1311EVM. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

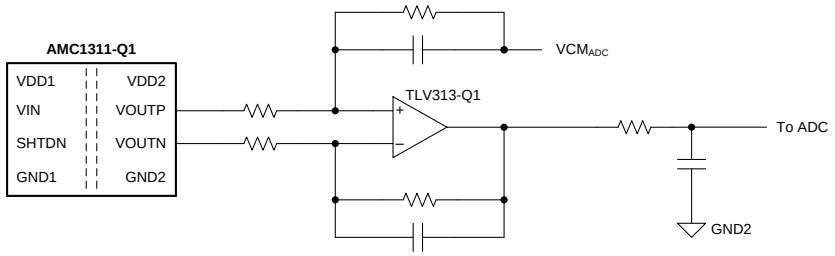


图 50. Connecting the AMC1311-Q1 Output to Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power*, available for download at www.ti.com.

9.2.3 Application Curve

In traction inverter applications, the power switches must be protected in case of an overvoltage condition. To allow for fast system power-off, a low delay caused by the isolated amplifier is required. 图 51 shows the typical full-scale step response of the AMC1311-Q1. Consider the delay of the required window comparator and the MCU to calculate the overall response time of the system.

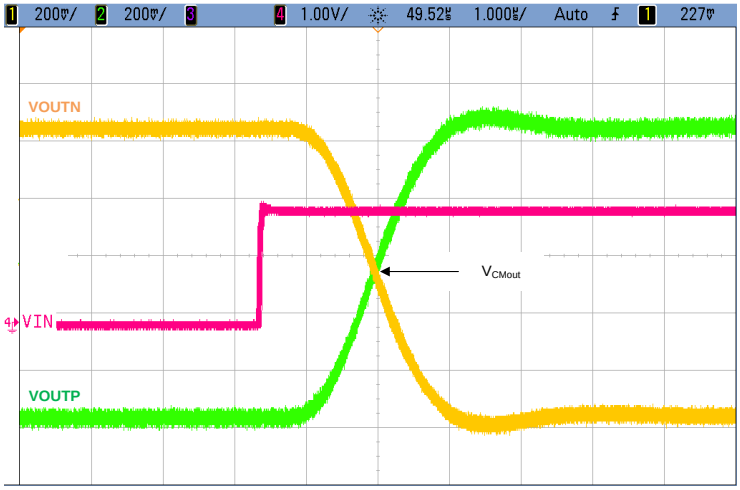


图 51. Step Response of the AMC1311B-Q1

9.3 Do's and Don'ts

Do not leave the analog input VIN of the AMC1311-Q1 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current may generate a negative input voltage that exceeds the specified input voltage range and the output of the device is invalid.

10 Power Supply Recommendations

In a typical traction inverter application, the high-side power supply (VDD1) for the AMC1311-Q1 is generated from the low-side supply (VDD2) of the device by an isolated dc/dc converter circuit. A low-cost solution is based on the push-pull driver SN6501-Q1 and a transformer that supports the desired isolation voltage ratings. TI recommends using a low-ESR decoupling capacitor of 0.1 µF and an additional capacitor of minimum 1 µF for both supplies of the AMC1311-Q1. Place these decoupling capacitors as close as possible to the AMC1311-Q1 power-supply pins to minimize supply current loops and electromagnetic emissions.

The AMC1311-Q1 does not require any specific power up sequencing. Consider the analog settling time t_{AS} as specified in the *Switching Characteristics* table after ramp up of the VDD1 high-side supply.

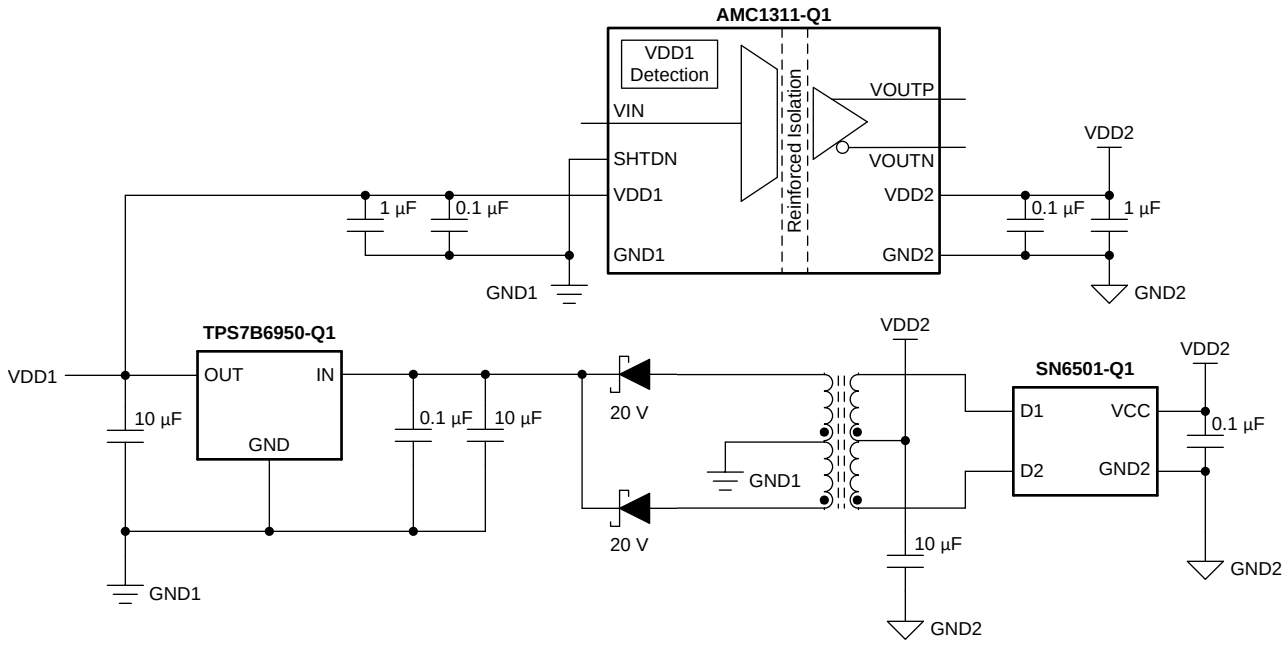


图 52. SN6501-Q1-Based, High-Side Power Supply

11 Layout

11.1 Layout Guidelines

For best performance, place the smaller 0.1-µF decoupling capacitors (C1 and C6) as close as possible to the AMC1311-Q1 power-supply pins, followed by the additional C2 and C5 capacitors with a minimum value of 1 µF. The resistors and capacitors used for the analog input (C3) and output filters (R5, R10, and C13) are placed next to the decoupling capacitors. Use 1206-size, SMD-type, ceramic decoupling capacitors and route the traces to the VIN and SHTDN pins underneath. Connect the supply voltage sources in a way that allows the supply current to flow through the pads of the decoupling capacitors before powering the AMC1311-Q1.

图 53 shows this approach as implemented on the AMC1311EVM. Capacitors C5 and C6 decouple the high-side supply VDD1 while capacitors C1 and C2 are used to support the low-side supply VDD2 of the AMC1311-Q1.

11.2 Layout Example

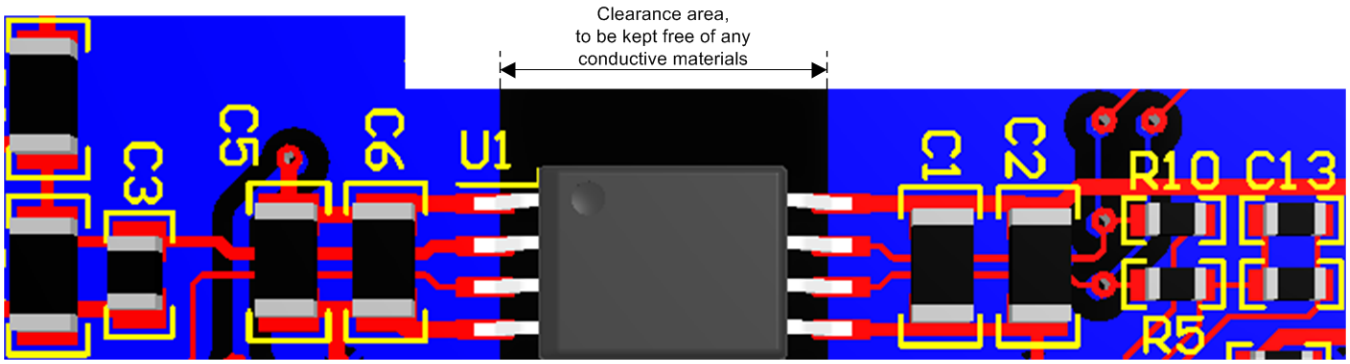


图 53. Recommended Layout of the AMC1311-Q1

12 器件和文档支持

12.1 文档支持

12.1.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.1.2 相关文档

请参阅如下相关文档：

- *隔离相关术语*
- *《ADC121S101x-Q1 单通道、0.5 至 1Msps、12 位模数转换器》*
- *半导体和集成电路 (IC) 封装热度量*
- *《ISO72x 数字隔离器磁场抗扰度》*
- *《具有 ±250mV 输入电压、3μs 延迟的 AMC1301-Q1 高精度增强隔离放大器》*
- *《适用于成本敏感型系统的 TLV313-Q1 低功耗、轨至轨输入/输出、750μV 典型偏移电压、1MHz 运算放大器》*
- *《AMC1311EVM 用户指南》*
- *《针对最低失真和最低噪声进行优化的 18 位 1MSPS 数据采集模块 (DAQ)》*
- *《针对最低功耗进行优化的 18 位 1MSPS 数据采集模块 (DAQ)》*
- *《用于隔离电源的 SN6501-Q1 变压器驱动器》*

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

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12.5 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1311BQDWVQ1	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	1311BQ1	Samples
AMC1311BQDWVRQ1	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	1311BQ1	Samples
AMC1311QDWVQ1	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	1311Q1	Samples
AMC1311QDWVRQ1	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	1311Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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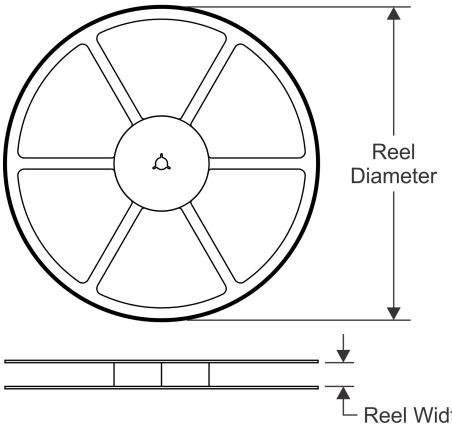
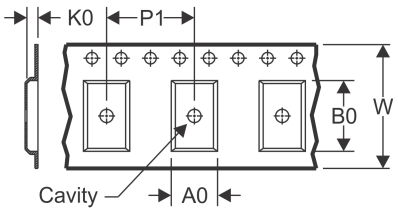
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

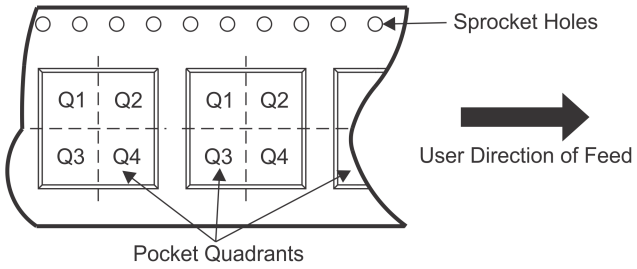


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

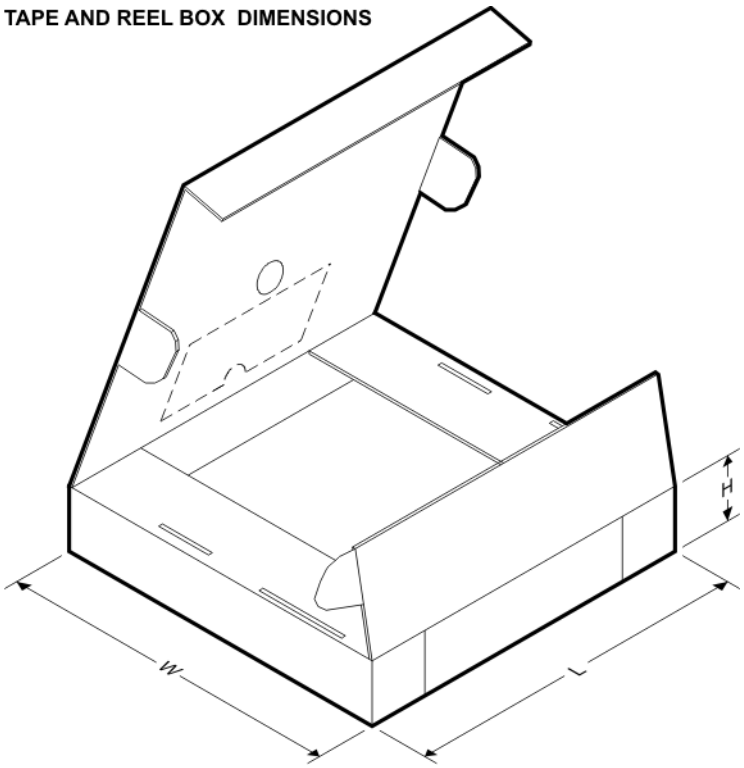
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

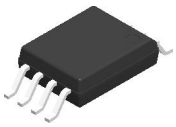
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1311BQDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1311QDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

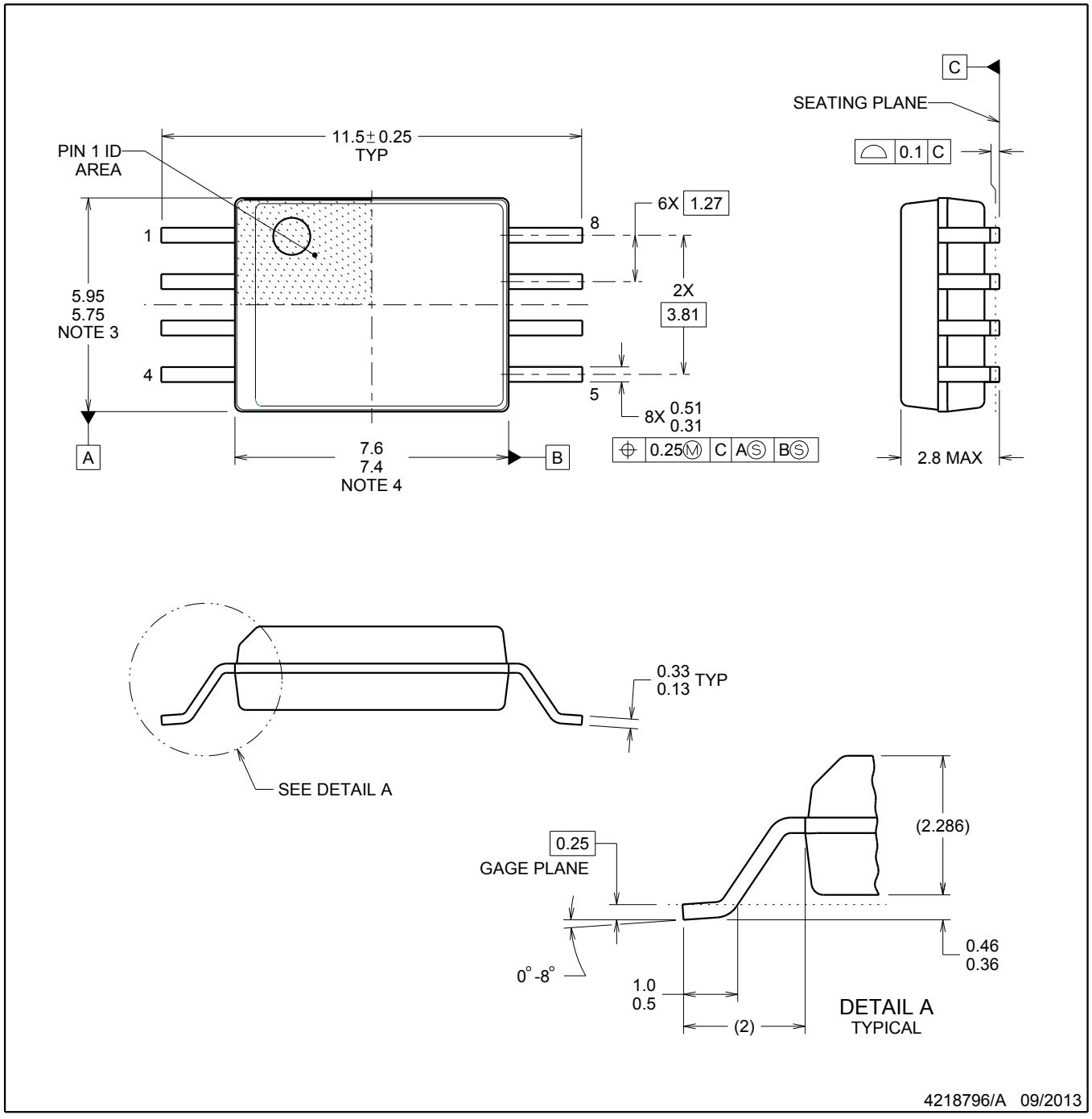
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1311BQDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1311QDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0



DWV0008A

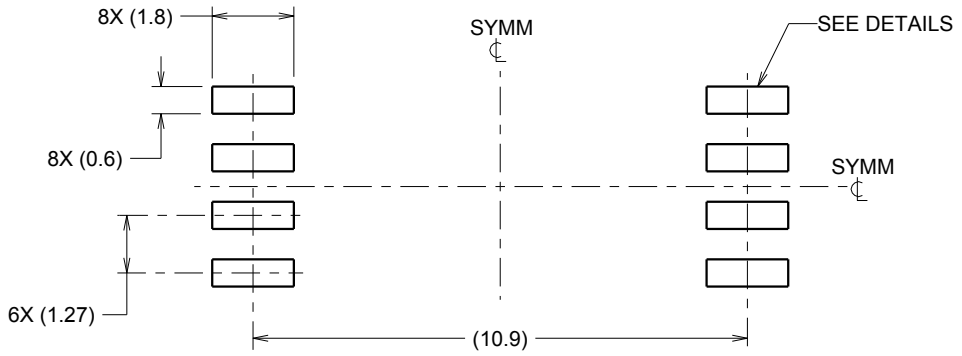
SOIC - 2.8 mm max height

SOIC

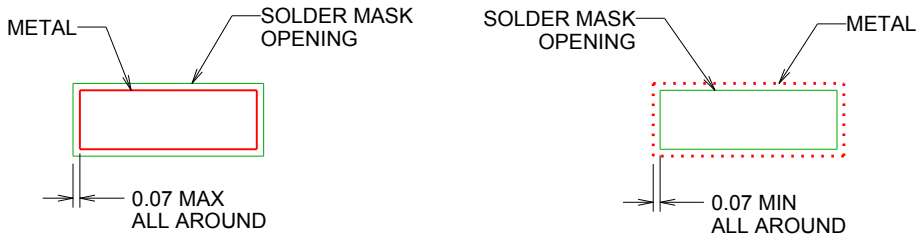


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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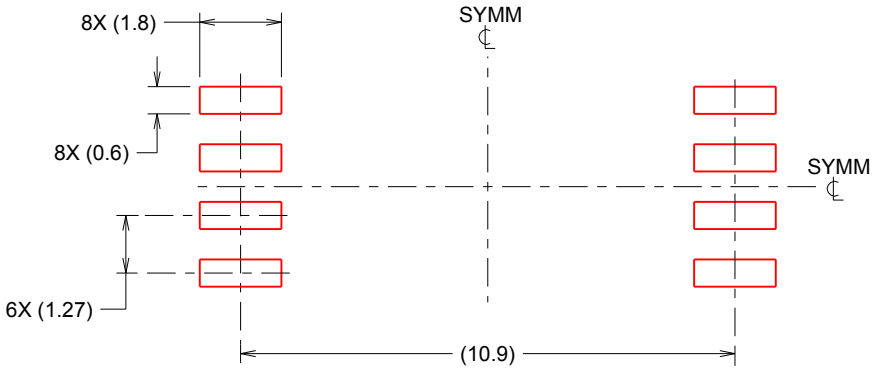
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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