

SN54AS286, SN74AS286 9-BIT PARITY GENERATORS/CHECKERS WITH BUS-DRIVER PARITY I/O PORT

SDAS050B – DECEMBER 1983 – REVISED DECEMBER 1994

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity
- Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port
- Glitch-Free Bus During Power Up/Down
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

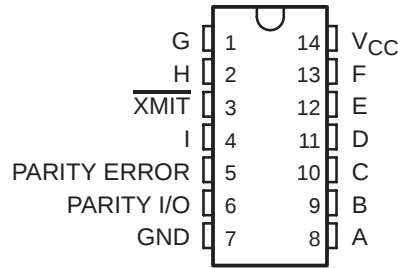
The SN54AS286 and SN74AS286 universal 9-bit parity generators/checkers feature a local output for parity checking and a 48-mA bus-driving parity input/output (I/O) port for parity generation/checking. The word-length capability is easily expanded by cascading.

The transmit ($\overline{\text{XMIT}}$) control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low, the parity tree is disabled and PARITY ERROR remains at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high, the parity tree is enabled. PARITY ERROR indicates a parity error when either an even number of inputs (A–I) are high and PARITY I/O is forced to a low logic level, or when an odd number of inputs are high and PARITY I/O is forced to a high logic level.

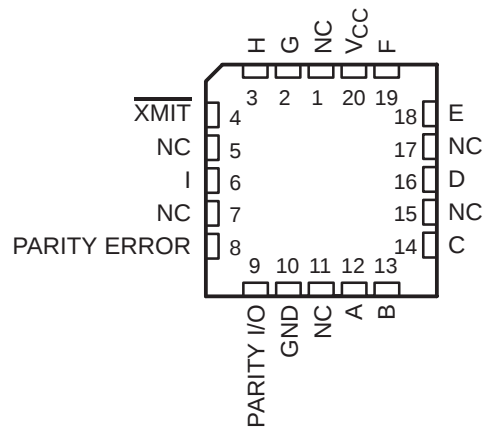
The I/O control circuitry was designed so that the I/O port remains in the high-impedance state during power up or power down to prevent bus glitches.

The SN54AS286 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS286 is characterized for operation from 0°C to 70°C .

SN54AS286 . . . J PACKAGE
SN74AS286 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS286 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

NUMBER OF INPUTS (A–I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	L	H	H
1, 3, 5, 7, 9	L	L	H
0, 2, 4, 6, 8	h	h	H
	h	L	L
1, 3, 5, 7, 9	h	h	L
	h	L	H

h = high input level
H = high output level

L = low input level
L = low output level

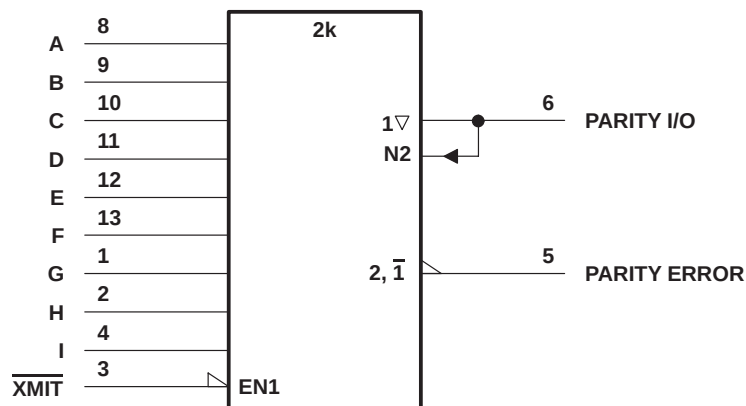
SN54AS286, SN74AS286

9-BIT PARITY GENERATORS/CHECKERS

WITH BUS-DRIVER PARITY I/O PORT

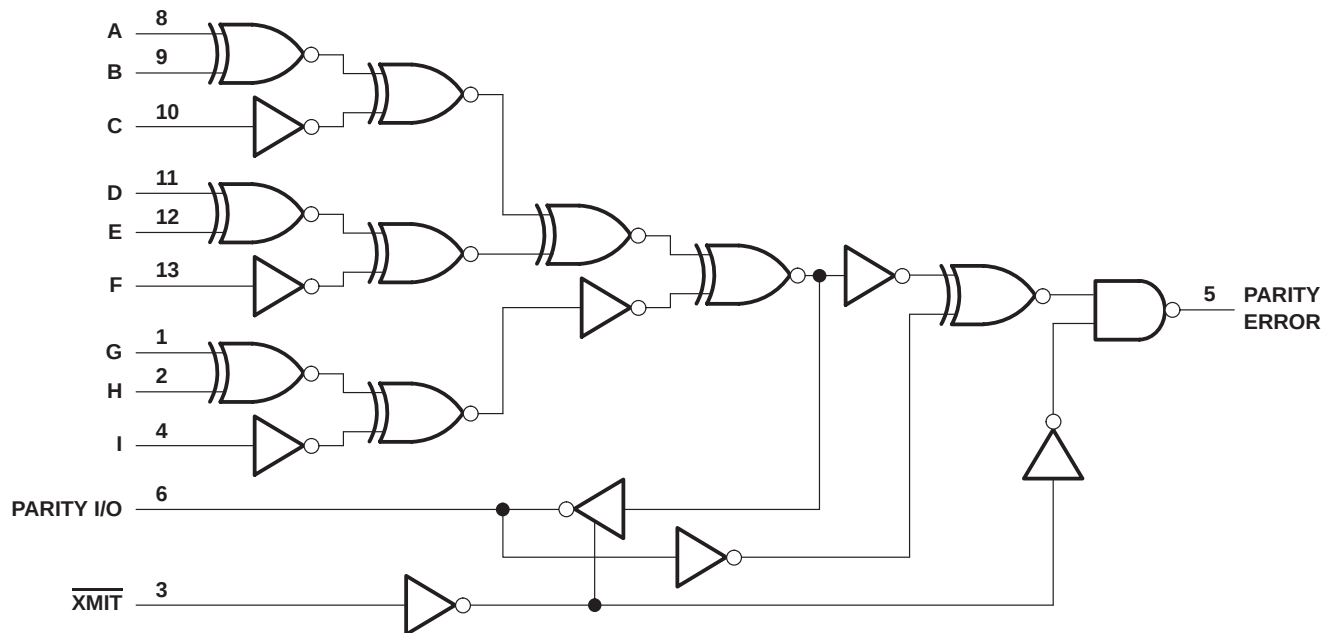
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54AS286	–55°C to 125°C
SN74AS286	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS286			SN74AS286			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
I _{OH}	High-level output current	PARITY ERROR	−2			−2			mA
		PARITY I/O	−12			−15			
I _{OL}	Low-level output current	PARITY ERROR	20			20			mA
		PARITY I/O	32			48			
T _A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS286			SN74AS286			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = 4.5 V,	I _I = –18 mA	–1.2			–1.2			V
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = –2 mA	V _{CC} – 2			V _{CC} – 2			V
	PARITY I/O	V _{CC} = 4.5 V	I _{OH} = –3 mA	2.4	2.9		2.4	3		
			I _{OH} = –12 mA	2.4						
			I _{OH} = –15 mA				2.4			
V _{OL}	PARITY ERROR	V _{CC} = 4.5 V	I _{OL} = 20 mA	0.35	0.5		0.35	0.5	V	
	PARITY I/O		I _{OL} = 32 mA		0.5					
			I _{OL} = 48 mA				0.5			
I _I	PARITY I/O	V _{CC} = 5.5 V	V _I = 5.5 V		0.1		0.1	mA		
	All other inputs		V _I = 7 V		0.1		0.1			
I _{IH}	PARITY I/O [§]	V _{CC} = 5.5 V,	V _I = 2.7 V		50		50	μA		
	All other inputs				20		20			
I _{IL}	PARITY I/O [§]	V _{CC} = 5.5 V,	V _I = 0.4 V		–0.5		–0.5	mA		
	All other inputs				–0.5		–0.5			
I _O [¶]		V _{CC} = 5.5 V,	V _O = 2.25 V	–30	–112	–30	–112	mA		
I _{CC}	Transmit	V _{CC} = 5.5 V		30	43		30	43	mA	
	Receive			35	50		35	50		

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[§] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

^{||} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



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switching characteristics (see Figure 3)

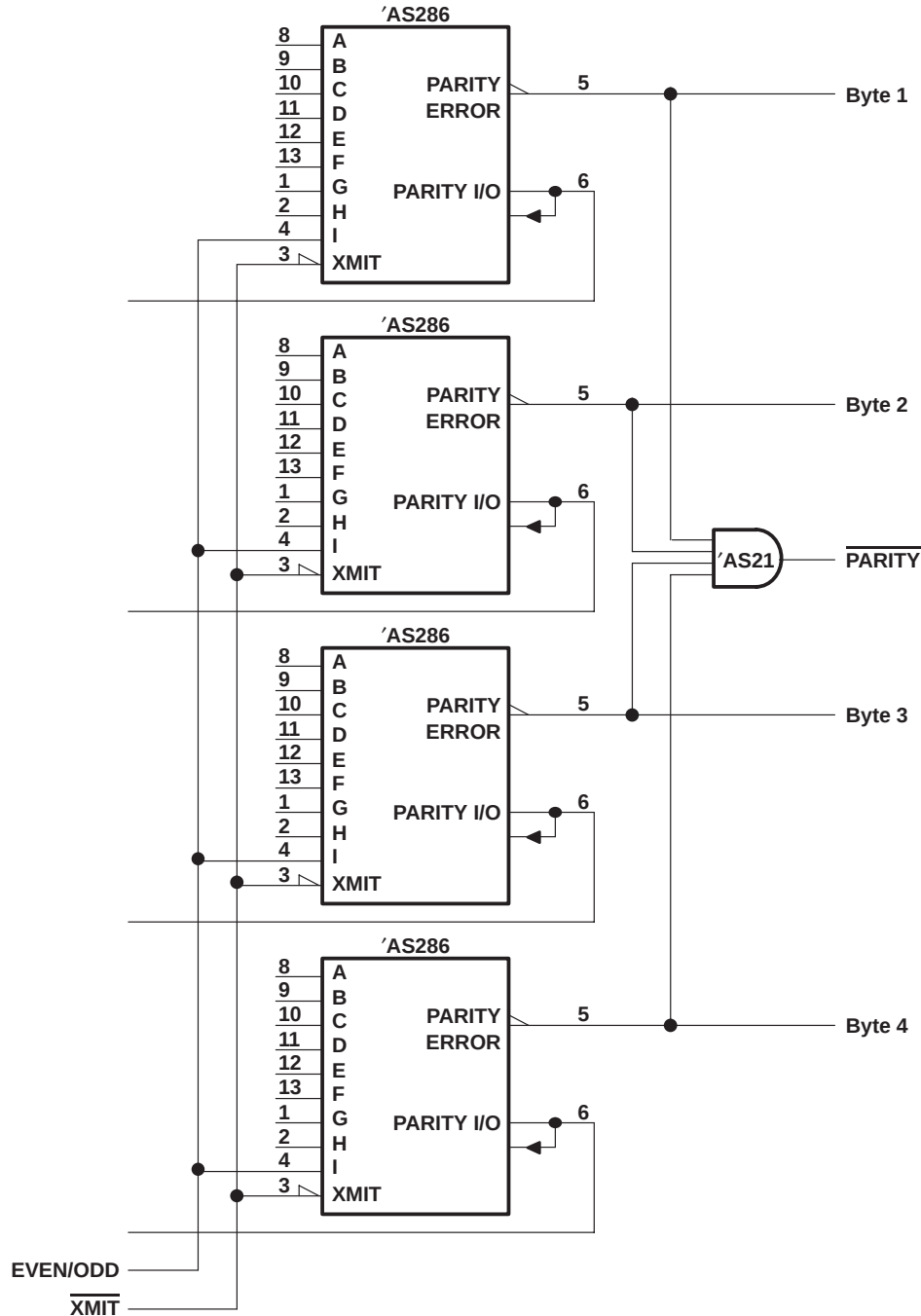
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS286		SN74AS286		
			MIN	MAX	MIN	MAX	
t _{PLH}	Any A – I	PARITY I/O	3	17	3	15	ns
t _{PHL}			3	15	3	14	
t _{PLH}	Any A – I	PARITY ERROR	3	20	3	16.5	ns
t _{PHL}			3	18	3	16.5	
t _{PLH}	PARITY I/O	PARITY ERROR	3	10	3	9	ns
t _{PHL}			3	10	3	9	
t _{PZH}	$\overline{\text{XMIT}}$	PARITY I/O	3	14	3	13	ns
t _{PZL}			3	17	3	16	
t _{PHZ}	$\overline{\text{XMIT}}$	PARITY I/O	3	13	3	11.5	ns
t _{PLZ}			3	11	3	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



APPLICATION INFORMATION

Figure 1 shows a 32-bit parity generator/checker with output polarity switching, parity-error detection, and parity on every byte.



Pin numbers shown are for the D, J, and N packages.

Figure 1. 32-Bit Parity Generator/Checker

SN54AS286, SN74AS286

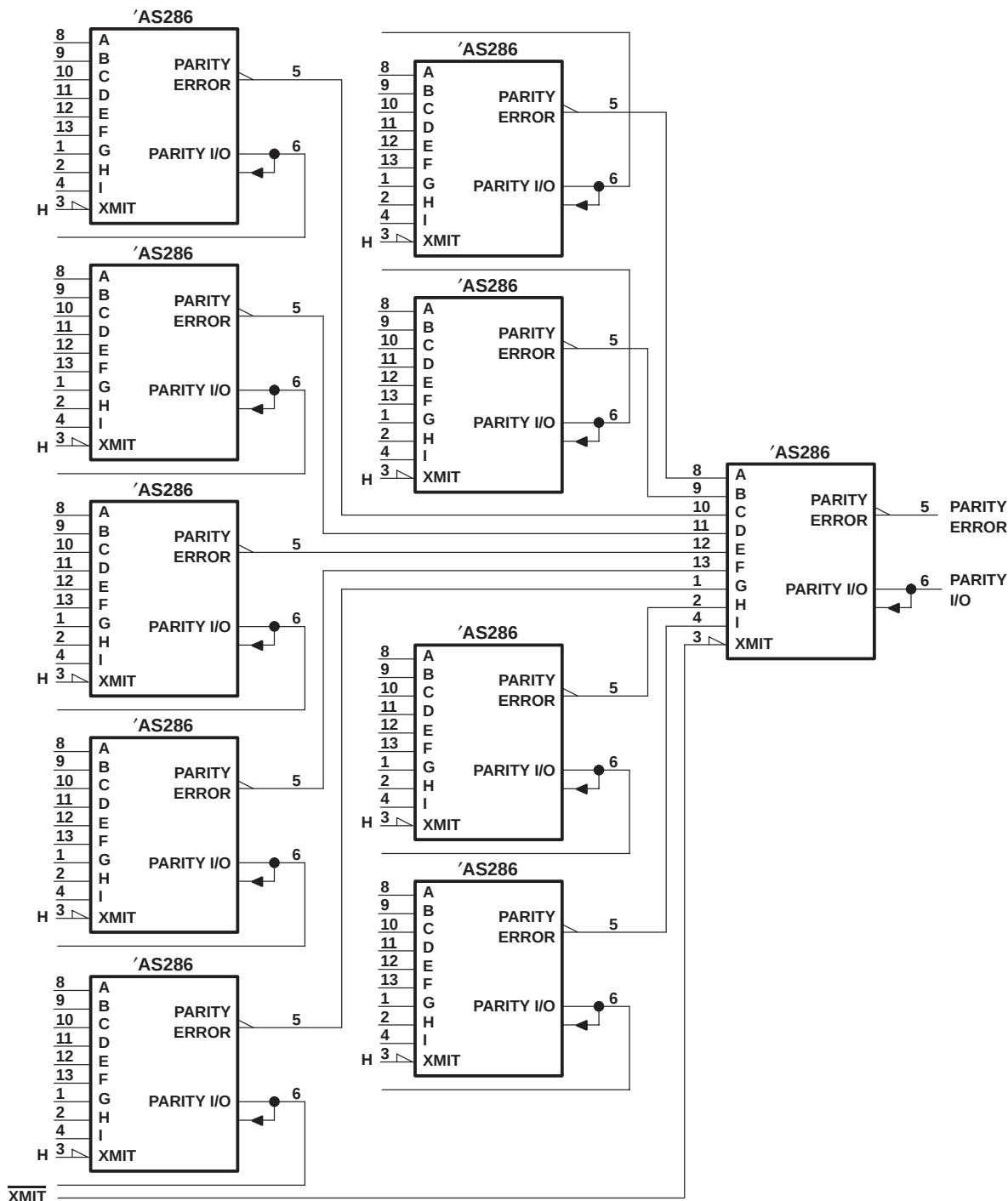
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APPLICATION INFORMATION

Figure 2 shows a 90-bit parity generator/checker with $\overline{\text{XMIT}}$ on the last stage available for use with parity detection.



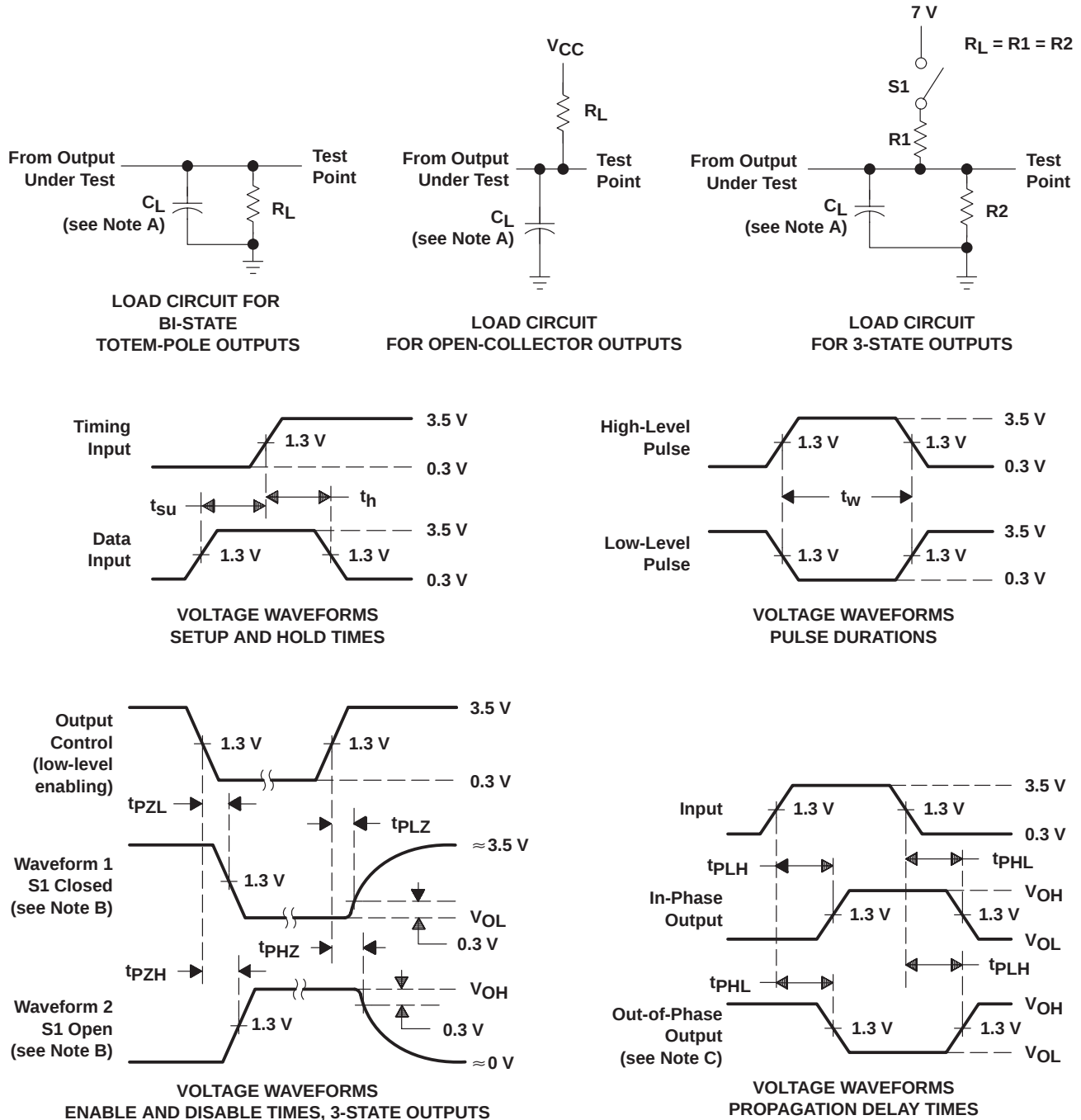
Pin numbers shown are for the D, J, and N packages.

Figure 2. 90-Bit Parity Generator/Checker With Parity-Error Detection



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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AS286D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS286	Samples
SN74AS286N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS286N	Samples
SN74AS286NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS286N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

10-Dec-2020

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

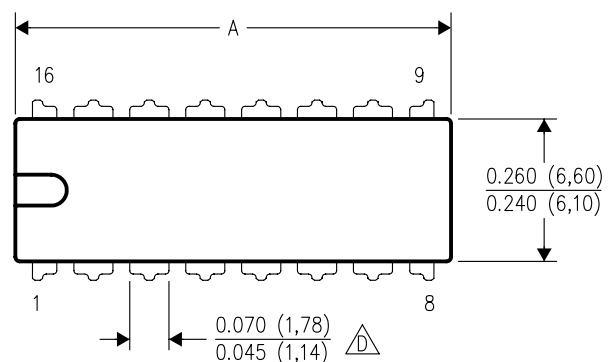


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

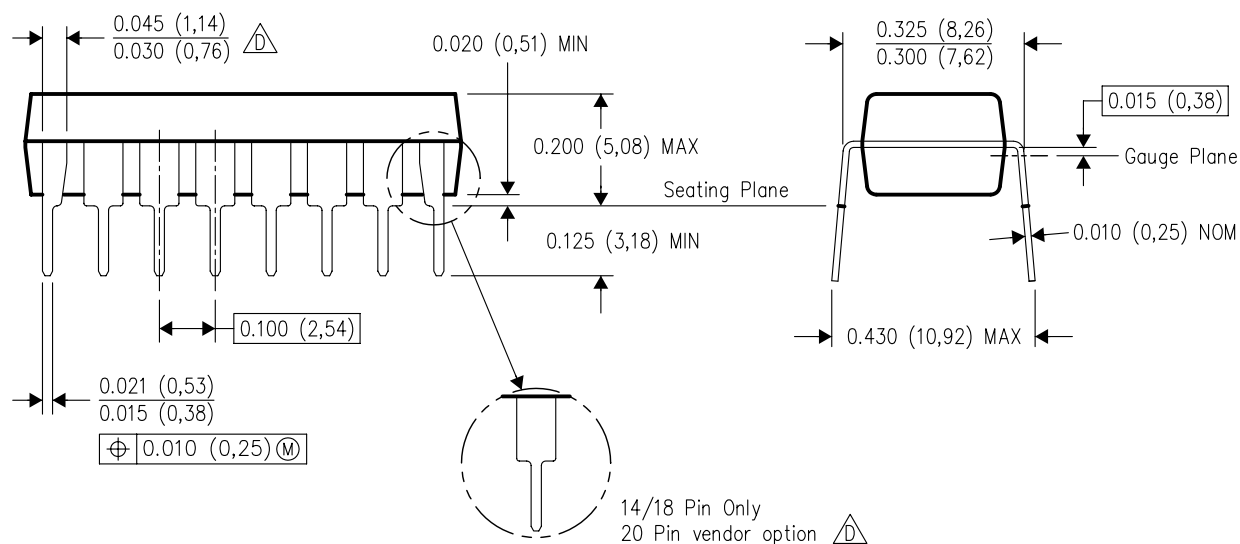
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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