

SN74AUP1G32 低功耗单路双输入正或门

1 特性

- 采用间距为 0.5mm 的超小型 0.64mm² 封装 (DPW)
- 低静态功耗
($I_{CC} = 0.9\mu A$, 最大值)
- 低动态功耗
(3.3V 时, $C_{pd} = 4.3pF$, 典型值)
- 低输入电容 ($C_i = 1.5pF$, 典型值)
- 低噪声 – 过冲和下冲
低于 V_{CC} 的 10%
- I_{off} 支持带电插入、局部断电模式和后驱动保护
- 输入迟滞在 $V_{hys} = 250mV$ (3.3V 时的典型值) 输入下
可实现缓慢的输入转换和更好的开关噪声抗扰度
- 宽工作 V_{CC} 范围为 0.8V 至 3.6V
- 针对 3.3V 运行进行了优化
- 3.6V 耐压 I/O 支持混合模式的信号操作
- 3.3V 时, $t_{pd} = 4.6ns$ (最大值)
- 适用于点对点应用
- 闩锁性能超过 100mA,
符合 JESD 78 II 类规范
- ESD 性能测试符合 JESD 22 标准
 - 2000V 人体放电模型 (A114-B, II 类)
 - 1000V 充电器件模型 (C101)

2 应用

- ATCA 解决方案
- 主动噪声消除 (ANC)
- 数据表末尾条形码扫描仪
- 血压监护仪
- CPAP 呼吸机
- 线缆解决方案
- DLP 3D 机器视觉、高光谱成像、光纤网络和光谱分析
- 电子书
- 嵌入式 PC
- 现场变送器: 温度或湿度传感器
- 指纹生物识别
- HVAC: 暖通空调
- 网络附加存储 (NAS)
- 服务器主板和 PSU
- 软件定义无线电 (SDR)
- 电视: 高清电视 (HDTV)、LCD 电视和数字电视
- 视频通信系统
- 无线数据存取卡、耳机、键盘、鼠标和 LAN 卡
- X 射线: 行李扫描仪、医疗和牙科

3 说明

此单路双输入正或门以正逻辑执行布尔函数

$$Y = A \bullet B \text{ or } Y = \overline{A + B}$$

器件信息⁽¹⁾

器件号	封装	封装尺寸 (标称值)
SN74AUP1G32	SOT (5)	1.60mm × 1.20mm
	USON (6)	1.45mm × 1.00mm
	X2SON (4)	0.80mm × 0.80mm
	DSBGA (6)	1.19mm × 0.79mm
	DSBGA (5)	1.41mm × 0.91mm

(1) 要了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

简化原理图



目录

1	特性	1	7.2	Enable and Disable Times	10
2	应用	1	8	Detailed Description	11
3	说明	1	8.1	Overview	11
4	修订历史记录	2	8.2	Functional Block Diagram	11
5	Pin Configuration and Functions	3	8.3	Feature Description	11
6	Specifications	4	8.4	Device Functional Modes	11
6.1	Absolute Maximum Ratings	4	9	Application and Implementation	12
6.2	Handling Ratings	4	9.1	Application Information	12
6.3	Recommended Operating Conditions	4	9.2	Typical Application	12
6.4	Thermal Information	5	10	Power Supply Recommendations	13
6.5	Electrical Characteristics	6	11	Layout	13
6.6	Switching Characteristics, $C_L = 5$ pF	6	11.1	Layout Guidelines	13
6.7	Switching Characteristics, $C_L = 10$ pF	7	11.2	Layout Example	13
6.8	Switching Characteristics, $C_L = 15$ pF	7	12	器件和文档支持	14
6.9	Switching Characteristics, $C_L = 30$ pF	7	12.1	接收文档更新通知	14
6.10	Operating Characteristics	7	12.2	支持资源	14
6.11	Typical Characteristics	8	12.3	商标	14
7	Parameter Measurement Information	9	12.4	静电放电警告	14
7.1	Propagation Delays, Setup and Hold Times, and Pulse Width	9	12.5	Glossary	14
			13	机械、封装和可订购信息	14

4 修订历史记录

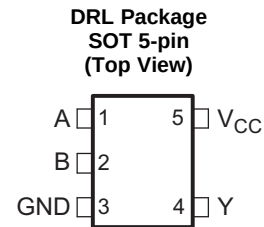
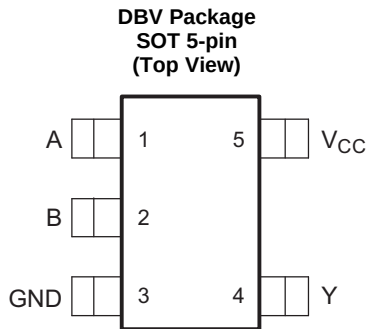
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision I (June 2014) to Revision J	Page
• Changed format of Pin Configuration images to allow for HTML search function	3
• Corrected YFP package pin descriptors in the Pin Functions table	3
• Added Thermal Information for the DPW package	5

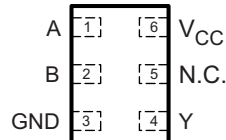
Changes from Revision H (August 2012) to Revision I	Page
• 将文档更新为新的 TI 数据表格式	1
• 删除了订购信息表	1
• 已添加 应用	1
• Added Handling Ratings table	4
• Added Thermal Information table	5
• Added Typical Characteristics	8

=====

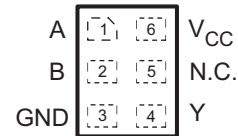
5 Pin Configuration and Functions



DSF Package
SON 6-pin
(Transparent Top View)

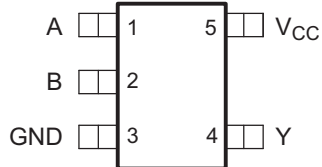


DRY Package
SON 6-pin
(Transparent Top View)

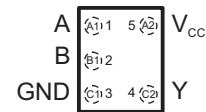


N.C. - No internal connection

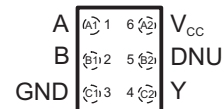
DCK Package
SC70 5-pin
(Top View)



YZP Package
DSBGA 5-balls
(Transparent Top View)

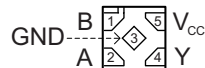


YFP Package
DSBGA 6-balls
(Transparent Top View)



DNU - Do Not Use

DPW Package
X2SON 5-pins
(Bottom View)



See mechanical drawings at the end of the data sheet for all package dimensions

Pin Functions

NAME	PIN					I/O	DESCRIPTION
	DRL, DCK, DBV	DPW	DRY, DSF	YZP	YFP		
A	1	2	1	A1	A1	I	Input A
B	2	1	2	B1	B1	I	Input B
GND	3	3	3	C1	C1	–	Ground
Y	4	4	4	C2	C2	O	Output Y
V _{CC}	5	5	6	A2	A2	–	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.5	4.6	V
V _I	Input voltage range ⁽²⁾	−0.5	4.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	−0.5	4.6	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50	mA
I _{OK}	Output clamp current	V _O < 0	−50	mA
I _O	Continuous output current		±20	mA
	Continuous current through V _{CC} or GND		±50	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		−65	125	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.6	
		V _{CC} = 3 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.9	
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	−20	mA
		V _{CC} = 1.1 V	−1.1	
		V _{CC} = 1.4 V	−1.7	
		V _{CC} = 1.65 V	−1.9	
		V _{CC} = 2.3 V	−3.1	
		V _{CC} = 3 V	−4	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

Recommended Operating Conditions⁽¹⁾ (continued)

		MIN	MAX	UNIT
I_{OL}	Low-level output current	$V_{CC} = 0.8\text{ V}$	20	μA
		$V_{CC} = 1.1\text{ V}$	1.1	mA
		$V_{CC} = 1.4\text{ V}$	1.7	
		$V_{CC} = 1.65\text{ V}$	1.9	
		$V_{CC} = 2.3\text{ V}$	3.1	
		$V_{CC} = 3\text{ V}$	4	
$\Delta t/\Delta v$	Input transition rise and fall rate	$V_{CC} = 0.8\text{ V to }1.95\text{ V}$	200	ns/V
T_A	Operating free-air temperature	–40	85	$^{\circ}\text{C}$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DBV	DCK	DRL	DSF	DRY	DPW	UNIT
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard data sheet value)	271.4	338.4	349.7	407.1	554.9	492.1	$^{\circ}\text{C/W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (standard data sheet value)	213.5	110.6	120.5	232.0	385.4	232.6	$^{\circ}\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance (standard data sheet value)	108.2	118.8	171.4	306.9	388.2	355.4	$^{\circ}\text{C/W}$
Ψ_{JT}	Junction-to-top characterization parameter (standard data sheet value)	89.3	3.0	10.8	40.3	159.0	37.4	$^{\circ}\text{C/W}$
Ψ_{JB}	Junction-to-board characterization parameter (standard data sheet value)	107.6	117.8	169.4	306.0	384.1	353.9	$^{\circ}\text{C/W}$
$\Psi_{JC(bot)}$	Junction-to-case (bottom) thermal resistance (standard data sheet value)	–	–	–	–	–	147.9	$^{\circ}\text{C/W}$

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = –20 μA		0.8 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
	I _{OH} = –1.1 mA		1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		
	I _{OH} = –1.7 mA		1.4 V	1.11			1.03		
	I _{OH} = –1.9 mA		1.65 V	1.32			1.3		
	I _{OH} = –2.3 mA		2.3 V	2.05			1.97		
	I _{OH} = –3.1 mA			1.9			1.85		
	I _{OH} = –2.7 mA		3 V	2.72			2.67		
	I _{OH} = –4 mA			2.6			2.55		
V _{OL}	I _{OL} = 20 μA		0.8 V to 3.6 V	0.1			0.1		V
	I _{OL} = 1.1 mA		1.1 V	0.3 × V _{CC}			0.3 × V _{CC}		
	I _{OL} = 1.7 mA		1.4 V	0.31			0.37		
	I _{OL} = 1.9 mA		1.65 V	0.31			0.35		
	I _{OL} = 2.3 mA		2.3 V	0.31			0.33		
	I _{OL} = 3.1 mA			0.44			0.45		
	I _{OL} = 2.7 mA		3 V	0.31			0.33		
	I _{OL} = 4 mA			0.44			0.45		
I _I	A or B input	V _I = GND to 3.6 V	0 V to 3.6 V	0.1			0.5	μA	
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V	0.2			0.6	μA	
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V	0.2			0.6	μA	
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V	0.5			0.9	μA	
ΔI _{CC}		V _I = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V	40			50	μA	
C _i		V _I = V _{CC} or GND	0 V	1.5					pF
			3.6 V	1.5					
C _o		V _O = GND	0 V	3					pF

 (1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

6.6 Switching Characteristics, C_L = 5 pF

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	0.8 V	18					ns
			1.2 V ± 0.1 V	2.6	7.3	13.5	2.1	16.8	
			1.5 V ± 0.1 V	1.4	5.2	9.1	0.9	11	
			1.8 V ± 0.15 V	1	4.2	7	0.5	8.8	
			2.5 V ± 0.2 V	1	3	4.7	0.5	6	
			3.3 V ± 0.3 V	1	2.4	3.7	0.5	4.6	

6.7 Switching Characteristics, $C_L = 10\text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		21				ns
			1.2 V $\pm$ 0.1 V	1.5	8.5	15.4	1	18.4	
			1.5 V $\pm$ 0.1 V	1	6.2	10.4	0.5	12	
			1.8 V $\pm$ 0.15 V	1	5	8.1	0.5	9.6	
			2.5 V $\pm$ 0.2 V	1	3.6	5.5	0.5	6.6	
			3.3 V $\pm$ 0.3 V	1	2.9	4.4	0.5	5	

6.8 Switching Characteristics, $C_L = 15\text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		24				ns
			1.2 V $\pm$ 0.1 V	3.6	9.9	17	3.1	21.1	
			1.5 V $\pm$ 0.1 V	2.3	7.2	11.5	1.8	13.9	
			1.8 V $\pm$ 0.15 V	1.6	5.8	9.1	1.1	11.2	
			2.5 V $\pm$ 0.2 V	1	4.3	6.2	0.5	7.8	
			3.3 V $\pm$ 0.3 V	1	3.4	5	0.5	6.2	

6.9 Switching Characteristics, $C_L = 30\text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3 and Figure 4)

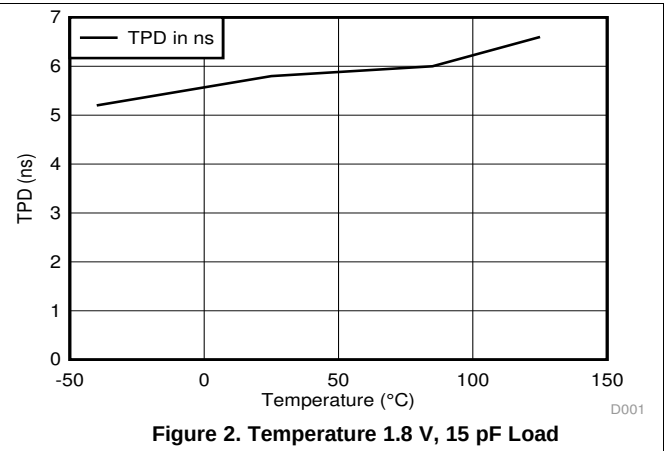
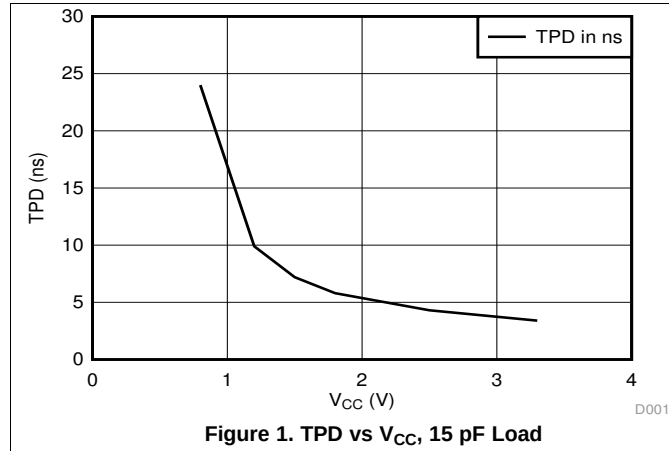
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		32.8				ns
			1.2 V $\pm$ 0.1 V	4.9	13.1	21.6	4.4	26.7	
			1.5 V $\pm$ 0.1 V	3.4	9.5	14.6	2.9	17.6	
			1.8 V $\pm$ 0.15 V	2.5	7.7	11.4	2	14.1	
			2.5 V $\pm$ 0.2 V	1.8	5.7	7.9	1.3	9.9	
			3.3 V $\pm$ 0.3 V	1.5	4.7	6.4	1	7.8	

6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

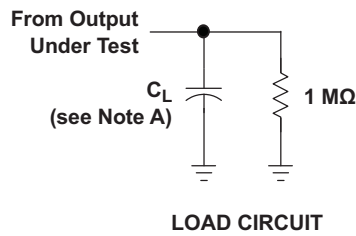
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	4.1	pF
			1.2 V $\pm$ 0.1 V	4.1	
			1.5 V $\pm$ 0.1 V	4.1	
			1.8 V $\pm$ 0.15 V	4.1	
			2.5 V $\pm$ 0.2 V	4.2	
			3.3 V $\pm$ 0.3 V	4.3	

6.11 Typical Characteristics

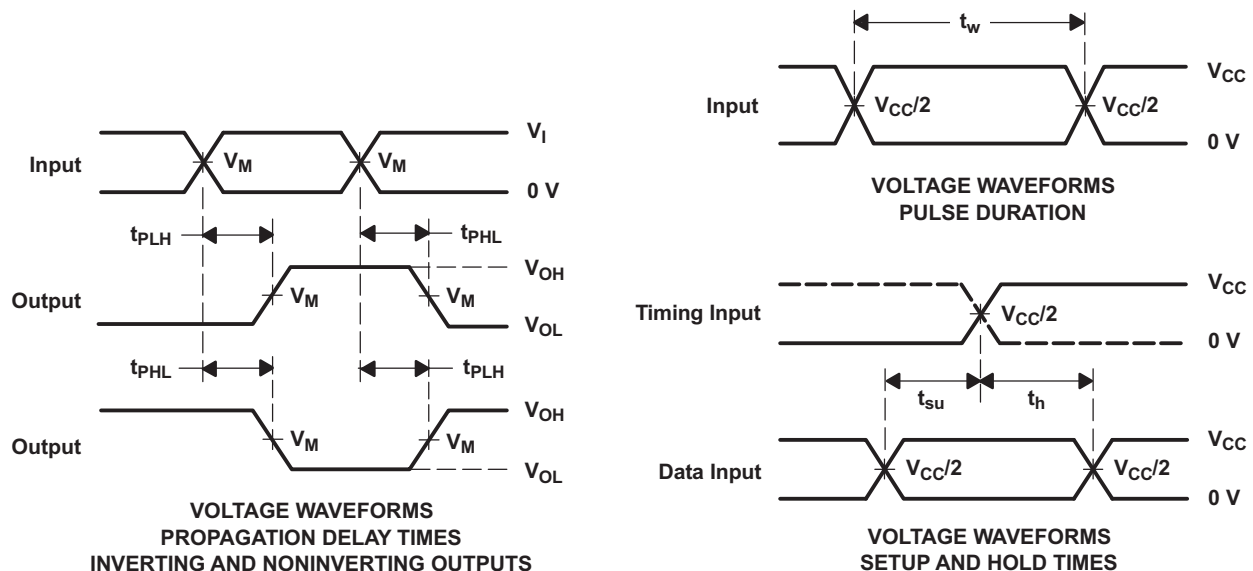


7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Width



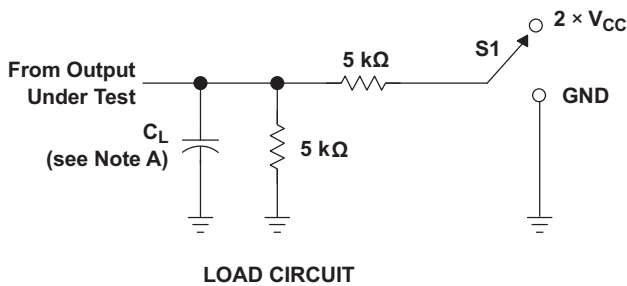
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- C_L includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, t_r and $t_f = 3 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

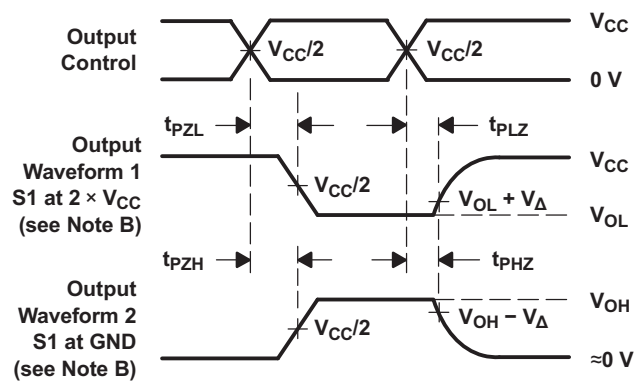
Figure 3. Load Circuit and Voltage Waveforms

7.2 Enable and Disable Times



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_D	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- A. C_L includes probe and jig capacitance.
- B.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, t_r and $t_f = 3 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

This single 2-input positive-OR gate that operates from 0.8 V to 3.6 V and performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

The AUP family of devices has quiescent power consumption less than 1 μ A and comes in the ultra small DPW package. The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating V_{CC} range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- Low noise due to slower edge rates

8.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	H

9 Application and Implementation

9.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire VCC range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

The AUP family of single gate logic makes excellent translators for the new lower voltage Micro- processors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

9.2 Typical Application

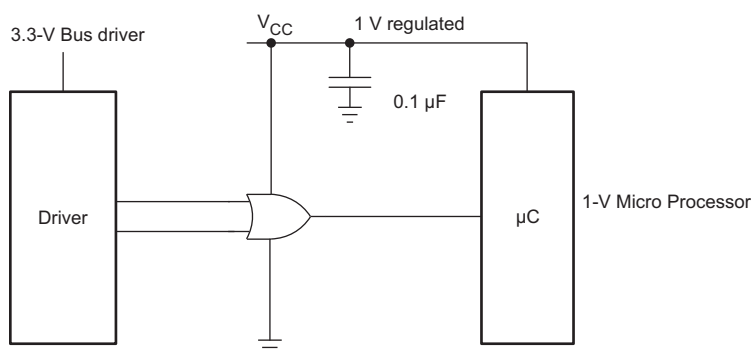


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

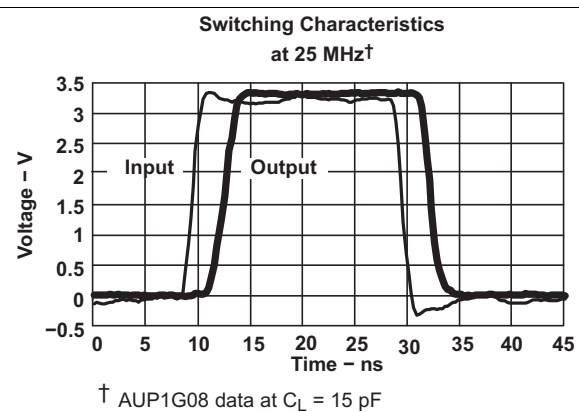
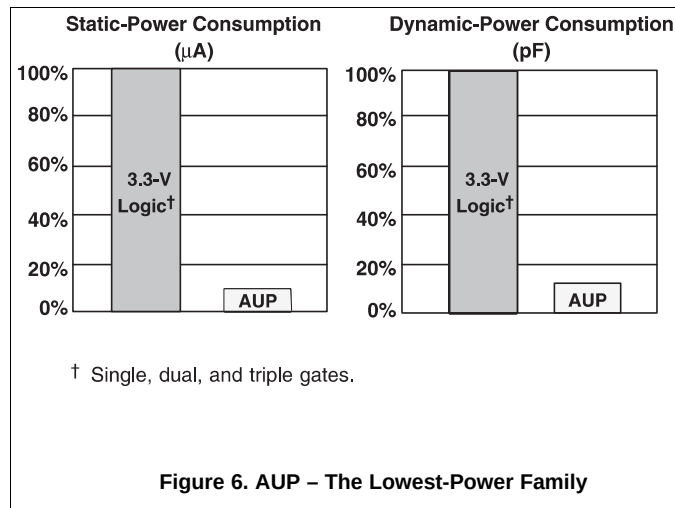
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

1. Recommended Input conditions
 - Rise time and fall time specifications. See ($\Delta t/\Delta V$) in [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}
2. Recommend output conditions
 - Load currents should not exceed 20 mA on the output and 50 mA total for the part
 - Outputs should not be pulled above V_{CC}

Typical Application (continued)

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended and if there are multiple V_{CC} terminals then .01 μ F or .022 μ F is recommended for each power terminal. It is ok to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

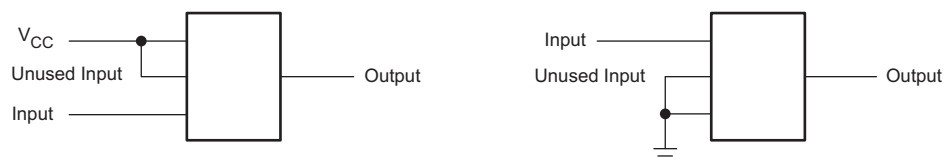
11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I/O's so they also cannot float when disabled.

11.2 Layout Example



12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G32DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R	Samples
SN74AUP1G32DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R	Samples
SN74AUP1G32DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HG5, HGF, HGK, HGR)	Samples
SN74AUP1G32DCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HG5, HGF, HGK, HGR)	Samples
SN74AUP1G32DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HG5, HGR)	Samples
SN74AUP1G32DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4	Samples
SN74AUP1G32DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HG7, HGR)	Samples
SN74AUP1G32DRY2	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG	Samples
SN74AUP1G32DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG	Samples
SN74AUP1G32DSF2	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG	Samples
SN74AUP1G32DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG	Samples
SN74AUP1G32YFPR	ACTIVE	DSBGA	YFP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		HGN	Samples
SN74AUP1G32YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HGN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

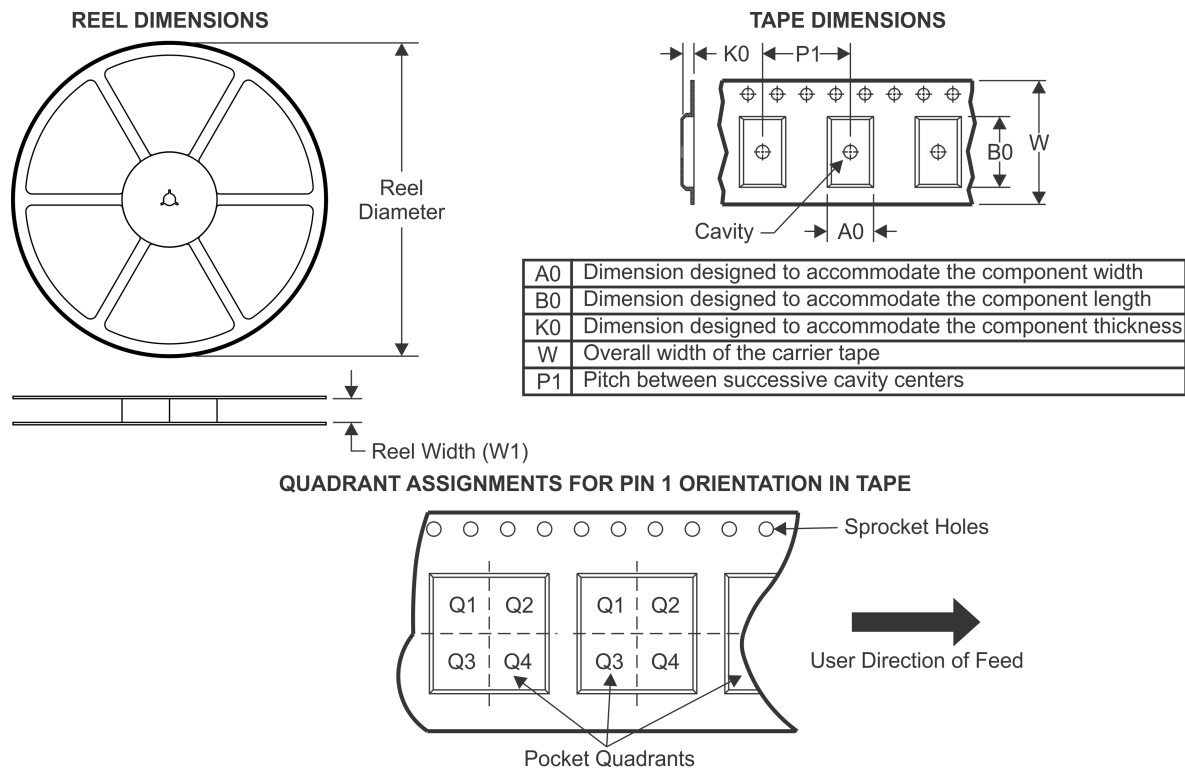
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

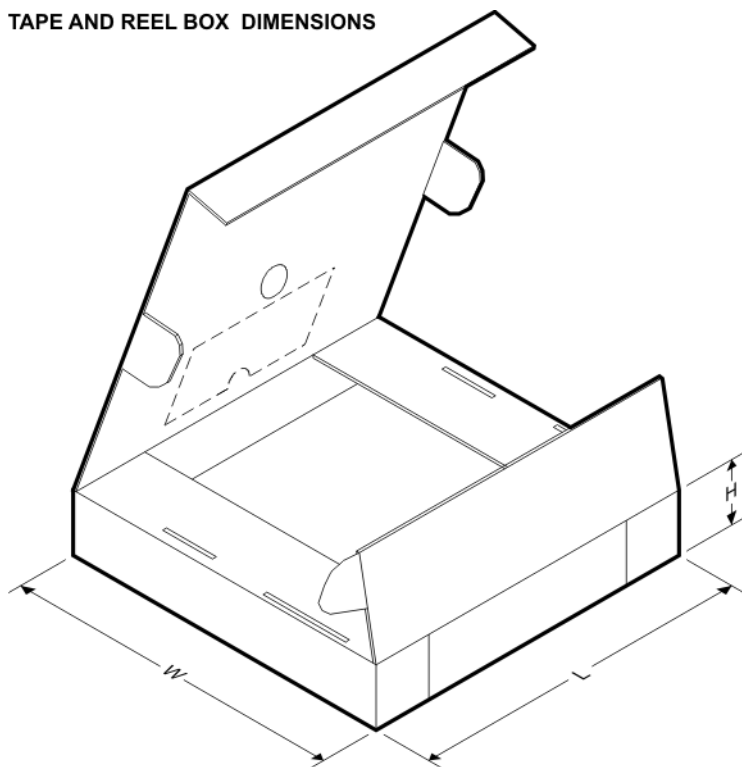
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

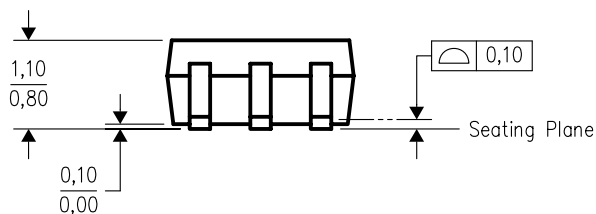
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G32DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G32DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G32DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G32DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G32DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74AUP1G32DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G32DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP1G32DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G32YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G32YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



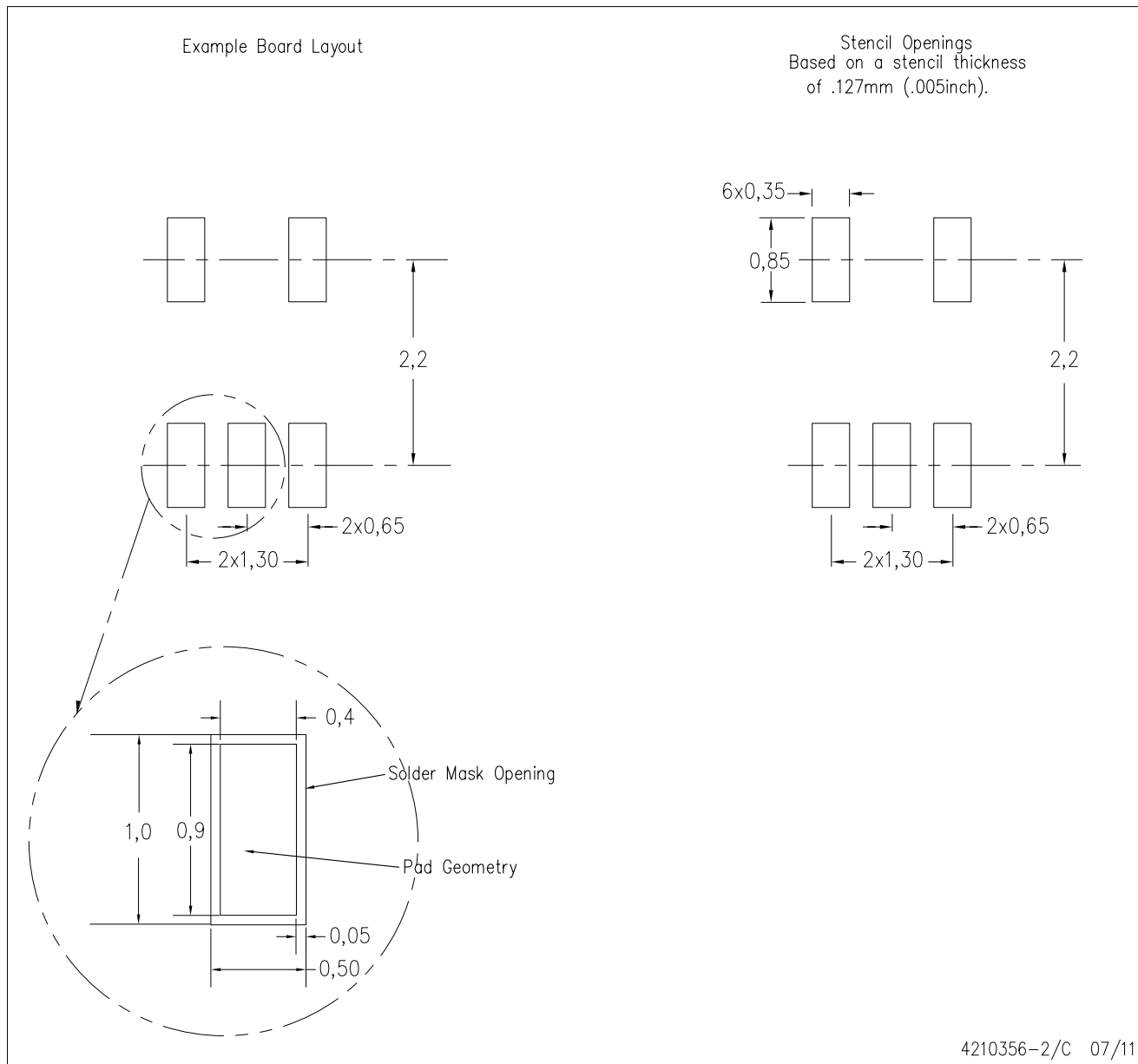
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G32DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G32DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G32DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G32DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G32DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G32DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G32DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G32DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G32YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G32YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



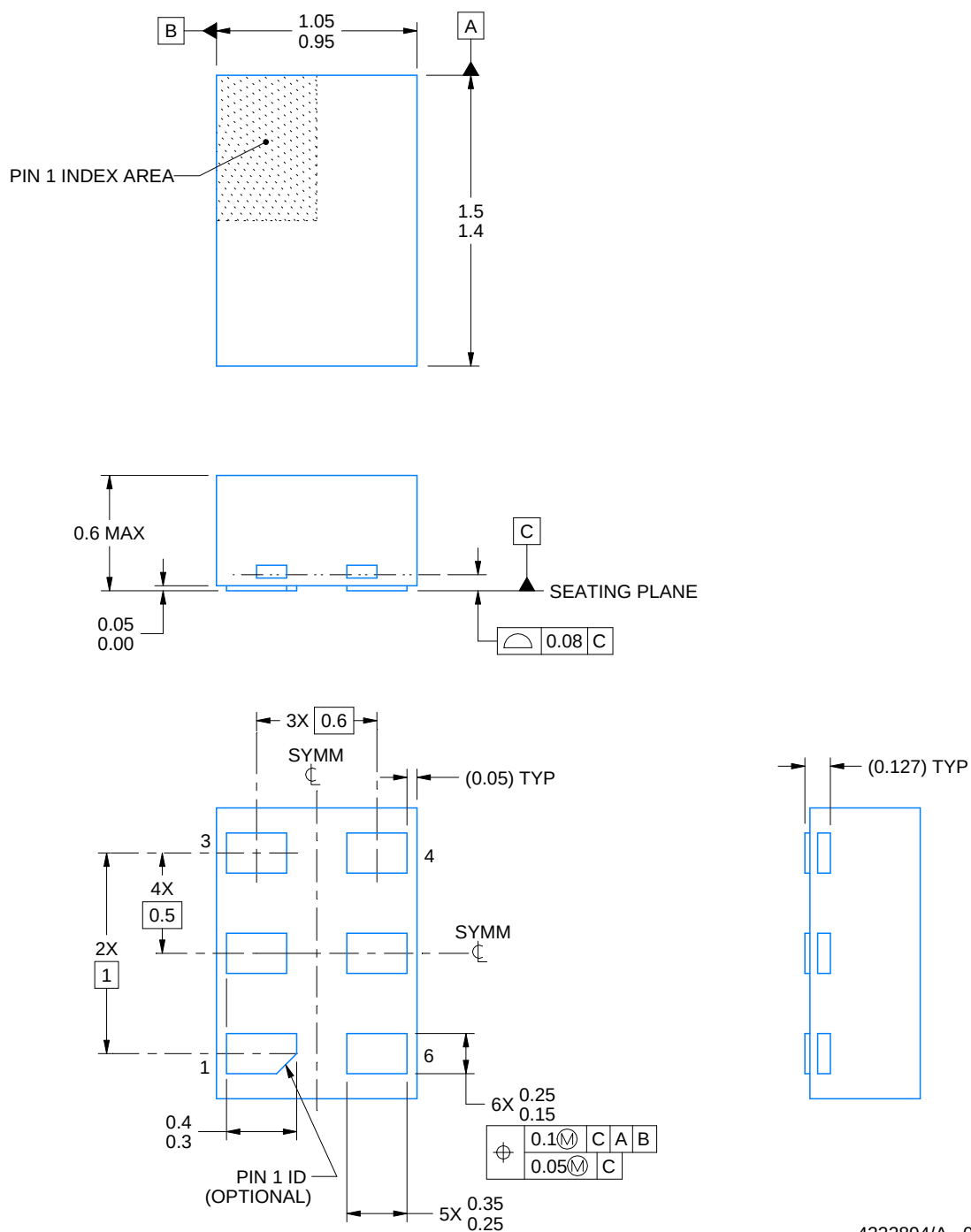
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G



USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

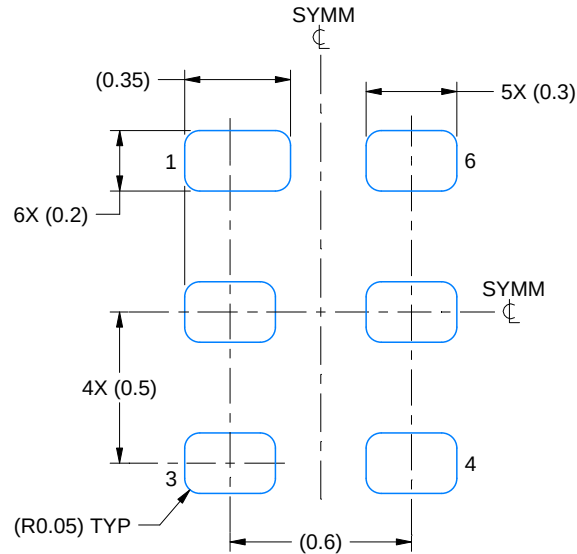
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

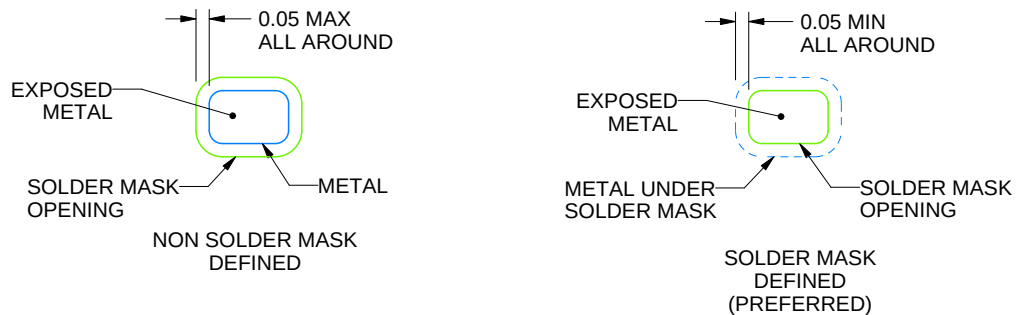
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

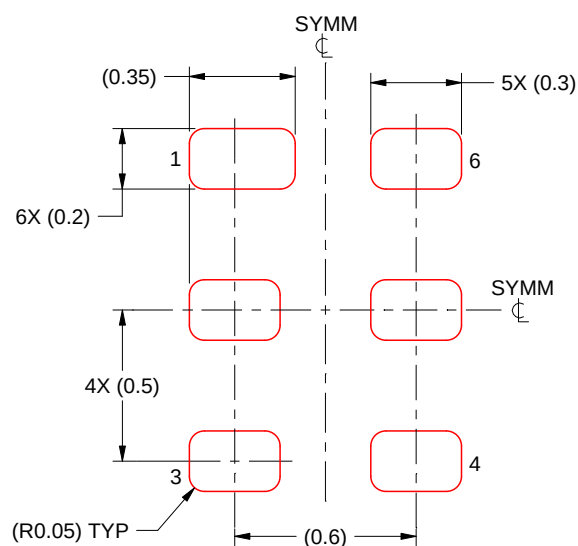
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

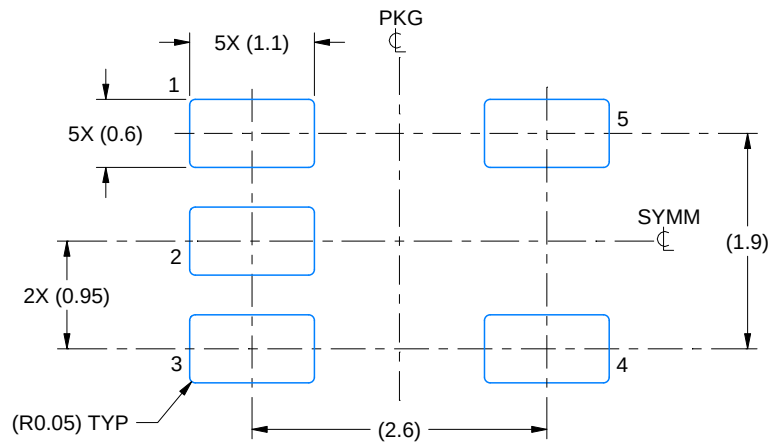
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

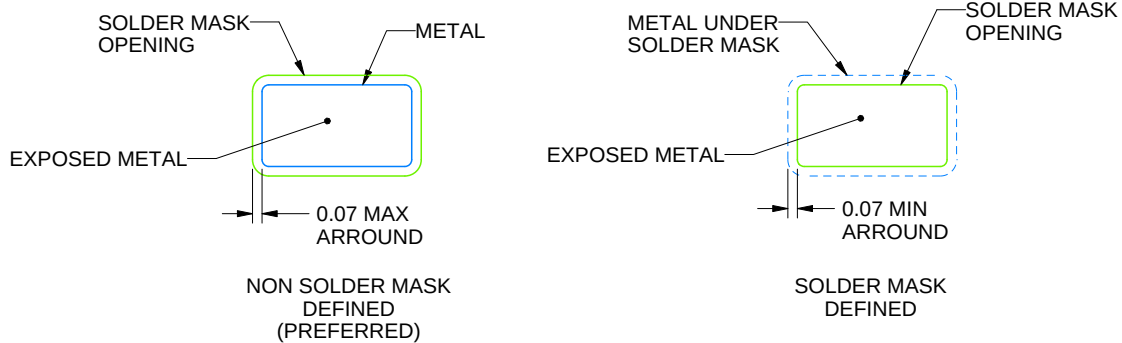
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

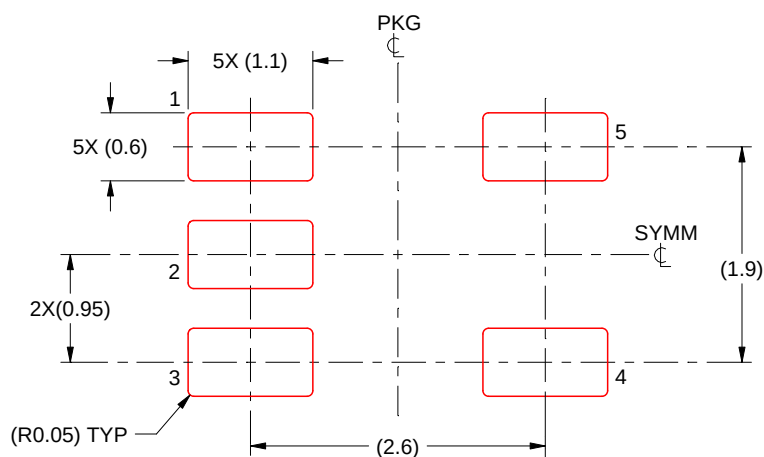
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

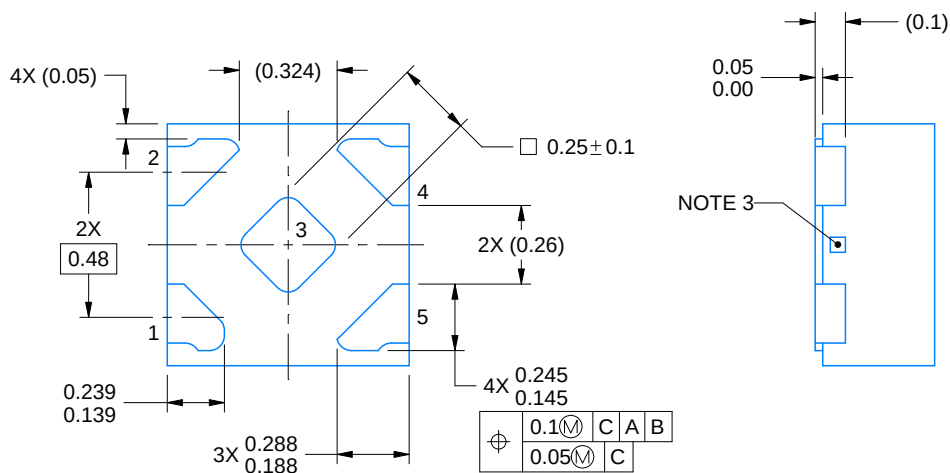
4211218-3/D



X2SON - 0.4 mm max height

Diagram illustrating the dimensions and pin index area of a component:

- Horizontal dimensions: 0.85 (total width) and 0.75 (width of the shaded area).
- Vertical dimensions: 0.85 (total height) and 0.75 (height of the shaded area).
- A shaded rectangular area is labeled "PIN 1 INDEX AREA".
- Reference points A and B are indicated at the corners of the component.



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

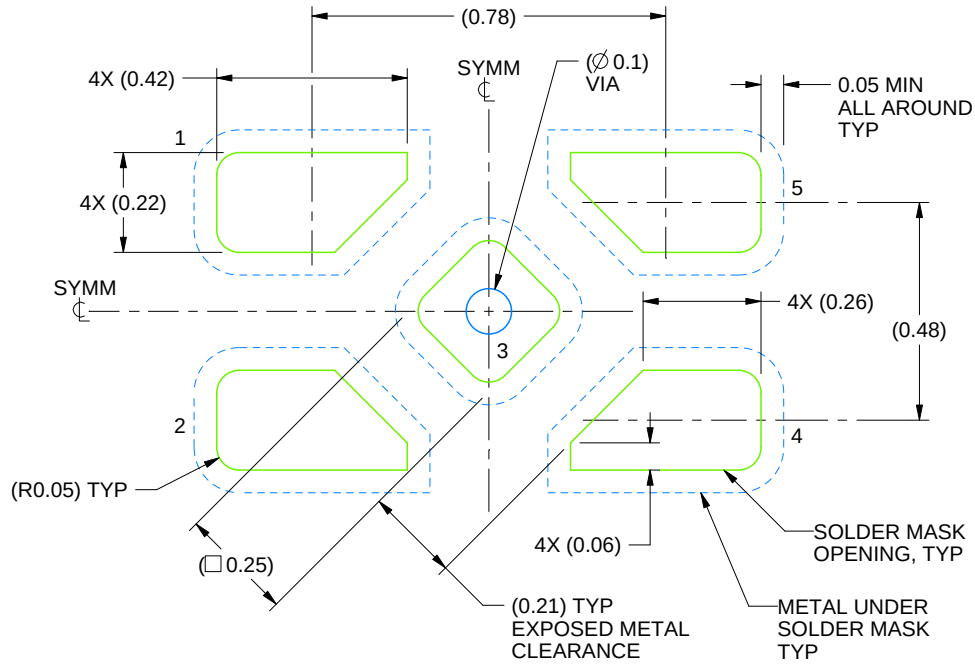
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/C 06/2021

NOTES: (continued)

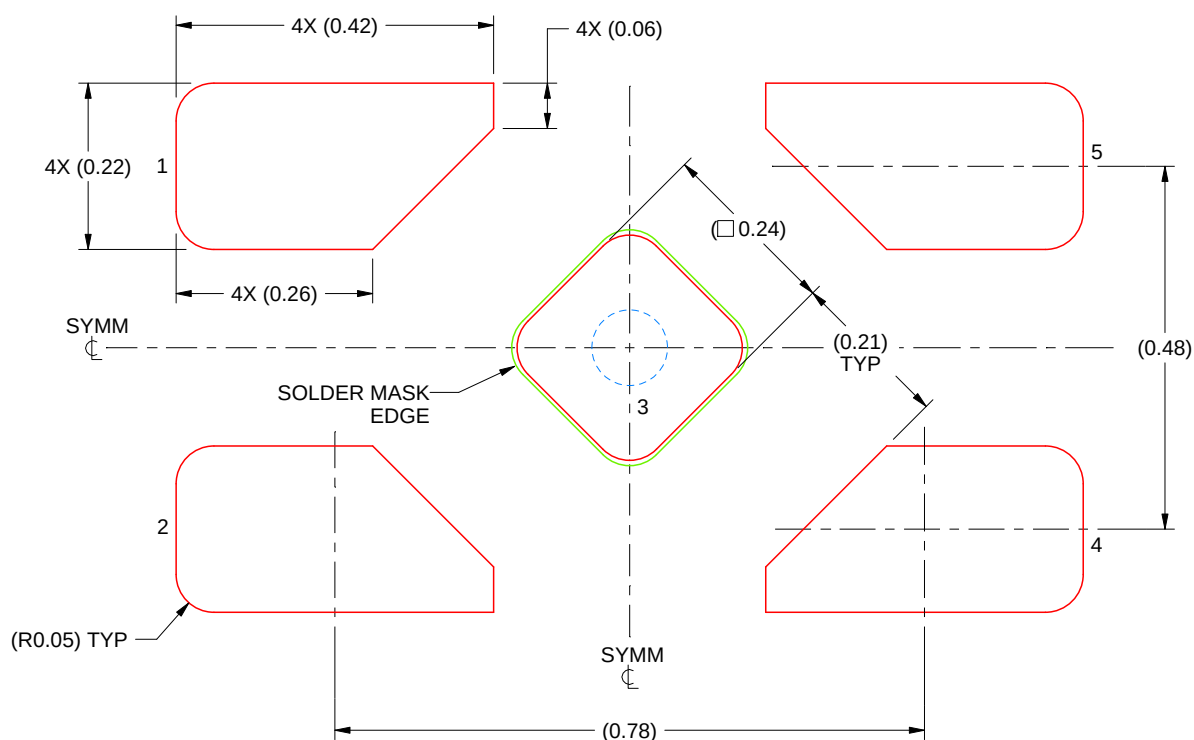
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/C 06/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

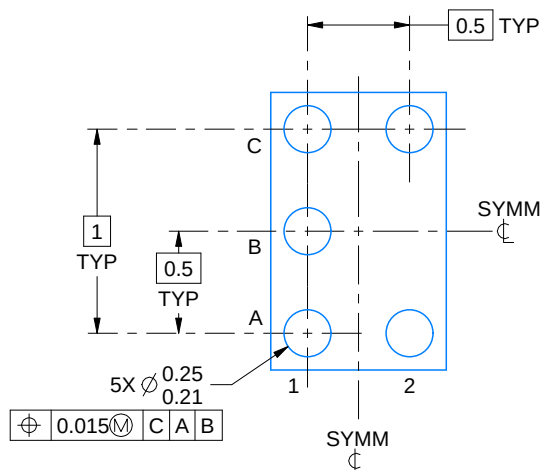
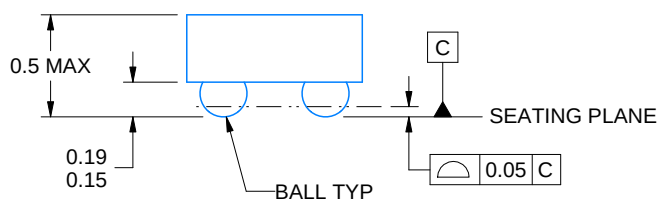
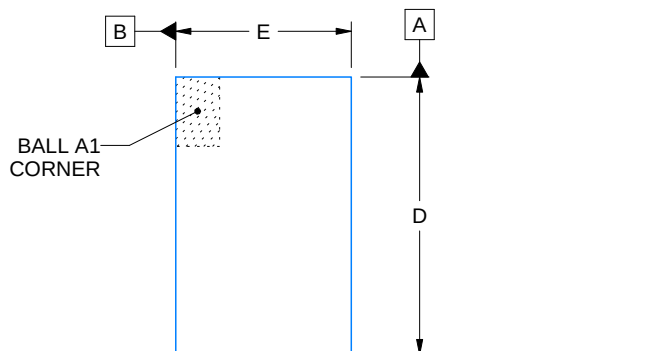
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm
E: Max = 0.918 mm, Min = 0.858 mm

4219492/A 05/2017

NOTES:

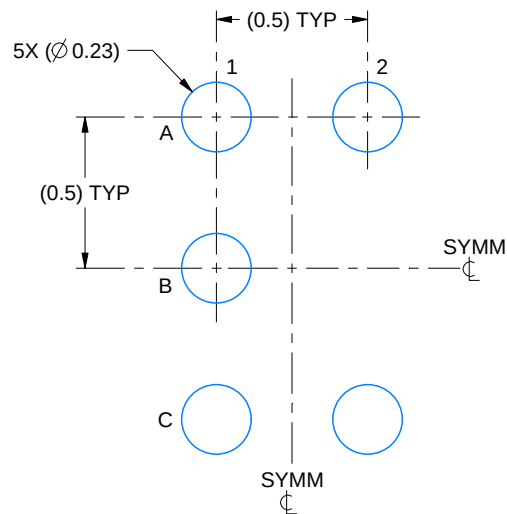
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

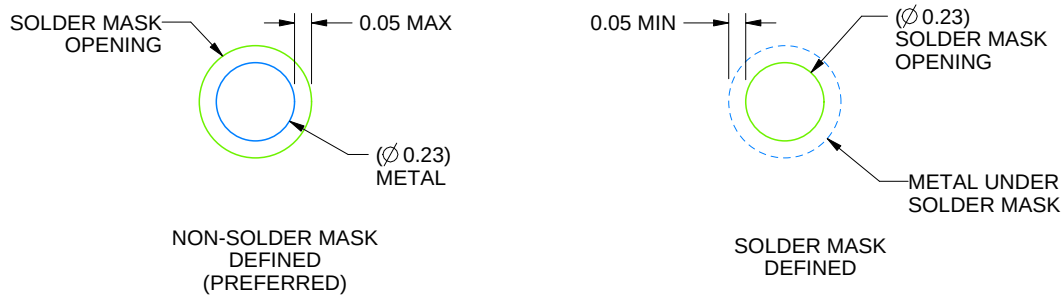
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

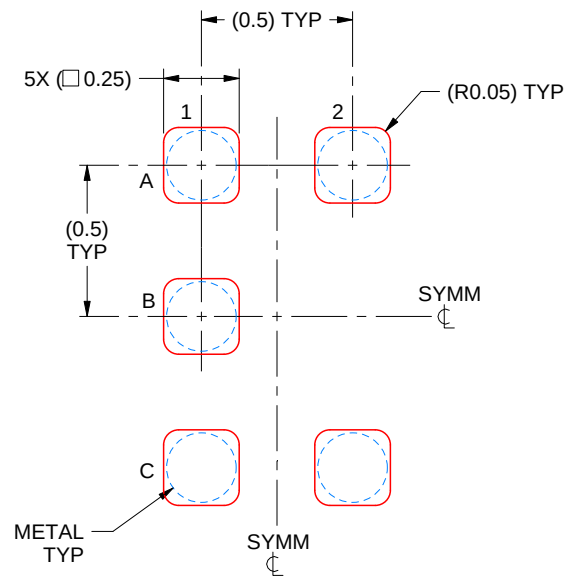
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

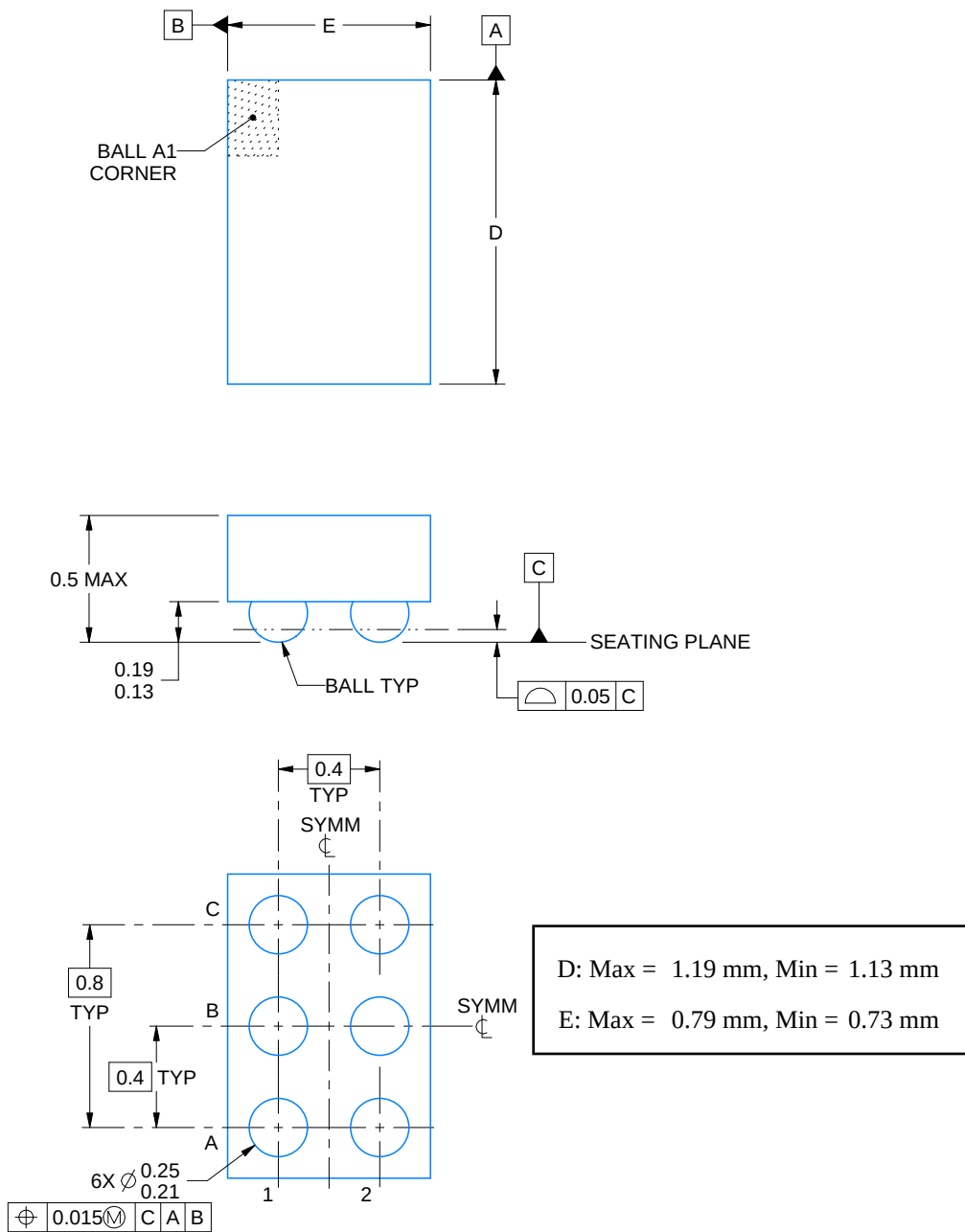
YFP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

NOTES:

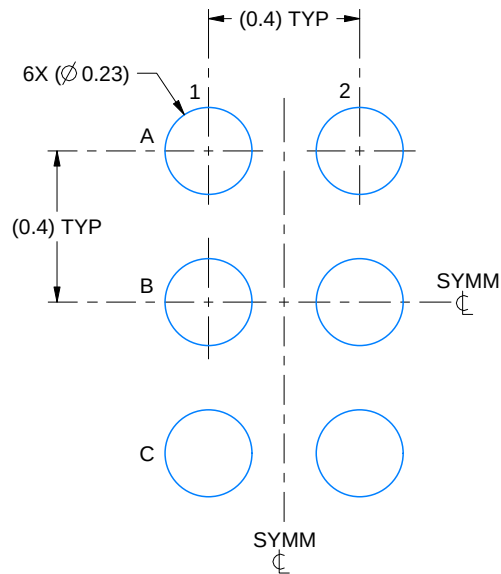
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

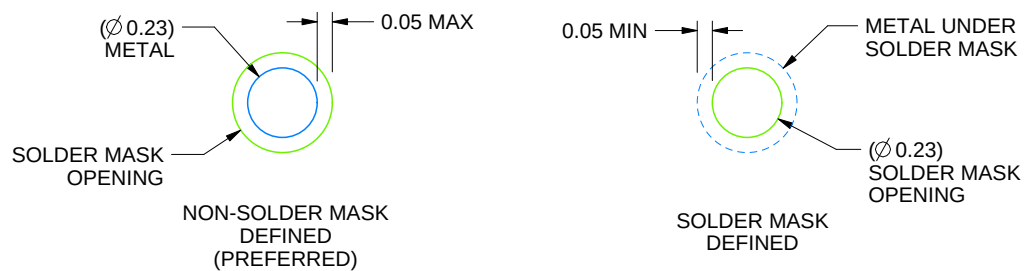
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X

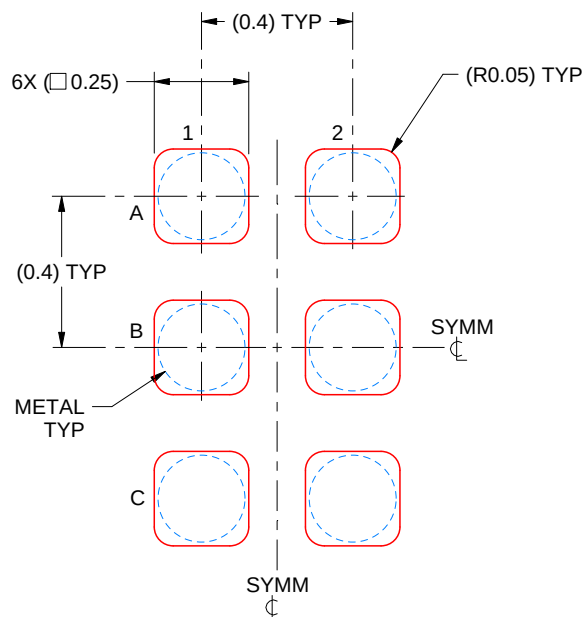


SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



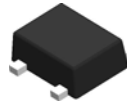
SOLDER PASTE EXAMPLE
 BASED ON 0.1 mm THICK STENCIL
 SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

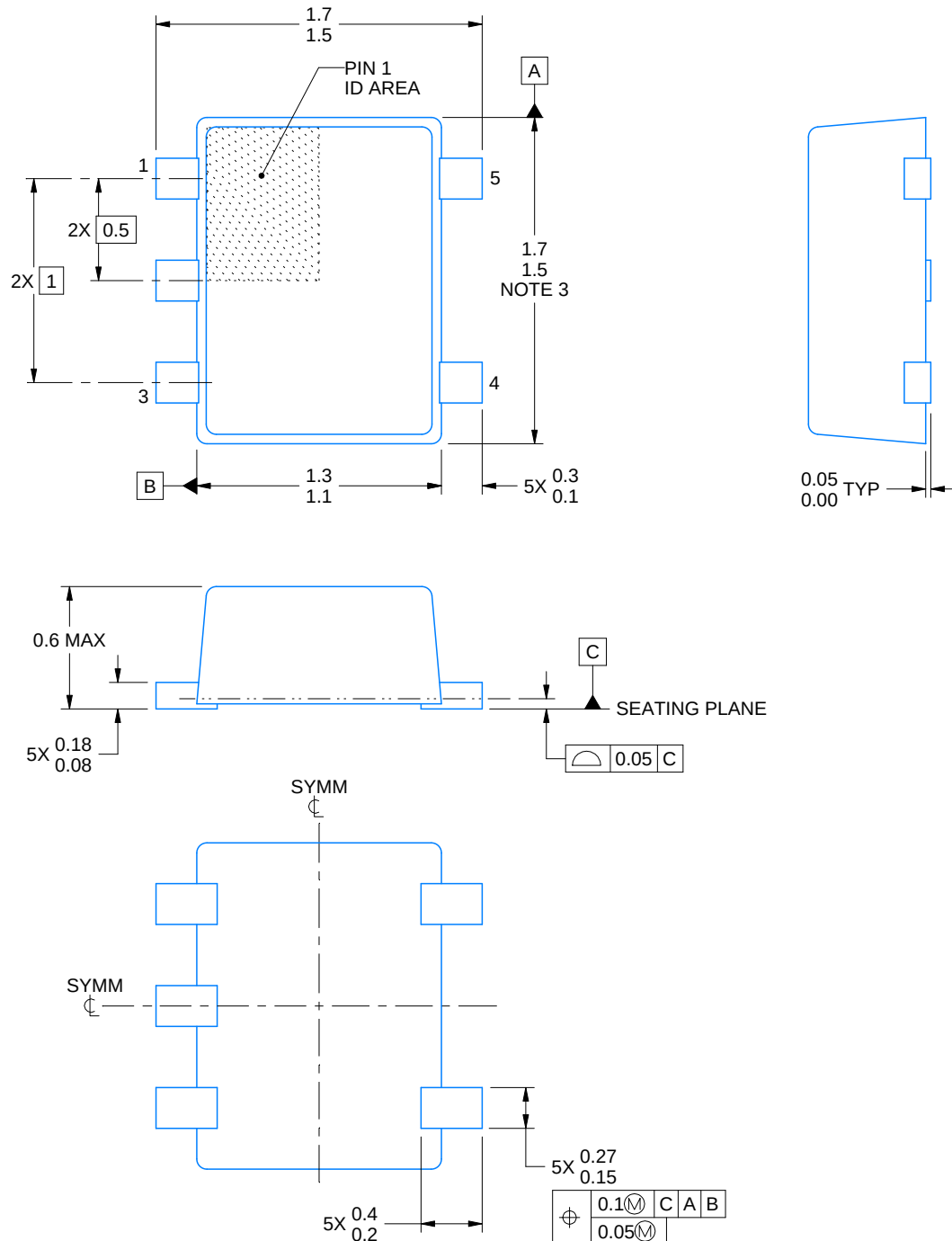
DRL0005A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/B 12/2020

NOTES:

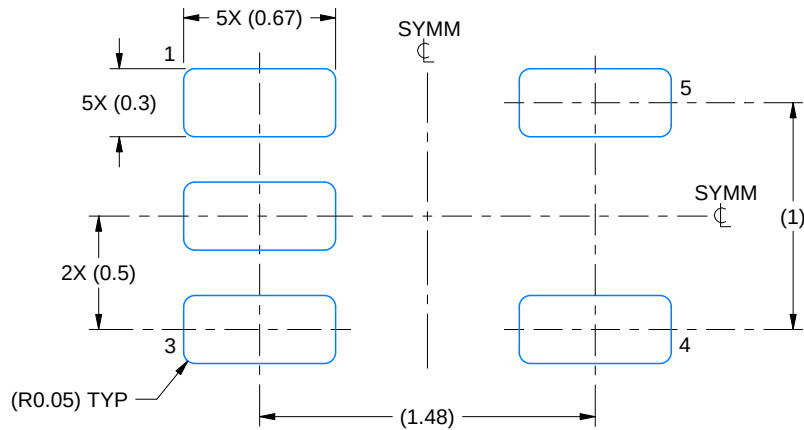
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

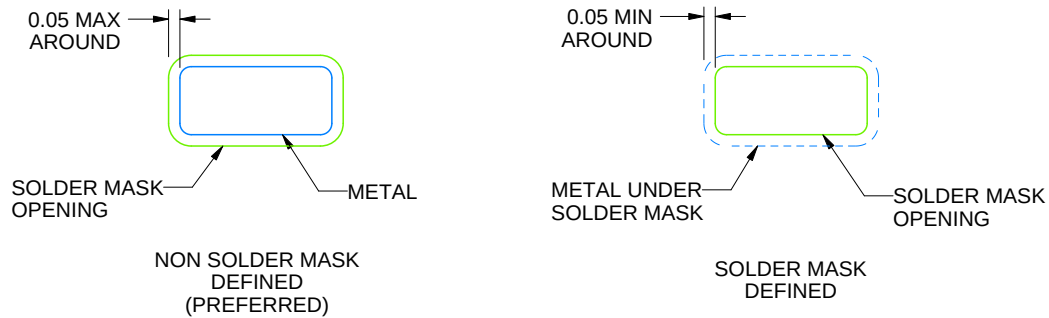
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

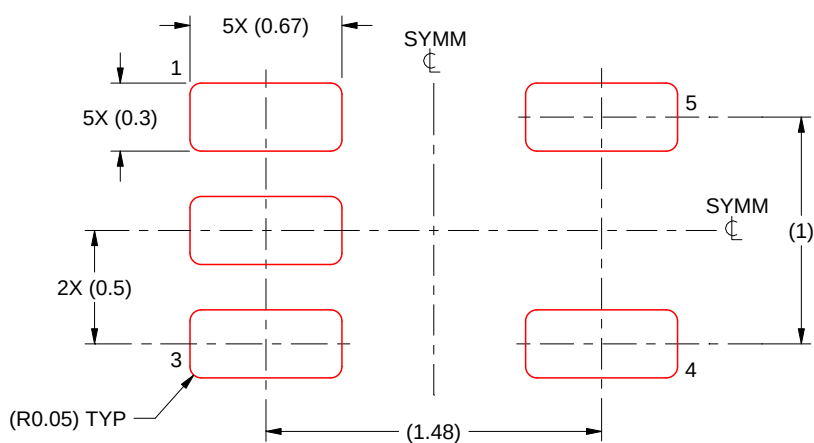
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

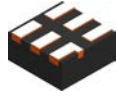


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

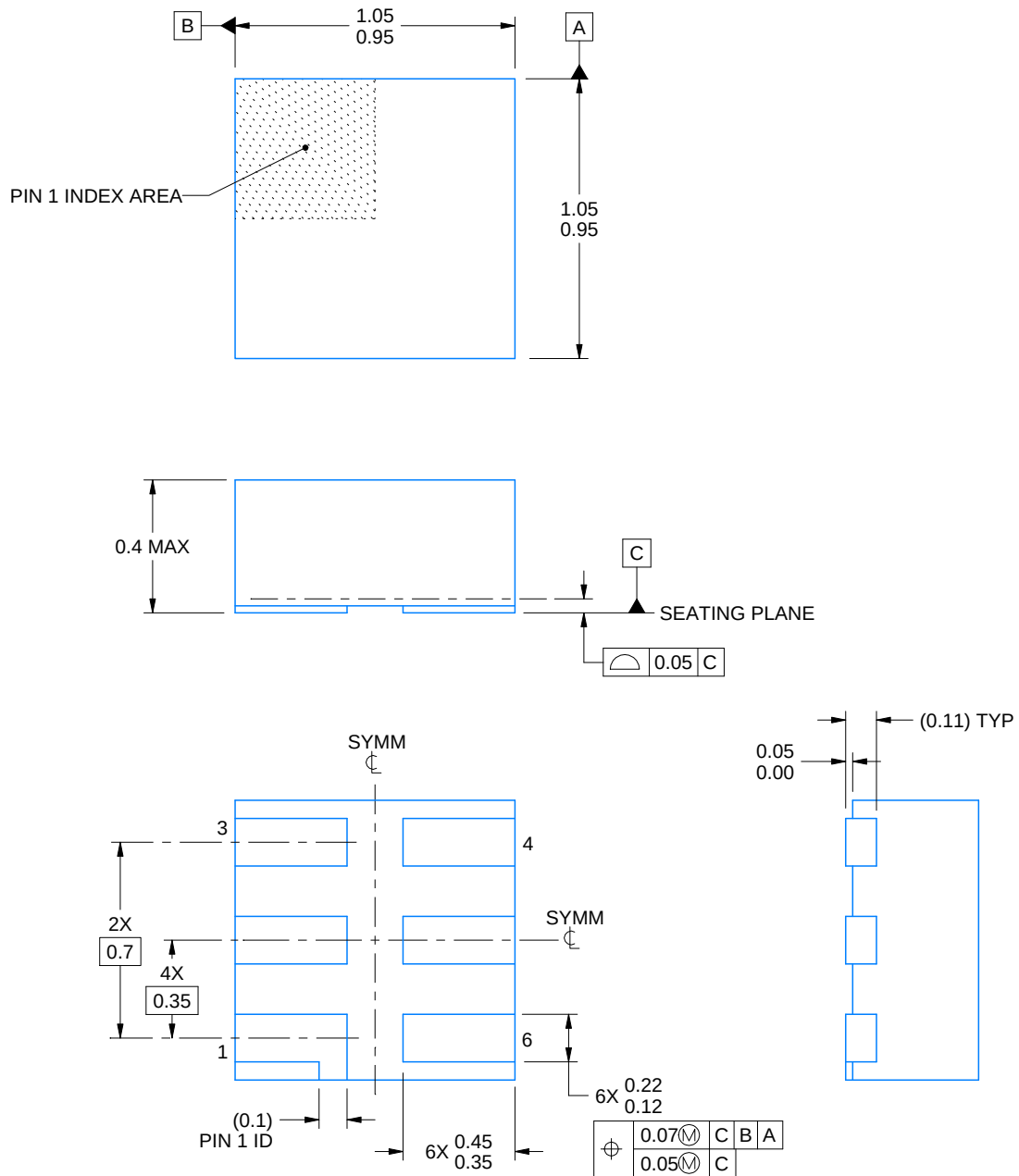


DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/A 06/2017

NOTES:

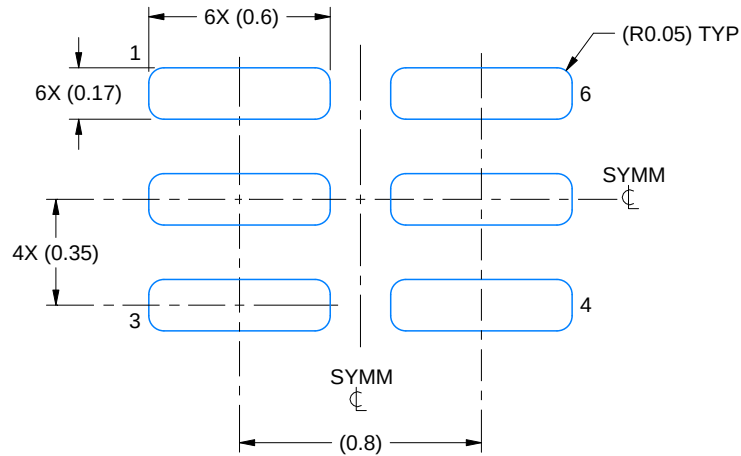
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

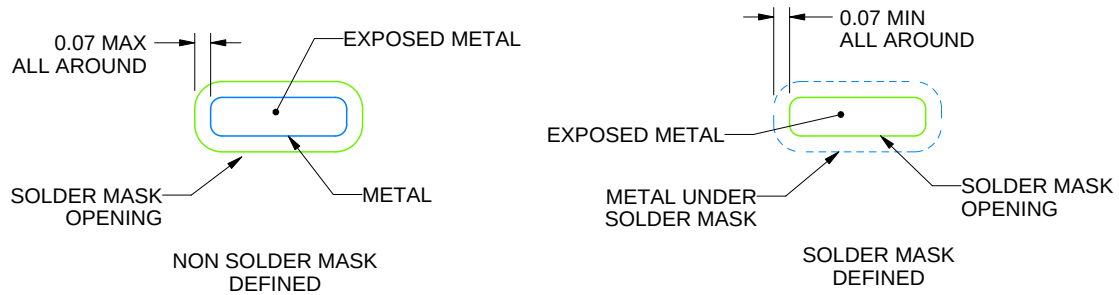
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

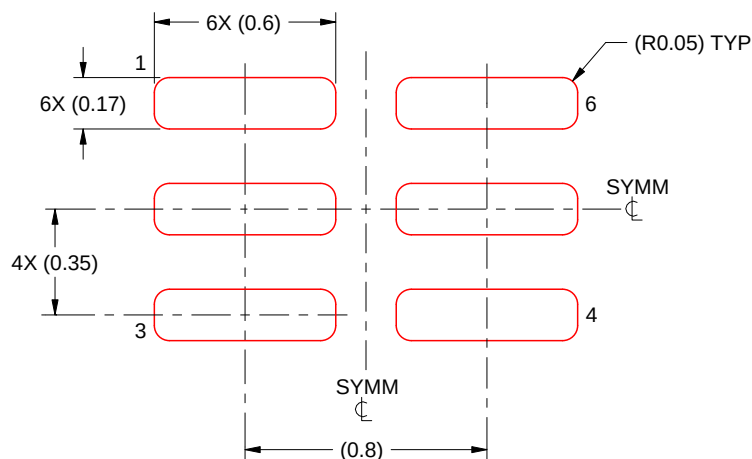
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 或 [ti.com.cn](https://www.ti.com.cn) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2021 德州仪器半导体技术（上海）有限公司