具有可配置电压转换和三态输出的 SN74AXC4T245 四位总线收发器

1 特性

- 完全可配置的双轨设计，实现各个端口在 0.65V 至 3.6V 的电源电压范围内运行
- 工作温度范围 -40°C 至 +125°C
- 多向控制引脚，支持同步升降转换
- 无干扰电源定序
- 从 1.8V 转换到 3.3V 时，支持高达 380Mbps 的转换速率
- V_{CC} 隔离特性
  - 如果任何一个 V_{CC} 输入低于 100mV，则所有 I/O 输出均禁用且处于高阻抗状态
- I_{off} 支持局部断电模式运行
- 兼容 AVC 系列电平转换器
- 闩锁性能超出 JESD 78 II 类规范要求的 100mA
- ESD 保护性能超过 JESD 22 规范要求
  - 8000V 人体放电模型
  - 1000V 充电器件模型

2 应用

- 企业与通信
- 工业
- 个人电子产品
- 无线基础设施
- 楼宇自动化
- 销售终端

3 说明

SN74AXC4T245 是一款使用两个独立可配置电源轨的四位同相总线收发器。V_{CCA} 和 V_{CCB} 电源电压低至 0.65V 时，该器件可正常工作。A 端口用于跟踪 V_{CCA}，该端口可支持 0.65V 至 3.6V 范围内的任何电源电压。B 端口用于跟踪 V_{CCB}，该端口也支持 0.65V 至 3.6V 范围内的任何电源电压。此外，SN74AXC4T245 还与单电源系统兼容。

SN74AXC4T245 器件旨在实现数据总线间的异步通信。根据方向控制输入（DIR1 和 2DIR）的逻辑电平，此器件将数据从 A 总线传输至 B 总线，或者将数据从 B 总线传输至 A 总线。输出使能输入（1$\overline{\text{OE}}$ 和 2$\overline{\text{OE}}$）可用于禁用输出，从而有效隔离总线。SN74AXC4T245 器件旨在使控制引脚（xDIR 和 x$\overline{\text{OE}}$）以 V_{CCA} 为基准。

为了确保电平转换器 I/O 在加电或断电期间的高阻抗状态，x$\overline{\text{OE}}$ 引脚应通过一个上拉电阻器连接至 V_{CCA}。

该器件完全 适用于 使用 I_{off} 电流的局部断电应用。当器件断电时，I_{off} 保护电路可确保不从输入/输出或偏置到特定电压的快速 I/O 获取或向其提供多余电流。

V_{CC} 隔离特性可确保当 V_{CCA} 或 V_{CCB} 低于 100mV 时，I/O 端口均禁用其输出并进入高阻抗状态。

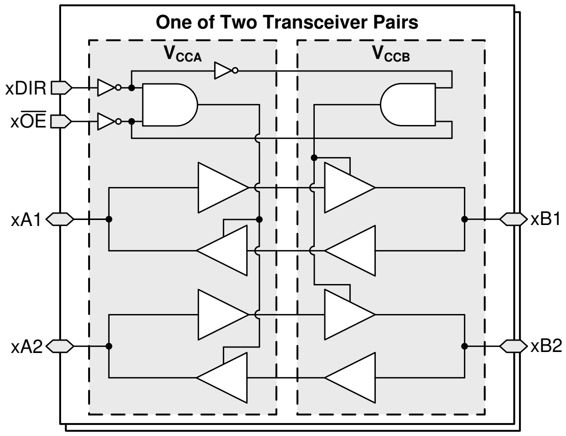
无干扰电源定序使电源轨能以任何顺序打开或关断，从而提供强大的电源定序性能。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
SN74AXC4T245PW	TSSOP (16)	5.00mm x 4.40mm
SN74AXC4T245RSV	UQFN (16)	2.60mm x 1.80mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能方框图



English Data Sheet: SCES877

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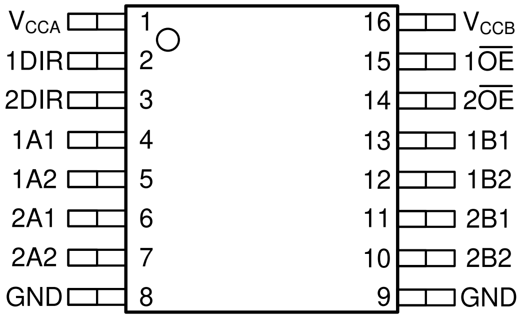
4 修订历史记录

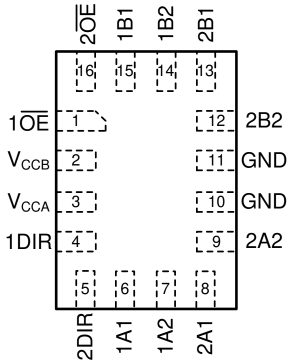
日期	修订版本	说明
2018 年 12 月	*	初始发行版。

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



RSV Package
16-Pin UQFN
Transparent Top View



Pin Functions

PIN	NO.		TYPE	DESCRIPTION
NAME	PW	RSV		
1A1	4	6	I/O	Input/output 1A1. Referenced to V_{CCA}.
1A2	5	7	I/O	Input/output 1A2. Referenced to V_{CCA}.
1B1	13	15	I/O	Input/output 1B1. Referenced to V_{CCB}.
1B2	12	14	I/O	Input/output 1B2. Referenced to V_{CCB}.
1DIR	2	4	I	Direction-control input for ‘1’ ports
1$\overline{\text{OE}}$	15	1	I	Tri-state output-mode enable. Pull $\overline{\text{OE}}$ high to place ‘1’ outputs in tri-state mode. Referenced to V_{CCA}.
2A1	6	8	I/O	Input/output 2A1. Referenced to V_{CCA}.
2A2	7	9	I/O	Input/output 2A2. Referenced to V_{CCA}.
2B1	11	13	I/O	Input/output 2B1. Referenced to V_{CCB}.
2B2	10	12	I/O	Input/output 2B2. Referenced to V_{CCB}.
2DIR	3	5	I	Direction-control input for ‘2’ ports
2$\overline{\text{OE}}$	14	16	I	Tri-state output-mode enable. Pull $\overline{\text{OE}}$ high to place ‘2’ outputs in tri-state mode. Referenced to V_{CCA}.
GND	8, 9	10, 11	—	Ground
V_{CCA}	1	3	—	A-port power supply voltage. $0.65\ V \le V_{CCA} \le 3.6\ V$
V_{CCB}	16	2	—	B-port power supply voltage. $0.65\ V \le V_{CCB} \le 3.6\ V$

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.2	V
V_{CCB}	Supply voltage B		–0.5	4.2	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.2	V
		I/O Ports (B Port)	–0.5	4.2	
		Control Inputs	–0.5	4.2	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.2	V
		B Port	–0.5	4.2	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.2	V
		B Port	–0.5	V_{CCB} + 0.2	
I_{IK}	Input clamp current	$V_I < 0$	–50		mA
I_{OK}	Output clamp current	$V_O < 0$	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			0.65	3.6	V
V_{CCB}	Supply voltage B			0.65	3.6	V
V_{IH}	High-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V	V_{CCI} x 0.70		V
			V_{CCI} = 0.76 V - 1 V	V_{CCI} x 0.70		
			V_{CCI} = 1.1 V - 1.95 V	V_{CCI} x 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	2		
		Control Inputs(xDIR, x$\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	V_{CCA} x 0.70		
			V_{CCA} = 0.76 V - 1 V	V_{CCA} x 0.70		
			V_{CCA} = 1.1 V - 1.95 V	V_{CCA} x 0.65		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	2		
V_{IL}	Low-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V		V_{CCI} x 0.30	V
			V_{CCI} = 0.76 V - 1 V		V_{CCI} x 0.30	
			V_{CCI} = 1.1 V - 1.95 V		V_{CCI} x 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control Inputs(xDIR, x$\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		V_{CCA} x 0.30	
			V_{CCA} = 0.76 V - 1 V		V_{CCA} x 0.30	
			V_{CCA} = 1.1 V - 1.95 V		V_{CCA} x 0.35	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage (3)			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
Δt/Δv	Input transition rate				10	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AXC4T245		UNIT
		PW (TSSOP)	RSV (UQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.9	130.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.3	70.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.3	57.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.1	4.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.4	55.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
						-40°C to 85°C			-40°C to 125°C			
						MIN	TYP (3)	MAX	MIN	TYP (3)	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = -100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = -50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = -200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = -500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = -12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_I	Input leakage current	Control inputs (xDIR, $x\overline{OE}$): $V_I = V_{CCA}$ or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	–0.5		0.5	–1		1	µA
		Data Inputs (xAx, xBx) $V_I = V_{CCI}$ or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	–4		4	–8		8	µA
I_{off}	Partial power down current	A or B Port V_I or V_O = 0 V - 3.6 V		0 V	0 V - 3.6 V	–4		4	–8		8	µA
				0 V - 3.6 V	0 V	–4		4	–8		8	
I_{OZ}	Tri-state output current (4)	A or B Port $V_I = V_{CCI}$ or GND, $V_O = V_{CCO}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	–4		4	–8		8	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND	$I_O = 0$	0.65 V- 3.6 V	0.65 V- 3.6 V			13			26	µA
				0 V	3.6 V	–2			–12			
				3.6 V	0 V			8			16	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND	$I_O = 0$	0.65 V- 3.6 V	0.65 V- 3.6 V			13			26	µA
				0 V	3.6 V			8			16	
				3.6 V	0 V	–2			–12			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND	$I_O = 0$	0.65 V- 3.6 V	0.65 V- 3.6 V			20			40	µA
C_i	Control input capacitance	V_I = 3.3 V or GND		3.3 V	3.3 V		4.5			4.5		pF
C_{io}	Data I/O capacitance	$\overline{OE} = V_{CCA}$, V_O = 1.65V DC +1 MHz -16 dBm sine wave		3.3 V	3.3 V		6.6			6.6		pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All typical data is taken at 25°C.
(4) For I/O ports, the parameter I_{OZ} includes the input leakage current.

6.6 Switching Characteristics, V_{CCA} = 0.7 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	155	0.5	108	0.5	76	0.5	40	0.5	37	0.5	40	0.5	67	0.5	185	ns
				-40°C to 125°C	0.5	155	0.5	108	0.5	76	0.5	40	0.5	37	0.5	40	0.5	67	0.5	185	
		B	A	-40°C to 85°C	0.5	156	0.5	128	0.5	106	0.5	55	0.5	21	0.5	15	0.5	11	0.5	10	
				-40°C to 125°C	0.5	156	0.5	128	0.5	106	0.5	55	0.5	21	0.5	15	0.5	11	0.5	10	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	ns
				-40°C to 125°C	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	
		$\overline{OE}$	B	-40°C to 85°C	0.5	154	0.5	121	0.5	101	0.5	55	0.5	54	0.5	56	0.5	65	0.5	125	
				-40°C to 125°C	0.5	154	0.5	121	0.5	101	0.5	55	0.5	54	0.5	56	0.5	65	0.5	125	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	ns
				-40°C to 125°C	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	
		$\overline{OE}$	B	-40°C to 85°C	0.5	286	0.5	194	0.5	146	0.5	94	0.5	76	0.5	70	0.5	69	0.5	146	
				-40°C to 125°C	0.5	286	0.5	194	0.5	146	0.5	94	0.5	76	0.5	70	0.5	69	0.5	146	

6.7 Switching Characteristics, V_{CCA} = 0.8 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	128	0.5	88	0.5	63	0.5	29	0.5	24	0.5	23	0.5	24	0.5	34	ns
				-40°C to 125°C	0.5	128	0.5	88	0.5	63	0.5	29	0.5	24	0.5	23	0.5	24	0.5	34	
		B	A	-40°C to 85°C	0.5	108	0.5	88	0.5	70	0.5	38	0.5	21	0.5	15	0.5	11	0.5	10	
				-40°C to 125°C	0.5	108	0.5	88	0.5	70	0.5	38	0.5	21	0.5	15	0.5	11	0.5	10	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	ns
				-40°C to 125°C	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	
		$\overline{OE}$	B	-40°C to 85°C	0.5	143	0.5	110	0.5	90	0.5	42	0.5	36	0.5	36	0.5	37	0.5	47	
				-40°C to 125°C	0.5	143	0.5	110	0.5	90	0.5	42	0.5	36	0.5	36	0.5	37	0.5	47	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	ns
				-40°C to 125°C	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	
		$\overline{OE}$	B	-40°C to 85°C	0.5	243	0.5	172	0.5	129	0.5	79	0.5	60	0.5	54	0.5	48	0.5	53	
				-40°C to 125°C	0.5	243	0.5	172	0.5	129	0.5	79	0.5	60	0.5	54	0.5	48	0.5	53	

6.8 Switching Characteristics, V_{CCA} = 0.9 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	106	0.5	70	0.5	53	0.5	24	0.5	18	0.5	17	0.5	16	0.5	19	ns
				-40°C to 125°C	0.5	106	0.5	70	0.5	53	0.5	24	0.5	18	0.5	17	0.5	16	0.5	19	
		B	A	-40°C to 85°C	0.5	76	0.5	63	0.5	53	0.5	27	0.5	18	0.5	13	0.5	10	0.5	9	
				-40°C to 125°C	0.5	76	0.5	63	0.5	53	0.5	27	0.5	18	0.5	13	0.5	10	0.5	9	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	ns
				-40°C to 125°C	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	
		$\overline{OE}$	B	-40°C to 85°C	0.5	138	0.5	105	0.5	84	0.5	37	0.5	30	0.5	28	0.5	26	0.5	30	
				-40°C to 125°C	0.5	138	0.5	105	0.5	84	0.5	37	0.5	30	0.5	28	0.5	26	0.5	30	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	ns
				-40°C to 125°C	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	
		$\overline{OE}$	B	-40°C to 85°C	0.5	222	0.5	148	0.5	116	0.5	71	0.5	52	0.5	46	0.5	39	0.5	39	
				-40°C to 125°C	0.5	222	0.5	148	0.5	116	0.5	71	0.5	52	0.5	46	0.5	39	0.5	39	

6.9 Switching Characteristics, V_{CCA} = 1.2 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	55	0.5	37	0.5	27	0.5	15	0.5	11	0.5	10	0.5	8	0.5	9	ns
				-40°C to 125°C	0.5	55	0.5	37	0.5	27	0.5	15	0.5	11	0.5	10	0.5	8	0.5	9	
		B	A	-40°C to 85°C	0.5	41	0.5	29	0.5	24	0.5	15	0.5	10	0.5	9	0.5	7	0.5	6	
				-40°C to 125°C	0.5	41	0.5	29	0.5	24	0.5	15	0.5	10	0.5	9	0.5	7	0.5	6	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	ns
				-40°C to 125°C	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	
		$\overline{OE}$	B	-40°C to 85°C	0.5	132	0.5	99	0.5	79	0.5	31	0.5	24	0.5	21	0.5	18	0.5	18	
				-40°C to 125°C	0.5	132	0.5	99	0.5	79	0.5	31	0.5	24	0.5	21	0.5	18	0.5	18	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	ns
				-40°C to 125°C	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	
		$\overline{OE}$	B	-40°C to 85°C	0.5	164	0.5	108	0.5	79	0.5	58	0.5	41	0.5	35	0.5	27	0.5	24	
				-40°C to 125°C	0.5	164	0.5	108	0.5	79	0.5	58	0.5	41	0.5	35	0.5	27	0.5	24	

6.10 Switching Characteristics, V_{CCA} = 1.5 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	21	0.5	21	0.5	18	0.5	11	0.5	9	0.5	8	0.5	7	0.5	6	ns
				-40°C to 125°C	0.5	21	0.5	21	0.5	18	0.5	11	0.5	9	0.5	8	0.5	7	0.5	6	
		B	A	-40°C to 85°C	0.5	37	0.5	24	0.5	18	0.5	11	0.5	9	0.5	8	0.5	5	0.5	5	
				-40°C to 125°C	0.5	37	0.5	24	0.5	18	0.5	11	0.5	9	0.5	8	0.5	5	0.5	5	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	ns
				-40°C to 125°C	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	
		$\overline{OE}$	B	-40°C to 85°C	0.5	131	0.5	97	0.5	77	0.5	29	0.5	21	0.5	19	0.5	15	0.5	15	
				-40°C to 125°C	0.5	131	0.5	97	0.5	77	0.5	29	0.5	21	0.5	19	0.5	15	0.5	15	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	ns
				-40°C to 125°C	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	
		$\overline{OE}$	B	-40°C to 85°C	0.5	109	0.5	84	0.5	68	0.5	47	0.5	35	0.5	29	0.5	22	0.5	20	
				-40°C to 125°C	0.5	109	0.5	84	0.5	68	0.5	47	0.5	35	0.5	29	0.5	22	0.5	20	

6.11 Switching Characteristics, V_{CCA} = 1.8 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	15	0.5	15	0.5	13	0.5	9	0.5	8	0.5	7	0.5	6	0.5	6	ns
				-40°C to 125°C	0.5	15	0.5	15	0.5	13	0.5	9	0.5	8	0.5	7	0.5	6	0.5	6	
		B	A	-40°C to 85°C	0.5	40	0.5	23	0.5	17	0.5	10	0.5	8	0.5	7	0.5	5	0.5	4	
				-40°C to 125°C	0.5	40	0.5	23	0.5	17	0.5	10	0.5	8	0.5	7	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	ns
				-40°C to 125°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	
		$\overline{OE}$	B	-40°C to 85°C	0.5	130	0.5	96	0.5	76	0.5	28	0.5	21	0.5	18	0.5	15	0.5	14	
				-40°C to 125°C	0.5	130	0.5	96	0.5	76	0.5	28	0.5	21	0.5	18	0.5	15	0.5	14	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	ns
				-40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	
		$\overline{OE}$	B	-40°C to 85°C	0.5	102	0.5	75	0.5	62	0.5	41	0.5	32	0.5	27	0.5	20	0.5	18	
				-40°C to 125°C	0.5	102	0.5	75	0.5	62	0.5	41	0.5	32	0.5	27	0.5	20	0.5	18	

6.12 Switching Characteristics, V_{CCA} = 2.5 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	11	0.5	11	0.5	10	0.5	7	0.5	5	0.5	5	0.5	5	0.5	5	ns
				-40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	7	0.5	5	0.5	5	0.5	5	0.5	5	
		B	A	-40°C to 85°C	0.5	67	0.5	24	0.5	16	0.5	8	0.5	7	0.5	6	0.5	5	0.5	4	
				-40°C to 125°C	0.5	67	0.5	24	0.5	16	0.5	8	0.5	7	0.5	6	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	ns
				-40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	
		$\overline{OE}$	B	-40°C to 85°C	0.5	128	0.5	95	0.5	76	0.5	27	0.5	20	0.5	17	0.5	13	0.5	13	
				-40°C to 125°C	0.5	128	0.5	95	0.5	76	0.5	27	0.5	20	0.5	17	0.5	13	0.5	13	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	ns
				-40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	
		$\overline{OE}$	B	-40°C to 85°C	0.5	120	0.5	70	0.5	56	0.5	36	0.5	26	0.5	22	0.5	18	0.5	16	
				-40°C to 125°C	0.5	120	0.5	70	0.5	56	0.5	36	0.5	26	0.5	22	0.5	18	0.5	16	

6.13 Switching Characteristics, V_{CCA} = 3.3 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	10	0.5	10	0.5	9	0.5	6	0.5	5	0.5	4	0.5	4	0.5	4	ns
				-40°C to 125°C	0.5	10	0.5	10	0.5	9	0.5	6	0.5	5	0.5	4	0.5	4	0.5	4	
		B	A	-40°C to 85°C	0.5	185	0.5	34	0.5	19	0.5	9	0.5	6	0.5	6	0.5	5	0.5	4	
				-40°C to 125°C	0.5	185	0.5	34	0.5	19	0.5	9	0.5	6	0.5	6	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	ns
				-40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	
		$\overline{OE}$	B	-40°C to 85°C	0.5	141	0.5	95	0.5	75	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12	
				-40°C to 125°C	0.5	141	0.5	95	0.5	75	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	ns
				-40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	
		$\overline{OE}$	B	-40°C to 85°C	0.5	189	0.5	82	0.5	59	0.5	35	0.5	24	0.5	20	0.5	16	0.5	14	
				-40°C to 125°C	0.5	189	0.5	82	0.5	59	0.5	35	0.5	24	0.5	20	0.5	16	0.5	14	

6.14 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.2		pF
			0.8 V	0.8 V		2.1		
			0.9 V	0.9 V		2.1		
			1.2 V	1.2 V		2.1		
			1.5 V	1.5 V		2.0		
			1.8 V	1.8 V		2.0		
			2.5 V	2.5 V		2.1		
			3.3 V	3.3 V		2.3		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.5		pF
			0.8 V	0.8 V		1.5		
			0.9 V	0.9 V		1.5		
			1.2 V	1.2 V		1.4		
			1.5 V	1.5 V		1.4		
			1.8 V	1.8 V		1.4		
			2.5 V	2.5 V		1.4		
			3.3 V	3.3 V		1.6		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		12.1		pF
			0.8 V	0.8 V		12.1		
			0.9 V	0.9 V		12.1		
			1.2 V	1.2 V		12.4		
			1.5 V	1.5 V		13.0		
			1.8 V	1.8 V		14.2		
			2.5 V	2.5 V		17.4		
			3.3 V	3.3 V		20.1		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.1		pF
			0.8 V	0.8 V		1.1		
			0.9 V	0.9 V		1.1		
			1.2 V	1.2 V		1.1		
			1.5 V	1.5 V		1.1		
			1.8 V	1.8 V		1.1		
			2.5 V	2.5 V		1.1		
			3.3 V	3.3 V		1.1		

Operating Characteristics: T_A = 25°C (continued)

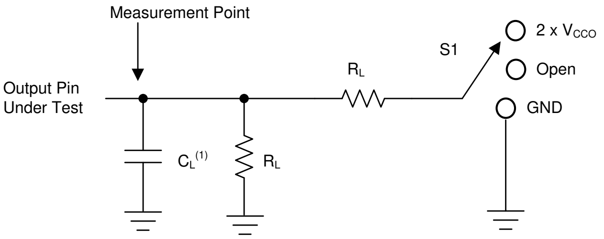
PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdB}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		12.1		pF
			0.8 V	0.8 V		12.1		
			0.9 V	0.9 V		12.1		
			1.2 V	1.2 V		12.4		
			1.5 V	1.5 V		12.9		
			1.8 V	1.8 V		14.1		
			2.5 V	2.5 V		17.2		
			3.3 V	3.3 V		20.1		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.1		pF
			0.8 V	0.8 V		1.1		
			0.9 V	0.9 V		1.1		
			1.2 V	1.2 V		1.1		
			1.5 V	1.5 V		1.1		
			1.8 V	1.8 V		1.1		
			2.5 V	2.5 V		1.1		
			3.3 V	3.3 V		1.1		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.2		pF
			0.8 V	0.8 V		1.8		
			0.9 V	0.9 V		1.8		
			1.2 V	1.2 V		1.7		
			1.5 V	1.5 V		1.7		
			1.8 V	1.8 V		1.7		
			2.5 V	2.5 V		2		
			3.3 V	3.3 V		2.5		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.1		pF
			0.8 V	0.8 V		1.8		
			0.9 V	0.9 V		1.8		
			1.2 V	1.2 V		1.7		
			1.5 V	1.5 V		1.7		
			1.8 V	1.8 V		1.7		
			2.5 V	2.5 V		2		
			3.3 V	3.3 V		2.1		

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- dv/dt ≤ 1 ns/V

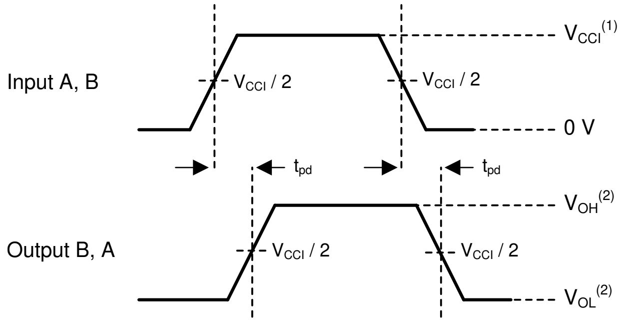


(1) C_L includes probe and jig capacitance.

图 1. Load Circuit

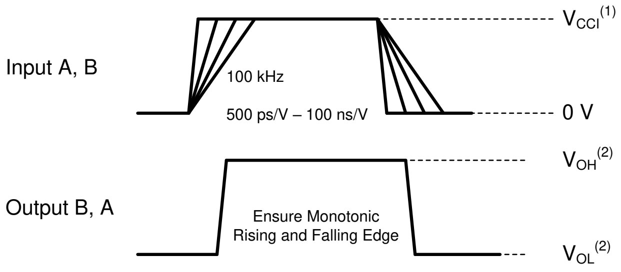
表 1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
Δt/Δv	Input transition rise or fall rate	0.65 V – 3.6 V	1 MΩ	15 pF	Open	N/A
t_{pd}	Propagation (delay) time	1.1 V – 3.6 V	2 kΩ	15 pF	Open	N/A
		0.65 V – 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	2 × V_{CCO}	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	2 × V_{CCO}	0.1 V
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	GND	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	GND	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	GND	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	GND	0.1 V



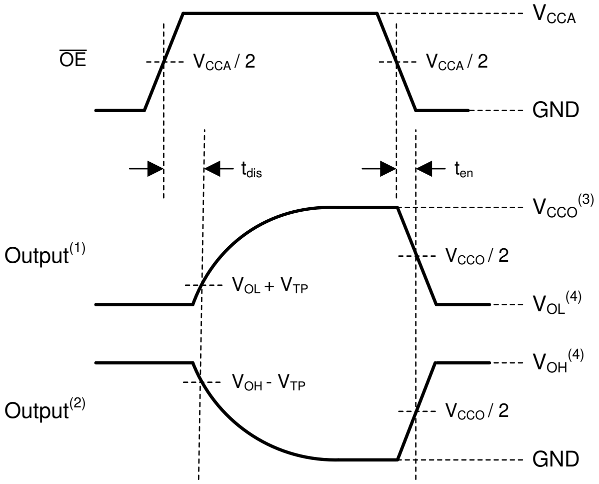
1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

图 2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

图 3. Input Transition Rise or Fall Rate



(1) Output waveform on the condition that input is driven to a valid Logic Low.

(2) Output waveform on the condition that input is driven to a valid Logic High.

(3) V_{CCO} is the supply pin associated with the output port.

(4) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

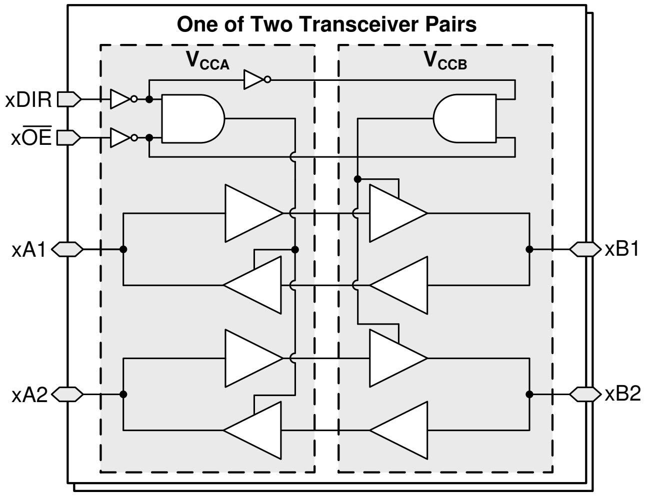
图 4. Enable Time And Disable Time

8 Detailed Description

8.1 Overview

The SN74AXC4T245 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (1DIR, 2DIR,$1\overline{OE}$, and $2\overline{OE}$) are referenced to V_{CCA} logic levels, and Bx pins are referenced to V_{CCB} logic levels. The A port is able to accept I/O voltages ranging from 0.65 V to 3.6 V, while the B port can accept I/O voltages from 0.65 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state. See *Device Functional Modes* for a summary of the operation of the control logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

8.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.4 V_{CC} Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is <100mV.

Feature Description (接下页)

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.3.6 Glitch-free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

8.3.7 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in 图 5.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

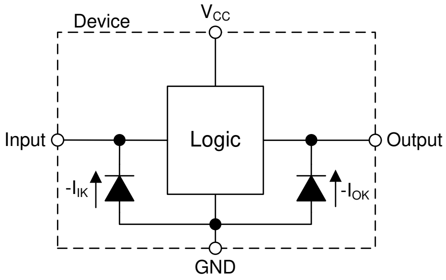


图 5. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.8 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 0.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V and 3.3 V).

8.3.9 Supports High-Speed Translation

The SN74AXC4T245 device can support high data-rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

8.4 Device Functional Modes

表 2. Function Table (Each 2-Bit Section)[1]

CONTROL INPUTS		Port Status		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AXC4T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AXC4T245 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380 Mbps when device translates a signal from 1.8 V to 3.3 V.

One example application is shown in 图 6, where the SN74AXC4T245 device is used to translate a low voltage UART signal from an SoC to a higher voltage signal which properly drive the inputs of the bluetooth module, and vice versa.

9.2 Typical Application

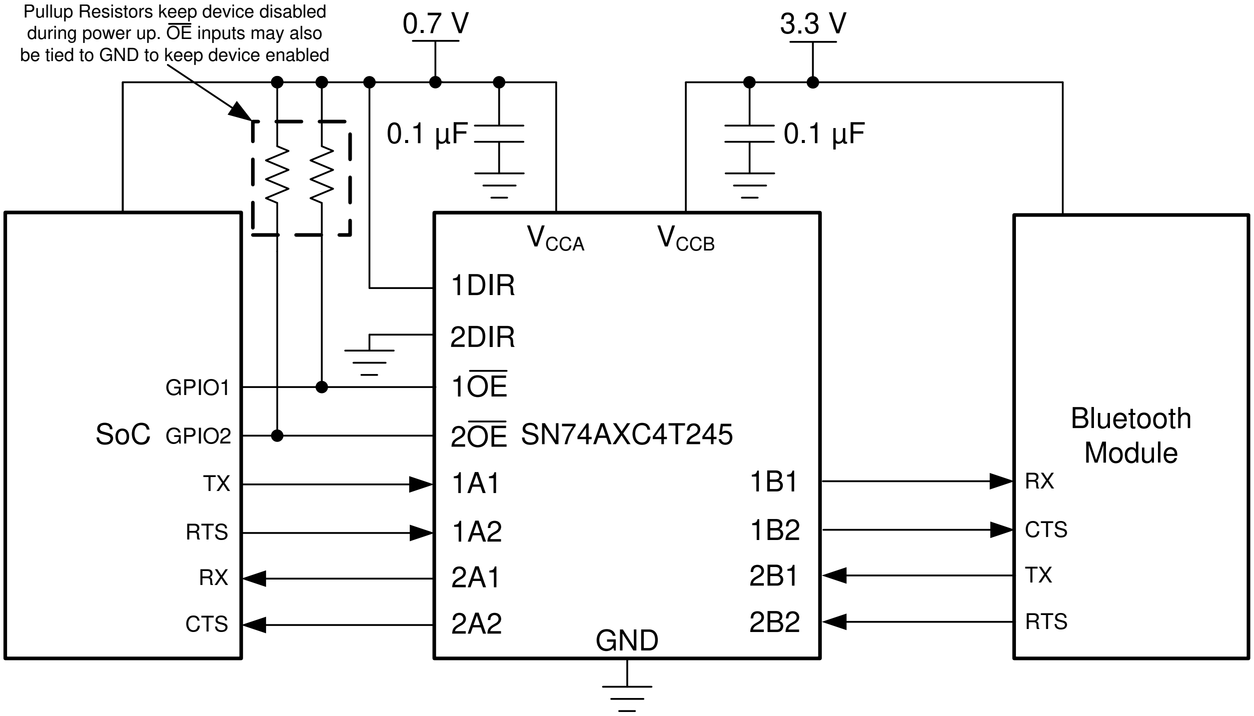


图 6. UART Interface Application

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 3.

表 3. Design Parameters

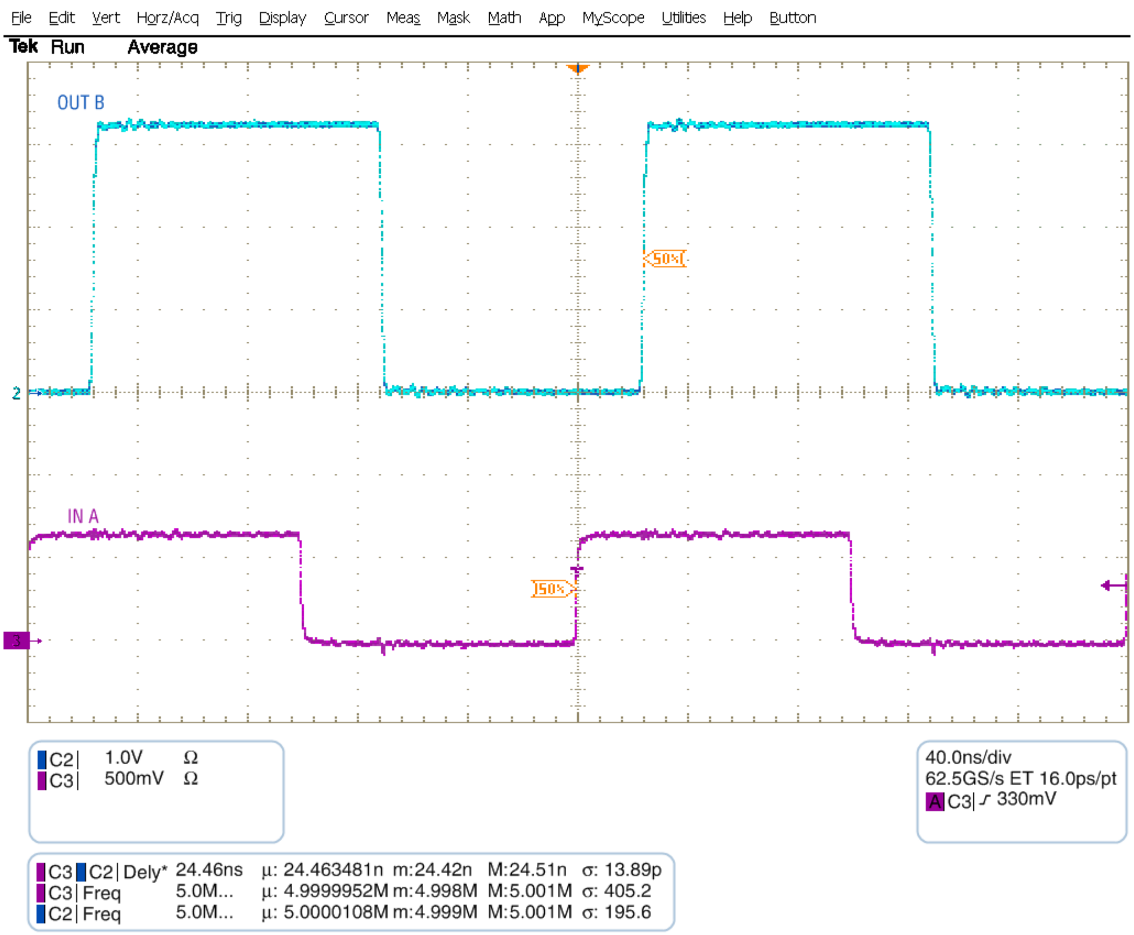
DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC4T245 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXC4T245 device is driving to determine the output voltage range.

9.2.3 Application Curve



```
C2|  1.0V    Ω
C3|  500mV   Ω
```

```
40.0ns/div
62.5GS/s ET 16.0ps/pt
A C3| ⌐ 330mV
```

```
C3 C2| Dely* 24.46ns  µ: 24.463481n m:24.42n  M:24.51n  σ: 13.89p
C3| Freq     5.0M...  µ: 4.9999952M m:4.998M  M:5.001M  σ: 405.2
C2| Freq     5.0M...  µ: 5.0000108M m:4.999M  M:5.001M  σ: 195.6
```

图 7. Up Translation at 2.5 MHz (0.7 V to 3.3 V)

10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible.
- Use short trace lengths to avoid excessive loading.

11.2 Layout Example

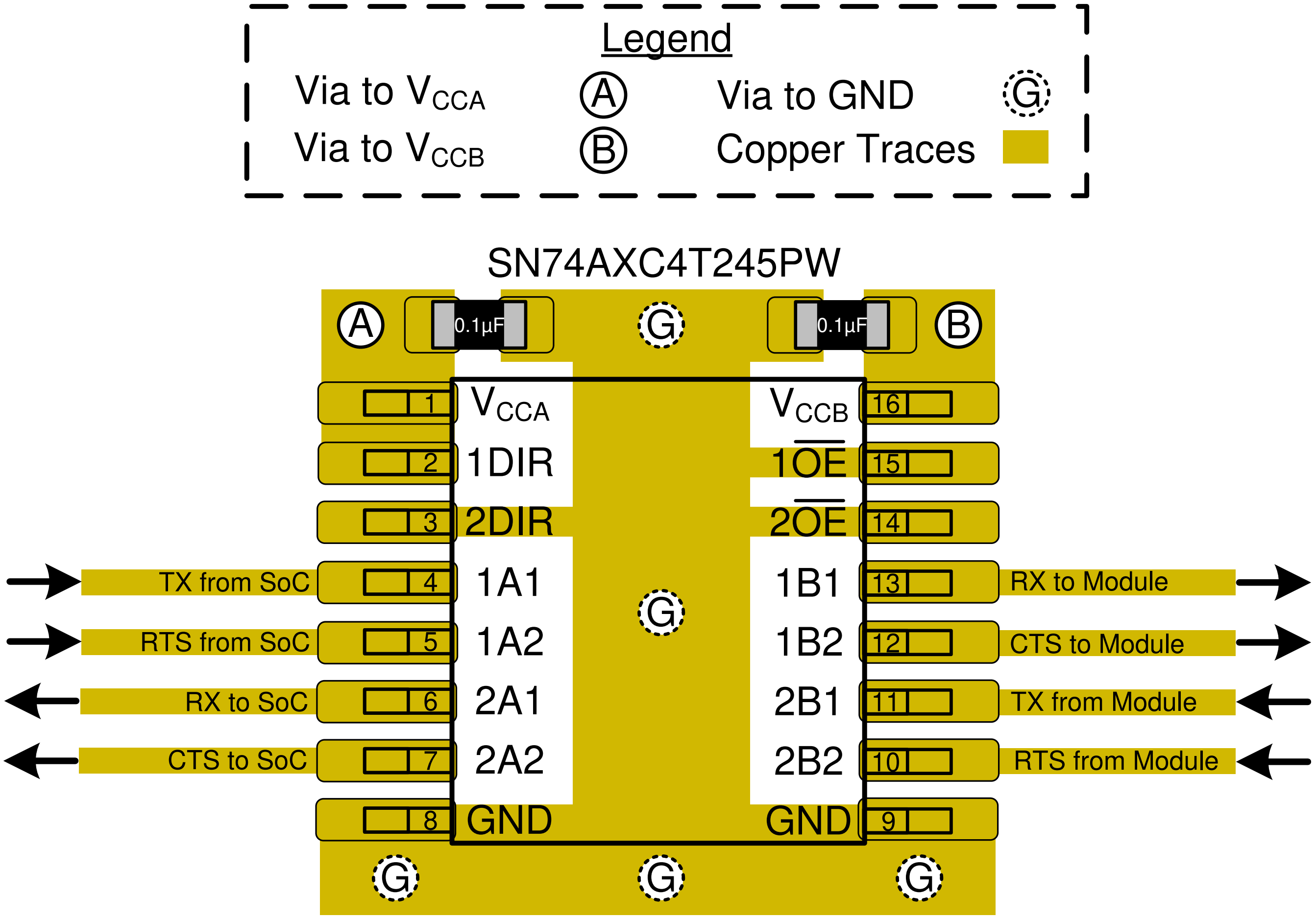


图 8. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

德州仪器 (TI)，*《慢速或浮点 CMOS 输入的影响》*应用报告
德州仪器 (TI)，*《AXC 系列器件电源定序》* 应用报告

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。
这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AXC4T245BQBR	PREVIEW	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4T245	
SN74AXC4T245PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SN4T245	Samples
SN74AXC4T245RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1TIR	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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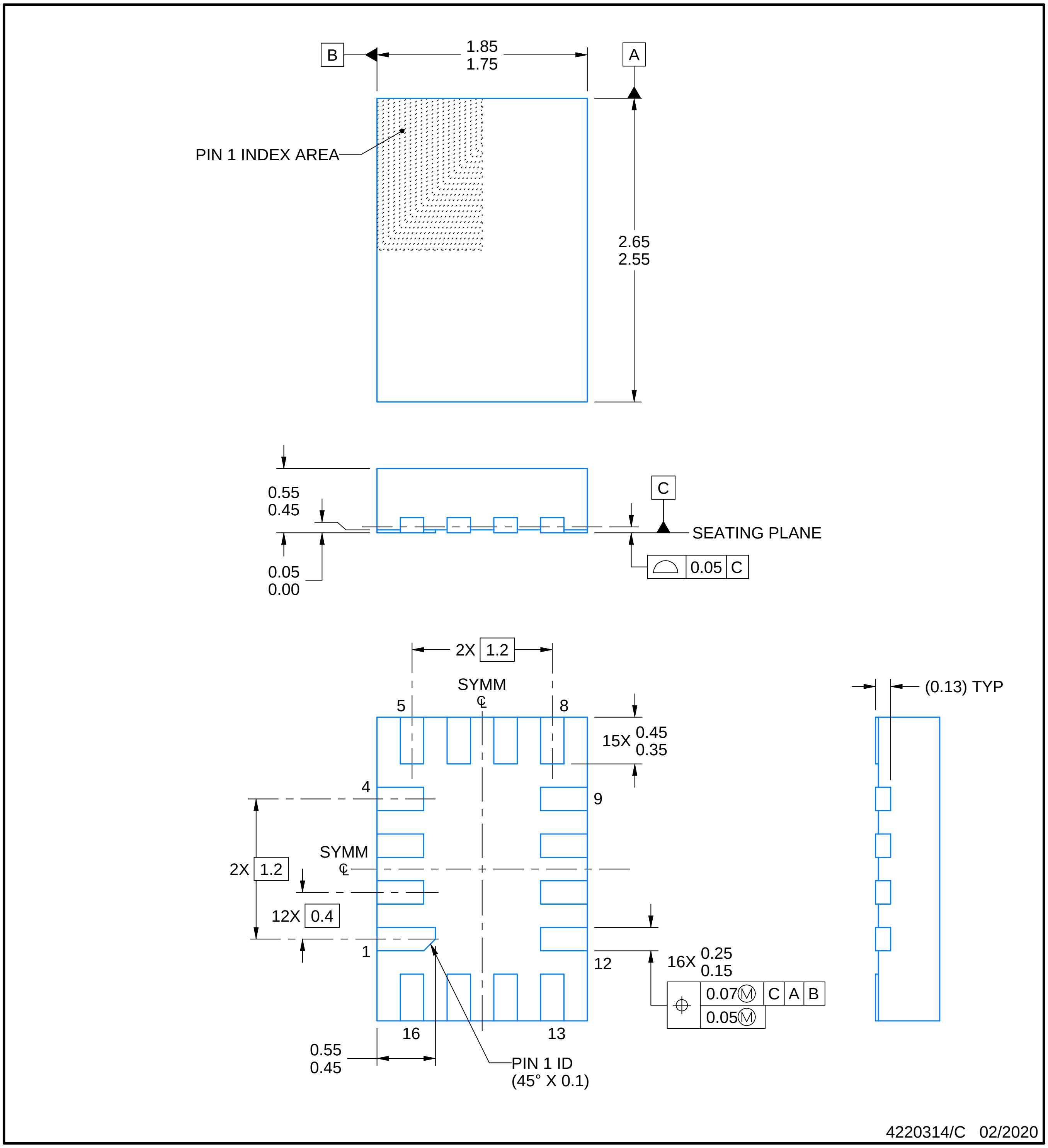
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RSV0016A

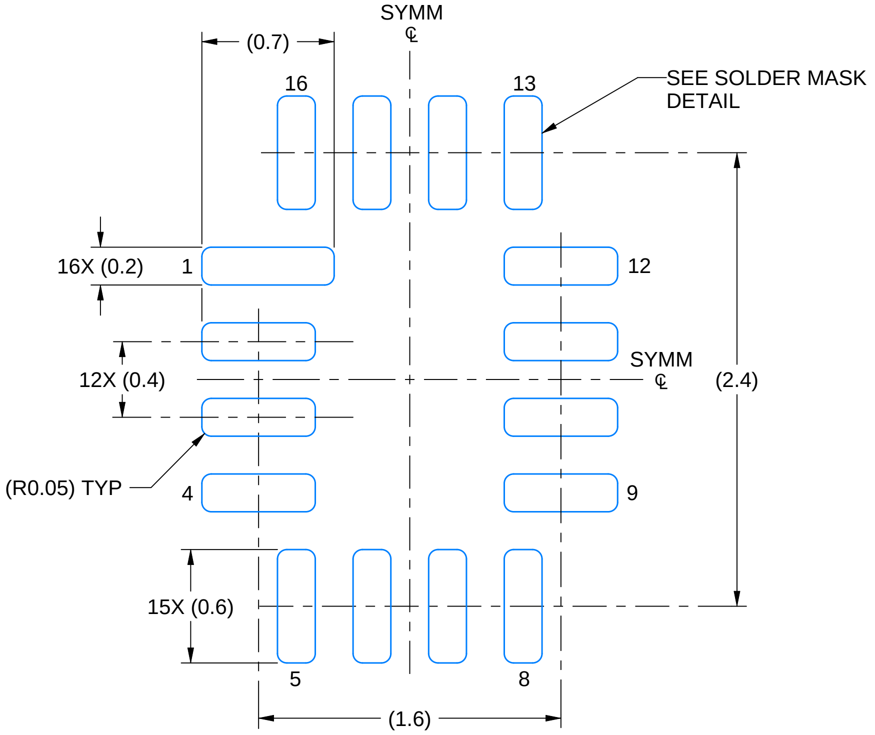
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

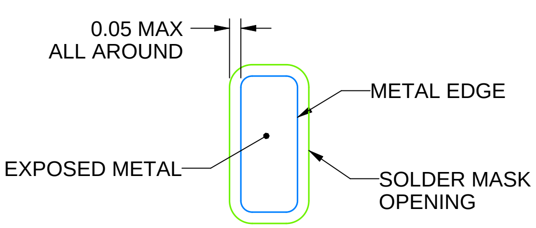


NOTES:

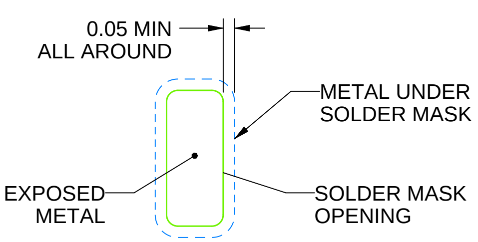
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



NON SOLDER MASK
DEFINED
(PREFERRED)

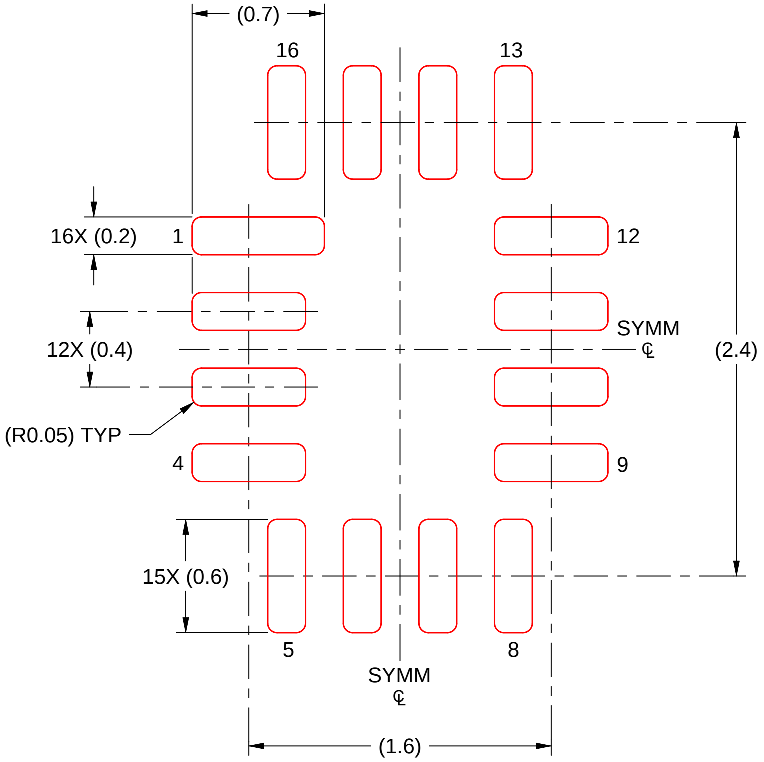


SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

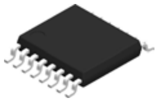


SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

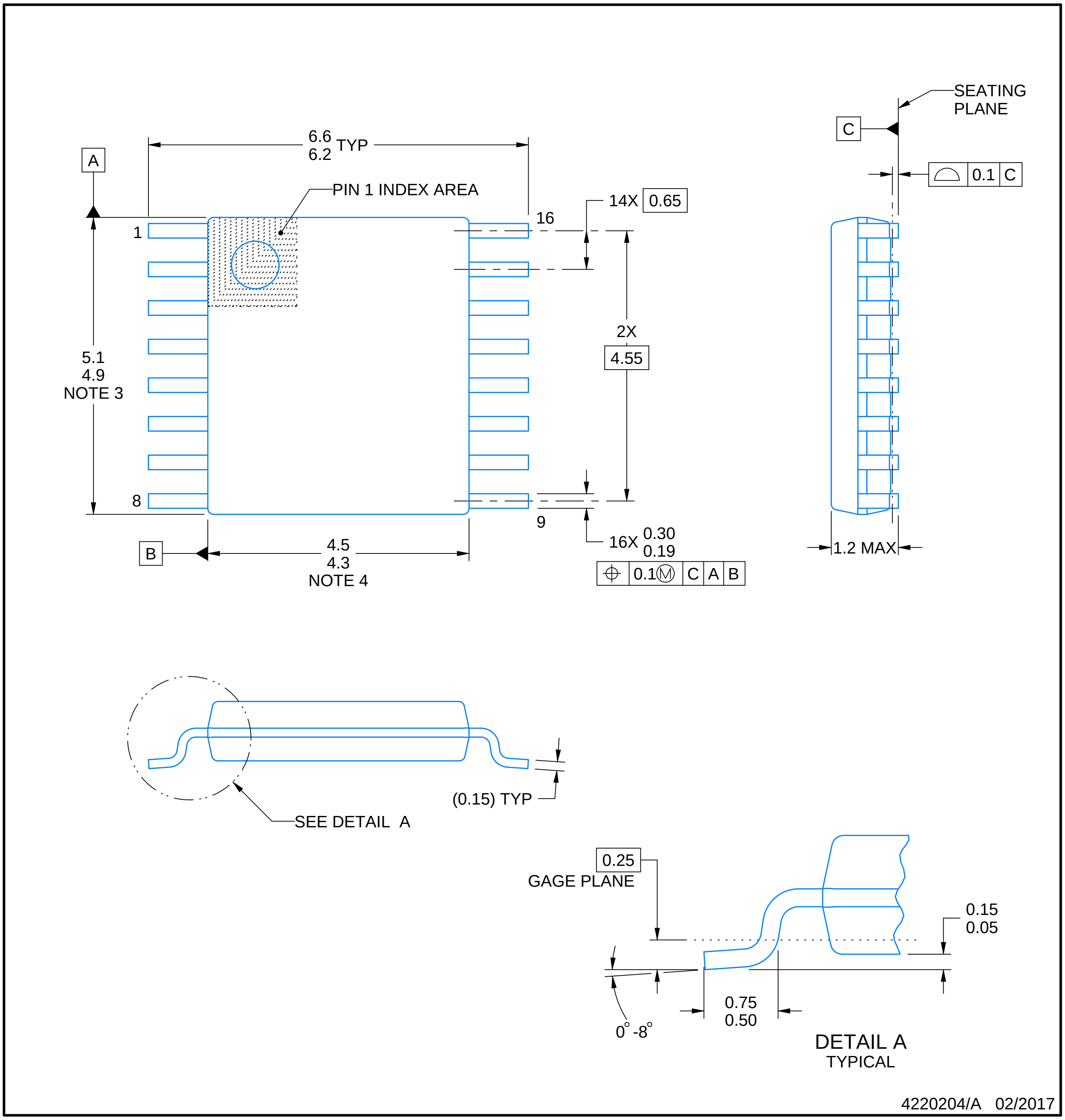
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PACKAGE OUTLINE

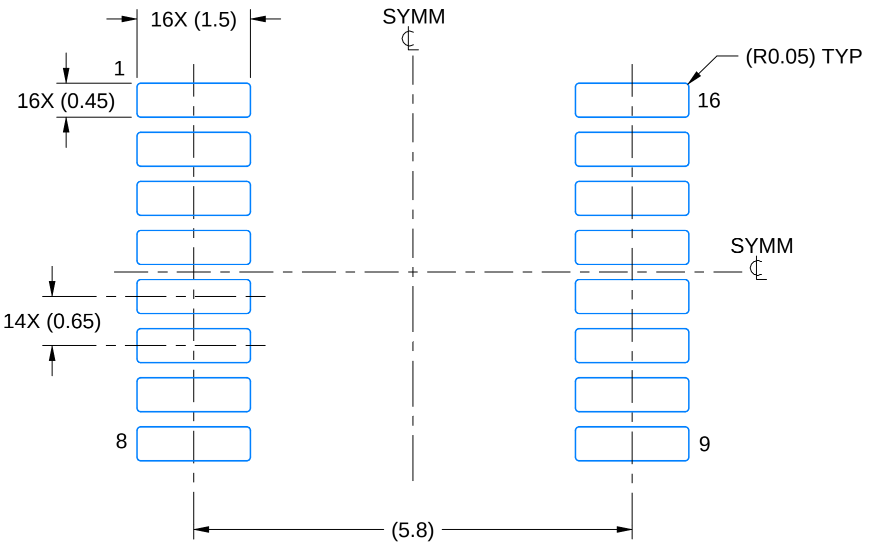
SMALL OUTLINE PACKAGE



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

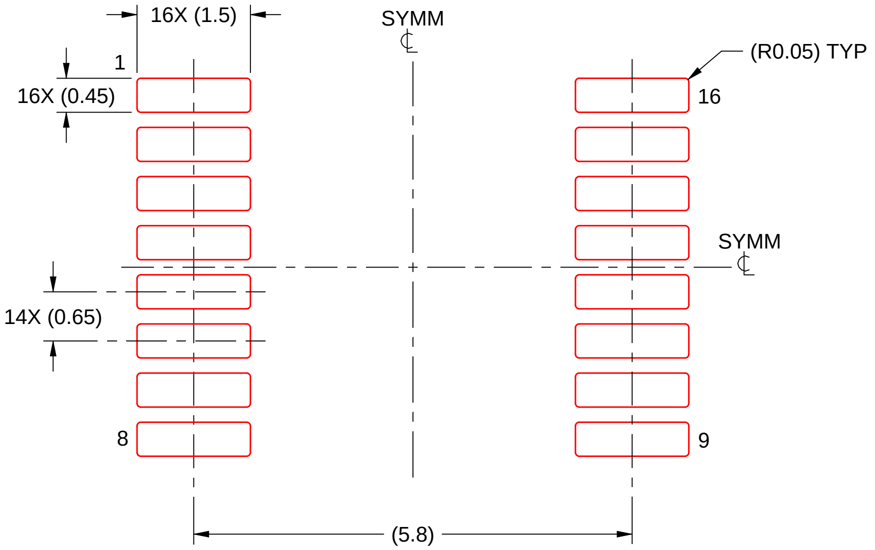
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

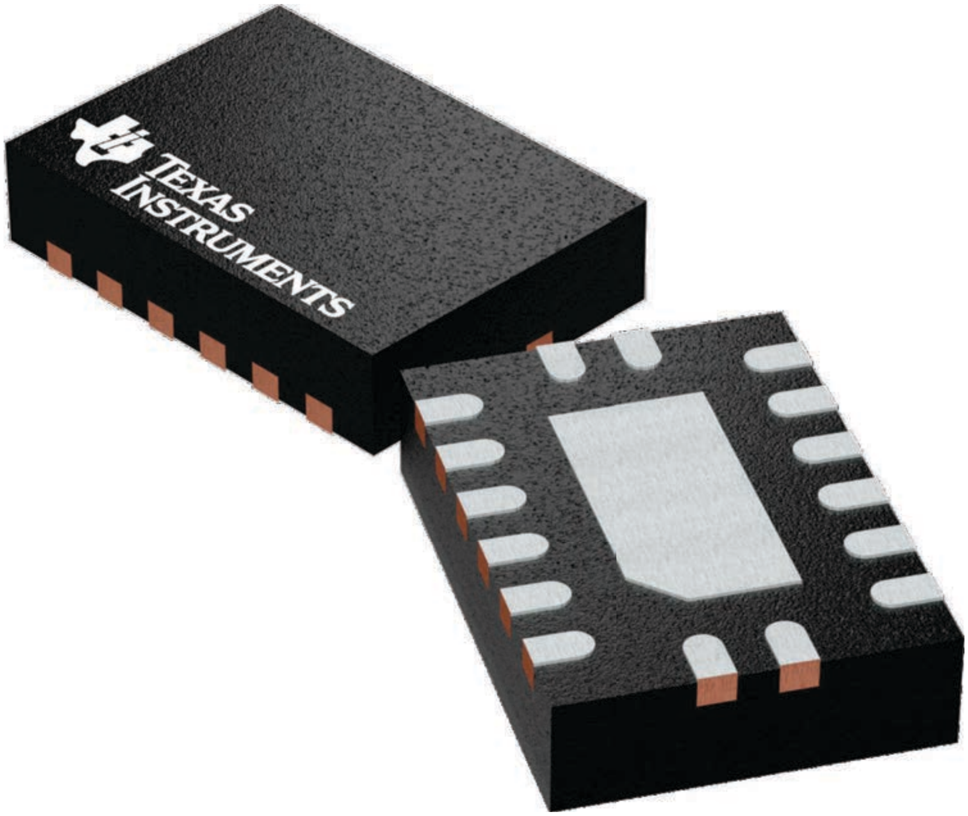
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

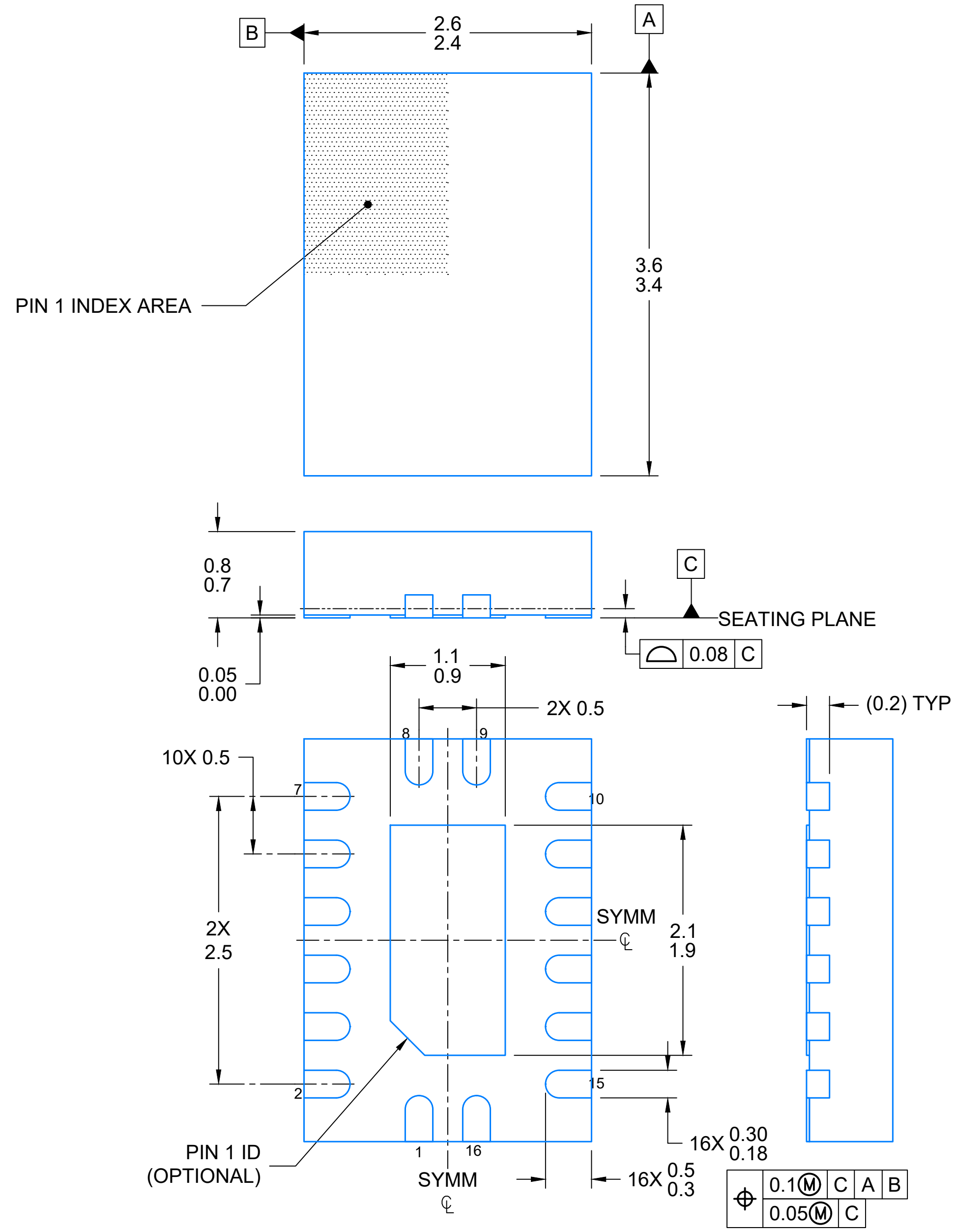


4226161/A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

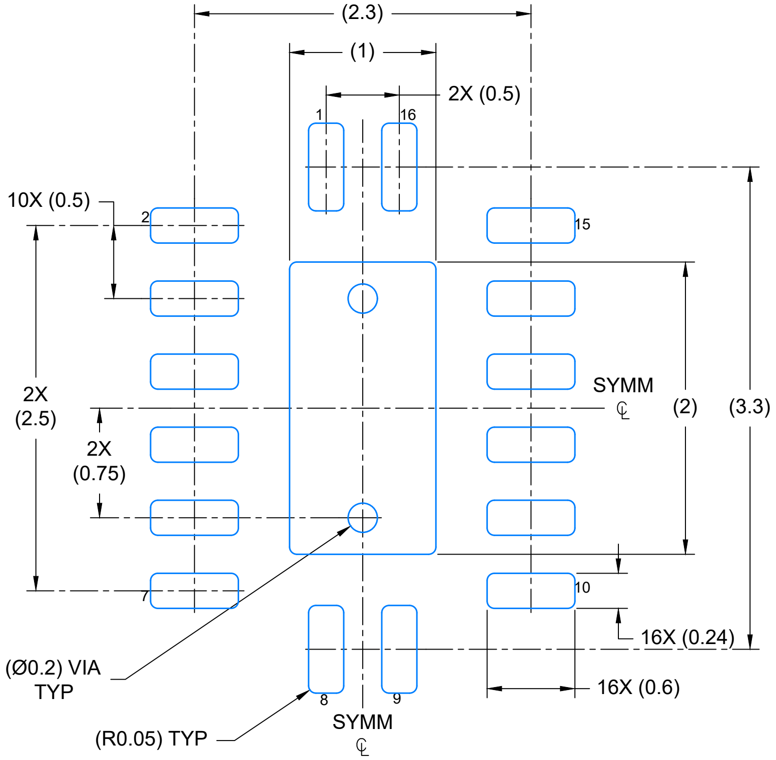
PLASTIC QUAD FLAT PACK-NO LEAD



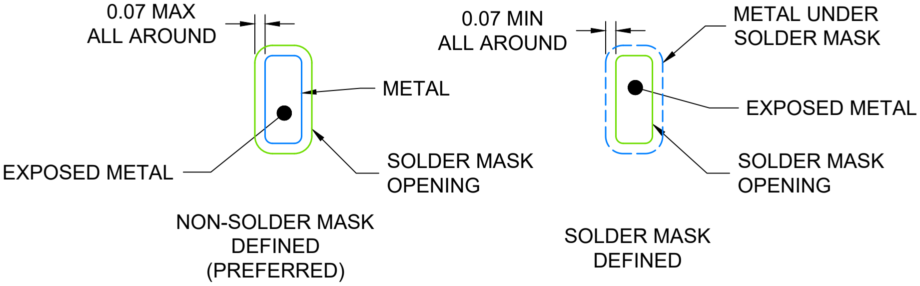
4224640/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



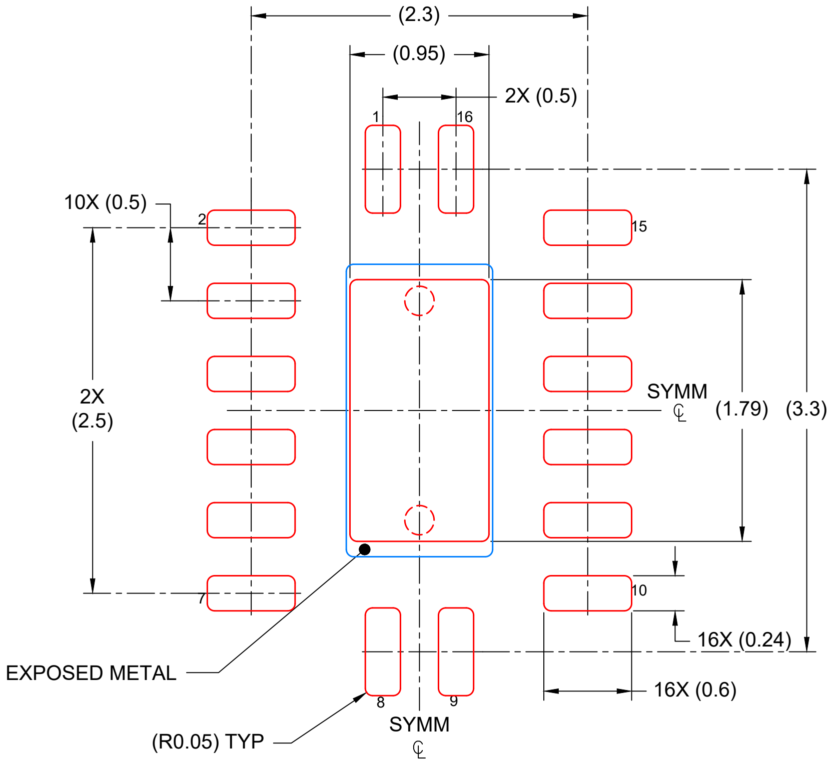
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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