16 位双电源总线收发器
此收发器具有可配置电压转换和 3 态输出

查询样品: SN74AVCB164245-EP

特性

- 德州仪器 **(TI) Widebus™** 系列
- **DOC™** 电路产品成员动态改变输出阻抗，从而在不降低速度的情况下达到降噪的目的。
- 动态驱动能力与 **2.5V** V_{CC}时 I_{OH}和 I_{OL}为 **±24mA** 的标准输出等效
- 控制输入 V_{IH}和 V_{IL}电平以 V_{CCB}电压为基准
- 如果任何一个 V_{CC}输入接地 **(GND)**，那么两个端口都处于高阻抗状态
- 过压耐受输入和输出可实现混合电压模式数据通信
- $I_{关闭}$支持部分断电模式运行
- 完全可配置双电源轨设计可使每个端口在整个 **1.4V-3.6V** 电源电压范围内运行
- 锁断性能超过 **100mA**（符合 **JESD 78**，**II** 类规范的要求）
- 静电放电 **(ESD)** 保护性能超过 **JESD 22** 规范要求
  - **2000V** 人体模型 **(A114-A)**
  - **200V** 机器模型 **(A115-A)**
  - **750V** 充电器件模型 **(C101)**

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 军用（**-55°C** 至 **125°C**）温度范围内可用 (1)
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

(1) 可定制工作温度范围

说明

这个 16 位（双八进制）非反相总线收发器使用两个独立的可配置电源轨。

A 端口被设计用于跟踪 V_{CCA}。 V_{CCA}可接受从 1.4V 到 3.6V 范围内的任一电源电压。B 端口被设计用于跟踪 V_{CCB}。 V_{CCB}可接受从 1.4 至 3.6V 间的任一电源电压值。这可实现 1.5V，1.8V，2.5V和 3.3V 电压节点间的通用低压双向转换。

SN74AVCB164245 被设计用来实现数据总线间的异步通信。 根据方向控制 (DIR) 输入上的逻辑电平，此器件将数据从 A 总线发送至 B 总线，或者将数据从 B 总线发送至 A 总线。 输出使能 ($\overline{OE}$) 可被用来禁用输出，这样可有效隔离总线。

SN74AVCB164245 的设计方式决定了控制引脚（1DIR，2DIR，1$\overline{OE}$和 2$\overline{OE}$）由 V_{CCB}供电。

为了确保加电或断电期间的高阻抗状态，$\overline{OE}$应通过一个上拉电阻器连接至 V_{CC}；该电阻器的最小值由驱动器的电流吸收能力来决定。

该器件完全符合使用 $I_{关闭}$的部分断电应用的规范要求。 $I_{关闭}$电路禁用输出，从而可防止其断电时破坏性电流从该器件回流。 如果任何一个 V_{CC}输入接地 (GND)，那么两个端口都处于高阻抗状态。

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	TSSOP-DGG	Reel of 2000	CAVCB164245MDGGREP	AVCB164245M	V62/13602-01XE
		Tube of 40	CAVCB164245MDGGEP		V62/13602-01XE-T

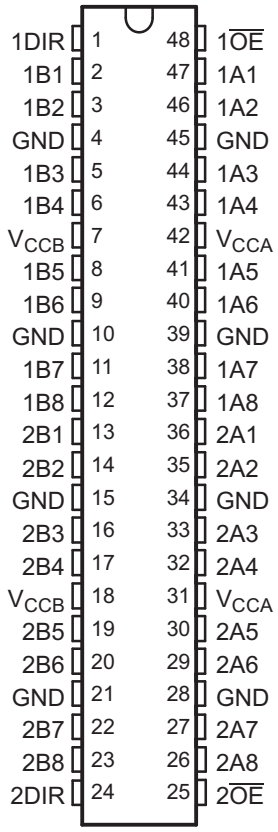
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus, DOC are trademarks of Texas Instruments.

TERMINAL ASSIGNMENTS

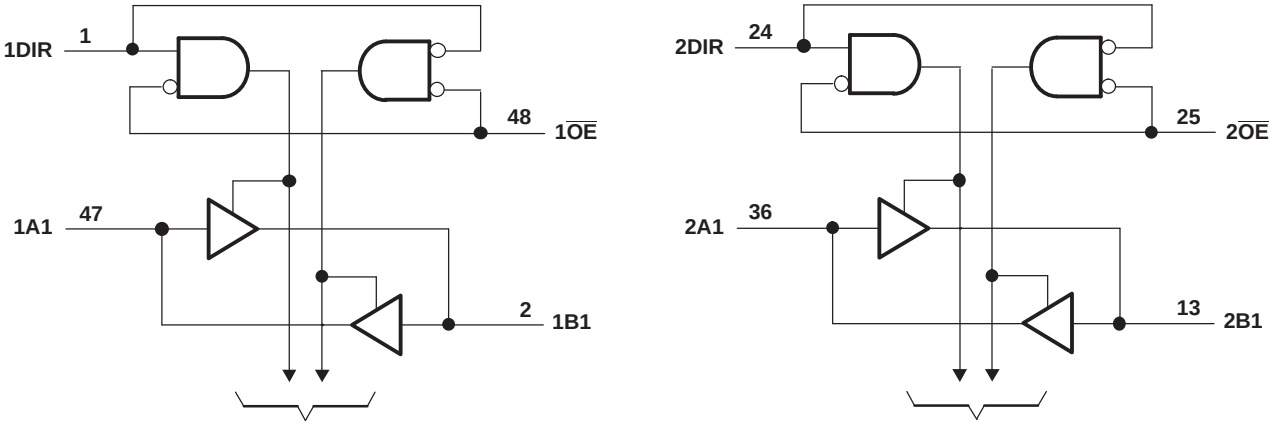
DGG PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH 8-BIT SECTION)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Figure 1. LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DGV packages.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

THERMAL INFORMATION

THERMAL METRIC(1)		SN74AVCB164245	UNITS
		DGG	
		48 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	59.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	13.9	
θ_{JB}	Junction-to-board thermal resistance(4)	27.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	26.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS(1)(2)(3)

T_A = −55°C to 125°C, over recommended input voltage range (unless otherwise noted)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.4	3.6	V
V_{CCB}	Supply voltage				1.4	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.4 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs	1.4 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCB})	1.4 V to 1.95 V		V_{CCB} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCB})	1.4 V to 1.95 V			V_{CCB} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.4 V to 1.6 V		–2	mA
				1.65 V to 1.95 V		–4	
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.4 V to 1.6 V		2	mA
				1.65 V to 1.95 V		4	
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–55	125	°C

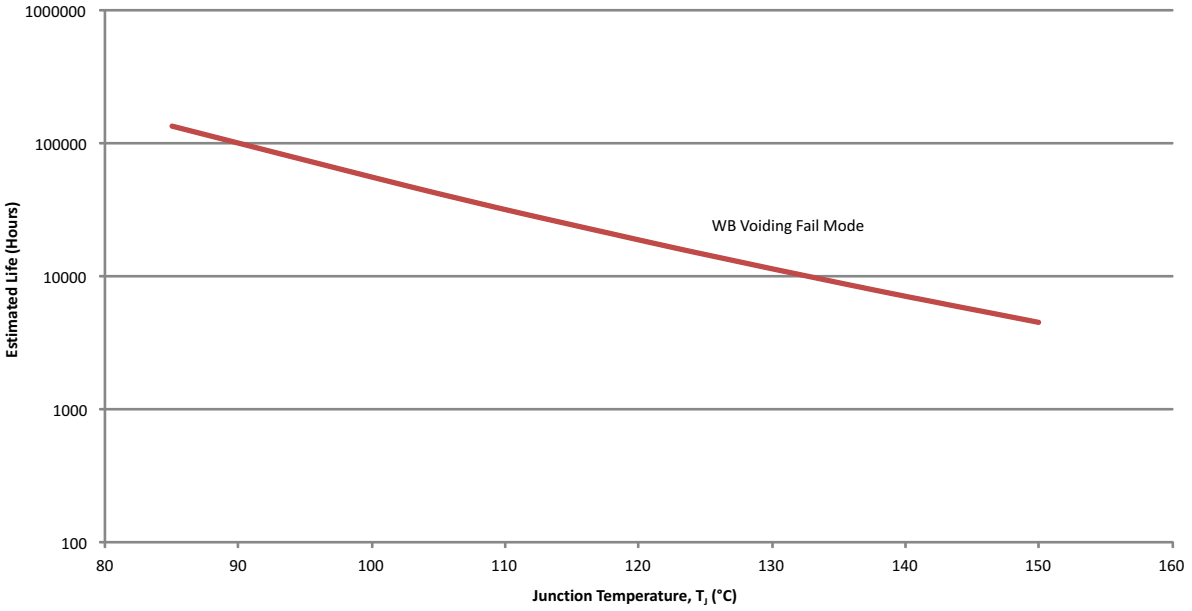
(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the data output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS(1)(2)

T_A = −55°C to 125°C, over recommended input voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP(3)	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.4 V to 3.6 V	1.4 V to 3.6 V	V_{CCO} – 0.2			V
		I_{OH} = –2 mA	$V_I = V_{IH}$	1.4 V	1.4 V	1.05			
		I_{OH} = –4 mA	$V_I = V_{IH}$	1.65 V	1.65 V	1.2			
		I_{OH} = –8 mA	$V_I = V_{IH}$	2.3 V	2.3 V	1.7			
		I_{OH} = –12 mA	$V_I = V_{IH}$	3 V	3 V	2.2			
V_{OL}		I_{OH} = 100 µA	$V_I = V_{IL}$	1.4 V to 3.6 V	1.4 V to 3.6 V			0.2	V
		I_{OH} = 2 mA	$V_I = V_{IL}$	1.4 V	1.4 V			0.35	
		I_{OH} = 4 mA	$V_I = V_{IL}$	1.65 V	1.65 V			0.45	
		I_{OH} = 8 mA	$V_I = V_{IL}$	2.3 V	2.3 V			0.6	
		I_{OH} = 12 mA	$V_I = V_{IL}$	3 V	3 V			0.75	
I_I	Control inputs	$V_I = V_{CCB}$ or GND		1.4 V to 3.6 V	3.6 V			±2.5	µA
I_{off}	A port	V_I or V_O = 0 to 3.6 V		0 V	0 to 3.6 V			±10	µA
	B port			0 to 3.6 V	0 V			±10	
I_{OZ} (4)	A or B ports	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V			±12.5	µA
	B port		$\overline{OE}$ = don't care	0 V	3.6 V			±12.5	
	A port			3.6 V	0 V			±12.5	
I_{CCA}		$V_I = V_{CCI}$ or GND,	I_O = 0	1.6 V	1.6 V			35	µA
				1.95 V	1.95 V			35	
				2.7 V	2.7 V			45	
				0 V	3.6 V			-50	
				3.6 V	0 V			50	
				3.6 V	3.6 V			50	
I_{CCB}		$V_I = V_{CCI}$ or GND,	I_O = 0	1.6 V	1.6 V			35	µA
				1.95 V	1.95 V			35	
				2.7 V	2.7 V			45	
				0 V	3.6 V			50	
				3.6 V	0 V			-50	
				3.6 V	3.6 V			50	
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		4		pF
C_{io}	A or B ports	V_O = 3.3 V or GND		3.3 V	3.3 V		5		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) All typical values are at T_A = 25°C.
(4) For I/O ports, the parameter I_{OZ} includes the input leakage current.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

Figure 2. SN74AVCB164245-EP Operating Life Derating Chart

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 1.5 V ± 0.1 V (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
t_{en}	$\overline{OE}$	A	2.5	8.4	2.4	7.4	2.1	5.2	1.9	4.2	ns
		B	2.1	9	2.9	9.8	3.2	10	3	9.8	
t_{dis}	$\overline{OE}$	A	2.2	6.9	2.3	6.1	1.3	3.6	1.3	3	ns
		B	2.1	7.1	2.3	6.4	1.7	5.1	1.6	4.8	

SWITCHING CHARACTERISTICS

T_A = −55°C to 125°C, V_{CCA} = 1.5 V ± 0.1 V (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		12.7		12.3		11.5		11.8	ns
	B	A		12.8		13.4		13.6		13.3	
t_{en}	$\overline{OE}$	A		14.8		13.9		12.4		11.9	ns
		B		15		15.8		16		15.8	
t_{dis}	$\overline{OE}$	A		12.9		12.1		9.6		9	ns
		B		13.1		12.4		11.1		10.8	

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 1.8 V ± 0.15 V (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.7	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
t_{en}	$\overline{OE}$	A	2.6	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.8	7.6	2.6	7.7	2.6	7.6	2.6	7.4	
t_{dis}	$\overline{OE}$	A	2.3	7	2.3	6.1	1.3	3.6	1.3	3	ns
		B	1.8	7	2.5	6.3	1.8	4.7	1.7	4.4	

SWITCHING CHARACTERISTICS

T_A = −55°C to 125°C, V_{CCA} = 1.8 V ± 0.15 V (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		12.7		12		10.7		10.3	ns
	B	A		11.5		12		11.8		11.5	
t_{en}	$\overline{OE}$	A		14.5		13.5		12.1		11.9	ns
		B		13.6		13.7		13.6		13.4	
t_{dis}	$\overline{OE}$	A		13		12.1		9.6		9	ns
		B		13		12.3		10.7		10.4	

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 2.5 V ± 0.2 V (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
t_{en}	$\overline{OE}$	A	3.1	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.7	5.7	2.2	5.5	2.2	5.3	2.2	5.1	
t_{dis}	$\overline{OE}$	A	2.4	7	3	6.1	1.4	3.6	1.2	3	ns
		B	1.2	5.8	1.9	5	1.4	3.6	1.3	3.3	

SWITCHING CHARACTERISTICS

T_A = −55°C to 125°C, V_{CCA} = 2.5 V ± 0.2 V (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		12		11.6		10		9.4	ns
	B	A		10.6		10.4		10		9.7	
t_{en}	$\overline{OE}$	A		14.5		13.5		11.3		10.2	ns
		B		11.7		11.5		11.3		11.1	
t_{dis}	$\overline{OE}$	A		13		12.1		9.6		9	ns
		B		11.8		11		9.6		9.3	

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 3.3 V ± 0.3 V (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
t_{en}	$\overline{OE}$	A	2.6	8.3	2.5	7.4	2.2	5.2	1.9	4.1	ns
		B	1.6	4.9	2	4.5	2	4.3	1.9	4.1	
t_{dis}	$\overline{OE}$	A	2.3	7	3	6	1.3	3.5	1.2	3.5	ns
		B	1.3	6.9	2.1	5.5	1.6	3.8	1.5	3.5	

SWITCHING CHARACTERISTICS

T_A = −55°C to 125°C, V_{CCA} = 3.3 V ± 0.3 V (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		11.9		11.4		9.7		9.1	ns
	B	A		10.5		9.8		9.3		9.1	
t_{en}	$\overline{OE}$	A		14.3		13.4		11.2		10.1	ns
		B		11.3		10.5		10.3		10.1	
t_{dis}	$\overline{OE}$	A		13		12		9.5		9.5	ns
		B		12.9		11.5		9.8		9.5	

OPERATING CHARACTERISTICS

V_{CCA} and V_{CCB} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pdA} (V_{CCA})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	C_L = 0, f = 10 MHz	14	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		20	
		Outputs disabled		7	
C_{pdB} (V_{CCB})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	C_L = 0, f = 10 MHz	20	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		14	
		Outputs disabled		7	

OUTPUT DESCRIPTION

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

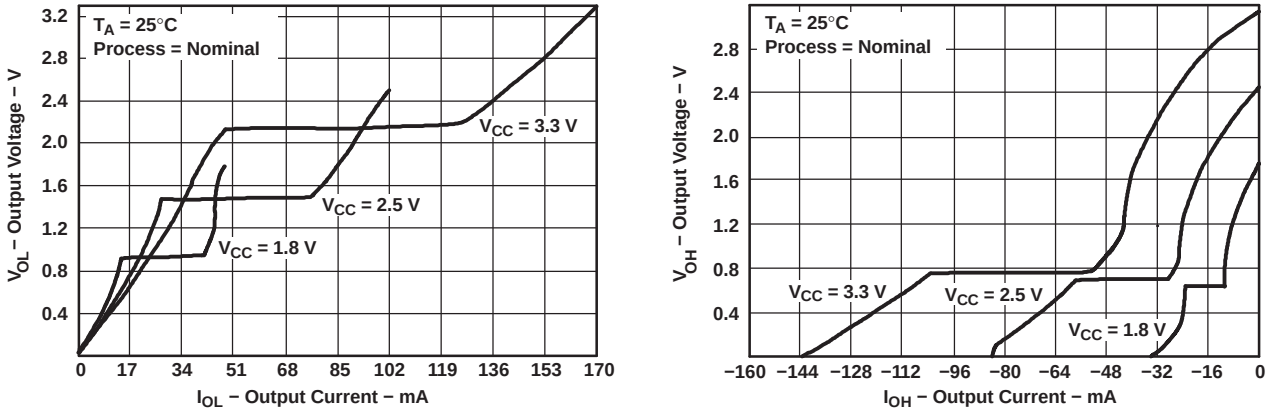
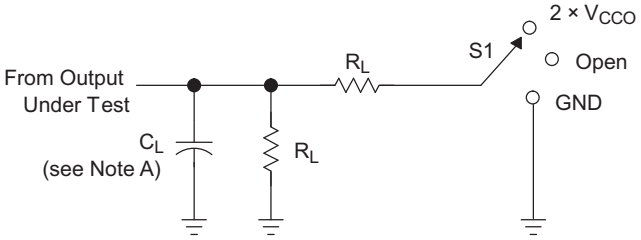


Figure 3. Typical Output Voltage vs Output Current

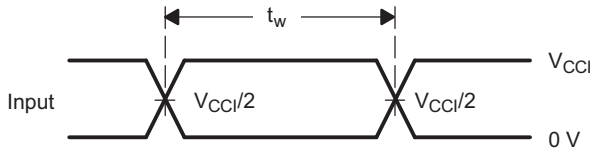
PARAMETER MEASUREMENT INFORMATION



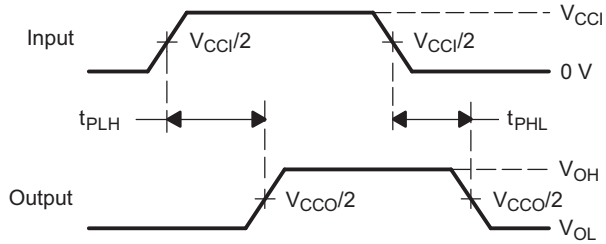
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

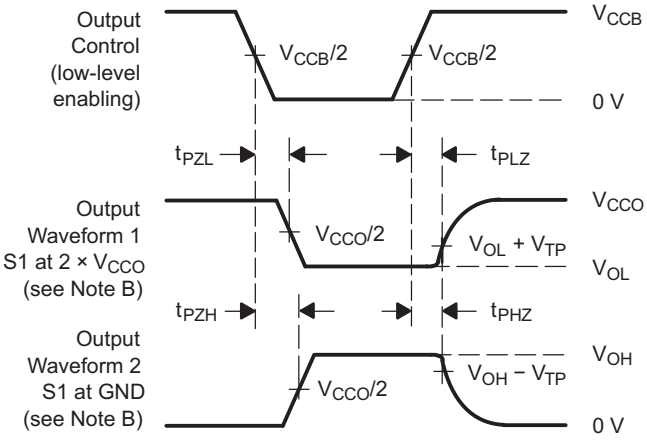
V_{CCO}	C_L	R_L	V_{TP}
1.5 V ± 0.1 V	15 pF	500 Ω	0.1 V
1.8 V ± 0.15 V	30 pF	500 Ω	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	30 pF	500 Ω	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAVCB164245MDGGEP	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AVCB164245M	Samples
CAVCB164245MDGGREP	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AVCB164245M	Samples
V62/13602-01XE	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AVCB164245M	Samples
V62/13602-01XE-T	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AVCB164245M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

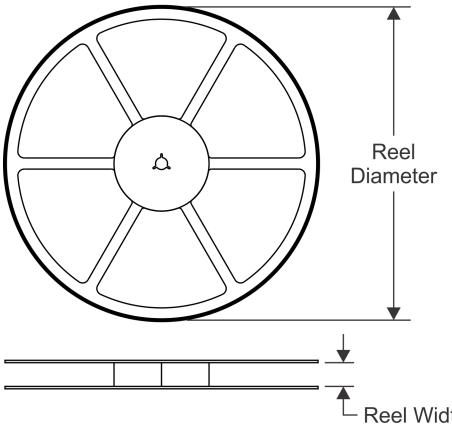
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

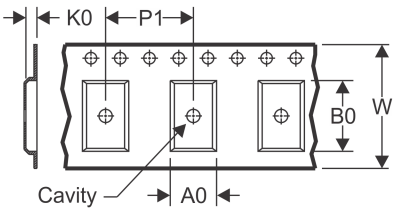
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

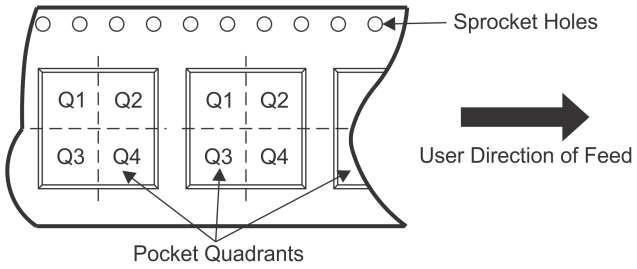


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

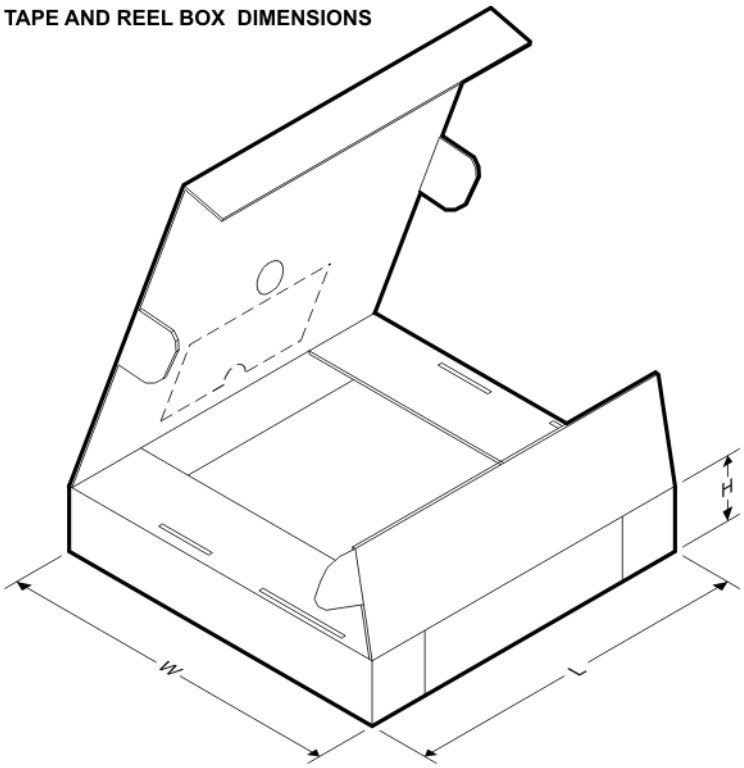
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

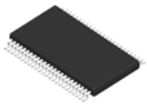
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAVCB164245MDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAVCB164245MDGGREP	TSSOP	DGG	48	2000	367.0	367.0	45.0

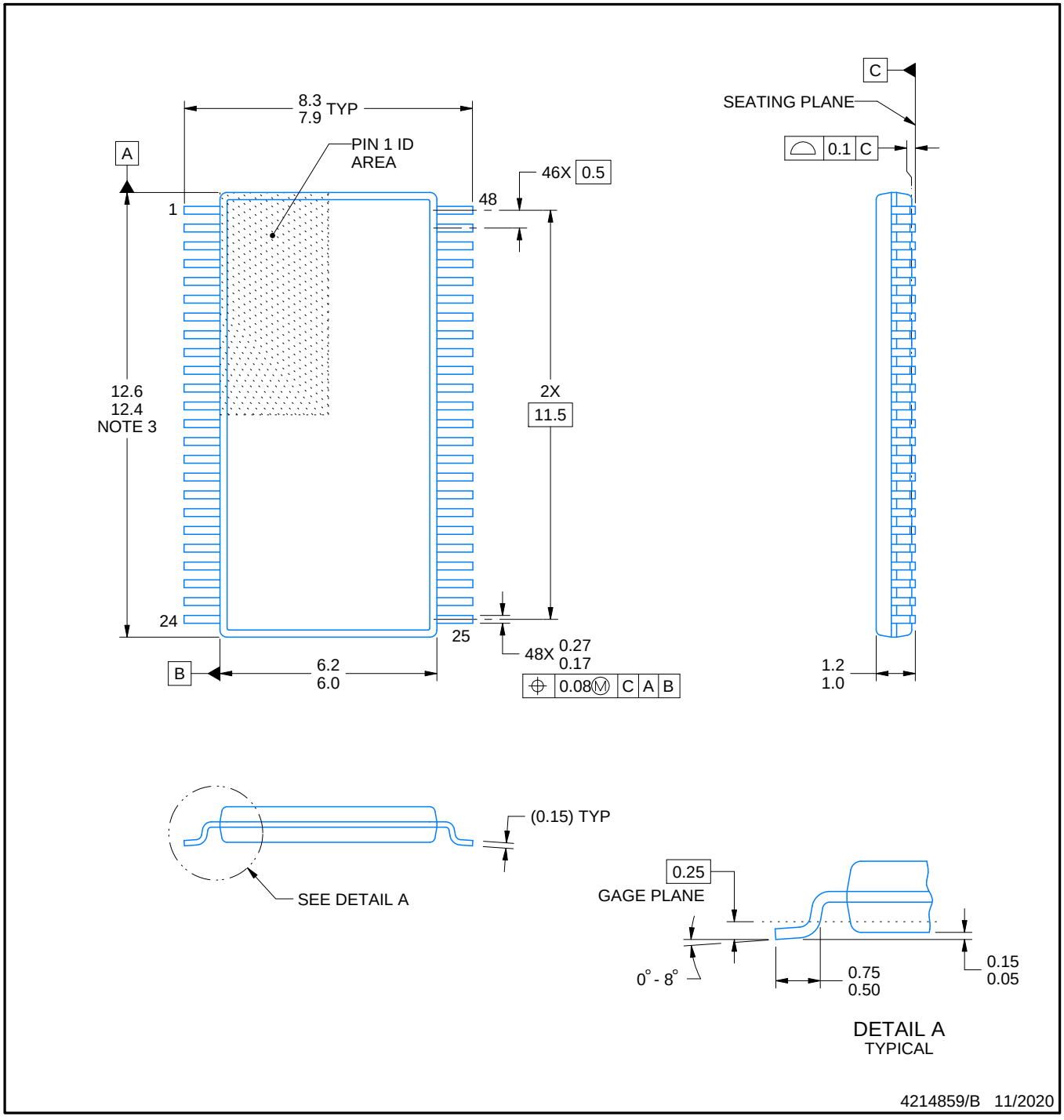


PACKAGE OUTLINE

DGG0048A

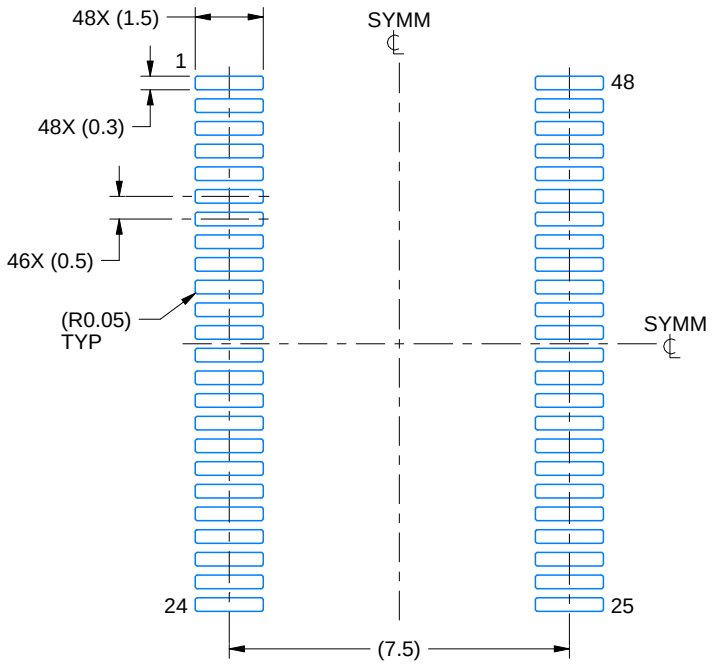
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

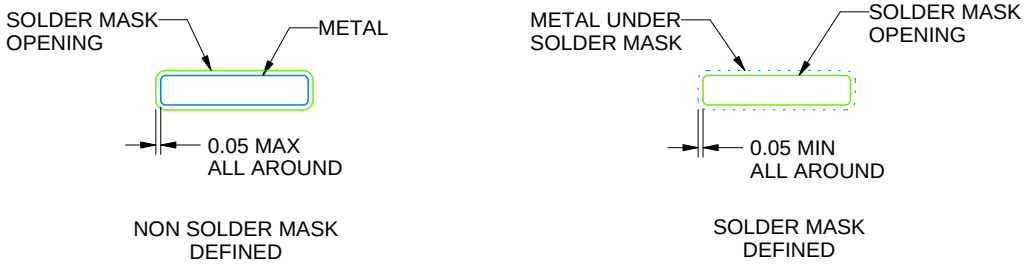


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

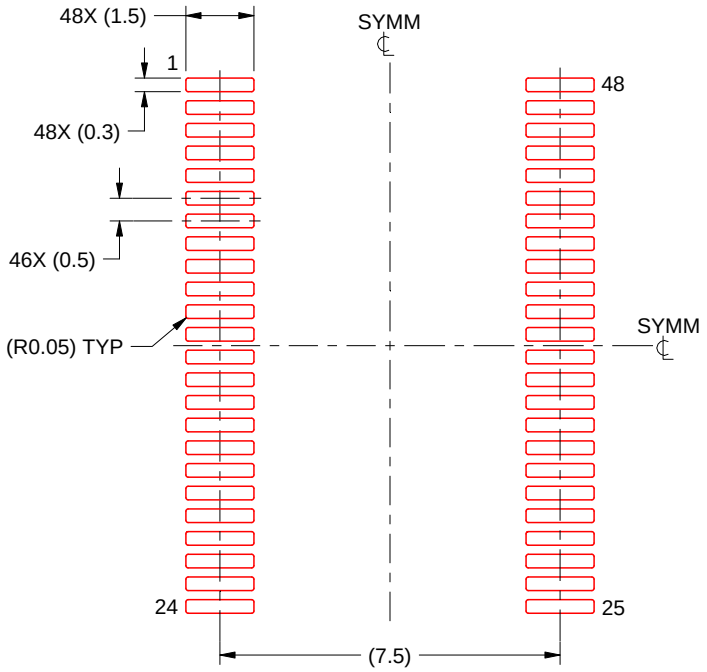


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

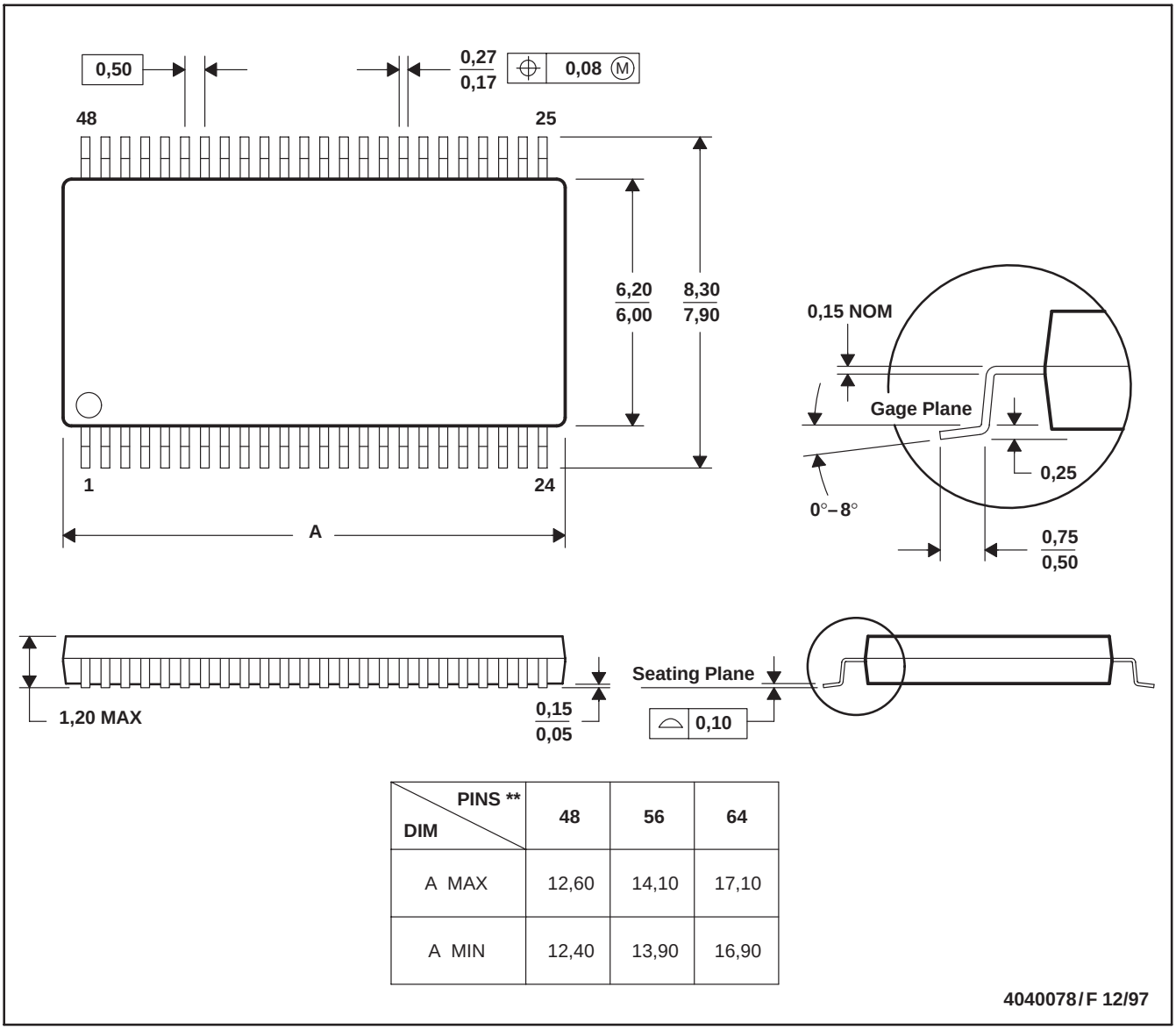
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122