LSF0204x 适用于漏极开路和推挽应用的 4 位双向多电压电平转换器

1 特性

- 用无方向端子提供双向电压转换
- 在不超过 30pF 的电容器负载条件下支持高达 100MHz 的上行转换和超过 100MHz 的下行转换，在 50pF 的电容器负载条件下支持高达 40MHz 的上行/下行转换
- 支持 I_{off}、局部断电模式（参阅 *特性 说明*）
- 可实现以下电压之间的双向电压电平转换
  - 0.8V ↔ 1.8、2.5、3.3、5V
  - 1.2V ↔ 1.8、2.5、3.3、5V
  - 1.8V ↔ 2.5、3.3、5V
  - 2.5V ↔ 3.3、5V
  - 3.3V ↔ 5V
- 低待机电流
- 支持 TTL 的 5V 耐受 I/O 端口
- 低导通电阻 R_{on} 提供较少的信号失真
- 针对 EN 为低电平的高阻抗 I/O 端子
- 直通引脚分配以简化印刷电路板 (PCB) 走线路由
- 锁断性能超过 100mA，符合 JESD17 规范
- -40°C 至 125°C 工作温度范围
- 静电放电 (ESD) 性能测试符合 JESD 22 规范
  - 2000V 人体放电模式（A114-B，II 类）
  - 200V 机器模型 (A115-A)
  - 1000V 充电器件模型 (C101)

2 应用

- G
  P
  I
  O
  ，
  MDIO，PMBus，SMBus，SDIO，UART，I^2C，和其他电信基础设施中的接口
- 工业应用
- 汽车应用
- 个人计算

3 说明

LSF 系列包含双向电压电平转换器，该转换器可在 0.8V 至 4.5V (Vref_A) 和 1.8V 至 5.5V (Vref_B) 电压范围内运行。该范围支持在 0.8 至 5.0V 之间进行双向电压转换，而无须使用漏极开路或推挽 应用中的方向终端。LSF 系列支持电平转换 应用 ，具有超过 100 MHz 的传输速度，可用于使用 15pF 电容和 165Ω 上拉电阻器的漏极开路系统。

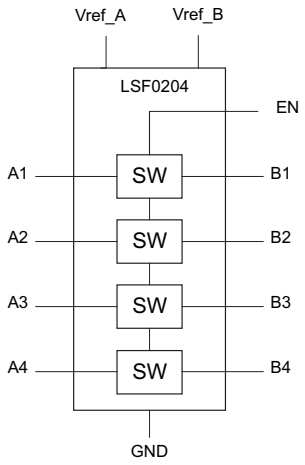
当 An 或 Bn 端口为低电平时，此开关处于接通状态，并且在 An 和 Bn 端口之间存在一个低电阻连接。开关的低 R_{on} 可用最小传播延迟和信号失真来实现连接。A 端或 B 端的电压将限制为 Vref_A，且可上拉至 Vref_A 到 5V 之间的任何电压水平。利用此功能，可在无需方向控制的情况下实现用户选择的较高和较低电压间的无缝转换。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LSF0204x	TSSOP (14)	5.00mm × 4.40mm
	UQFN (12)	2.00mm × 1.70mm
	VQFN (14)	3.50mm x 3.50mm
	DSBGA (12)	1.90mm × 1.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (December 2018) to Revision F — **Page**

- Changed location of YZP-package indicator dot to A3 position. ... 3
- Added YZP package to *Thermal Information* table ... 5

Changes from Revision D (December 2015) to Revision E — **Page**

- Changed location of YZP-package A1-pin indicator dot. View is looking through the device, as in an X-ray. ... 3

Changes from Revision C (August 2015) to Revision D — **Page**

- Added Type Column to *Pin Functions* table ... 4
- Added Junction Temperatures to *Thermal Information* table ... 5

Changes from Revision B (April 2015) to Revision C — **Page**

- 从 特性 中删除了“最高传播延迟低于 1.5ns”。 ... 1
- 在 特性 中删除了“最高传播延迟低于 1.5ns”。 ... 1

Changes from Revision A (December 2014) to Revision B — **Page**

- 已添加 器件的 YZP 封装。 ... 1

Changes from Original (November 2014) to Revision A **Page**

- 从首页产品预览更改为完整数据表 1
- 已将*说明*中的文本从“传输速度大于 100Mbps”改为“传输速度大于 100MHz” 1

5 说明 （续）

每个通道的电源电压 ($V_{pu\#}$) 可以用上拉电阻器单独进行设置。例如，CH1 可用于上行转换模式 (1.2V ↔ 3.3V)，CH2 可用于下行转换模式 (2.5V ↔ 1.8V)。

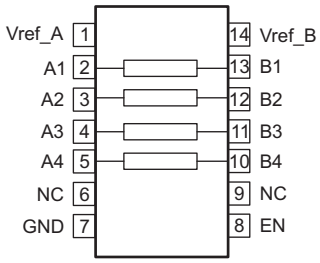
当 EN 为高电平时，转换器开关打开，并且 An I/O 被分别连接至 Bn I/O，从而实现端口间的双向数据流。当 EN 为低电平时，转换器开关关闭，在端口之间存在一个高阻抗状态。EN 输入电路被设计成由 Vref_A 供电。EN 必须为低电平，以确保上电或断电期间的高阻抗状态。

器件比较表

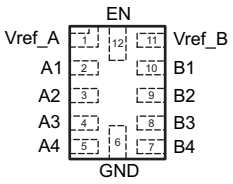
器件编号	EN	An	Bn	说明
LSF0204D	H	将所有数据引脚置于三态模式 (Hi-Z)	将所有数据引脚置于三态模式 (Hi-Z)	三态输出模式启用（低电平有效；以 Vref_A 为基准）
LSF0204D	L	输入或输出	输入或输出	
LSF0204	H	输入或输出	输入或输出	三态输出模式启用（高电平有效，以 Vref_A 为基准）
LSF0204	L	将所有数据引脚置于三态模式 (Hi-Z)	将所有数据引脚置于三态模式 (Hi-Z)	

6 Pin Configuration and Functions

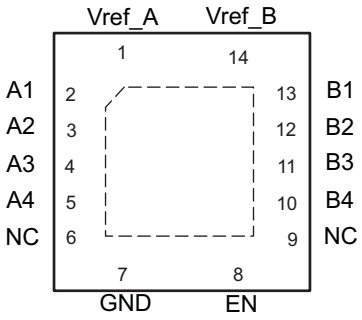
PW Package
14-Pin TSSOP
Top View



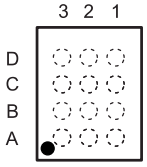
RUT Package
12-Pin UQFN
Transparent Top View



RGY Package
14-Pin VQFN
Transparent Top View



YZP Package
12-Pin DSBGA
Transparent Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	NO.				
	PW, RGY	RUT	YZP		
V_{ref_A}	1	1	B2	--	Reference supply voltage; see Application and Implementation section
A1	2	2	A3	I/O	Input/output 1.
A2	3	3	B3	I/O	Input/output 2.
A3	4	4	C3	I/O	Input/output 3.
A4	5	5	D3	I/O	Input/output 4.
NC	6	–	–	--	No connection. Not internally connected.
GND	7	6	D2	--	Ground
EN	8	12	C2	I	Switch enable input; LSF0204: EN is high-active; LSF0204D: EN is low-active
NC	9	–	–	--	No connection. Not internally connected.
B4	10	7	D1	I/O	Input/output 4.
B3	11	8	C1	I/O	Input/output 3.
B2	12	9	B1	I/O	Input/output 2.
B1	13	10	A1	I/O	Input/output 1.
V_{ref_B}	14	11	A2	--	Reference supply voltage; see Application and Implementation section

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_I	Input voltage (2)		–0.5	7	V
$V_{I/O}$	Input/output voltage (2)		–0.5	7	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	VI < 0		–50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5	V
$V_{ref\_A/B/EN}$	Reference voltage	0	5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC (1)		LSF0204				UNIT
		RGY (VQFN)	RUT (UQFN)	PW (TSSOP)	YZP (DSBGA)	
		14 PINS	12 PINS	14 PINS	12 BALLS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.2	195.8	157.9	83.7	°C
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.2	98.7	82.3	0.6	°C
$R_{\theta JB}$	Junction-to-board thermal resistance	59.2	122.6	100.0	23.7	°C
ψ_{JT}	Junction-to-top characterization parameter	17.4	6.2	22.9	0.4	°C
ψ_{JB}	Junction-to-board characterization parameter	59.4	122.6	99.0	23.7	°C
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	38.7	N/A	N/A	N/A	°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}		I_I = -18 mA, V_{EN} = 0				–1.2	V
I_{IH}		V_I = 5 V, V_{EN} = 0				5.0	µA
I_{CCBA}	Leakage from Vref_B to Vref_A	V_{ref_B} = 3.3 V, V_{ref_A} = 1.8 V, V_{EN} = V_{ref_A} I_O = 0, V_I = 3.3 V or GND				3.5	µA
I_{CCA} + I_{CCB} (2)	Total Current through GND	V_{ref_B} = 3.3 V, V_{ref_A} = 1.8 V, V_{EN} = V_{ref_A} I_O = 0, V_I = 3.3 V or GND			0.2		µA
I_{IN}	Control pin current	V_{ref_B} = 5.5 V, V_{ref_A} = 4.5 V, V_{EN} = 0 to V_{ref_A} I_O = 0				±1	µA
I_{off}	Power Off Leakage Current	V_{ref_B} = V_{ref_A} = 0 V, V_{EN} = GND I_O = 0, V_I = 5 V or GND				±1	µA
$C_{I(ref\_A/B/EN)}$		V_I = 3 V or 0			7		pF
$C_{io(off)}$		V_O = 3 V or 0, VEN = 0			5.0	6.0	pF
$C_{io(on)}$		V_O = 3 V or 0, VEN = Vref_A			10.5	13	pF
(3)V_{IH} (EN pin)	High-level input voltage	V_{ref_A} = 1.5 V to 4.5 V		0.7×Vref_A			V
V_{IL} (EN pin)	Low-level input voltage	V_{ref_A} = 1.5 V to 4.5 V				0.3×Vref_A	V
V_{IH} (EN pin)	High-level input voltage	V_{ref_A}= 1.0 V to 1.5 V		0.8×Vref_A			V
V_{IL} (EN pin)	Low-level input voltage	V_{ref_A} = 1.0 V to 1.5 V				0.3×Vref_A	V
Δt/Δv (EN pin)	Input transition rise or fall rate for EN pin				10		ns/V
r_{on} (4)		V_I = 0, I_O = 64 mA	V_{ref_A} = V_{EN} = 3.3 V; V_{ref_B} = 5 V		3		Ω
			V_{ref_A} = V_{EN} = 1.8 V; V_{ref_B} = 5 V		4		
		V_I = 0, I_O = 32 mA	V_{ref_A} = V_{EN} = 1.0 V; V_{ref_B} = 5 V		9		Ω
			V_{ref_A} = V_{EN} = 1.8 V; V_{ref_B} = 5 V		4		
		V_I = 0, I_O = 32 mA , V_{ref_A} = V_{EN} = 2.5 V; V_{ref_B} = 5 V			10		Ω
		V_I = 1.8 V, I_O = 15 mA, V_{ref_A} = V_{EN} = 3.3 V; V_{ref_B} = 5 V			5		Ω
		V_I = 1.0 V, I_O = 10 mA, V_{ref_A} = V_{EN} = 1.8 V; V_{ref_B} = 3.3 V			8		Ω
		V_I = 0 V, I_O = 10 mA, V_{ref_A} = V_{EN} = 1.0 V; V_{ref_B} = 3.3 V			6		Ω
		V_I = 0 V, I_O = 10 mA, V_{ref_A} = V_{EN} = 1.0 V; V_{ref_B} = 1.8 V			6		Ω

(1) All typical values are at T_A = 25°C.
(2) The actual supply current for LSF0204 is I_{CCA} + I_{CCB}; the leakage from Vref_B to Vref_A can be measured on Vref_A and Vref_B pin
(3) Enable pin test conditions are for the LSF0204. The enable pin test conditions for LSF0204D are oppositely set.
(4) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

7.6 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.8 V)

over recommended operating free-air temperature range, $V_{rev\text{-}A}$ = 1.8 V, $V_{rev\text{-}B}$ = 3.3 V, V_{EN} = 1.8 V, Vpu_1 = 3.3 V, Vpu_2 = 1.8 V, R_L = NA, V_{IH} = 3.3 V, V_{IL} = 0 V_M = 1.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	0.7	5.49	0.5	5.29	0.3	5.19	ns
t_{PHL}			0.9	4.9	0.7	4.7	0.5	4.5	ns
t_{PLZ}			13	18	12	16.5	11	15	ns
t_{PZL}			33	45	30	40	23	37	ns
f_{MAX}			50		100		100		MHz

7.7 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.2 V)

over recommended operating free-air temperature range V_{rev-A} = 1.2 V, V_{rev-B} = 3.3 V, V_{EN} = 1.2 V, Vpu_1 = 3.3 V, Vpu_2 = 1.2 V, R_L = NA, V_{IH} = 3.3V, V_{IL} = 0 V_M = 0.85 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	0.8	4.1	0.5	3.9	0.3	3.8	ns
t_{PHL}			0.9	4.7	0.7	4.5	0.6	4.3	ns
f_{MAX}			50		100		100		MHz

7.8 Switching Characteristics: AC Performance (Translating Up, 1.8 V to 3.3 V)

over recommended operating free-air temperature range V_{rev-A} = 1.8 V, V_{rev-B} = 3.3 V, V_{EN} = 1.8 V, Vpu_1 = 3.3 V, Vpu_2 = 1.8V, R_L = 500 Ω, V_{IH} = 1.8V, $_{VIL}$ = 0 V_M = 0.9V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	0.6	5.7	0.4	5.3	0.2	5.13	ns
t_{PHL}			1.3	6.7	1	6.4	0.7	5.3	ns
t_{PLZ}			13	18	12	16.5	11	15	ns
t_{PZL}			33	45	30	40	23	37	ns
f_{MAX}			50		100		100		MHz

7.9 Switching Characteristics: AC Performance (Translating Up, 1.2 V to 1.8 V)

over recommended operating free-air temperature range, V_{rev-A} = 1.2 V, V_{rev-B} = 1.8 V, V_{EN} = 1.2 V, Vpu_1 = 1.8 V, Vpu_2 = 1.2 V, R_L = 500 Ω, V_{IH} = 1.2V, V_{IL} = 0 V_M = 0.6 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	0.65	7.25	0.4	7.05	0.2	6.85	ns
t_{PHL}			1.6	7.03	1.3	6.5	1	5.4	ns
f_{MAX}			50		100		100		MHz

7.10 Typical Characteristics

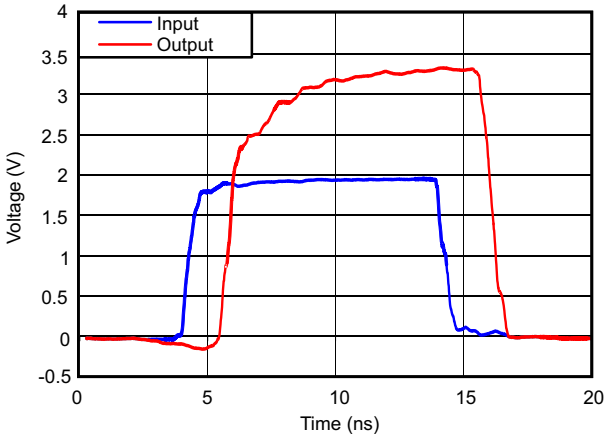
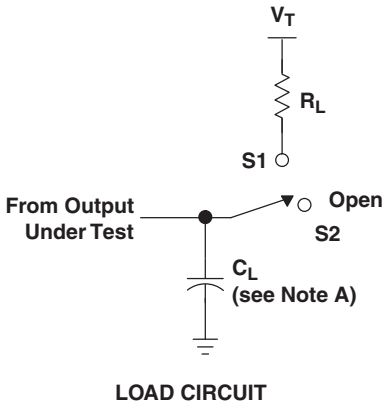


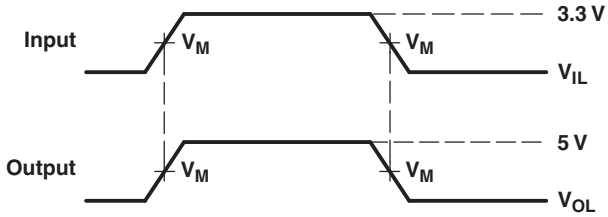
Figure 1. Signal Integrity (1.8 V to 3.3 V Translation Up at 50 MHz)

8 Parameter Measurement Information

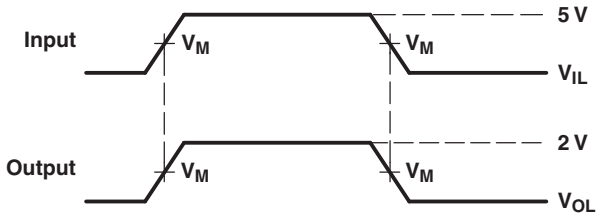


LOAD CIRCUIT

USAGE	SWITCH
Translating up	S1
Translating down	S2



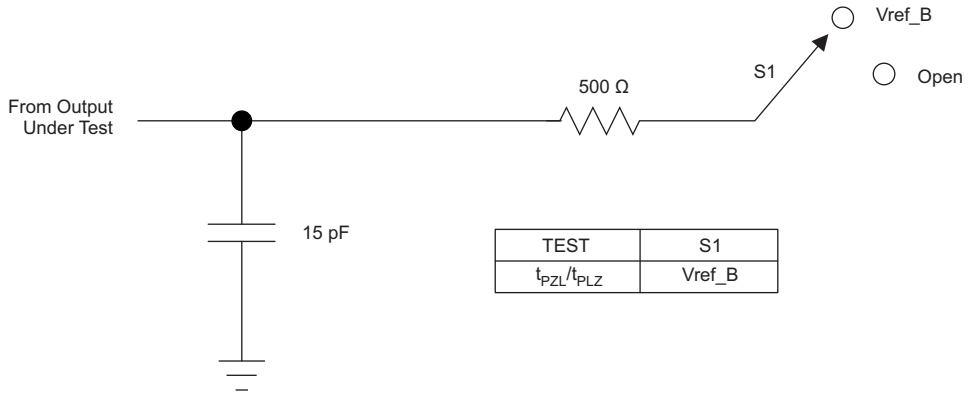
TRANSLATING UP



TRANSLATING DOWN

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit for Outputs



TEST	S1
t_{PZL}/t_{PLZ}	Vref_B

Figure 3. Load Circuit for Enable/Disable Time Measurement

8.1 Load Circuit AC Waveform for Outputs

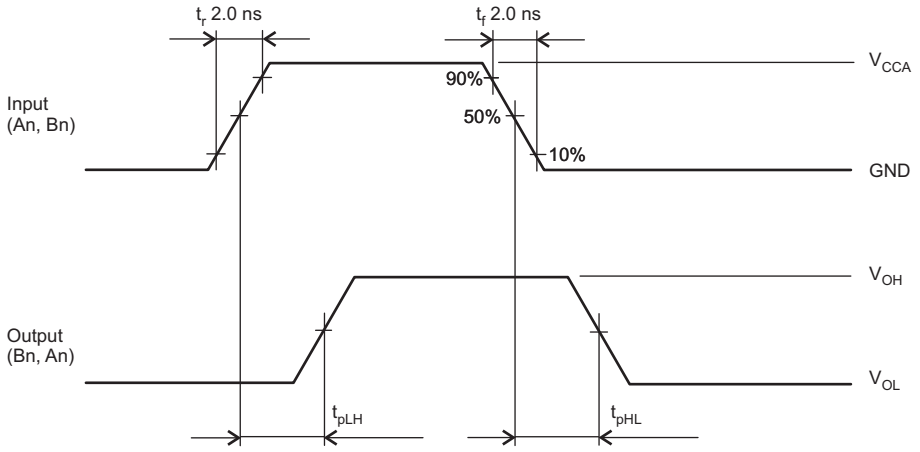


Figure 4. t_{PLH}, t_{PHL}

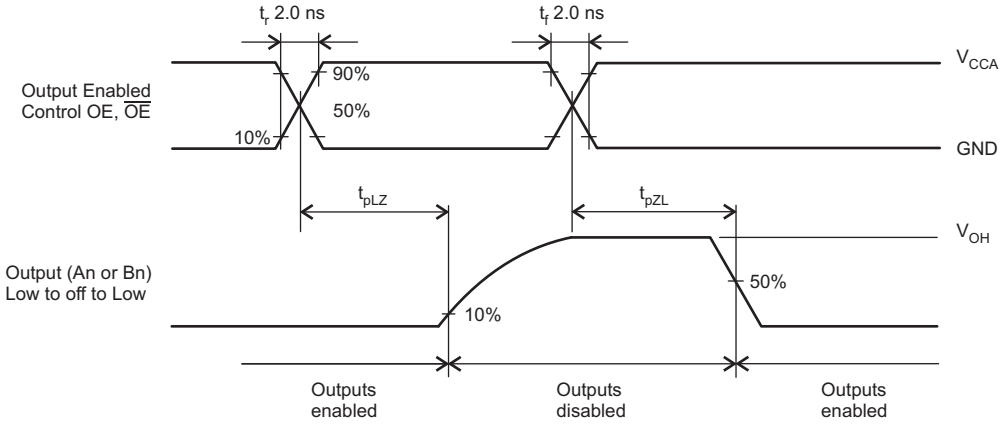


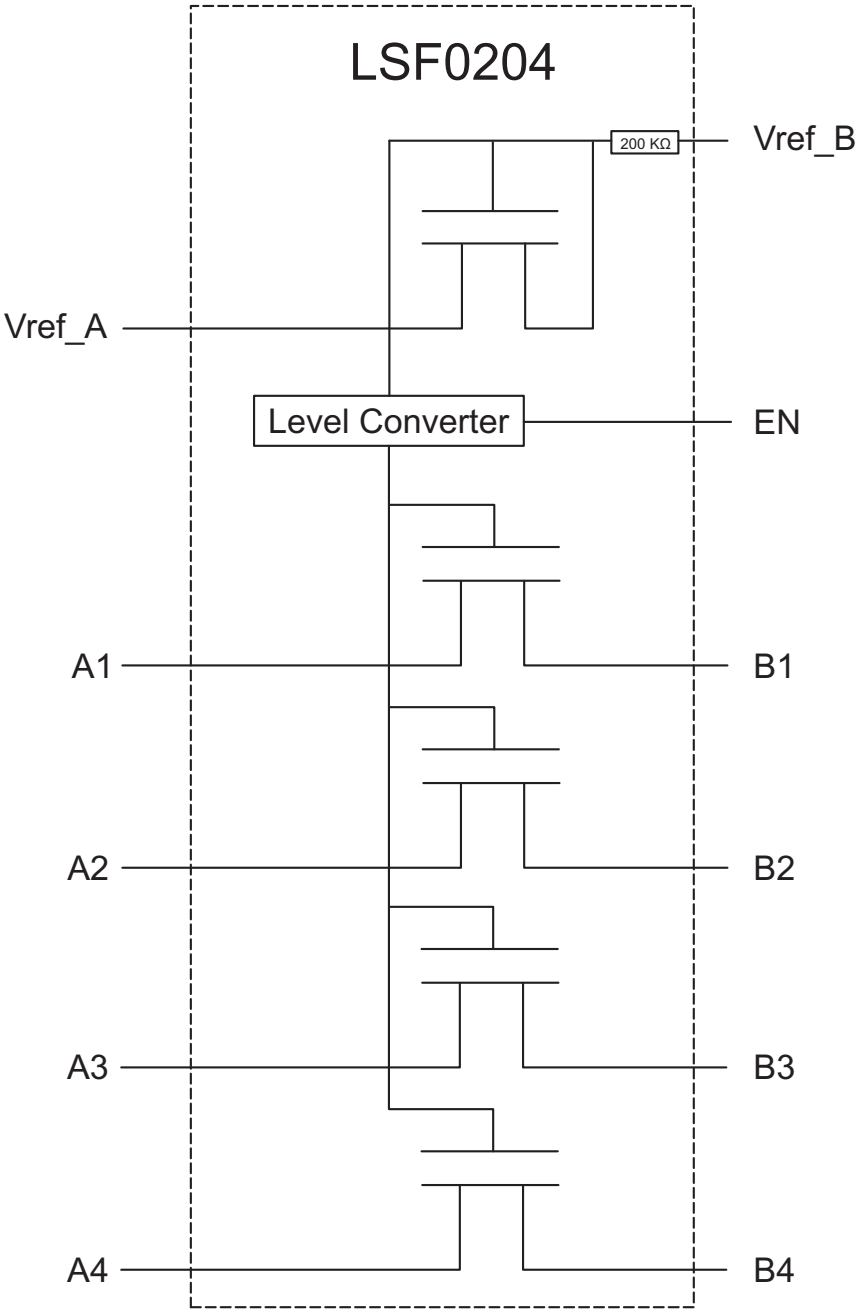
Figure 5. t_{PLZ}, t_{PZL}

9 Detailed Description

9.1 Overview

The LSF Family may be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The LSF Family is ideal for use in applications where an open-drain driver is connected to the data I/Os. LSF can achieve 100 MHz with the appropriate pull-up resistors and layout. The LSF Family may also be used in applications where a push-pull driver is connected to the data I/Os.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Support High Speed Translation, Greater than 100 MHz

Allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO).

9.3.2 Bidirectional Voltage Translation Without DIR Terminal

Minimizes system effort to develop voltage translation for bidirectional interface (PMBus, I2C, or SMbus).

9.3.3 5-V Tolerance on IO Port and 125°C Support

The LSF family, with 5-V tolerance and 125°C support, is flexible and compliant with TTL levels in industrial and telecom applications.

9.3.4 Channel Specific Translation

The LSF family is able to set up different voltage translation levels on each channel.

9.3.5 Ioff, Partial Power Down Mode

When V_{ref_A}, V_{ref_B} = 0, all of data pins and EN pin are Hi-Z.

EN logic circuit is supplied by V_{ref_A}, once V_{ref_A} power up first and all of data pins are unknown state until V_{ref_B} and EN ready. No power sequence is required to enable LSF0204 and operate function normally.

9.4 Device Functional Modes

Table 1 lists the device functional modes of the LSF0204x family of devices.

Table 1. Function Table

INPUT EN(1) TERMINAL	FUNCTION
H	An = Bn
L	Hi-Z

(1) EN is controlled by V_{ref_A} logic levels.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

LSF performs voltage translation for open-drain or push-pull interface. Table 2 provides some consumer/telecom interfaces as reference in regards to the different channel numbers that are supported by the LSF family.

Table 2. Voltage Translator for Consumer/Telecom Interface

PART NAME	CH#	INTERFACE
LSF0101	1	GPIO
LSF0102	2	GPIO, MDIO, SMBus, PMBus, I2C
LSF0204	4	GPIO, SPI. MDIO, SMBus, PMBus, I2C, UART, SVID
LSF0108	8	GPIO, MDIO, SDIO, SVID, UART, SMBus, PMBus, I2C, SPI

10.2 Typical Applications

10.2.1 I^2C PMBus, SMBus, GPIO, Application

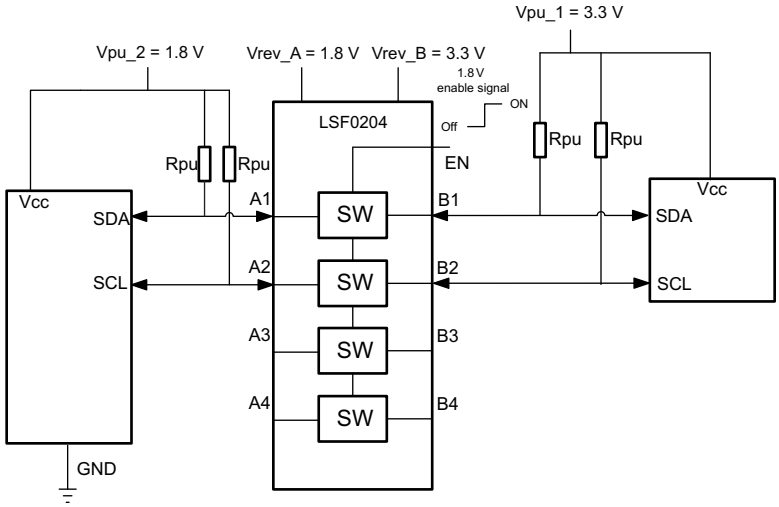


Figure 6. Bidirectional Translation to Multiple Voltage Levels

10.2.1.1 Design Requirements

10.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

The LSF family has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. Since LSF family is switch-type voltage translator, the power consumption is very low. It is recommended to always enable LSF family for bidirectional application (I2C, SMBus, PMBus, or MDIO).

Typical Applications (continued)

Table 3. Application Operating Condition

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Vref_A	Reference voltage (A)	0.8		4.5	V
Vref_B	Reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$ (1)	Input voltage on EN terminal	0		Vref_A	V
Vpu	Pull-up supply voltage	0		Vref_B	V

(1) Refer V_{IH} and V_{IL} for $V_{I(EN)}$

Also Vref_B is recommended to be at 1.0 V higher than Vref_A for best signal integrity.

The LSF Family is able to set different voltage translation level on each channel.

NOTE

Vref_A must be set as lowest voltage level.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Bidirectional Translation

The master output driver may be push-pull or open-drain (pull-up resistors may be required) and the slave device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

NOTE

However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

In Figure 6, the reference supply voltage (Vref_A) is connected to the processor core power supply voltage. When Vref_B is connected through to a 3.3 V Vpu power supply, and Vref_A is set 1.0V. The output of A3 and B4 has a maximum output voltage equal to Vref_A, and the bidirectional interface (Ch1/2, MDIO) has a maximum output voltage equal to Vpu.

10.2.1.2.1.1 Pull-up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, to calculate the pull-up resistor value use Equation 1.

$$Rpu = (Vpu – 0.35\ V) / 0.015\ A \quad (1)$$

Table 4 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF family device at 0.175 V, although the 15 mA applies only to current flowing through the LSF family device.

Table 4. Pullup Resistor Values(1)(2)

PULLUP RESISTOR VALUE (Ω)						
V_{DPU}	15 mA		10 mA		3 mA	
	NOMINAL	+10%(3)	NOMINAL	+10%(3)	NOMINAL	+10%(3)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

10.2.1.2.2 LS Family Bandwidth

The maximum frequency of the LSF family is dependent on the application. The device may operate at speeds of >100MHz gave the correct conditions. The maximum frequency is dependent upon the loading of the application. The LSF family behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

Figure 7 shows a bandwidth measurement of the LSF family using a two-port network analyzer.

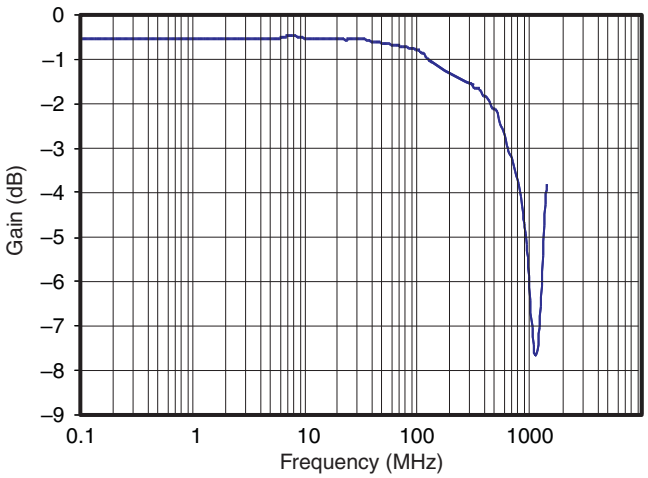


Figure 7. 3-dB Bandwidth

The 3-dB point of the LSF family is ≈600MHz; however, this measurement is an analog type of measurement. For digital applications, the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is important in determining the overall shape of the digital signal. In the case of the LSF family, a digital clock frequency of greater than 100 MHz may be achieved.

The LSF family does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the LSF family is being driven by standard CMOS totem pole output driver. Best practice is to minimize the trace length from the LSF family on the sink side (1.8 V) to minimize signal degradation.

All fast edges have an infinite spectrum of frequency components; however, there is an inflection (or *knee*) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate the maximum *practical* frequency component, or the *knee* frequency (f_{knee}), use the following equations:

$$f_{knee} = 0.5/RT \text{ (10–80%)} \quad (2)$$

$$f_{knee} = 0.4/RT \text{ (20–80%)} \quad (3)$$

For signals with rise time characteristics based on 10- to 90-percent thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20% to 80% thresholds, which is very common in many of today's device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the LSF family close to the I^2C output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

10.2.1.3 Application Curve

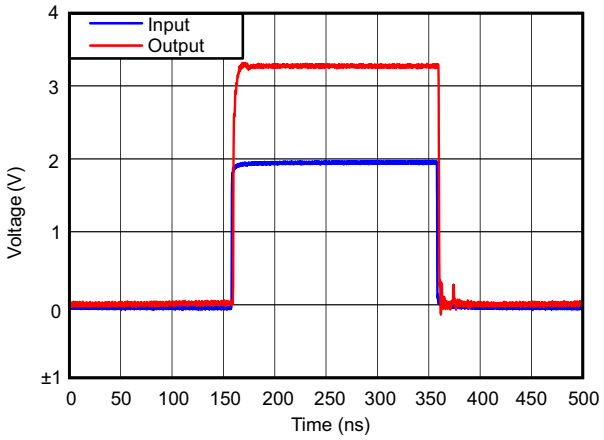


Figure 8. Captured Waveform From Above I^2C Set-Up (1.8 V to 3.3 V at 2.5 MHz)

10.2.2 MDIO Application

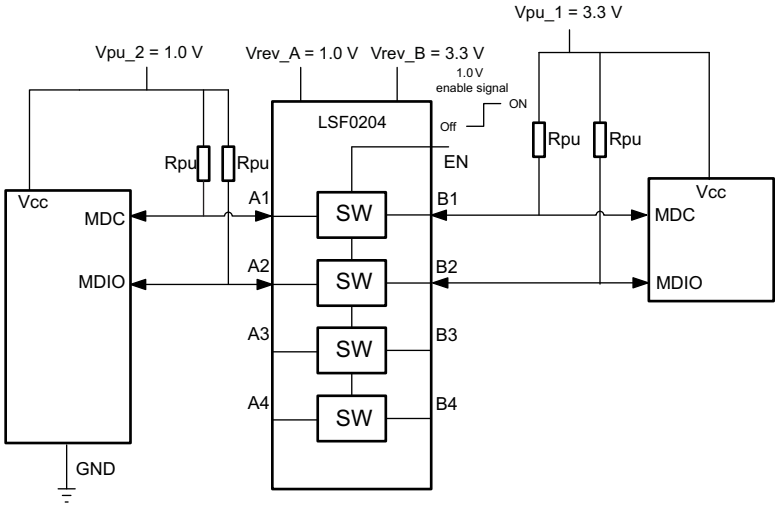


Figure 9. Typical Application Circuit (MDIO/Bidirectional Interface)

10.2.2.1 Design Requirements

Refer to *Design Requirements*.

10.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*

10.2.2.3 Application Curve

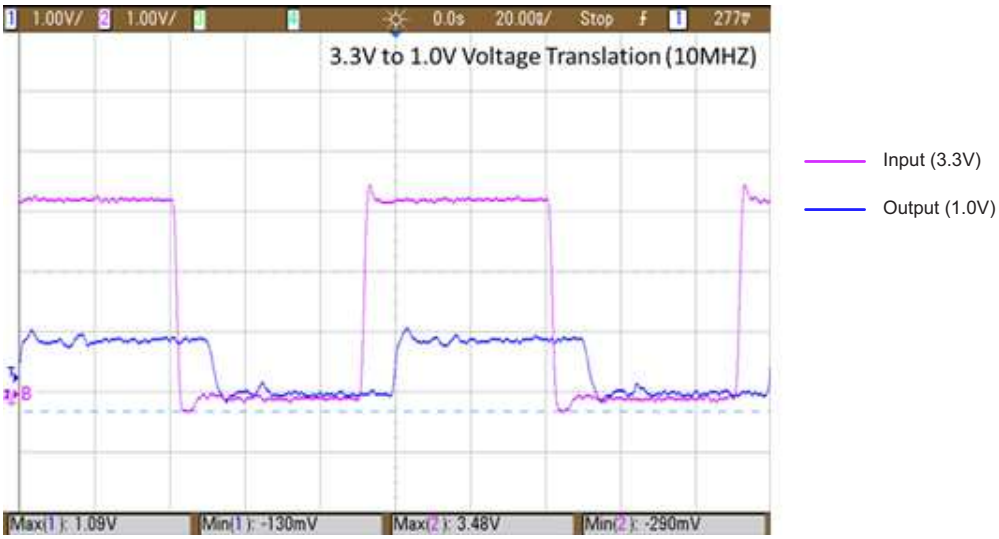
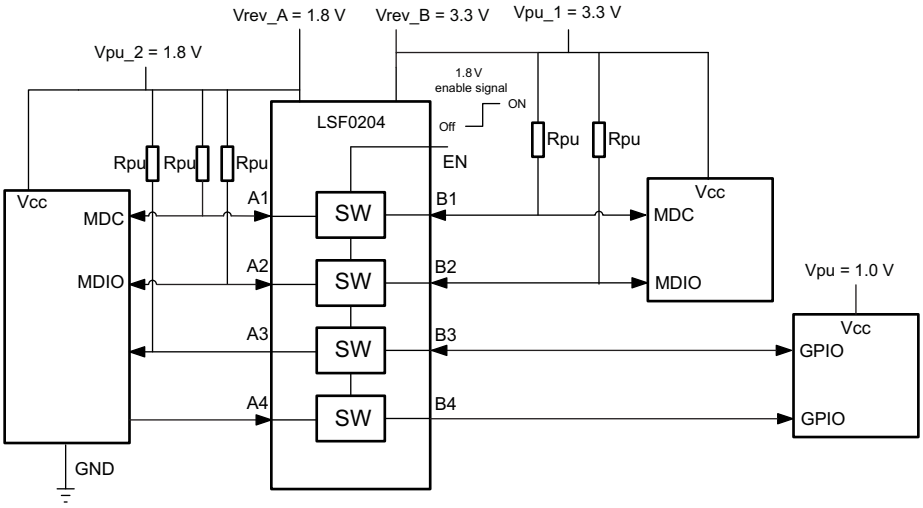


Figure 10. Captured Waveform From Above MDIO Setup

10.2.3 Multiple Voltage Translation in Single Device, Application



10.2.3.1 Design Requirements

Refer to *Design Requirements*.

10.2.3.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*

10.2.3.3 Application Curve

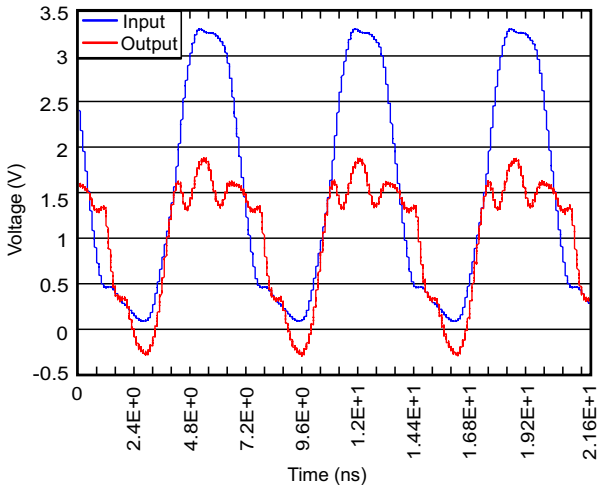


Figure 11. Translation Down (3.3 V to 1.8 V) at 150 MHz

11 Power Supply Recommendations

There are no power sequence requirements for the LSF Family. Refer to the *Enable, Disable, and Reference Voltage Guidelines* for enabling and reference voltage guidelines.

12 Layout

12.1 Layout Guidelines

The signal integrity is highly related with pull-up resistor and PCB capacitance condition because LSF Family is switch-type level translator

- Short signal trace as possible to reduce capacitance and minimize stub from pull-up resistor.
- Place LSF close to high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of transmitter.

12.2 Layout Example

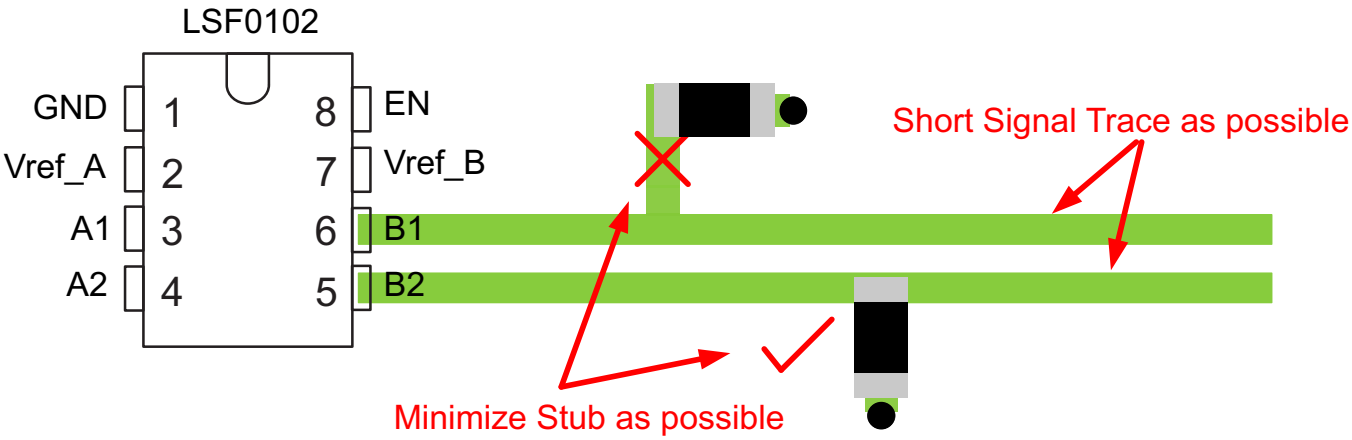


Figure 12. Short Trace Layout

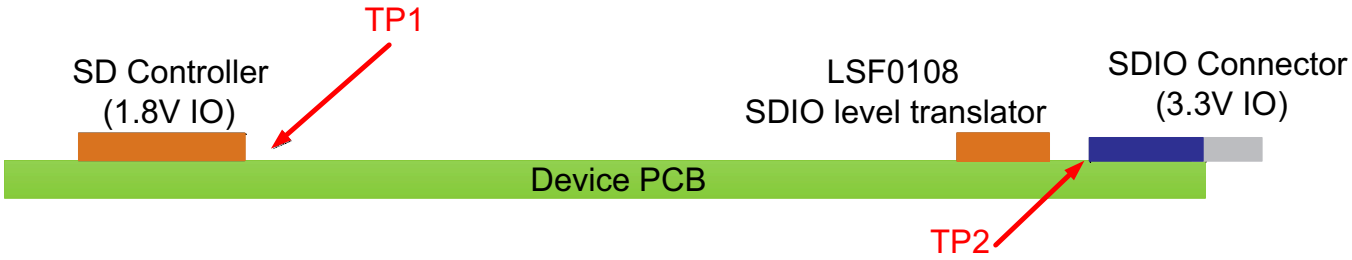


Figure 13. Device Placement

Layout Example (接下页)

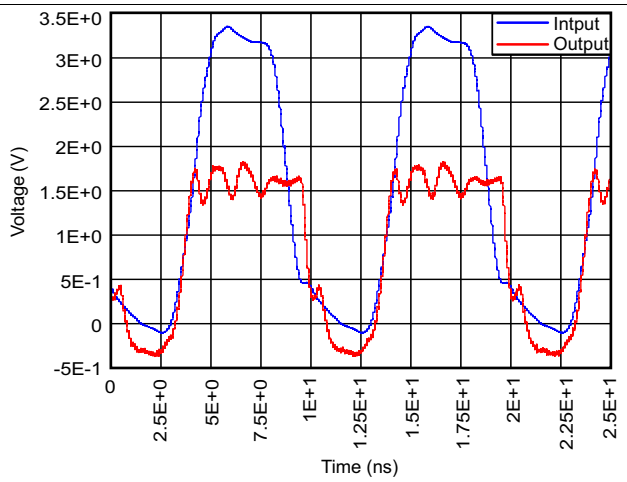


Figure 14. Waveform From TP1 (Pullup Resistor: 160-Ω and 50-pF Capacitance 3.3 to 1.8 V at 100 MHz)

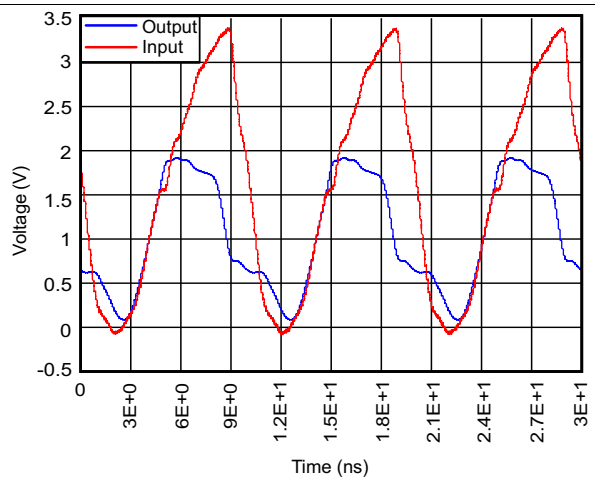


Figure 15. Waveform From TP2 (Pullup Resistor: 160-Ω and 50-pF Capacitance 1.8 to 3.3 V at 100 MHz)

13 器件和文档支持

13.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 5. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
LSF0204	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LSF0204D	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

13.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

14.1 Package Option Addendum

14.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking(5)(6)
LSF0204DPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	–40 to 125	LSF204D
LSF0204DRGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-UNLIM	–40 to 125	LSF24D
LSF0204DRUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	–40 to 125	SIO
LSF0204DYZPR	ACTIVE	DSBGA	YZP	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	–40 to 125	G6
LSF0204PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	–40 to 125	LSF204
LSF0204RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-UNLIM	–40 to 125	LSF24
LSF0204RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	–40 to 125	SIN
LSF0204YZPR	ACTIVE	DSBGA	YZP	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	–40 to 125	G5

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LSF0204:

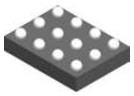
– Automotive: LSF0204-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

LSF0204/LSF0204D

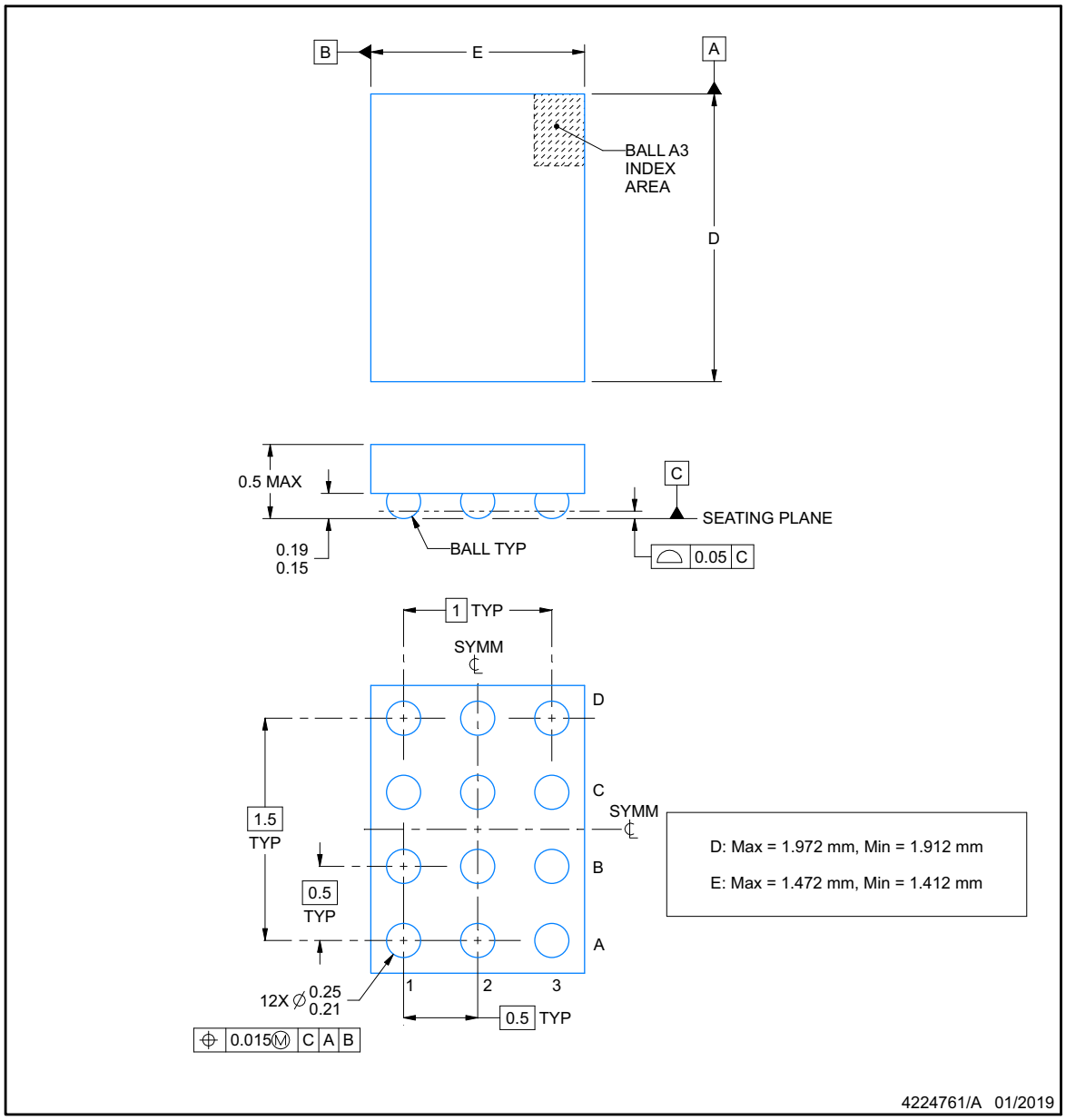
YZP0012-C01



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

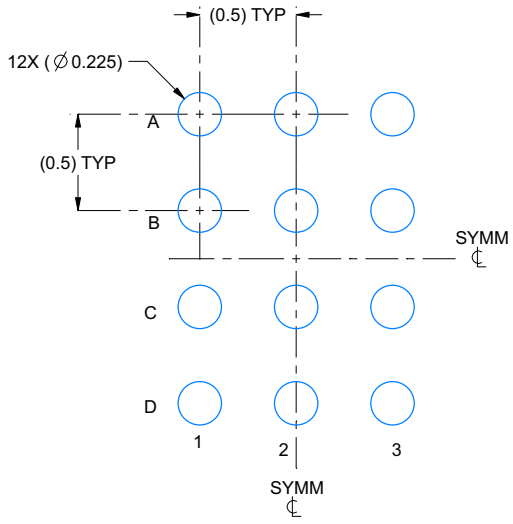
LSF0204/LSF0204D

YZP0012-C01

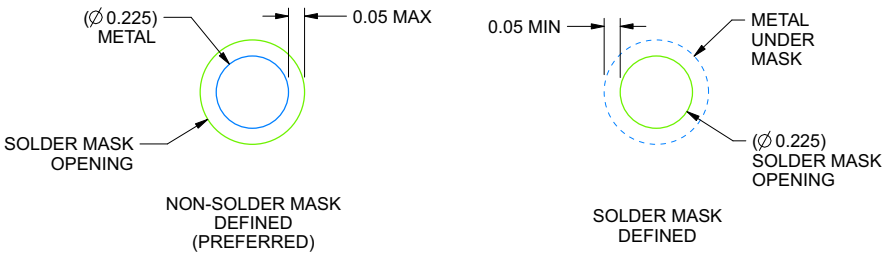
EXAMPLE BOARD LAYOUT

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4224761/A 01/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

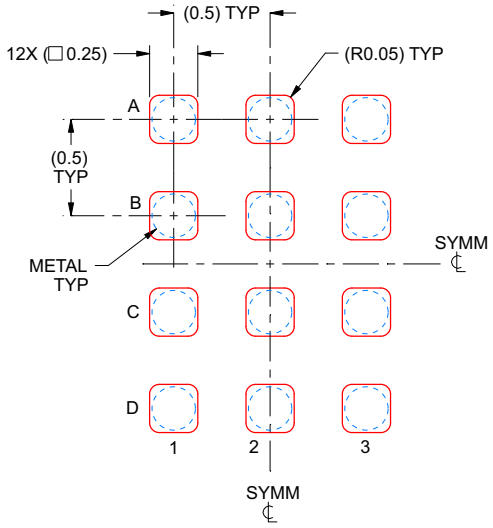
LSF0204/LSF0204D

YZP0012-C01

EXAMPLE STENCIL DESIGN

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224761/A 01/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0204DPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LSF204D	Samples
LSF0204DRGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LSF24D	Samples
LSF0204DRUTR	ACTIVE	UQFN	RUT	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIO	Samples
LSF0204DYZPR	ACTIVE	DSBGA	YZP	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G6	Samples
LSF0204PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LSF204	Samples
LSF0204RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LSF24	Samples
LSF0204RUTR	ACTIVE	UQFN	RUT	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIN	Samples
LSF0204YZPR	ACTIVE	DSBGA	YZP	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

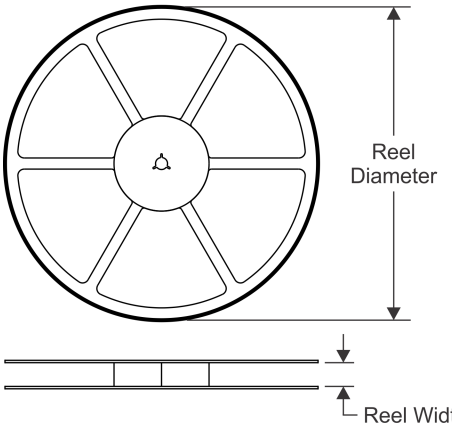
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

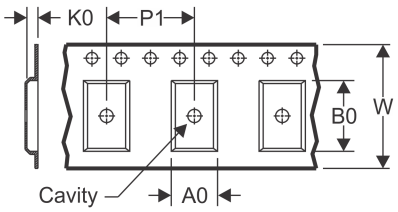
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

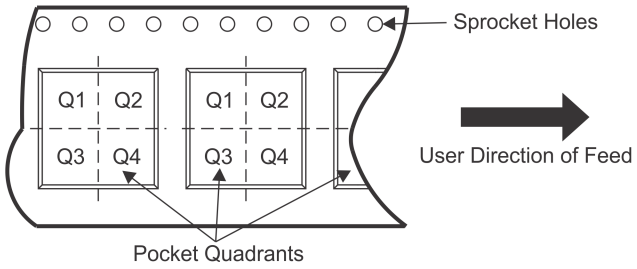


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

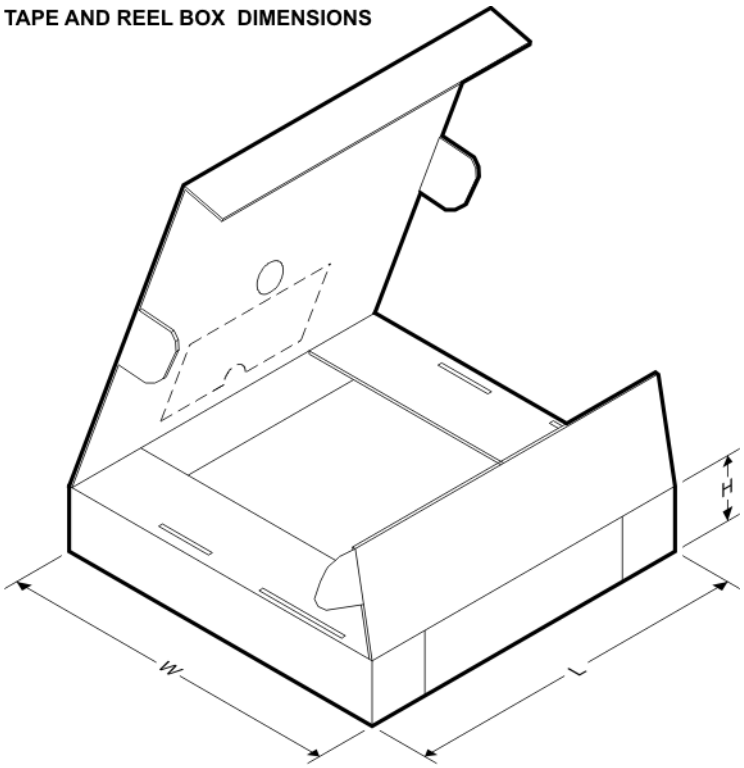
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LSF0204DPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LSF0204DRGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
LSF0204DRUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
LSF0204DYZPR	DSBGA	YZP	12	3000	180.0	8.4	1.63	2.08	0.69	4.0	8.0	Q2
LSF0204PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LSF0204RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
LSF0204RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
LSF0204YZPR	DSBGA	YZP	12	3000	180.0	8.4	1.63	2.08	0.69	4.0	8.0	Q2

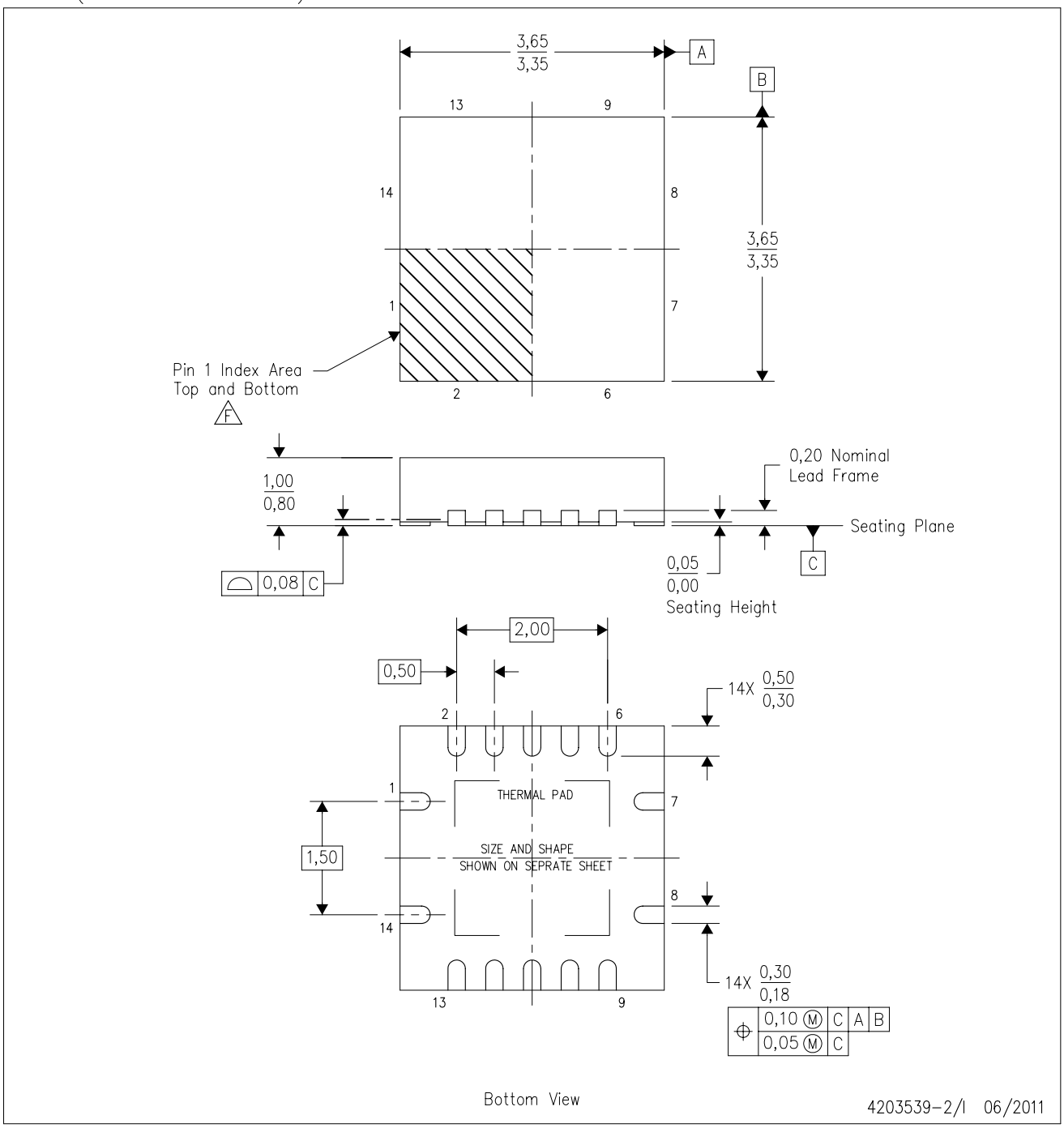
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LSF0204DPWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LSF0204DRGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
LSF0204DRUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
LSF0204DYZPR	DSBGA	YZP	12	3000	182.0	182.0	20.0
LSF0204PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LSF0204RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
LSF0204RUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
LSF0204YZPR	DSBGA	YZP	12	3000	182.0	182.0	20.0

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

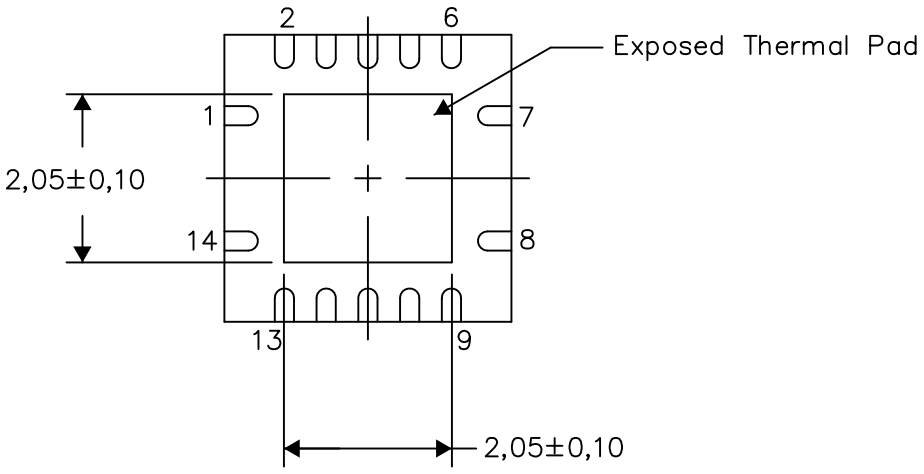
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



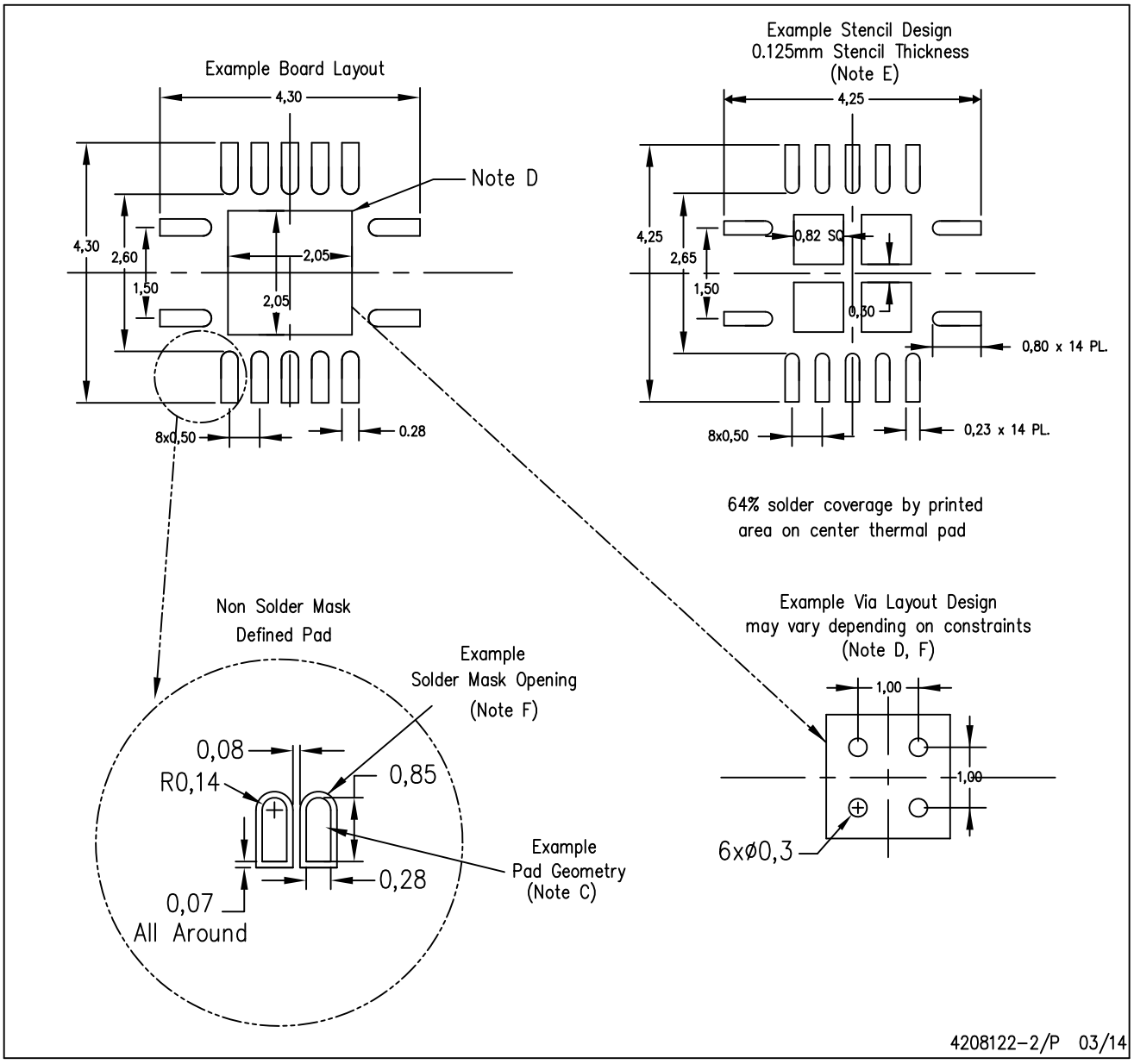
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

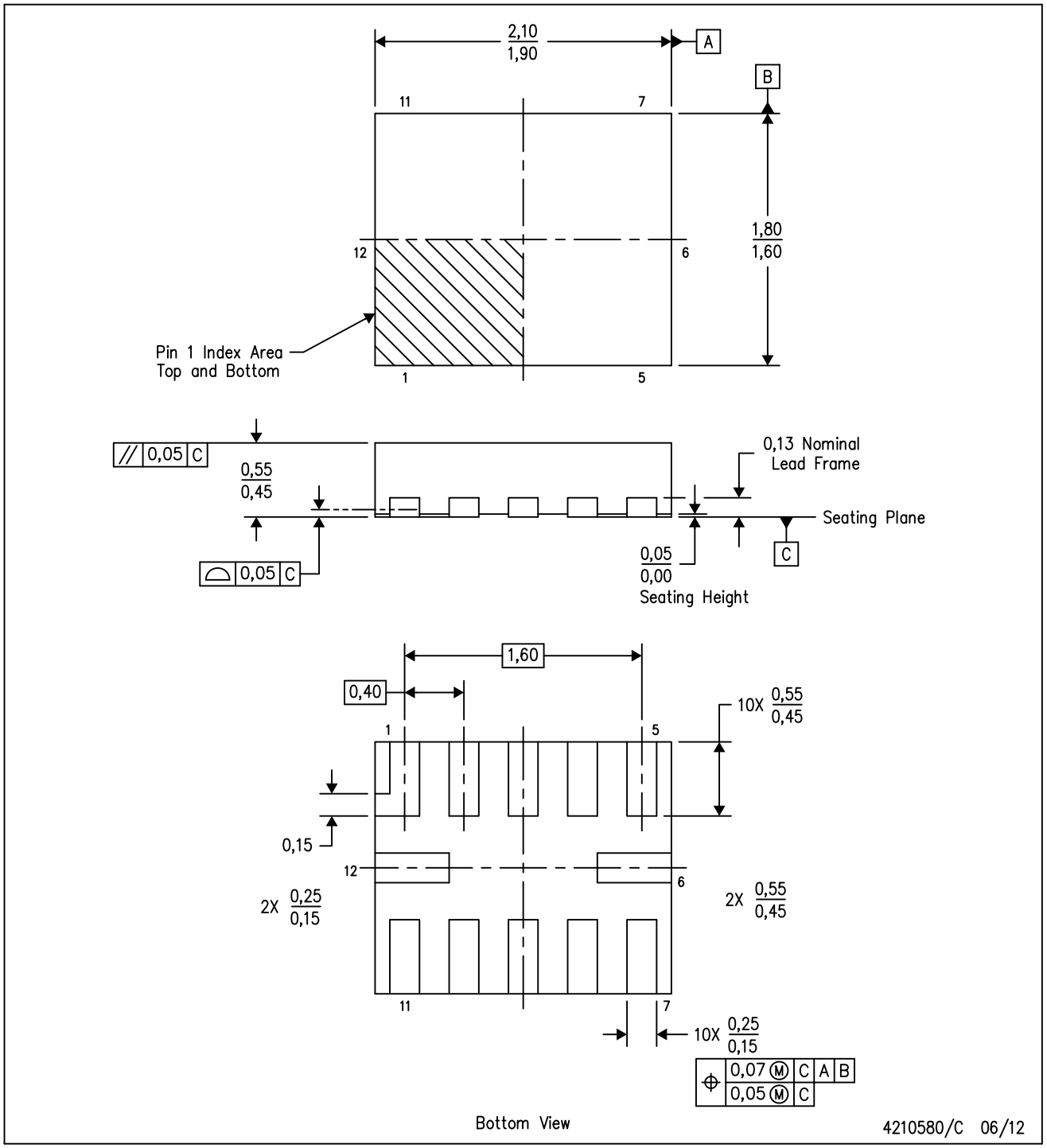
NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



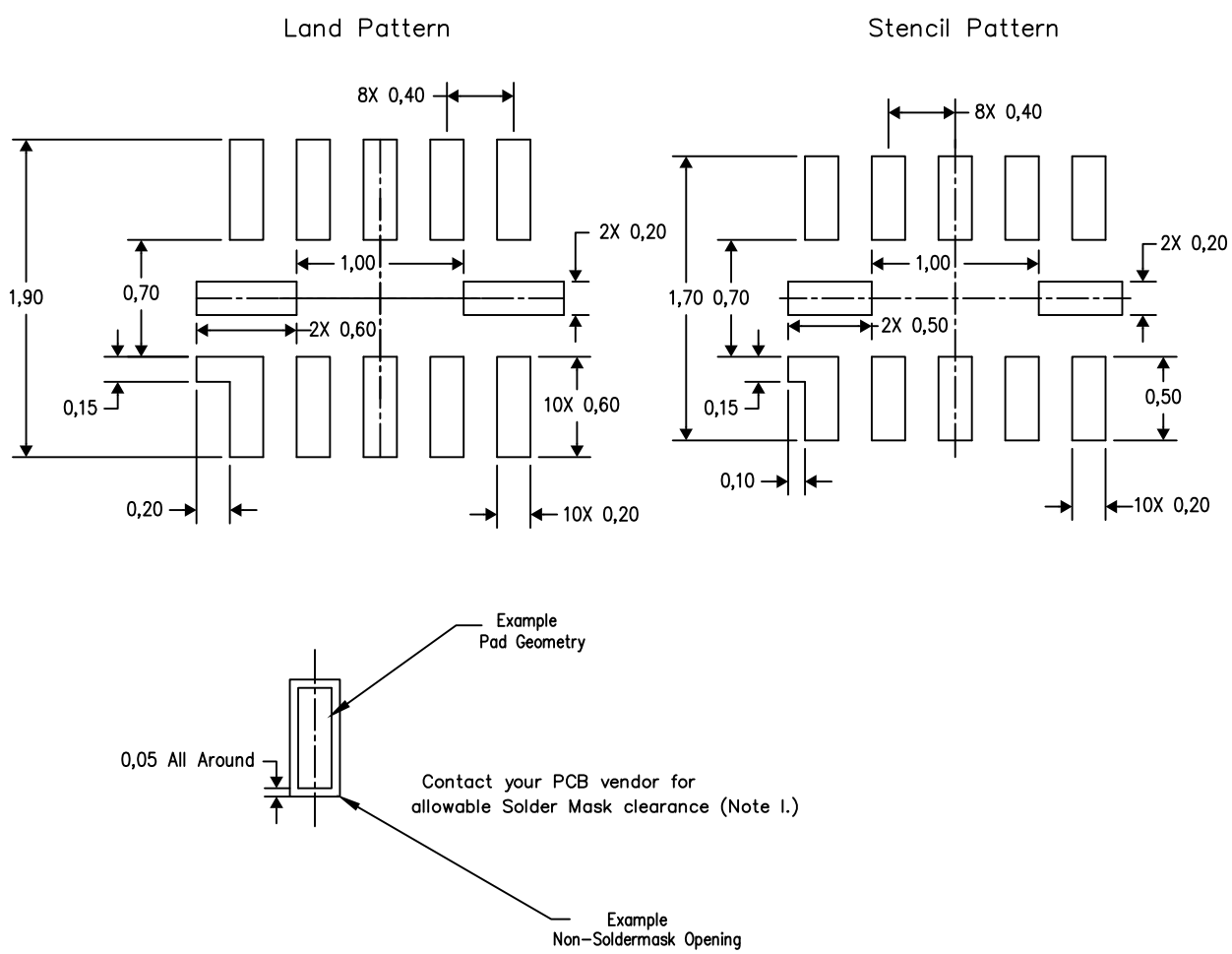
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



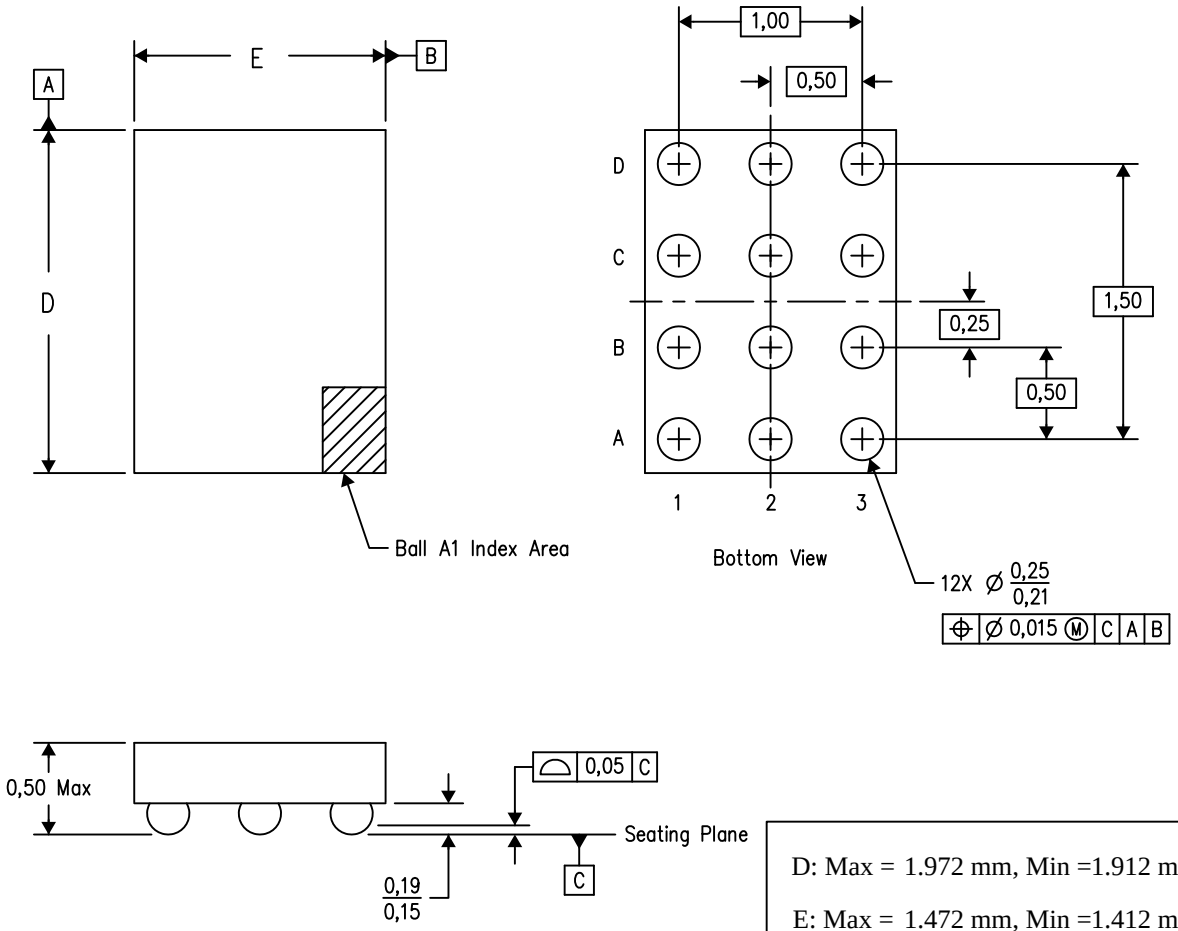
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Over–printing land for larger area ratio is not advised due to land width and bridging potential. Exersize extreme caution.
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
I. Component placement force should be minimized to prevent excessive paste block deformation.

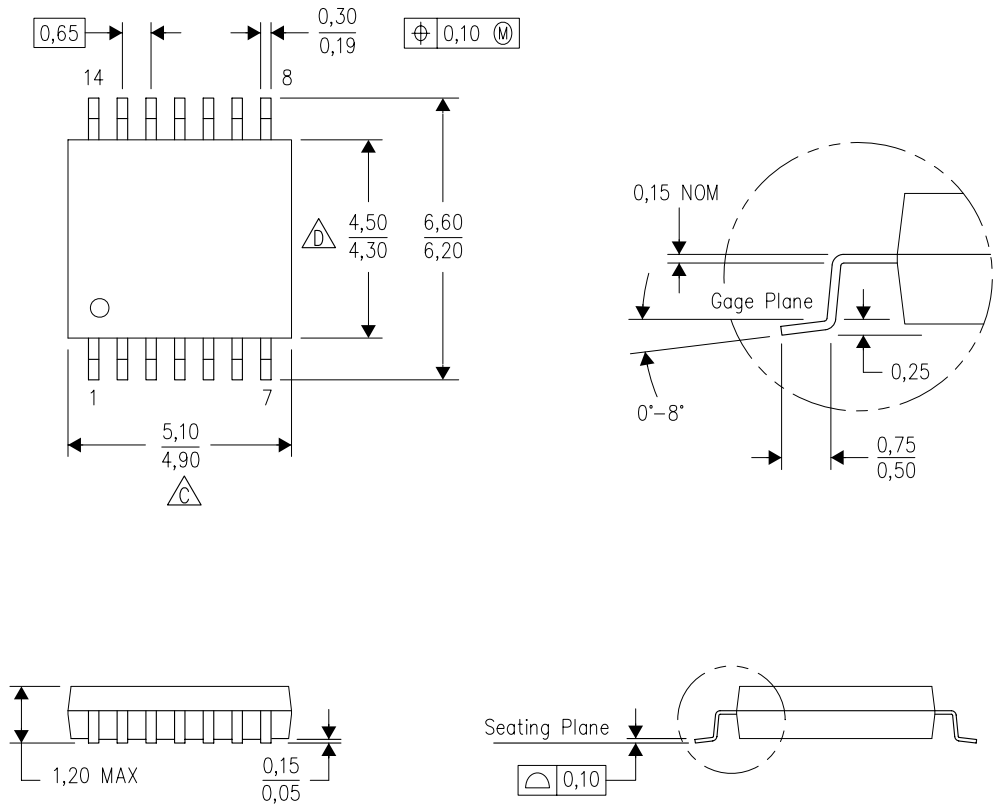
YZP (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

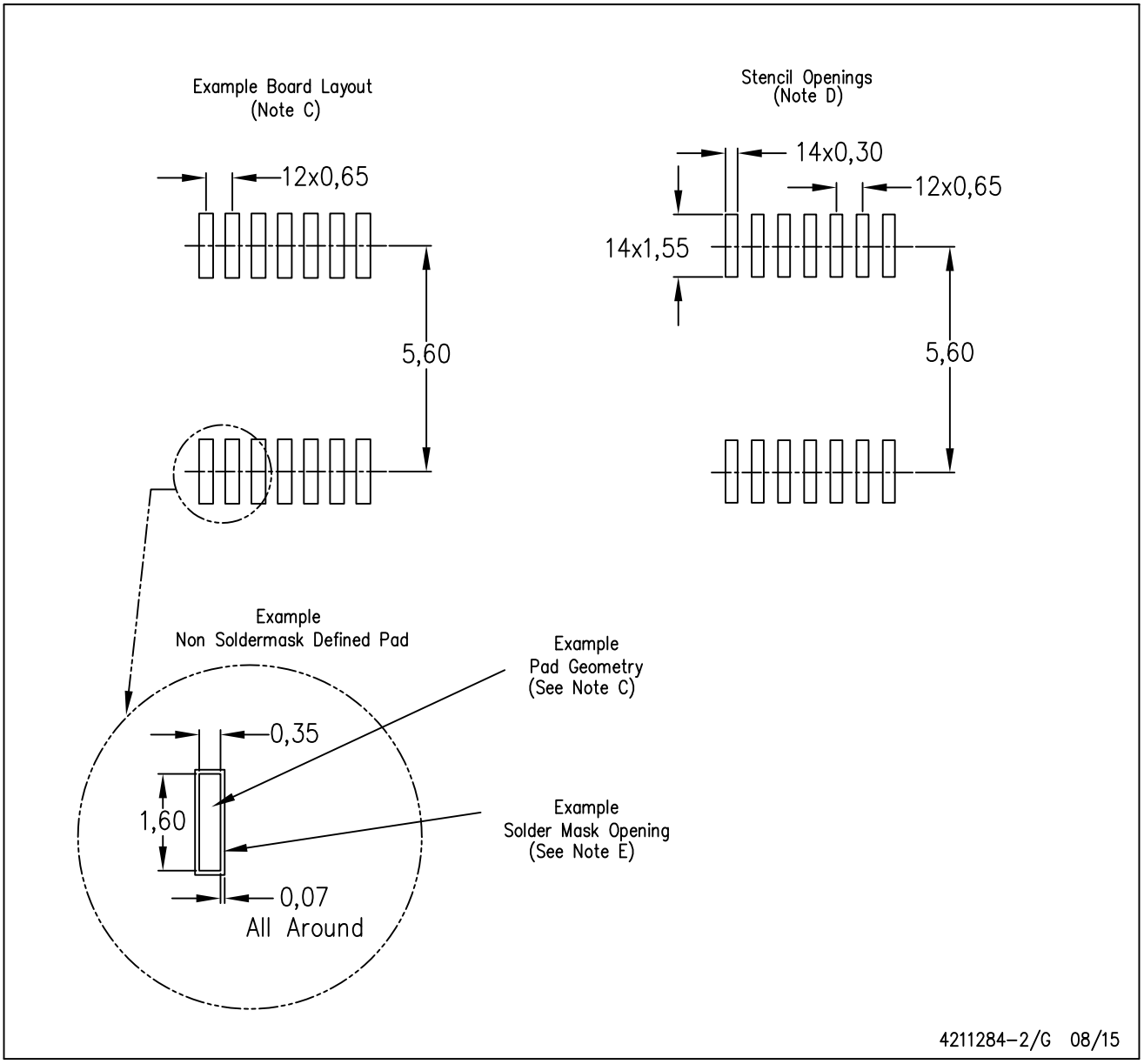
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122