

## SN74GTL2003 8 位双向低压转换器

### 1 特性

- 无需方向控制即可提供双向电压转换
- 支持 0.95V 至 5V 范围内的电压转换
- 可与 GTL、GTL+、低电压晶体管-晶体管逻辑电路 (LVTTTL)/晶体管晶体管逻辑电路 (TTL) 以及 5V 互补金属氧化物半导体 (CMOS) 电平直接相连
- 容性负载  $\leq 20\text{pF}$  时, 支持 50 MHz 升压/降压转换
- 输入和输出引脚之间的导通状态电阻 ( $S_n/D_n$ ) 较低
- 支持热插入
- 无需电源 – 不会发生锁断
- 5V 耐压输入
- 低待机电流
- 采用直通引脚分配, 可简化印刷电路板布线

### 2 应用

- 需要实现 0.95V 至 5V 范围内任意两电压双向或单向转换的应用
- 低电压处理器 I<sup>2</sup>C 端口到 3.3V 或 5V I<sup>2</sup>C 总线信号电平的转换
- GTL/GTL+ 到 LVTTTL/TTL 信号电平的转换
- 高性能计算 (HPC) 服务器
- 透析机
- 服务路由器
- 服务器

### 3 说明

SN74GTL2003 器件提供有 8 个 N 型金属氧化物半导体 (NMOS) 导通晶体管 ( $S_n$  和  $D_n$ )、1 个公共栅极 ( $G_{REF}$ ) 和 1 个基准晶体管 ( $S_{REF}$  和  $D_{REF}$ )。此开关具有低导通状态电阻, 可以最短传播延迟建立连接。该器件无需方向控制引脚即可实现 0.95V 至 5V 范围内任意两电压的双向转换。

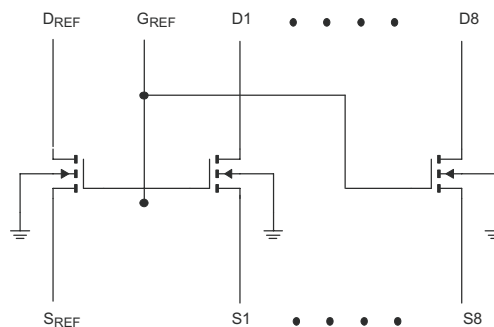
SN74GTL2003 中的所有晶体管具有相同的电气特性, 而且各输出间的电压偏差或传播延迟偏差非常小。这能够为晶体管装配不对称的分立晶体管电压转换解决方案提供出色的匹配特性。由于所有晶体管是相同的, 因此可将基准晶体管 ( $S_{REF}/D_{REF}$ ) 置于其他 8 个匹配的  $S_n/D_n$  晶体管中的任意一个上, 从而简化电路板布线。该转换晶体管集成有静电放电 (ESD) 电路, 可提供出色的 ESD 保护。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
SN74GTL2003	薄型小外形尺寸封装 (TSSOP) (20)	6.50mm x 4.40mm
	VQFN (20)	4.50mm x 2.50mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

简化钳位电路原理图



SA00647



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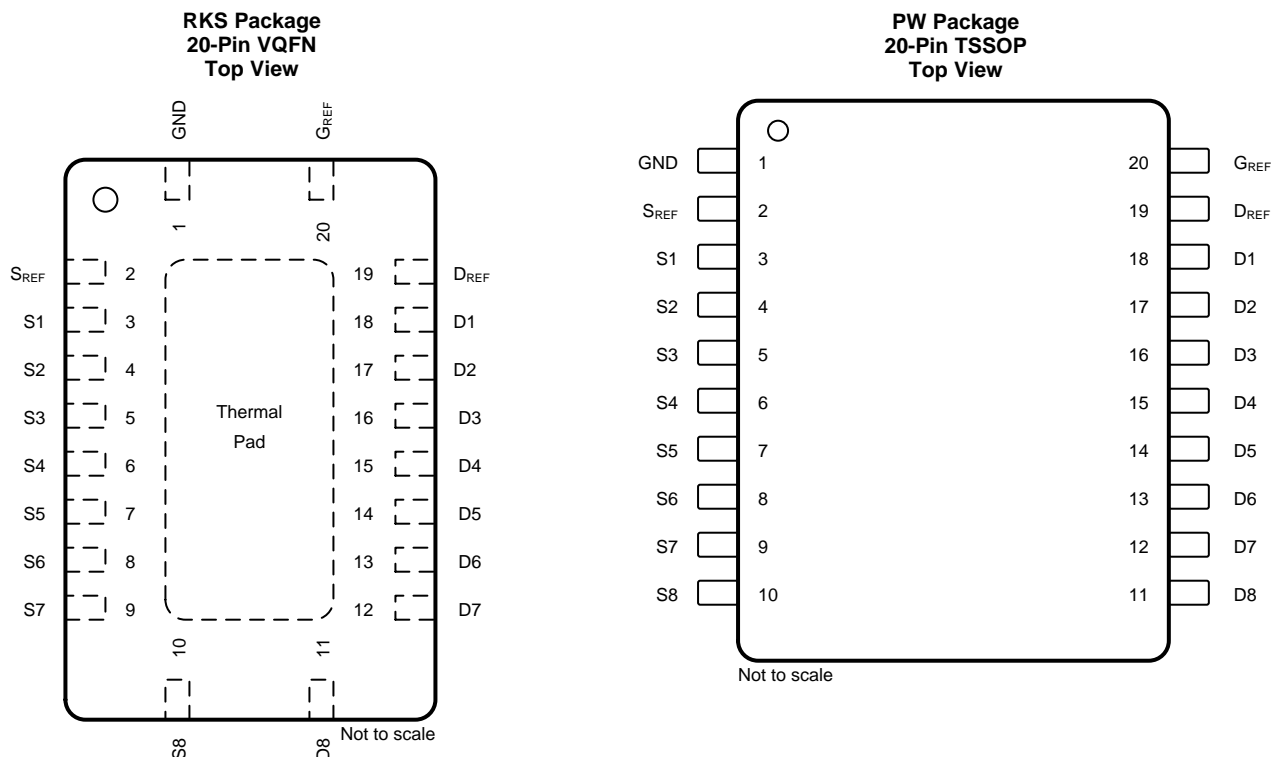
## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (June 2015) to Revision C		Page
•	已更新特性 .....	<b>1</b>
•	Updated pinout images to new format .....	<b>3</b>
•	已添加 接收文档更新通知部分 .....	<b>16</b>

Changes from Revision A (March 2013) to Revision B		Page
•	已添加 <b>ESD</b> 额定值表，特性 描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分 .....	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D1	18	I/O	GTL drain port
D2	17	I/O	GTL drain port
D3	16	I/O	GTL drain port
D4	15	I/O	GTL drain port
D5	14	I/O	GTL drain port
D6	13	I/O	GTL drain port
D7	12	I/O	GTL drain port
D8	11	I/O	GTL drain port
D <sub>REF</sub>	19	—	Drain of reference transistor, tie directly to G <sub>REF</sub> and pull up to reference voltage through a 200-kΩ resistor
GND	1	—	Ground
G <sub>REF</sub>	20	—	Gate of reference transistor, tie directly to D <sub>REF</sub> and pull up to reference voltage through a 200-kΩ resistor
S1	3	I/O	LVTTL/TTL source port
S2	4	I/O	LVTTL/TTL source port
S3	5	I/O	LVTTL/TTL source port
S4	6	I/O	LVTTL/TTL source port
S5	7	I/O	LVTTL/TTL source port
S6	8	I/O	LVTTL/TTL source port
S7	9	I/O	LVTTL/TTL source port
S8	10	I/O	LVTTL/TTL source port
S <sub>REF</sub>	2	—	Source of reference transistor

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>SREF</sub>	DC source reference voltage		–0.5	7	V
V <sub>DREF</sub>	DC drain reference voltage		–0.5	7	V
V <sub>GREF</sub>	DC gate reference voltage		–0.5	7	V
V <sub>Sn</sub>	DC voltage port Sn		–0.5	7	V
V <sub>Dn</sub>	DC voltage port Dn		–0.5	7	V
I <sub>REFK</sub>	DC diode current on reference pins	V <sub>I</sub> < 0 V		–50	mA
I <sub>SK</sub>	DC diode current port Sn	V <sub>I</sub> < 0V		–50	mA
I <sub>DK</sub>	DC diode current port Dn	V <sub>I</sub> < 0 V		–50	mA
I <sub>MAX</sub>	DC clamp current per channel	Channel is ON state		±128	mA
T <sub>stg</sub>	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>I/O</sub>	Input/output voltage (Sn, Dn)	0	5.5	V
V <sub>SREF</sub>	DC source reference voltage <sup>(1)</sup>	0	5.5	V
V <sub>DREF</sub>	DC drain reference voltage	0	5.5	V
V <sub>GREF</sub>	DC gate reference voltage	0	5.5	V
I <sub>PASS</sub>	Pass transistor current		64	mA
T <sub>A</sub>	Operating ambient temperature (in free air)	–40	85	°C

- (1) V<sub>SREF</sub> = V<sub>DREF</sub> – 1.5 V for best results in level-shifting applications.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74GTL2003		UNIT
		PW (TSSOP)	RKS (VQFN)	
		20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	83	81	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	32	36	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 3 V, V <sub>SREF</sub> = 1.365 V, V <sub>Sn</sub> or V <sub>Dn</sub> = 0.175 V, I <sub>clamp</sub> = 15.2 mA			260	350	mV	
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = −18 mA	V <sub>GREF</sub> = 0 V			−1.2	V	
I <sub>IH</sub>	Gate input leakage	V <sub>I</sub> = 5 V	V <sub>GREF</sub> = 0 V			5	μA	
C <sub>I(GREF)</sub>	Gate capacitance	V <sub>I</sub> = 3 V or 0 V			56		pF	
C <sub>IO(OFF)</sub>	OFF capacitance	V <sub>O</sub> = 3 V or 0 V	V <sub>GREF</sub> = 0 V		7.4		pF	
C <sub>IO(ON)</sub>	ON capacitance	V <sub>O</sub> = 3 V or 0 V	V <sub>GREF</sub> = 3 V		18.6		pF	
r <sub>on</sub> <sup>(2)</sup>	ON-state resistance	V <sub>I</sub> = 0 V	V <sub>GREF</sub> = 4.5 V	I <sub>O</sub> = 64 mA		3.5	5	Ω
			V <sub>GREF</sub> = 3 V			4.4	7	
			V <sub>GREF</sub> = 2.3 V			5.5	9	
			V <sub>GREF</sub> = 1.5 V			67	105	
			V <sub>GREF</sub> = 1.5 V,	I <sub>O</sub> = 30 mA		9	15	
		V <sub>I</sub> = 2.4 V	V <sub>GREF</sub> = 4.5 V	I <sub>O</sub> = 15 mA		7	10	
			V <sub>GREF</sub> = 3 V			58	80	
			V <sub>I</sub> = 1.7 V		V <sub>GREF</sub> = 2.3 V		50	

(1) All typical values are measured at  $T_A = 25^\circ\text{C}$ .

(2) Measured by the voltage drop between the Sn and the Dn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (Sn or Dn) terminals.

## 6.6 Switching Characteristics

$V_{REF} = 1.365 \text{ V}$  to  $1.635 \text{ V}$ ,  $V_{DD1} = 3 \text{ V}$  to  $3.6 \text{ V}$ ,  $V_{DD2} = 2.36 \text{ V}$  to  $2.64 \text{ V}$ ,  $GND = 0 \text{ V}$ ,  $t_r = t_f \leq 3 \text{ ns}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

(see Figure 6)<sup>(1)</sup>

PARAMETER	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$t_{PLH}$ <sup>(3)</sup> Propagation delay (Sn to Dn, Dn to Sn)	0.5	1.5	5.5	ns
$t_{PD}$ Propagation delay <sup>(4)</sup>			250	ps

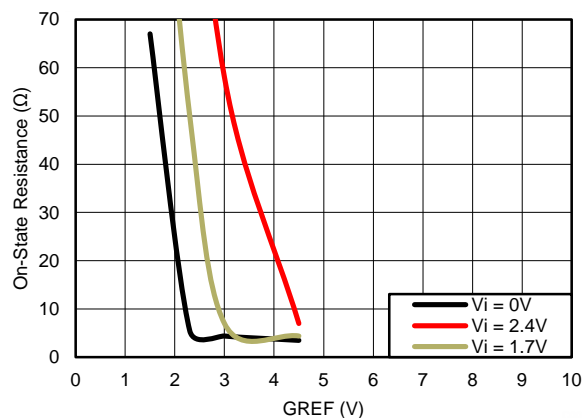
(1)  $C_{ON(max)}$  of 30 pF and a  $C_{OFF(max)}$  of 15 pF is specified by design.

(2) All typical values are measured at  $V_{DD1} = 3.3 \text{ V}$ ,  $V_{DD2} = 2.5 \text{ V}$ ,  $V_{REF} = 1.5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

(3) Propagation delay specified by characterization.

(4) This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

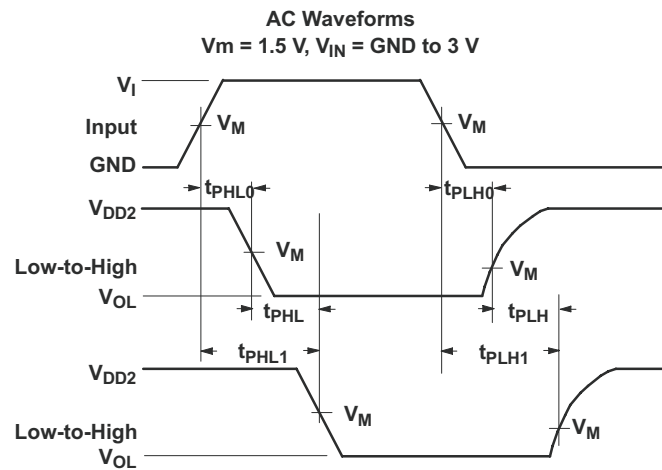
## 6.7 Typical Characteristics



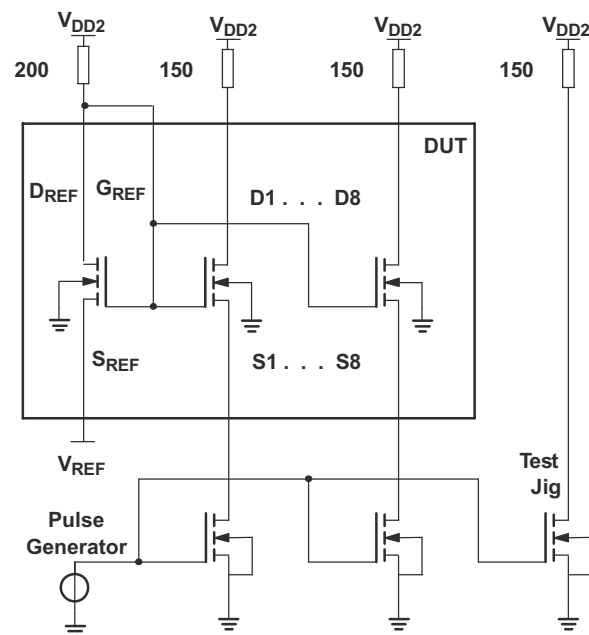
**Figure 1. ON-Resistance vs  $G_{REF}$  Typical Curves**

## 7 Parameter Measurement Information

$C_L$  = Load Capacitance, includes jig and probe capacitance (see [Electrical Characteristics](#) for value)

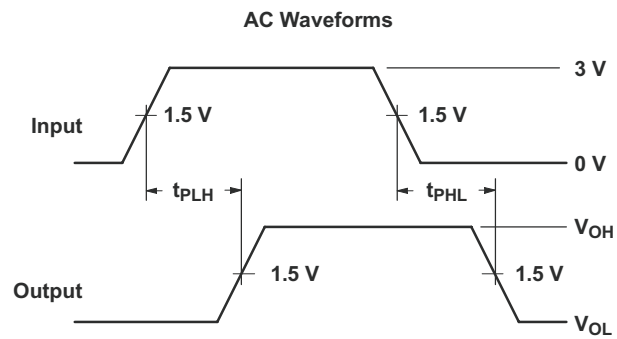


**Figure 2. Input (Sn) to Output (Dn) Propagation Delays**

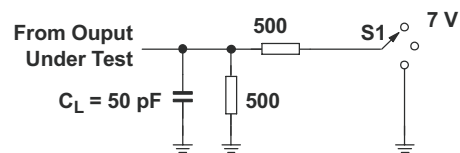


**Figure 3. Load Circuit**

## Parameter Measurement Information (continued)



**Figure 4. Input (Sn) to Output (Dn) Propagation Delays**



**Figure 5. Load Circuit**

**Table 1. Test Conditions**

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$T_{PHZ}/T_{PZH}$	Open

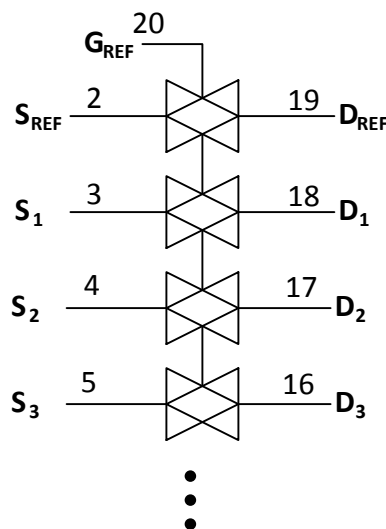
## 8 Detailed Description

### 8.1 Overview

The SN74GTL2003 device provides eight NMOS pass transistors ( $S_n$  and  $D_n$ ) with a common gate ( $G_{REF}$ ) and a reference transistor ( $S_{REF}$  and  $D_{REF}$ ). The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. With no direction control pin required, the device allows bidirectional voltage translations any voltage (0.95 V to 5 V) to any voltage (0.95 V to 5 V).

When the  $S_n$  or  $D_n$  port is LOW, the clamp is in the ON state and a low-resistance connection exists between the  $S_n$  and  $D_n$  ports. Assuming the higher voltage is on the  $D_n$  port, when the  $D_n$  port is HIGH, the voltage on the  $S_n$  port is limited to the voltage set by the reference transistor ( $S_{REF}$ ). When the  $S_n$  port is HIGH, the  $D_n$  port is pulled to VCC by the pullup resistors.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Provides Bidirectional Voltage Translation With No Direction Control Required

Because the circuit acts essentially as a pass transistor, no direction pin is needed, as data is allowed to flow both ways.

#### 8.3.2 Flow Through Pinout

Allocated pins for input and output A on right side and input and output B on left side. Reduces the need for multi-layer board layout or long traces through system.



## 8.4 Device Functional Modes

**Table 2. High to Low Translation  
(Assuming Dn is at the Higher Voltage Level)<sup>(1)</sup>**

$G_{REF}^{(2)}$	$D_{REF}$	$S_{REF}$	INPUTS D8–D1	OUTPUT S8–S1	TRANSISTOR
H	H	0 V	X	X	Off
H		$V_{TT}^{(3)}$	H	$V_{TT}^{(4)}$	On
H		$V_{TT}$	L	$L^{(5)}$	On
L	L	$0 - V_{TT}$	X	X	Off

- (1) H = HIGH voltage level, L = LOW voltage level, X = don't care.
- (2)  $G_{REF}$  should be at least 1.5 V higher than  $S_{REF}$  for best translator operation.
- (3)  $V_{TT}$  is equal to the  $S_{REF}$  voltage.
- (4) Sn is not pulled up or pulled down.
- (5) Sn follows the Dn input LOW.

**Table 3. Low to High Translation  
(Assuming Dn is at the Higher Voltage Level)<sup>(1)</sup>**

$G_{REF}^{(2)}$	$D_{REF}$	$S_{REF}$	INPUTS D8–D1	OUTPUT S8–S1	TRANSISTOR
H	H	0 V	X	X	Off
H	H	$V_{TT}^{(3)}$	$V_{TT}$	$H^{(4)}$	Nearly Off
H	H	$V_{TT}$	L	$L^{(5)}$	On
L	L	$0 - V_{TT}$	X	X	Off

- (1) H = HIGH voltage level, L = LOW voltage level, X = don't care.
- (2)  $G_{REF}$  should be at least 1.5 V higher than  $S_{REF}$  for best translator operation.
- (3)  $V_{TT}$  is equal to the  $S_{REF}$  voltage.
- (4) Dn is pulled up to VCC through an external resistor.
- (5) Dn follows the Sn input LOW.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

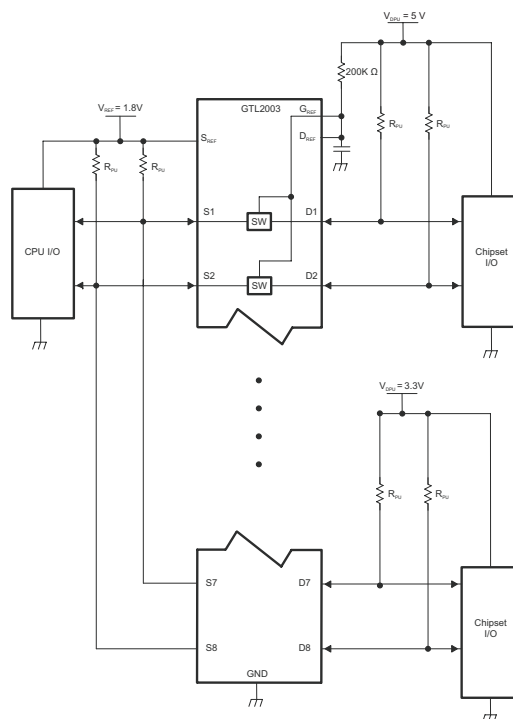
### 9.1 Application Information

SN74GTL2003 is a GTL/GTL+ to LVTTTL/TTL bidirectional voltage level translator. This device can be used in both unidirectional applications and bidirectional. Please find the reference schematics and recommended values for passive components in the [Typical Applications](#).

### 9.2 Typical Applications

#### 9.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the  $G_{REF}$  input must be connected to  $D_{REF}$  and both pins pulled to HIGH-side  $V_{CC}$  through a pullup resistor (typically 200 k $\Omega$ ). TI recommends a filter capacitor on  $D_{REF}$ . The processor output can be totem pole or open drain (pullup resistors) and the chipset output can be totem pole or open drain (pullup resistors are required to pull the Dn outputs to  $V_{CC}$ ). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-statable, and the outputs must be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open drain, no direction control is needed. The opposite side of the reference transistor ( $S_{REF}$ ) is connected to the processor core power-supply voltage. When  $D_{REF}$  is connected through a 200-k $\Omega$  resistor to a 3.3-V to 5.5-V  $V_{CC}$  supply and  $S_{REF}$  is set from 1 V to  $V_{CC}$  1.5 V, the output of each Sn has a maximum output voltage equal to  $S_{REF}$ , and the output of each Dn has a maximum output voltage equal to  $V_{CC}$ .



**Figure 6. Bidirectional Translation to Multiple Higher Voltage Levels  
(Such as an I<sup>2</sup>C or SMBus Applications)**

## Typical Applications (continued)

### 9.2.1.1 Design Requirements

- SN74GTL2003 requires industry standard GTL and LVTTTL/TTL voltage levels.
- Place pullup resistors of ~200kΩ in all inputs/outputs to the GTL/TTL voltage levels.
- Place 0.1-μF bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.
- Comply to the parameters in the [Recommended Operating Conditions](#).

### 9.2.1.2 Detailed Design Procedure

#### 9.2.1.2.1 Sizing Pullup Resistors

The pullup resistor value should limit the current through the pass transistor when it is in the on state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$\text{Resistor value}(\Omega) = \frac{\text{Pullup voltage(V)} - 0.35 \text{ V}}{0.015 \text{ A}} \quad (1)$$

[Table 4](#) shows resistor values for various reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column, or a larger value, should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL device at 0.175 V, although the 15 mA only applies to current flowing through the SN74GTL2003.

**Table 4. Pullup Resistor Values<sup>(1)(2)(3)</sup>**

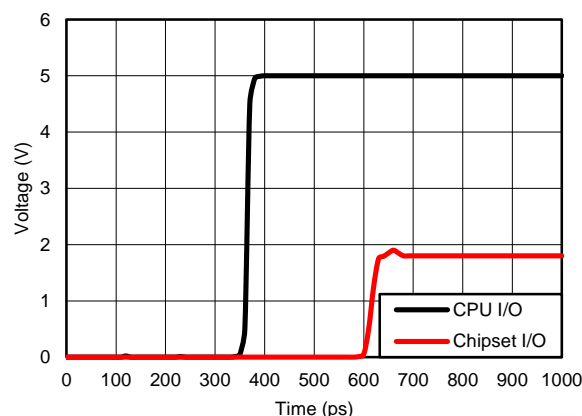
VOLTAGE	PULLUP RESISTOR VALUE (Ω)					
	15 mA		10 mA		3 mA	
	NOMINAL	+10%	NOMINAL	+10%	NOMINAL	+10%
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for  $V_{OL} = 0.35 \text{ V}$

(2) Assumes output driver  $V_{OL} = 0.175 \text{ V}$  at stated current

(3) +10% to compensate for  $V_{DD}$  range and resistor tolerance

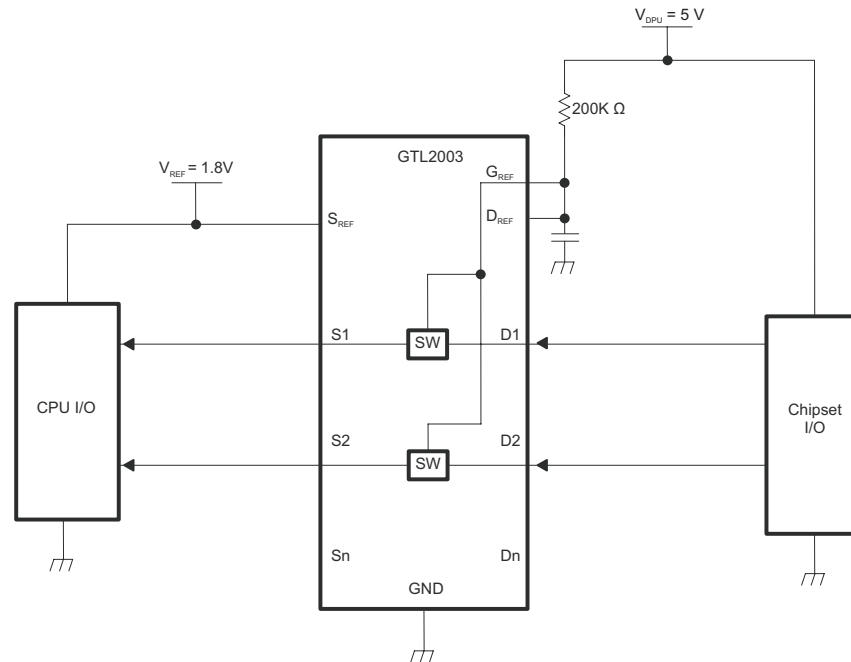
#### 9.2.1.3 Application Curve



**Figure 7. Signal Voltage vs Time (ps) (Simulated Design Results)**

## 9.2.2 Unidirectional Down Translation

For unidirectional clamping (higher voltage to lower voltage), the  $G_{REF}$  input must be connected to  $D_{REF}$  and both pins pulled to the higher-side  $V_{CC}$  through a pullup resistor (typically 200 k $\Omega$ ). TI recommends a filter capacitor on  $D_{REF}$ . Pullup resistors are required if the chipset I/Os are open drain. The opposite side of the reference transistor ( $S_{REF}$ ) is connected to the processor core power supply voltage. When  $D_{REF}$  is connected through a 200-k $\Omega$  resistor to a 3.3-V to 5.5-V  $V_{CC}$  supply and  $S_{REF}$  is set from 1 V to  $V_{CC} - 1.5$  V, the output of each  $S_n$  has a maximum output voltage equal to  $S_{REF}$ .



**Figure 8. Unidirectional Down Translation to Protect Low-Voltage Processor Pins**

### 9.2.2.1 Design Requirements

- SN74GTL2003 requires industry standard GTL and LVTTTL/TTL voltage levels.
- Place pullup resistors of approximately 200 k $\Omega$  in all inputs/outputs to the GTL/TTL voltage levels.
- Place 0.1- $\mu$ F bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.
- Comply to the parameters in the [Recommended Operating Conditions](#).

### 9.2.2.2 Detailed Design Procedure

#### 9.2.2.2.1 Sizing Pullup Resistors

The pullup resistor value should limit the current through the pass transistor when it is in the on state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$\text{Resistor value}(\Omega) = \frac{\text{Pullup voltage}(V) - 0.35 V}{0.015 A} \quad (2)$$

[Table 5](#) shows resistor values for various reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column, or a larger value, should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL device at 0.175 V, although the 15 mA only applies to current flowing through the SN74GTL2003.

**Table 5. Pullup Resistor Values<sup>(1)(2)(3)</sup>**

VOLTAGE	PULLUP RESISTOR VALUE ( $\Omega$ )					
	15 mA		10 mA		3 mA	
	NOMINAL	+10%	NOMINAL	+10%	NOMINAL	+10%
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

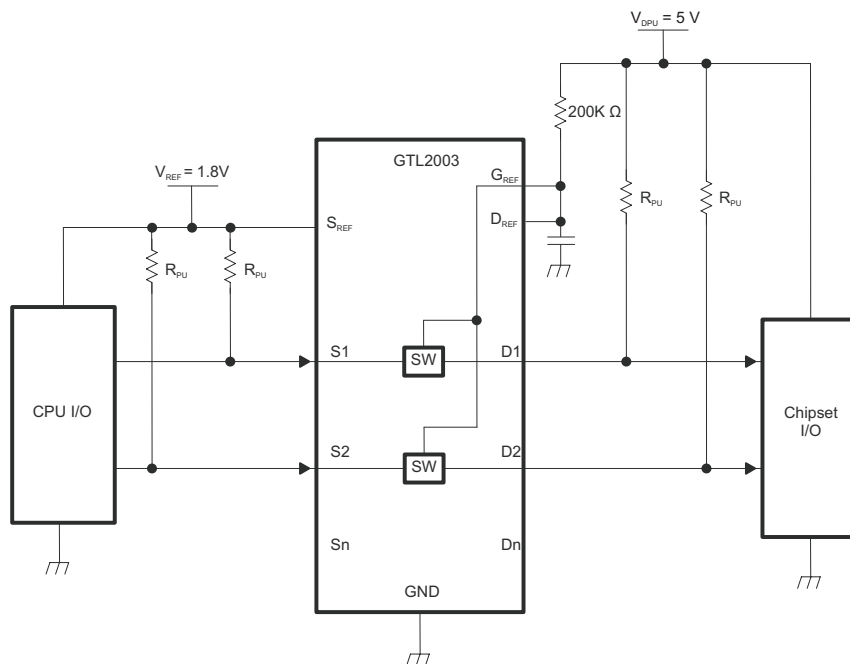
(1) Calculated for  $V_{OL} = 0.35$  V

(2) Assumes output driver  $V_{OL} = 0.175$  V at stated current

(3) +10% to compensate for  $V_{DD}$  range and resistor tolerance

### 9.2.3 Unidirectional Up Translation

For unidirectional up translation (lower voltage to higher voltage), the reference transistor is connected the same as for a down translation. A pullup resistor is required on the higher voltage side ( $D_n$  or  $S_n$ ) to get the full HIGH level, because the GTL device only passes the reference source ( $S_{REF}$ ) voltage as a HIGH when doing an up translation. The driver on the lower voltage side only needs pullup resistors if it is open drain.



**Figure 9. Unidirectional Up Translation to Higher-Voltage Chipsets**

#### 9.2.3.1 Design Requirements

- SN74GTL2003 requires industry standard GTL and LVTTL/TTL voltage levels.
- Place pullup resistors of  $\sim 200k\Omega$  in all inputs/outputs to the GTL/TTL voltage levels.
- Place 0.1- $\mu$ F bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.
- Comply to the parameters in the [Recommended Operating Conditions](#)

### 9.2.3.2 Detailed Design Procedure

#### 9.2.3.2.1 Sizing Pullup Resistors

The pullup resistor value should limit the current through the pass transistor when it is in the on state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$\text{Resistor value}(\Omega) = \frac{\text{Pullup voltage(V)} - 0.35 \text{ V}}{0.015 \text{ A}} \quad (3)$$

Table 6 shows resistor values for various reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column, or a larger value, should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL device at 0.175 V, although the 15 mA only applies to current flowing through the SN74GTL2003.

**Table 6. Pullup Resistor Values<sup>(1)(2)(3)</sup>**

VOLTAGE	PULLUP RESISTOR VALUE (Ω)					
	15 mA		10 mA		3 mA	
	NOMINAL	+10%	NOMINAL	+10%	NOMINAL	+10%
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for  $V_{OL} = 0.35 \text{ V}$

(2) Assumes output driver  $V_{OL} = 0.175 \text{ V}$  at stated current

(3) +10% to compensate for  $V_{DD}$  range and resistor tolerance

## 10 Power Supply Recommendations

Place 0.1-μF bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

## 11 Layout

### 11.1 Layout Guidelines

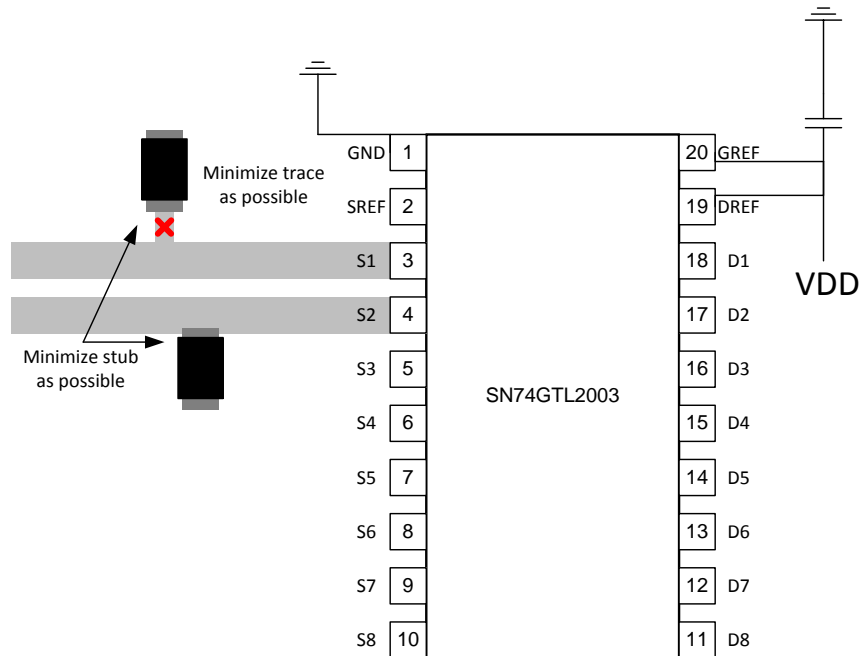
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.

## Layout Guidelines (continued)

- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Example



**Figure 10. Layout Example for GTL Trace**

## 12 器件和文档支持

### 12.1 接收文档更新通知

如需接收文档更新通知，请访问 [www.ti.com.cn](http://www.ti.com.cn) 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

### 12.2 社区资源

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**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.5 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74GTL2003PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GK2003	<a href="#">Samples</a>
SN74GTL2003PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GK2003	<a href="#">Samples</a>
SN74GTL2003RKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GK2003	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL2003PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74GTL2003RKSR	VQFN	RKS	20	3000	177.8	12.4	2.73	4.85	1.03	4.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL2003PWR	TSSOP	PW	20	2000	853.0	449.0	35.0
SN74GTL2003RKSR	VQFN	RKS	20	3000	202.0	201.0	28.0

## GENERIC PACKAGE VIEW

**RKS 20**

**VQFN - 1 mm max height**

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



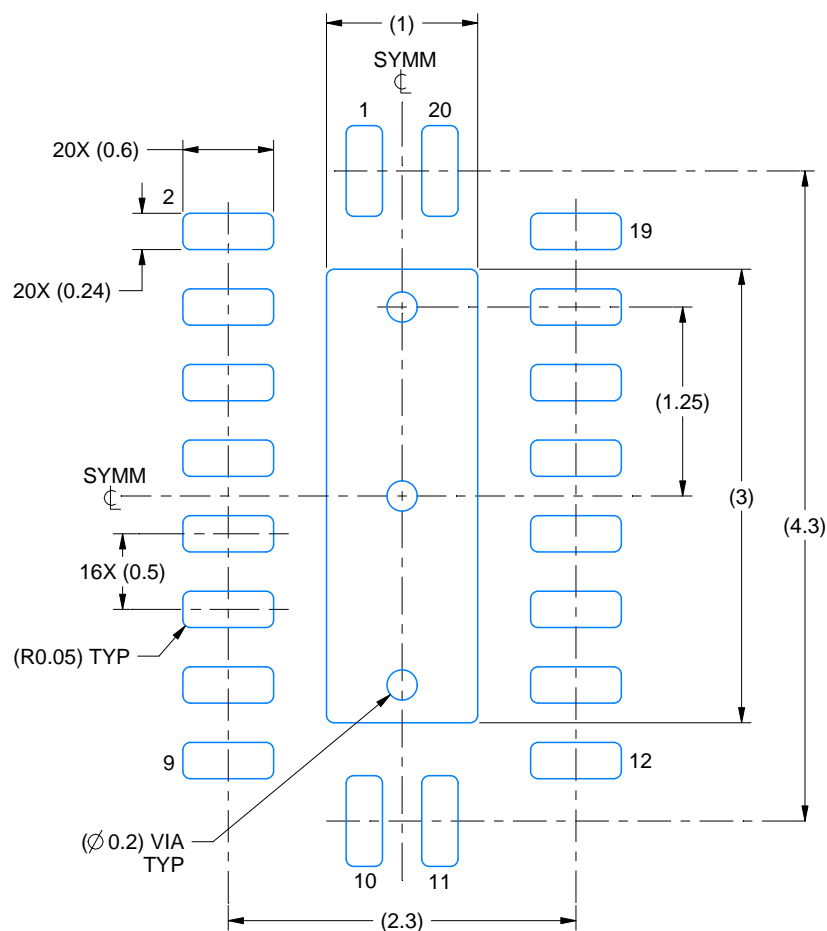


# EXAMPLE BOARD LAYOUT

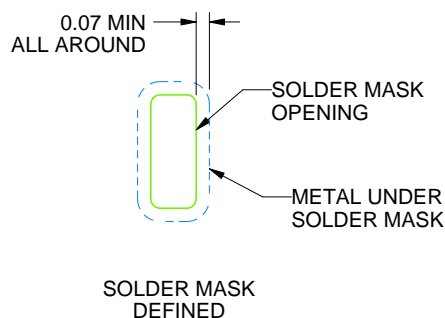
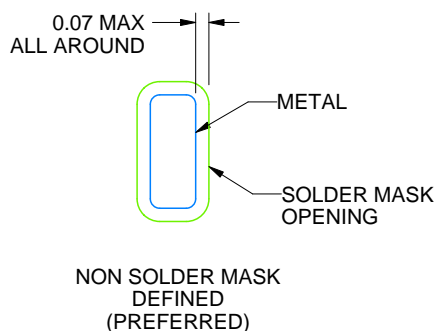
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

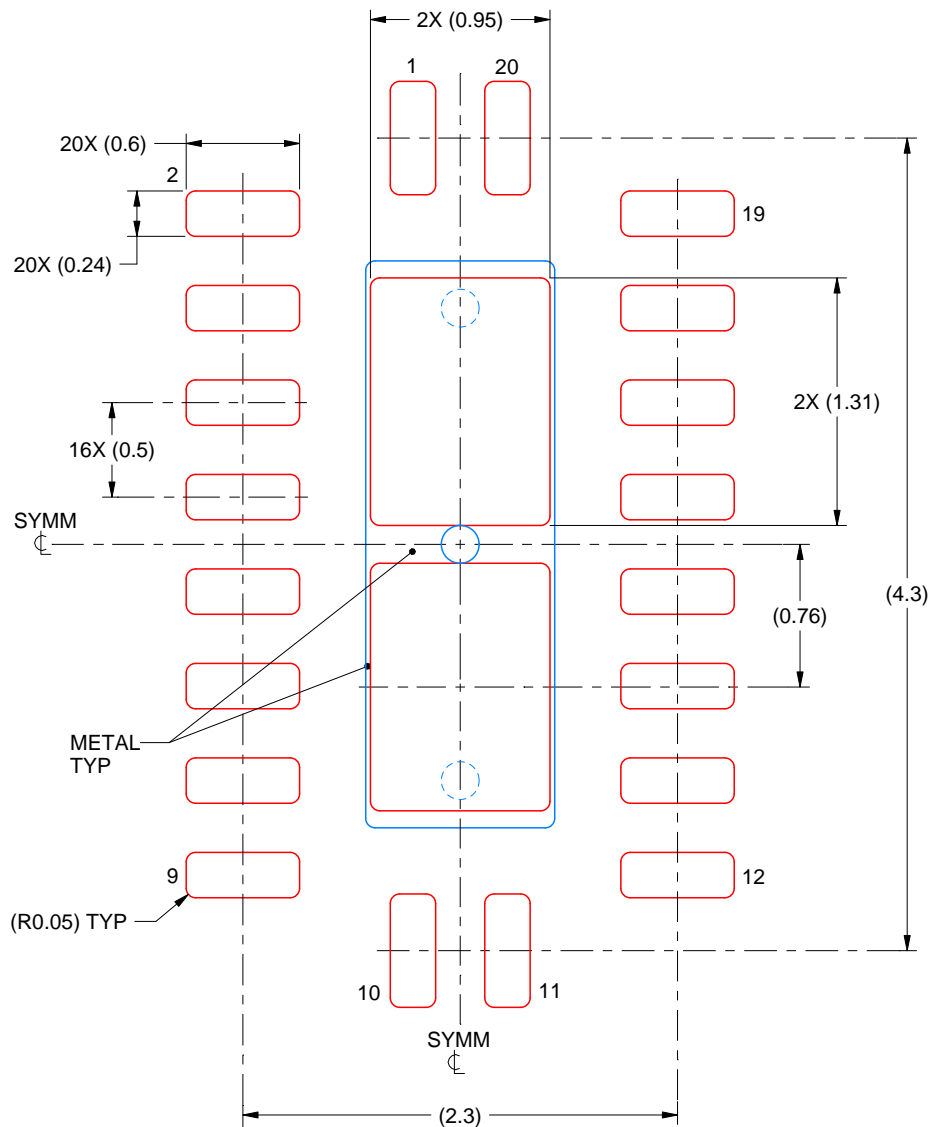
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
83% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4222490/B 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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