

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Ideal for Use in PC133 Register DIMM
- Typical Output Skew . . . <250 ps
- $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  . . . Normal Range
- $V_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$  . . . Extended Range
- $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$
- Rail-to-Rail Output Swing for Increased Noise Margin
- Balanced Output Drivers . . .  $\pm 18\text{ mA}$
- Low Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

This 18-bit universal bus driver is designed for 2.3-V to 3.6-V  $V_{CC}$  operation.

Data flow from A to Y is controlled by the output-enable ( $\overline{OE}$ ) input. The device operates in the transparent mode when the latch-enable ( $\overline{LE}$ ) input is low. When  $\overline{LE}$  is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If  $\overline{LE}$  is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The ALVCF162834 has series damping resistors in the device output structure that reduce switching noise in 128-MB and 256-MB SDRAM modules. Designed with a drive capability of  $\pm 18\text{ mA}$ , this device is a midway drive between the ALVC162834 ( $\pm 12\text{ mA}$ ) and ALVC16834 ( $\pm 24\text{ mA}$ ).

The SN74ALVCF162834 is a faster version of the SN74ALVC162834. It is suitable for PC133 applications, particularly for SDRAM modules clocked at 133 MHz.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)

NC	1	56	GND
NC	2	55	NC
Y1	3	54	A1
GND	4	53	GND
Y2	5	52	A2
Y3	6	51	A3
$V_{CC}$	7	50	$V_{CC}$
Y4	8	49	A4
Y5	9	48	A5
Y6	10	47	A6
GND	11	46	GND
Y7	12	45	A7
Y8	13	44	A8
Y9	14	43	A9
Y10	15	42	A10
Y11	16	41	A11
Y12	17	40	A12
GND	18	39	GND
Y13	19	38	A13
Y14	20	37	A14
Y15	21	36	A15
$V_{CC}$	22	35	$V_{CC}$
Y16	23	34	A16
Y17	24	33	A17
GND	25	32	GND
Y18	26	31	A18
$\overline{OE}$	27	30	CLK
$\overline{LE}$	28	29	GND

NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCF162834DL	ALVCF162834
		Tape and reel	SN74ALVCF162834DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCF162834GR	ALVCF162834
	TVSOP - DGV	Tape and reel	SN74ALVCF162834VR	VF162834

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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Widebus is a trademark of Texas Instruments.

# SN74ALVCF162834 3.3-V CMOS 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

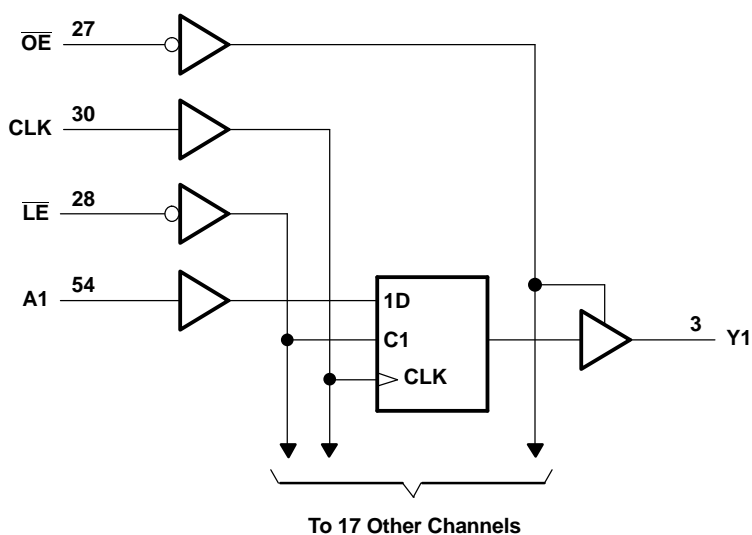
SCES409B–AUGUST 2002–REVISED OCTOBER 2004

**FUNCTION TABLE**

INPUTS				OUTPUT Y
$\overline{OE}$	$\overline{LE}$	CLK	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	$Y_0^{(1)}$

(1) Output level before the indicated steady-state conditions were established

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50 mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through each V <sub>CC</sub> or GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package		64
		DGV package		48
		DL package		56
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.3 V	-6		mA
			-8		
		V <sub>CC</sub> = 2.7 V	-6		
			-12		
		V <sub>CC</sub> = 3 V	-8		
			-18		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V	6		mA
			8		
		V <sub>CC</sub> = 2.7 V	6		
			12		
		V <sub>CC</sub> = 3 V	8		
			18		
Δt/Δv	Input transition rise or fall rate		10		ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74ALVCF162834

## 3.3-V CMOS 18-BIT UNIVERSAL BUS DRIVER

### WITH 3-STATE OUTPUTS

SCES409B–AUGUST 2002–REVISED OCTOBER 2004

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -0.1 mA	2.3 V to 3.6 V	V <sub>CC</sub> - 0.2			V
		I <sub>OH</sub> = -6 mA	2.3 V	1.9			
		I <sub>OH</sub> = -8 mA		1.7			
		I <sub>OH</sub> = -6 mA	2.7 V	2.2			
		I <sub>OH</sub> = -12 mA		2			
		I <sub>OH</sub> = -8 mA	3 V	2.4			
		I <sub>OH</sub> = -18 mA		2			
V <sub>OL</sub>		I <sub>OL</sub> = 0.1 mA	2.3 V to 3.6 V			0.2	V
		I <sub>OL</sub> = 6 mA	2.3 V			0.4	
		I <sub>OL</sub> = 8 mA				0.55	
		I <sub>OL</sub> = 6 mA	2.7 V			0.4	
		I <sub>OL</sub> = 12 mA				0.6	
		I <sub>OL</sub> = 8 mA	3 V			0.55	
		I <sub>OL</sub> = 18 mA				0.8	
V <sub>IK</sub>		V <sub>CC</sub> = 2.3 V, I <sub>I</sub> = -18 mA	3.6 V			-1.2	V
V <sub>hys</sub>		V <sub>CC</sub> = 3.6 V	3.6 V	100			mV
I <sub>I</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	μA
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	0.1		40	μA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
C <sub>i</sub>	Inputs	V <sub>I</sub> = 0 V	3.3 V	3			pF
C <sub>o</sub>	Outputs	V <sub>O</sub> = 0 V	3.3 V	4			pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 2)

				V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			150		150		150		MHz
t <sub>w</sub>	Pulse duration	LE low		3.3		3.3		3.3		ns
		CLK high or low		3.3		3.3		3.3		
t <sub>su</sub>	Setup time	Data before CLK↑		1.8		1.5		1		ns
		Data before LE↑	CLK high	1.9		1.6		1.5		
			CLK low	1.3		1.1		1		
t <sub>h</sub>	Hold time	Data after CLK↑		0.6		0.6		0.6		ns
		Data after LE↑	CLK high or low		1.4		1.7		1.4	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			150		150		150		MHz
$t_{pd}$	A	Y	1	4		4.6	1	3.5	ns
	$\overline{LE}$		1.3	5.5		5.4	1.3	4.6	
	CLK		1.4	5.9		5.6	1.4	3.5	
$t_{en}$	$\overline{OE}$	Y	1.4	5.9		6	1.1	5	ns
$t_{dis}$	$\overline{OE}$	Y	1	4.7		4.6	1.3	4.2	ns
$t_{sk(o)}$								500	ps

## SWITCHING CHARACTERISTICS

from 0°C to 65°C,  $C_L = 50\text{ pF}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.15\text{ V}$		UNIT
			MIN	MAX	
$t_{pd}$	CLK	Y	1.8	3.5	ns

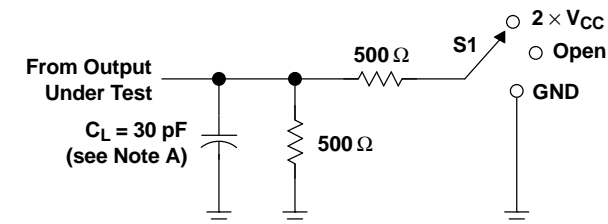
## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	
$C_{pd}$	Power dissipation capacitance	$C_L = 0, f = 10\text{ MHz}$	28	33	pF
	Outputs disabled		16	21	

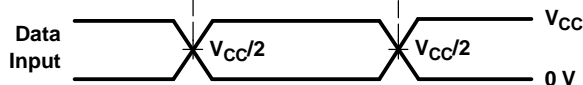
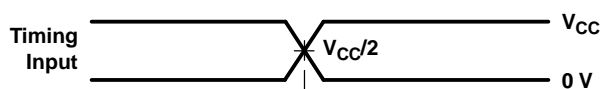
# PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

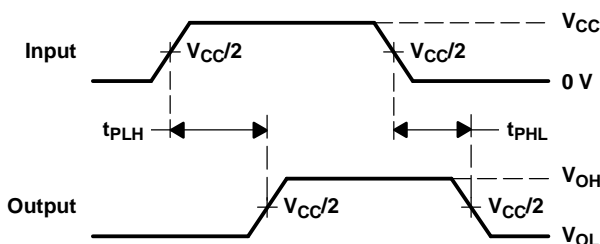


LOAD CIRCUIT

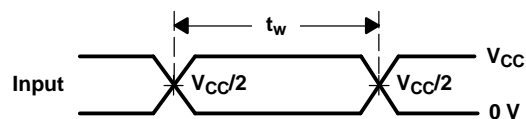
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



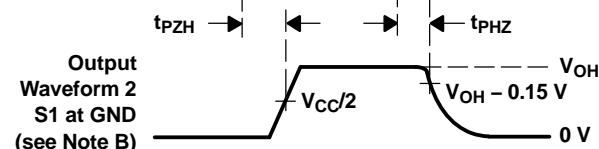
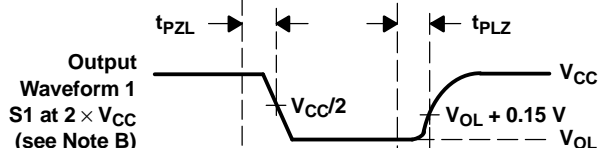
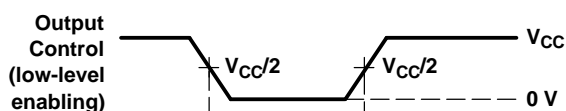
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



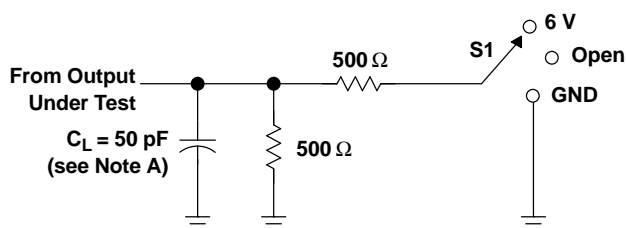
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

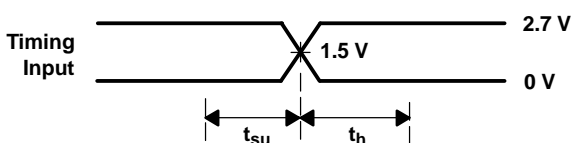
Figure 1. Load Circuit and Voltage Waveforms

# PARAMETER MEASUREMENT INFORMATION

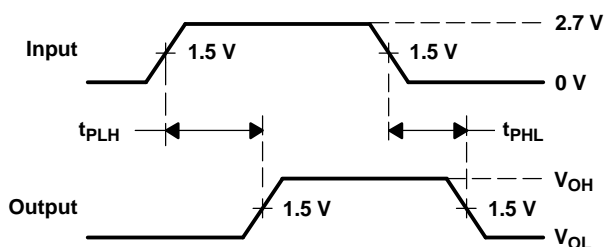
$V_{CC} = 2.7\text{ V}$  AND  $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

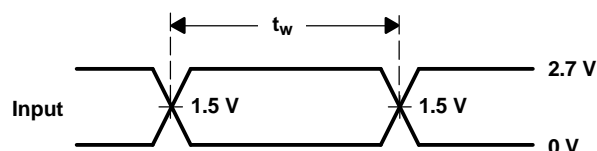


VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES

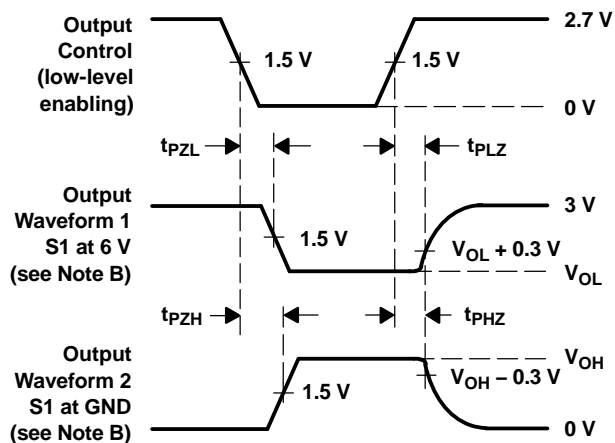


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVCF162834DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCF162834	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

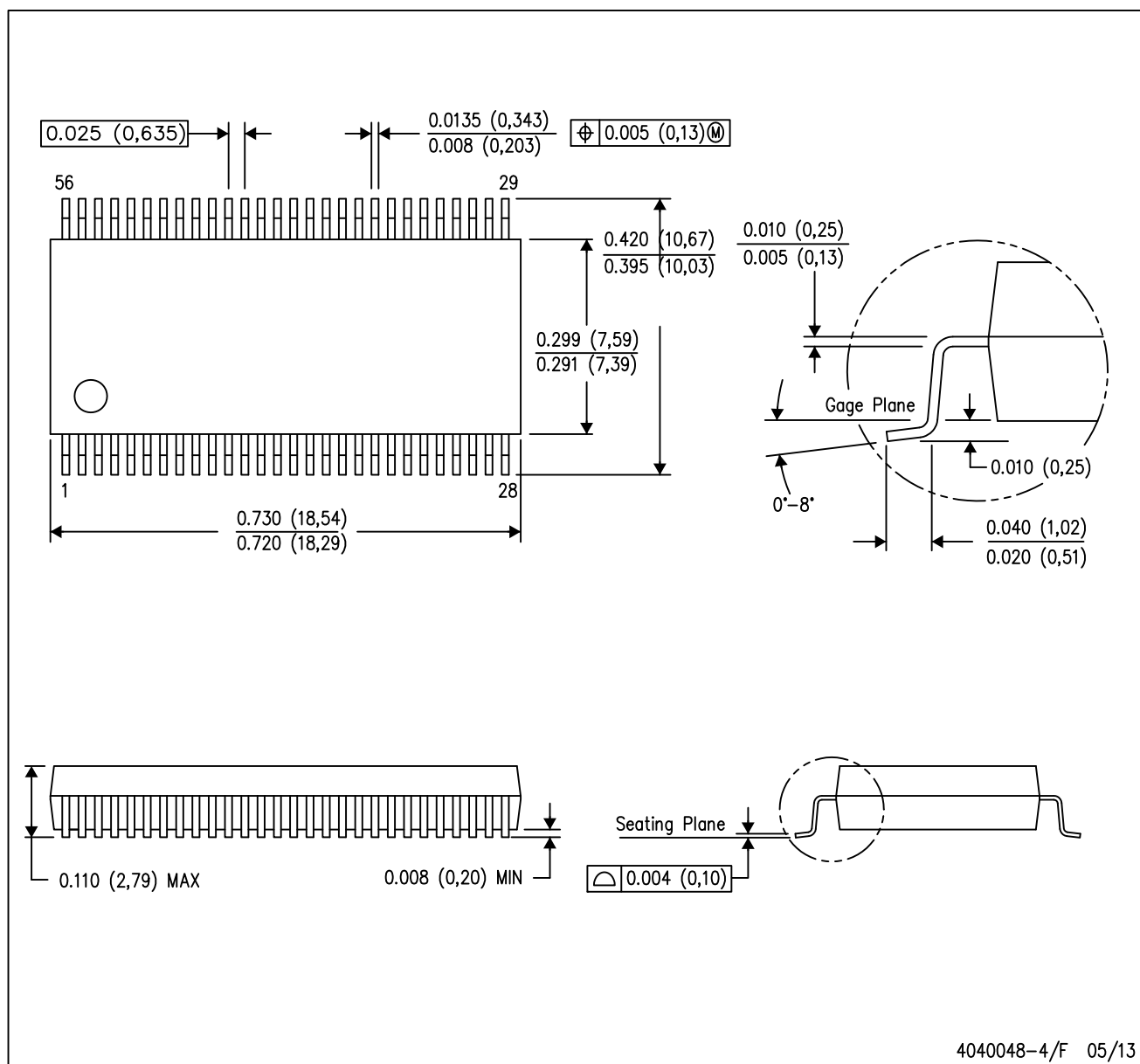
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DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



## NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed  $0.006$  (0,15).
- Falls within JEDEC MO-118

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