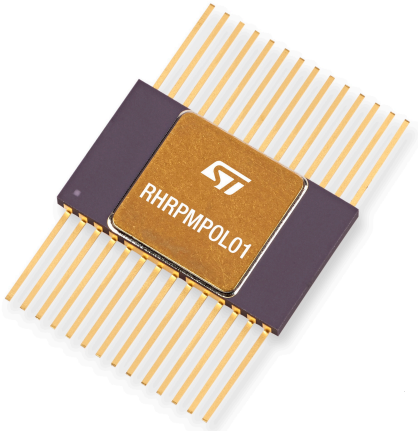
RHRPMPOL01

Datasheet

Rad-hard 7 A point-of-load synchronous step-down regulator



Product status link
RHRPMPOL01

Features

- 3.0 V to 12 V input operating voltage range
- 0.8 V to (0.85xV_{IN}) output voltage range
- Up to 7 A output current
- Wide operating temperature range -55 °C to +125 °C
- Single supply
- Integrated N-channel MOSFETs for synchronous step-down conversion
- Integrated BOOT diode
- Programmable switching frequency: from 100 kHz to 1 MHz
- Fast load transient response and simple loop compensation based on peak current mode control loop
- Easy synchronization with 180° out-of-phase (up to 2 ICs) management
- Current sharing configuration for higher load requirements
- Lossless current sensing based on sense-FET
- Not-latched output overvoltage protection
- Adjustable output overcurrent protection
- Input undervoltage protection
- Latched overtemperature protection
- Power Good output pin
- Programmable soft-start with increased current capability
- Hermetic ceramic package qualified for space applications FLAT-28
- Radiation performance:
  - Total ionizing dose: 100 krad
  - Tested ELDRS-free
  - SEL/SESB-free up to 86.1 MeV/mg/cm2 (@ V_{CC} up to 7 V)
  - SEU-SEFI characterized up to V_{CC} 7 V
  - Proton free
  - No performance degradation due to SET
  - QML-V qualified, SMD 5962R20208

Applications

- Point of load regulation for space application
- FPGA, DSP, CPU and ASICS supply
- Low voltage, high density distributed power systems

Description

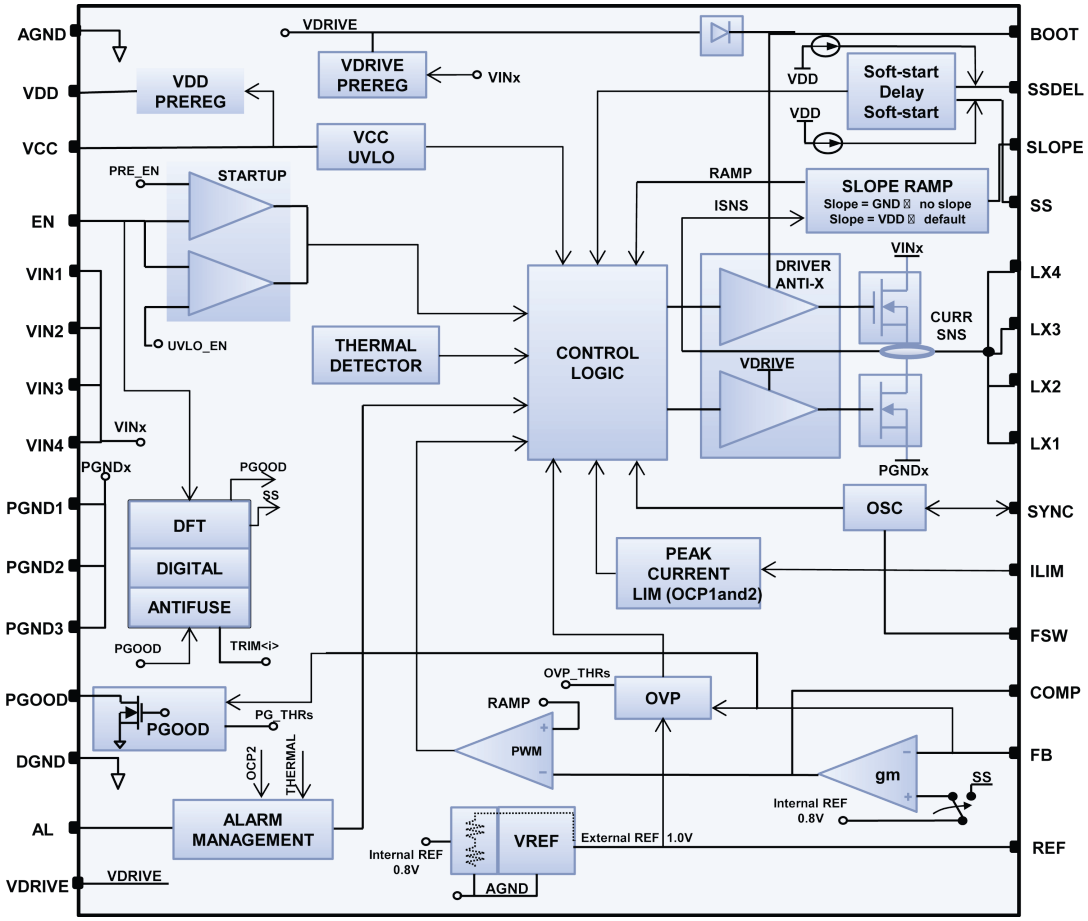
The RHRPMPOL01 is a single phase, step-down monolithic switching regulator with high precision internal voltage reference and integrated power MOSFETs for synchronous conversion. The device has been developed using SOI technology that offers good performance against SEL effect.

The regulator converts 3.0 V to 12 V input voltage to 0.8 V to ($0.85xV_{IN}$) output voltage. It has been designed to supply FPGA, DSP, MCU and ASICS in general for space applications.

The controller is based on peak current mode architecture, which ensures a fast load transient response and very stable switching frequency. An embedded integrator compensates the DC voltage error due to the output voltage ripple. The fault management consists of not-latched output overvoltage protection, overcurrent protection and auto recovery thermal protection.

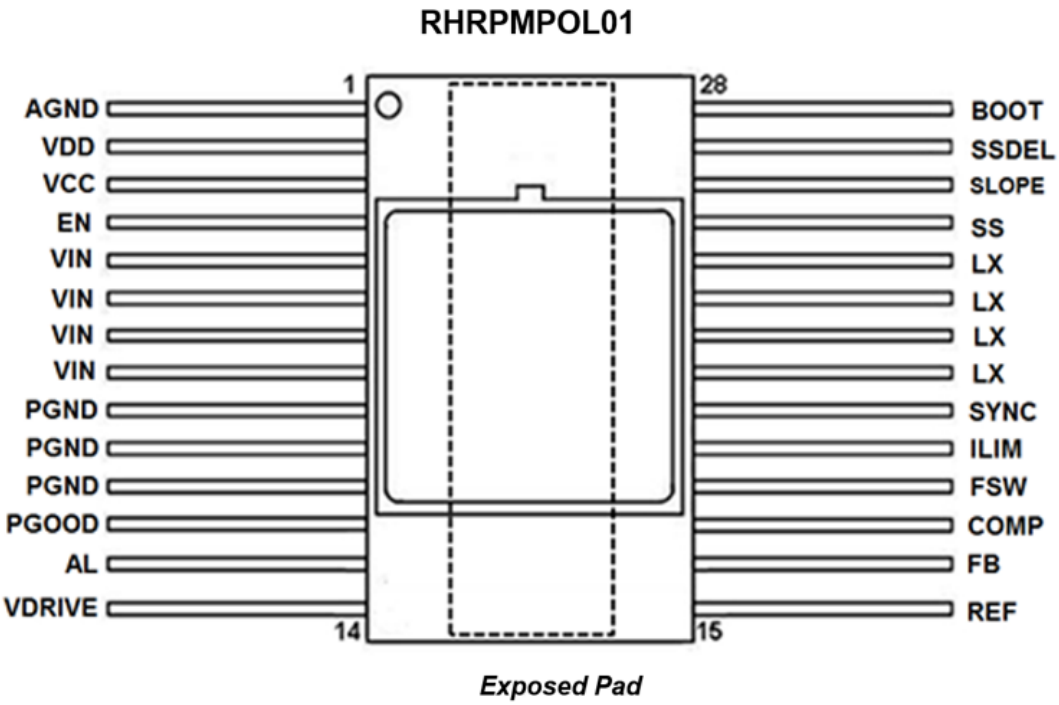
1 Device block diagram

Figure 1. **Block diagram**



2 Pinout and pin description

Figure 2. **Pinout (top view)**



2.1 Pin description

Table 1. Pin description

#	Name	I/O	Description
1	AGND/DGND	-	Signal ground. This is the ground for IC control loop, bias and internal voltage reference. Connect to PCB ground plane through multiple vias.
2	VDD	I/O	IC internal supply output. Bypass to GND with a 1 µF ceramic capacitor. Maximum load allowed on this pin is 100 µA. No current injection is allowed.
3	VCC	I	Filtered input power for control circuitry. Filter and bypass to GND with 4.7 Ω -1 µF R-C network.
4	EN	I	Enable pin, active high.
5,6,7,8	VIN	I	Power supply input. Bypass to PGND close to the IC package with capacitors with a low ESR (MLCC 3x47 µF + 2x10 µF is suggested).
9, 10,11	PGND	-	Power ground. This is the reference ground for internal power MOSFETs driver and V_{IN} input rail. Connect to PCB ground plane through multiple vias.
12	PGOOD	O	Power Good signal, open drain. Pulled-up to V_{IN} or lower rail. This pin goes to high state if V_{OUT} stays inside +/-10% of target output voltage.
13	AL	I/O	Alarm pin, Bypassing to GND with a capacitor provides timing alarm window proportional to capacitor value.
14	VDRIVE	O	Internal generated and filtered rail for power MOS driver supply of the low-side and the high-side through bootstrap capacitor. One external capacitor (1 µF) is required. Maximum load allowed on this pin is 100 µA. No current injection is allowed.
15	REF	I/O	Control loop voltage reference. Bypass to GND with a ceramic capacitor (1 µF). Maximum load allowed on this pin is 100 µA. No current injection is allowed.
16	FB	I	Remote sensing input pin. Connect to the central tap of a resistor divider between VOUT and GND in order to program the output voltage level. Maximum load/sink allowed on this pin is 1 µA.
17	COMP	I/O	Loop compensation pin. Connect to GND through an R-C network, for loop compensation.
18	FSW	I/O	Switching frequency programming pin. Connect FSW to GND through a resistor R_{FSW} (and optional capacitor < 1 nF for filtering purpose). Connect to GND for slave mode operation (refer to SYNC pin description). Pull-up to VDD or higher rail (3.6 V max.) to set default frequency (500 kHz).
19	ILIM	I/O	First and second level current limit thresholds programming. I_{LIM1} and I_{LIM2} can be adjusted through a single resistor. Connect I_{LIM} to GND through a resistor to program a current limit I_{LIM1} lower than 10 A and I_{LIM2} = (1.3* I_{LIM1}). An optional capacitor < 1 nF can be connected for filtering purpose in parallel to resistor. Pull-up to VDD or higher rail (3.6 V max.) for I_{LIM1} =10 A and I_{LIM2} = 13 A (typ.).
20	SYNC	I/O	Synchronization clock input (slave mode) or output (master mode) for 2 ICs synchronization. Max. allowed capacitive load (equivalent) for slave devices is 150 pF.
21, 22, 23, 24	LX	I/O	Regulator switching node. Connect directly to the inductor.
25	SS	I/O	Soft-start programming pin. Connect to GND through a ceramic capacitor in order to program the proper turn-on timing.
26	SLOPE		Current sensing additional ramp programming.

#	Name	I/O	Description
			Connect to GND through a resistor (and capacitor < 1 nF for filtering purpose) for control loop compensation tuning. Pull-up to VDD or higher rail (3.6 V max.) to enable the internal default slope compensation.
27	SSDEL	I/O	Soft-start delay programming pin. A capacitor must be connected between this pin and GND to program the switching regulator turn-on delay.
28	BOOT	I/O	Bootstrap pin. It provides power supply for the floating high-side driver. Connect to LX through a bootstrap capacitor (100 nF suggested).
EP	EP	-	Exposed pad. Connect to GND plane to improve thermal dissipation. Maximum voltage between this pin and PGND must be lower than +/- 50 V in any operating conditions.
Lid	Lid		Connected to PGND.

3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{JMAX}	Absolute maximum junction temperature	175	°C
V_{DD}	Internal supply voltage	AGND - 0.3 to AGND + 3.6	V
V_{CC}	Analog supply voltage	AGND - 0.3 to AGND + 15	
V_{IN}	Power supply voltage	PGND - 0.3 to PGND + 15	
V_{DRIVE}	Power MOS driver supply voltage	AGND - 0.3 to AGND + 3.6	V
EN , SYNC, SS, SSDEL,SLOPE,ILIM,FSW, COMP, AL,FB	Signal pins	AGND - 0.3 to AGND + 3.6	V
V_{BOOT}	Boot pin voltage (V_{BOOT}-V_{LX})	PGND - 0.3 to PGND + 18	V
V_{LX}	Switching node	PGND - 0.3 to VIN + 0.3	V
V_{PG}	Power Good pin voltage	AGND - 0.3 to VCC + 0.3	V
V_{REF}	Reference voltage	AGND - 0.3 to AGND + 3.6	V

3.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{Th,J-EP}$	Thermal resistance between junction and case (exposed pad)	3.4	°C/W
$R_{Th,J-A}$	Thermal resistance between junction and ambient pad	12.3	
T_{AMB}	Operating ambient temperature range	-55 to +125	°C

Note: The $R_{Th,J-A}$ is defined and obtained by simulation as per JEDEC specification JESD51.

3.2 Recommended operating conditions

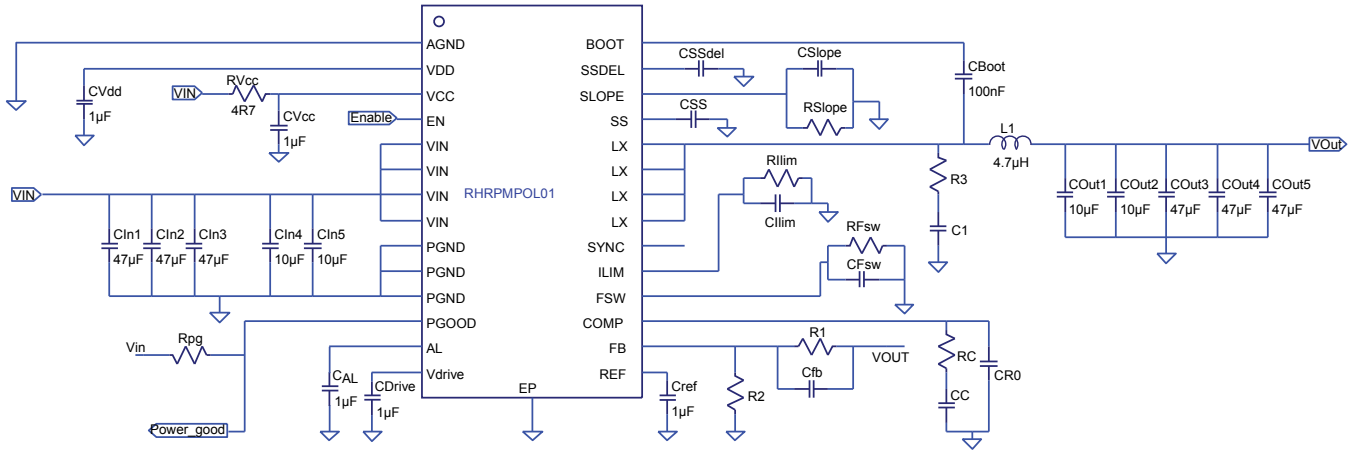
Table 4. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{IN}, V_{CC}	Input voltage range	3.0		12	V
V_{FSW}	Default frequency mode		VDD		V
	Slave mode		GND		V
R_{FSW}	Programmed frequency mode	50		500	kΩ
V_{SLOPE}	Default slope compensation		VDD		V
P	Dissipated power			3	W
I_{OUT}	Output current			7	A
T_{amb}	Operating ambient temperature	-55		125	°C
F_{SW}	Switching frequency	100		1000	kHz

Note: No electrical parameter is guaranteed for V_{CC} < 3 V.

4 Application circuit

Figure 3. **Typical application circuit**



4.1 Output voltage setting

The output voltage of the device is set by an external resistor divider that must be connected between VOUT and GND. The middle point of the divider must be connected to FB. Use Eq. (1) and Eq. (2) to calculate the output voltage and the resistor value.

$$VOUT = VFB \times \left(\frac{R1 + R2}{R2}\right) \quad (1)$$

$$R1 = R2 \times \left(\frac{VOUT}{VFB} - 1\right) \quad (2)$$

To obtain a better output voltage accuracy it is recommended to use low tolerance resistors (eg: 1%).

4.2 Inductor selection

The inductor value is calculated through the Eq. (3) and it is determined by operating frequency, input voltage, output voltage, and inductor ripple current. The amplitude of the inductor ripple current is typically set between 20% - 40% of the maximum output current. The inductor ripple current is filtered by the output capacitor, therefore COUT must be selected to have a rated ripple current equal to or greater than the ripple current of the inductor.

A high inductor value results in a lower ripple current and therefore has a better efficiency, but has a slower transient response; a reduced inductor value results in a higher ripple current and therefore has a lower efficiency, but has a faster transient response.

$$LMIN = \frac{VOUT \times (VIN - MAX - VOUT)}{VIN - MAX \times fsw \times \Delta IL} \quad (3)$$

Whereas that the duty cycle is $D=V_{OUT}/V_{IN}$.

$$LMIN = \frac{VOUT \times (1 - D)}{fsw \times \Delta IL} \quad (4)$$

$$\Delta IL = \frac{VOUT \times (VIN - MAX - VOUT)}{VIN - MAX \times fsw \times LMIN} \quad (5)$$

The peak inductor current is calculated as follows:

$$ILPEAK = IOUT + \frac{\Delta IL}{2} \quad (6)$$

The RMS inductor current is calculated by the eqaution below:

$$ILRMS = \sqrt{IOUT^2 + \frac{\Delta IL^2}{12}} \quad (7)$$

4.3 Input capacitor selection

The selection of the input capacitor affects the value of the input ripple voltage caused to the switching current between Cin, high-side and low-side. The input capacitor must be placed as close as possible to the power supply pins.

The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor must also have a ripple current rating greater than the maximum input current ripple value calculated from the Eq. (8).

$$ICIN - RMS = IOUT \times \sqrt{\frac{VOUT}{VIN - MIN} \times \frac{(VIN - MIN - VOUT)}{VIN - MIN}} \quad (8)$$

$$ICIN - RMS = IOUT \times \sqrt{D \times (1 - D)} \quad (9)$$

The worst case occurs at D = 50% (i.e. V_{IN} = 2 x V_{OUT}), which yields:

$$ICIN - RMS = \frac{IOUT}{2} \quad (10)$$

The input capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across the capacitor increases. The input voltage ripple can be calculated using Eq. (11) :

$$CIN - MIN \ = IOUT\_MAX \times \left(\frac{D \times (1 - D)}{\Delta VIN\_ripple \times fsw}\right) \quad (11)$$

The maximum ripple voltage occurs at D = 50% duty cycle and is calculated by Eq. (12):

$$\Delta VIN\_ripple = \frac{IOUT - MAX}{4 \times CIN\_MIN \times fsw} \quad (12)$$

5 Electrical characteristics

Pre-radiation

Unless otherwise specified, $T_J = T_A = 25$ °C, $V_{IN} = V_{CC} = 5$ V, $V_{OUT} = 2.5$ V, $I_{OUT} = 3$ A, $F_{SW} = 500$ kHz, $C_{IN} = C_{OUT} = 3$ x 47 µF ceramic low ESR + 2 x 10 µF ceramic low ESR, L = 4.7 µH, pre-radiation.

Temperature drift not tested in production, guaranteed by design and characterization. The temperature drift refers to the measured value on the sample at $T_A = 25$ °C.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply collection						
V_{FB}(1)	Feedback voltage			0.8		V
	Initial accuracy		-1		+1	%
	Temperature drift	-55 °C < T_J < +125 °C	-1.25		+1	%
I_Q	I_{VCC}+I_{VIN} quiescent current	EN = 1 V (no switching)	2.5	3.5	4.5	mA
I_{SHDN}	I_{VCC}+I_{VIN} shutdown current	EN = GND	250	400	550	µA
V_{CC_UVLO}	VCC undervoltage lockout upper threshold	Rising edge, device disabled below this level	2.65	2.85	3.05	V
	VCC undervoltage lockout lower threshold	Falling edge, device enabled above this level	2.45	2.65	2.85	V
	UVLO hysteresis			200		mV
Efficiency	Power efficiency	L = 2.2 µH, DCR = 6 mΩ		92		%
Switching frequency and synchronization						
F_{SW}	Default switching frequency	Voltage on F_{SW} > 2 V		500		kHz
		Initial accuracy	-10		+10	%
		Temperature drift, -55 °C < T_J < +125 °C	-10		+12	
F_{SWP}	Programmable switching frequency	R_{FSW} connected	100		1000	kHz
		Initial accuracy, R_{FSW} = 50 kΩ	450	500	550	kHz
		Temperature drift, -55 °C < T_J < +125 °C	-10		+12	%
V_{FSW}	Voltage on FSW pin	R_{FSW} connected		1		V
V_{SYNC_HI}	Sync. HIGH input threshold	V_{FSW} < 0.1 V (slave configuration)	2.3			V
V_{SYNC_LOW}	Sync LOW input threshold				1	
V_{SYNC_OUT}	Sync output voltage high level	RFSW connected (master configuration)		VDD		V
	Sync output voltage low level				0.4(2)	V
	Sync output fan-out			1		mA
On-time						
$T_{ON,MIN}$	Minimum on-time			120		ns
Internal supply voltages, soft-start						
V_{REF}(2)(3)	Switching regulator reference voltage level			1		V
		Initial accuracy	-1		+1	%

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{REF}[(2)(3)]	Switching regulator reference voltage level	Temperature drift, -55 °C < T_J < +125 °C	-2		+2	%
I_{SSDEL}	Soft-start delay capacitor charging current		90	100	110	µA
V_{SSDEL_THR}	Soft-start delay voltage threshold	Delay time starts from EN > 0.7 V	0.9	1	1.1	V
ISS	Soft-start capacitor charging current		45	50	55	µA
V_{DD}[(3)]	Internal supply bus voltage		2.6	2.7	2.8	V
V_{DRIVE}[(3)]	Power MOS driver supply voltage		2.85	2.95	3.1	V
Current limit						
I_{LIM1}	Default first level OCP	ILIM pin to V_{DD}		10		A
	Programmed first level OCP	Initial accuracy, R_{ILIM} = 75 kOhm,	1	1.26	1.5	A
		Temperature drift, -55 °C < T_J < +125 °C	-20		+18	%
		Initial accuracy, R_{ILIM} = 33 kOhm,	2.7	3	3.3	A
		Temperature drift, -55 °C < T_J < +125 °C	-5		+5	%
I_{LIM2}	Default second level OCP	I_{LIM} pin to VDD, initial tolerance		13		A
	Programmed second level OCP	Initial accuracy, R_{ILIM} = 75 kOhm	1.32	1.66	2	A
		Temperature drift, -55 °C < T_J < +125 °C	-20		+25	%
		Initial accuracy, R_{ILIM} = 33 kOhm	3.5	3.9	4.3	A
		Temperature drift, -55 °C < T_J < +125 °C	-5		+5	%
V_{ILIM}	Voltage on ILIM pin	I_{LIM} programmed by external resistor	0.97	1	1.03	V
High-side and low-side integrated MOSFET						
$R_{DSon,HS}$	High-side MOS on-resistance	I_{OUT} = 1 A	15	25	30	mΩ
$R_{DSon,LS}$	Low-side MOS on-resistance	I_{OUT} = 1A	15	25	35	mΩ
Overvoltage protection and Power Good signal						
$V_{OVP,TH}$	OVP threshold	Initial accuracy, referred to V_{FB} = 0.8 V	0.98	1	1.02	V
	OVP reset threshold		0.82	0.85	0.88	
	OVP threshold	Temperature drift, -55 °C < T_J < +125 °C	-17		+5	%
	OVP reset threshold		-6.0		+18	
V_{PGOOD}	Upper rising threshold	Referred to V_{FB} = 0.8 V	106	110	115	%
	Lower falling threshold		88	90	96	
	Output voltage low level	Open drain, I_{PGOOD} = 5 mA			0.6	V
Overtemperature protection (OVP)						
T_{OTP}	Shutdown temperature			155		°C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{OTP}	Hysteresis			20		°C
Alarm pin (AL)						
I_{AL}	Alarm pin source/sink current	Device in fault condition		20		µA
Enable and UVLO						
PRE_EN	Pre-enable rising threshold	Device turned ON, but not switching	0.67	0.7	0.73	V
	Pre-enable rising threshold hysteresis		0.08	0.1	0.12	
UVLO_EN	UVLO enable HIGH threshold(4)	Device switching	1.18	1.24	1.3	
	UVLO enable hysteresis		0.1	0.2	0.3	
Slope compensation						
Slope_Comp	Voltage slope	Initial accuracy, R_{SLOPE} = 12 kOhm, F_{SW} = 500 kHz	225	250	275	mV/µs
		Temperature drift, -55 °C < T_J < +125 °C	-18		+32	%
V_{SLOPE}	Voltage at SLOPE pin	Slope programmed by external resistor		0.8		V
Error amplifier(2)(4)						
V_{INOFF}	Input offset	F_{SW}= 500 kHz		0.3		mV
TC_{EA}	Trans conductance	V_{COMP} = 1.35 V		0.94		mS
DCG_{EA}	DC gain	V_{FB} = 0.8 V		72		dB
I_{EA_OUT}	Output source/sink current	V_{COMP} = 1.35 V, 100 mV overdrive		220		µA
Interleaving						
I_{MATCH} (2)	Current mismatch between master and slave ICs				10	%

1. *Trimmable by the user. Please contact STMicroelectronics for the trimming procedure.*
2. *Guaranteed by design and characterization. Not tested in production.*
3. *Maximum load allowed on this pin is 100 µA. No current injection is allowed.*
4. *More information about parameter variation can be provided upon request.*

Post-radiation

After 100k Rad (Si).

Unless otherwise specified, $T_J = T_A = 25$ °C, $V_{IN} = V_{CC} = 5$ V, $V_{OUT} = 2.5$ V, $I_{OUT} = 3$ A, $F_{SW} = 500$ kHz, $C_{IN} = C_{OUT} = 3$ x 47 µF ceramic low ESR + 2 x 10 µF ceramic low ESR, L = 4.7 µH.

Table 6. Post radiation electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply section						
V_{FB}(1)	Feedback voltage			0.8		V
	Accuracy		-1		+1	%
I_Q	I_{VCC} + I_{VIN} quiescent current	EN = 1 V (no switching)	2.5	3.5	4.5	mA
I_{SHDN}	I_{VCC} + I_{VIN} shutdown current	EN = GND	250	400	550	µA
V_{CC_UVLO}	VCC undervoltage lockout upper threshold	Rising edge, device disabled below this level	2.65	2.85	3.05	V
	VCC undervoltage lockout lower threshold	Falling edge, device enabled above this level	2.45	2.65	2.85	V
	UVLO hysteresis			200		mV
Efficiency	Power efficiency	L = 2.2 µH, DCR = 6 mΩ		92		%
Switching frequency and synchronization						
F_{SW}	Default switching frequency	Voltage on F_{SW} > 2 V		500		kHz
		Accuracy	-10		+10	%
F_{SWP}	Programmable switching frequency	R_{FSW} connected	100		1000	kHz
		Accuracy, R_{FSW} = 50 kΩ	450	500	550	kHz
V_{FSW}	Voltage on FSW pin	R_{FSW} connected		1		V
V_{SYNC_HI}	Sync. HIGH input threshold	V_{FSW} < 0.1 V (slave configuration)	2.3			V
V_{SYNC_LOW}	Sync. LOW input threshold				1	
V_{SYNC_OUT}	Sync. output voltage high level	R_{FSW} connected (master configuration)		VDD		V
	Sync. output voltage low level				0.4(2)	V
	Sync. output fan-out			1		mA
On-time						
$T_{ON,MIN}$	Minimum on-time			120		ns
Internal supply voltages, soft-start						
V_{REF}(2)(3)	Switching regulator reference voltage level	Accuracy	0.984	1	1.016	V
I_{SSDEL}	Soft-start delay capacitor charging current		90	100	130	µA
V_{SSDEL_THR}	Soft-start delay voltage threshold	Delay time starts from EN > 0.7 V	0.9	1	1.1	V
I_{SS}	Soft-start capacitor charging current		45	50	66	µA
V_{DD}(3)	Internal supply bus voltage		2.6	2.7	2.8	V
V_{DRIVE}(3)	Power MOS driver supply voltage		2.85	2.95	3.1	V
Current limit						

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIM1}	Default first level OCP	ILIM pin to V_{DD}		10		A
	Programmed first level OCP	Accuracy, R_{ILIM} = 75 kOhm,	0.8	1.26	1.5	A
		Accuracy R_{ILIM} = 33 kOhm,	2.7	3	3.3	A
I_{LIM2}	Default second level OCP	I_{LIM} pin to VDD, initial tolerance		13		A
	Programmed second level OCP	Accuracy[4], R_{ILIM} = 75 kOhm,	1.05	1.66	2	A
		Accuracy, R_{ILIM} = 33 kOhm,	3.5	3.9	4.3	A
V_{ILIM}	Voltage on ILIM pin	I_{LIM} programmed by external resistor	0.97	1	1.03	V
High-side and low-side integrated MOSFET						
$R_{DSon,HS}$	High-side MOS on-resistance	I_{OUT} = 1 A	15	25	30	mΩ
$R_{DSon,LS}$	Low-side MOS on-resistance	I_{OUT} = 1A	15	25	35	mΩ
Overvoltage protection and Power Good signal						
$V_{OVP,TH}$	OVP threshold	Accuracy, referred to V_{FB} = 0.8 V	0.97	1	1.02	V
	OVP reset threshold		0.82	0.85	1.00	
V_{PGOOD}	Upper rising threshold	Referred to V_{FB} = 0.8 V	106	110	115	%
	Lower falling threshold		88	90	98	
	Output voltage low level	Open drain, I_{PGOOD} = 5 mA			0.6	V
Overtemperature protection (OVP)						
T_{OTP}	Shutdown temperature			155		°C
	Hysteresis			20		
Alarm pin (AL)						
I_{AL}	Alarm pin source/sink current	Device in fault condition		20		µA
Enable and UVLO						
PRE_EN	Pre-enable rising threshold	Device turned ON, but not switching	0.67	0.7	0.74	V
	Pre-enable rising threshold hysteresis		0.08	0.1	0.13	
UVLO_EN	UVLO enable HIGH threshold[4]	Device switching	1.18	1.24	1.3	
	UVLO enable hysteresis		0.1	0.2	0.3	
Slope compensation						
Slope_Comp	Voltage slope	Accuracy, R_{SLOPE} = 12 kOhm, F_{SW} = 500 kHz	225	250	275	mV/µs
V_{SLOPE}	Voltage on SLOPE pin	Slope programmed by external resistor		0.8		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Error amplifier[2][4]						
V_{INOFF}	Input offset	F_{SW}= 500 kHz		0.3		mV
TC_{EA}	Trans conductance	V_{COMP} = 1.35 V		0.94		mS
DCG_{EA}	DC gain	V_{FB} = 0.8 V		72		dB
I_{EA_OUT}	Output source/sink current	V_{COMP} = 1.35 V, 100 mV overdrive		220		µA
Interleaving						
I_{MATCH} [2]	Current mismatch between master and slave ICs				10	%

1. *Trimmable by the user. Please contact STMicroelectronics for the trimming procedure.*
2. *Guaranteed by design and characterization. Not tested in production.*
3. *Maximum load allowed on this pin is 100 µA. No current injection is allowed.*
4. *More information about parameter variation can be provided upon request.*

6 Radiations

6.1 Total ionizing dose (MIL-STD-883 test method 1019)

The RHRPMPOL01 is RHA QML-V qualified, tested and characterized in full compliance with the MIL-STD-883 specification, both below 10 mrad/s (low dose rate) and between 50 and 300 rad/s (high dose rate).

- Testing is performed in accordance with MIL-PRF-38535 and the test method 1019 of the MIL-STD-883 for total ionizing dose (TID)
- ELDRS characterization is performed in qualification only on both biased and unbiased parts, on a sample of minimum twenty units from two different wafer lots
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Table 7. TID test results

Type	Conditions	Value	Unit
TID	50 rad(Si)/s high dose rate up to Compliance with electrical specification	100	krad
	10 mrad (Si)/s low dose rate up to Compliance with electrical specification	100	
	ELDRS free up to Compliance with electrical specification	100	

6.2 Single event effect

The behavior of the product when submitted to heavy ions is not tested in production. Heavy Ions trials are performed on qualification lots only.

Table 8. Test results

Parameter	Conditions	Value	Unit
SEL /SEB linear energy transfer (LET)	No latch-up / snapback events found w/ VCC up to 7 V	86.1	MeV.cm2/mg
SET: linear energy transfer threshold (LETth)	25 °C	Characterized	MeV.cm2/mg

6.2.1 Single event upset and single event functional interrupt

During the different test sessions performed at RADFE, a certain sensitivity to SEU (pin AL) and SEFI has been observed.

In order to better explore these phenomenon and their impact on device applicative behavior FIT was calculated on the worst data points for the three different configurations used under irradiation and worstcase assumptions for the device (i.e. only one sensitive volume of 2 mm thickness). Here below are reported therates for GEO GCR in solar minimum activity and 1 g/cm2 of Al shielding:

SEU on pin AL: 1 event every ~127 years (avg)

SEFI: 1 event every ~836 years (avg)

6.2.2 Proton test

In addition, a proton test session has been also performed as complementary test for a full characterization of the RHRPMPOL01 device in a hardness environment. In fact, because of proton abundance in space, ut represents a significant SEE threat. Even if proton interaction with the silicon electrons is weak, due to the fact they have a single charge, (i.e. generally they do not contribute to SEEs by direct ionization, having small LETs), indeed high energy protons interact with the silicon nuclei producing secondary particles with larger masses and higher LETs.

These secondary particles can have LETs up to about 15 MeV.cm2/mg in silicon, which may cause SEUs. Due to the fact the RHRPMPOL01 device showed to be a bit sensitive to ions with high LET value, it seemed reasonable to have them tested for proton SEE sensitivity especially in the range of LETth ≤ 15 MeV.cm2/mg, as space is dominated by protons.

The proton test session was performed at Paul Scherrer Institute (PSI) facility, Villigen (Switzerland) in June 2019, in accordance with both MIL-PRF-38535 andESCC25100 specification. Since LET value is not a well-defined number for the group of secondary particles emitted by the silicon nucleus, a better metric used was the proton energy, whose range went from 50 MeV to 200 MeV (with 50 MeV step). Used flux values were from 1 E6p+/cm2.s to 1 E8p+/cm2.s.

Results of proton test was positive, the RHRPMPOL01 device did not show any sensitivity to protons.

7 The device description

The RHRPMPOL01 is a radiation hardened and SEE hardened high efficiency synchronous step-down monolithic switching regulator capable of delivering up to 7 A continuous output current.

The power input voltage (V_{IN}) can range from 3 V to 12 V and, thanks to a 0.8 V internal voltage reference, the RHRPMPOL01 can precisely regulate the output voltage in the range of 0.8 V to 85% of V_{IN}.

Low $R_{DS(on)}$ N-channel MOSFETs for both HS (high-side) and LS (low-side) and also the boot diode are embedded, for minimum external component requirement.

The peak current mode control loop, with a high bandwidth error amplifier and an external compensation, enables a stable operation with a wide range of output filter configurations (including MLCC solutions) ensuring a fast response to load transient. For maximum design flexibility, all the most important features are programmable.

The RHRPMPOL01 features a full set of protections and output voltage monitoring:

- Programmable and accurate dual level overcurrent protection (internally compensated against temperature variations)
- Overvoltage protection (not latched)
- Overtemperature protection (latched after 16 consecutive fault events)
- Undervoltage lockout on input supply rail
- Power Good open drain output, which provides real-time information about the output voltage

When connecting two RHRPMPOL01 through the SYNC pin, they can be synchronized each other with 180 ° phase shift switching interleaving, reducing RMS current absorption from the input filter and preventing from beating frequency noise, therefore allowing a reduction in the size and cost of the input filter.

For higher output current requirements, two RHRPMPOL01 can be connected in current share configuration, providing up to 14 A.

The dedicated enable pin (EN), the programmable soft-start duration and delay offer easy control on the power sequencing and inrush current.

The RHRPMPOL01 is provided in a FLAT-28 lead ceramic package.

7.1 Power section

The RHRPMPOL01 integrates two low on-resistance N-channel MOSFETs as low-side and high-side switches, optimized for fast switching transition and high efficiency over all the load range. The power stage is designed to deliver a continuous output current up to 7 A.

The high-side MOSFET drain is connected to the VIN pins (power input), the low-side MOSFET source is connected to the PGND pins (power ground); high-side MOSFET source and low-side MOSFET drain are connected together and to the LX pins (see Figure 1. Block diagram). The driving section is supplied by VIN pins through the internal voltage regulator (VDRIVE) that assures the proper driving voltage over all the supply range.

The following suggestions are very important for proper design of the power section:

- Bypass VIN pins to PGND pins as close as possible to the IC package with high quality MLCC capacitors
- Connect the bootstrap capacitor (typically a 100 nF ceramic capacitor rated to stand V_{IN} voltage) from the BOOT pin to the LX pin to supply the HS driver
- Do not connect an external bootstrap diode. The IC already integrates a bootstrap diode to charge the bootstrap capacitor, saving the cost of this external component

The RHRPMPOL01 embodies an anti-shoot-through and adaptive dead-time control to minimize the conduction time of low-side body diode and consequently reduce power losses.

When the voltage at the LX pin drops (to check high-side MOSFET turn-off), the LS MOSFET is suddenly switched ON.

When the gate driving voltage of LS drops (to check low-side MOSFET turn-off), the HS MOSFET is suddenly switched ON.

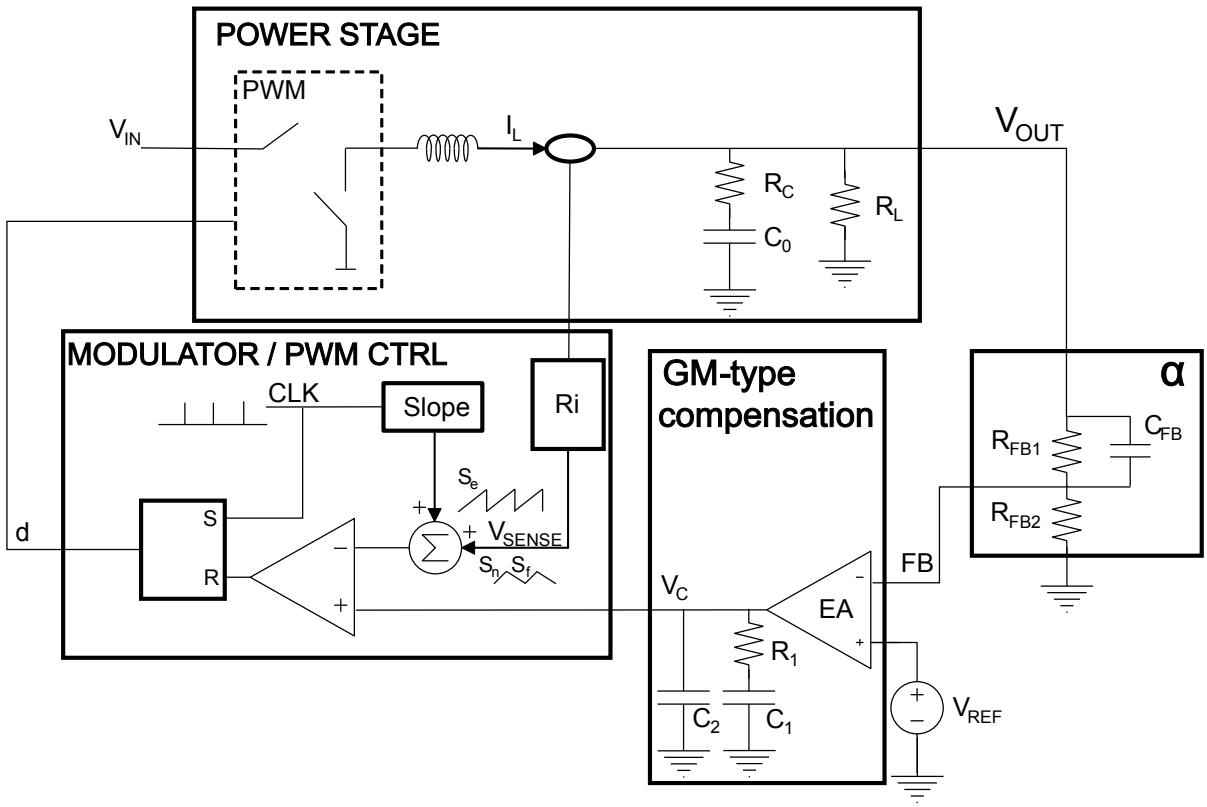
The device is able to regulate even if the current is negative (full PWM).

In fact, if the current flowing in the inductor is negative, voltage on the LX pin never drops. A watchdog controller is implemented to allow the LS MOSFET to turn on even in this case.

7.2 Control loop

The RHRPMPOL01 is a constant-frequency peak current-mode switching regulator as shown below.

Figure 4. Peak current mode control loop model



It employs two control loops: an external loop to control the output voltage and an inner loop to control the peak current which flows through the coil. The external loop (or voltage loop) compares the feedback voltage V_{FB} with the internally generated precise reference voltage at 0.8V through the error amplifier GM. The error amplifier is a trans-conductance amplifier (OTA) that multiplies the difference of input voltage by a certain gain and generates a current into the output node V_C (pin COMP). The external compensation circuit, RC network tied between V_C and ground, converts the current generated by the error amplifier into a voltage. Into the inner loop (or current loop), the current sense circuit converts the current flowing through the coil into a sense voltage V_{SENSE} with gain factor R_i (0.1 Ω). The voltages V_C and V_{SENSE} are compared by a PWM comparator and a pulse width modulated (PWM) signal is generated, defining the duty cycle *d*. The power stage can be seen as a controlled current generator which provides the current I_L to the power stage output capacitor and load. Finally, voltage ramp S_e, programmable by the external R_{SLOPE} resistor, is added to the V_{SENSE} signal to stabilize the converter in case of duty cycle greater than 50% operation.

The control-to-output equivalent transfer function is described in equation below:

$$F(s) = \frac{V_0(s)}{V_C(s)} = \frac{R_L}{R_i} \cdot \frac{(sC_0R_C + 1)}{sC_0(R_C + R_L) + 1} \quad (13)$$

where C_0 and R_C are the output capacitance and its equivalent series resistance and *Ro* represents the output load.

In order to obtain the typical integrative loop transfer function, the signal stage must compensate for the power stage pole (due to the output capacitor and the load) and zero (above the loop bandwidth if ceramic output capacitors are selected). The signal stage transfer function is shown by the equation below:

$$G(s) = \alpha g_m R_{OUT} = \frac{(1 + R_1 C_1 s)}{(1 + R_{OUT} C_1 s)(1 + R_1 C_2 s)} \quad (14)$$

where

- g_m is small signal gains of trans-conductance stage
- α is the gain due to the output resistor divider (V_{REF} / V_{OUT})
- R_{OUT} is the output impedance of the amplifier (R_{OUT} ≈ 4 MΩ)

Eq. (14) is calculated assuming C_1 >> C_2 and R_{OUT} >> R_1.

The external compensation network (R_1, C_1 and C_2) must be designed in order to obtain:

- One zero, matching the power stage pole (equation below)

$$C_1 R_1 = C_0 (R_L + R_C) \quad (15)$$

- One pole in order to delete the static output voltage error
- One pole, if necessary, matching the high frequency zero due to the output capacitor ESR, R_C (see the equation below)

$$C_2 R_1 = C_0 R_C \quad (16)$$

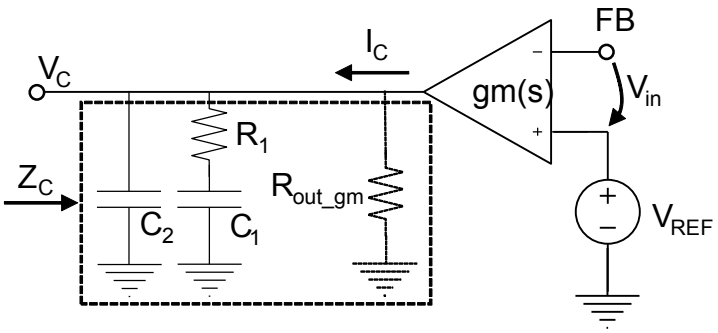
The resulting control loop transfer function is the product of G(s) by F(s):

$$G_{LOOP}(s) = F(s)G(s) = \alpha g_m R_{OUT} \frac{R_L}{R_i} \frac{(1 + R_1 C_1 s)}{(1 + R_{OUT} C_1 s)(1 + R_1 C_2 s)} \frac{(1 + R_C C_O s)}{1 + (R_C + R_L) C_O s} \quad (17)$$

This model provides good results if the control loop bandwidth is lower than about F_{SW}/10.

The error amplifier can be modeled as shown in the figure below.

Figure 5. Simplified model of the error amplifier



It provides an output current I_C proportional to the trans-conductance gm and the input differential voltage Vin. The trans-conductance is function of the frequency. Its DC gain is given by the following formula:

$$A_v = gm \cdot R_{OUT} \quad (18)$$

where R_{OUT} is the output impedance of the amplifier (R_{OUT} ≈ 4 MΩ).

Finally, the transfer function of the error amplifier is given by the following formula:

$$\frac{V_C}{V_{in}} = gm(s) \cdot Z_C \quad (19)$$

Z_C is the equivalent impedance at the output of the error amplifier and it can be displayed as the parallel of the output impedance and the compensation network:

$$Z_C = \frac{1}{C_2 s} \parallel \left(R_1 + \frac{1}{C_1 s}\right) \parallel R_{OUT} \quad (20)$$

For simplicity, the error amplifier is supposed to have a single pole, single zero at the frequency of w_{p1} and w_{z1}. Thus, its trans-conductance can be expressed as:

$$gm(s) = gm \cdot \frac{1 + s\frac{1}{w_{z1}}}{1 + s\frac{1}{w_{p1}}} \quad (21)$$

The typical values of w_{z1} and w_{p1} are $w_{z1} \approx 2\pi \cdot 350$ k rad/s and $w_{z1} \approx 2\pi \cdot 1.6$M rad/s.

Accurate modelling of the PWM modulator up to high frequency is a must for a proper loop stability analysis. Linear time-invariant (LTI) model such as Ridley model or similar is typically used for these purposes.

7.3 Ridley modeling applied to the RHRPMPOL01

A more accurate model for stability is based on the approach suggested by Ridley for a peak current mode control scheme, it is accurate up to half of switching frequency, and it allows us to precisely estimate phase margin of the complete loop.

According to the Ridley model, an extra gain $F_h(s)$, representing the high frequency correction term of the controller transfer function, must be added to the main transfer function. Thanks to this term, the sub-harmonic oscillations that appear for duty cycle values above 50% are taken into account. This extra gain comes from second order approximation of the continuous time modeling by Ridley and is valid up to half of the switching frequency. The effect of a feed-forward capacitor in the feedback net is also taken into account into α(s).

Figure 6. Global loop transfer function

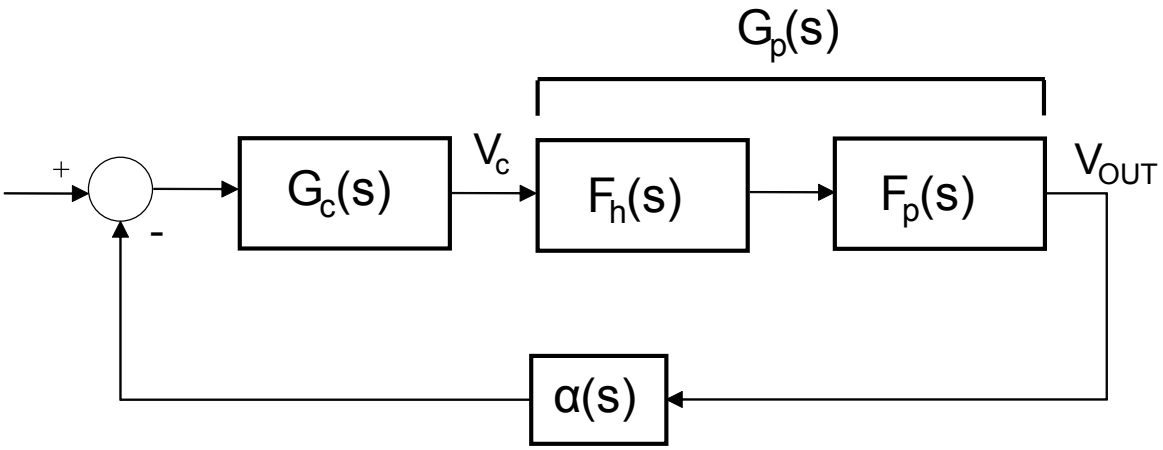


Figure 6. Global loop transfer function shows the global loop transfer function according to Ridley's modeling where:

$$G_C(s) = \frac{V_C(s)}{V_{FB}(s)} = g_m R_{OUT} \frac{1 + R_1 C_1 s}{(1 + R_{OUT} C_1 s)(1 + R_1 C_2 s)} \quad (22)$$

$$\alpha(s) = \alpha(0) \frac{1 + R_{fb1} C_{fb} s}{1 + \alpha(0) R_{fb1} C_{fb} s} \qquad \alpha(0) = \frac{R_{fb2}}{R_{fb1} + R_{fb2}} \quad (23)$$

$$F_p(s) = \frac{R_L}{R_i} \frac{1}{1 + \frac{R_L T_{SW}}{L}\left[m_c(1 - D) - 0.5\right]} \frac{1 + R_C C_O s}{1 + \frac{s}{\omega_p}} \quad (24)$$

$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}} \quad (25)$$

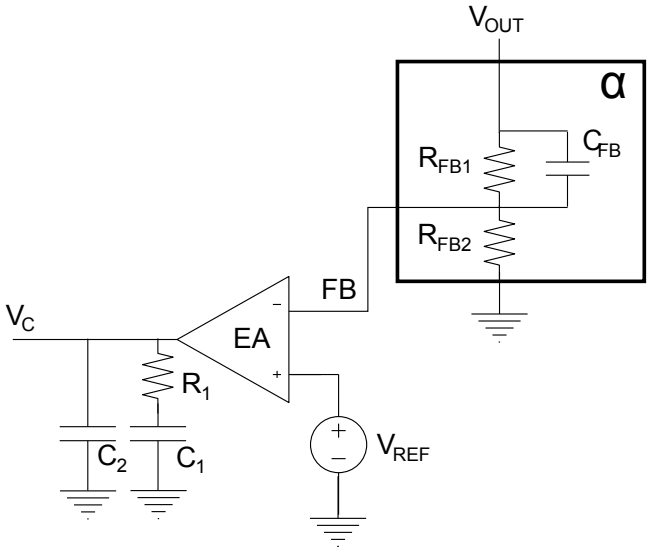
Eq. (25) is valid up to $F_{SW}/2$, high frequency correction term.

Refer to Figure 7. Feedback network with feed-forward capacitor for $R_{FB1}/R_{FB2}/C_{FB}$ configuration. The parameters m_c, ω_n, ω_p and Q_p can be calculated as follows:

$$\omega_p = \frac{1}{(R_L + R_C)C_O} + \frac{T_{SW}}{LC_O}\left[m_c(1-D) - 0.5\right]; \qquad Q_p = \frac{1}{\pi\left[m_c(1-D) - 0.5\right]};$$

$$\boldsymbol{\omega_n = \frac{\pi}{T_{SW}} = \pi f_{SW}}; \qquad \boldsymbol{m_c = 1 + \frac{S_e}{S_n} = 1 + \frac{\frac{V_{SLOPE}}{T_{SW}}}{\frac{V_{IN} - V_{OUT}}{L} R_i}} \tag{26}$$

Figure 7. Feedback network with feed-forward capacitor



The resulting complete open loop gain transfer function, accurate if C_1 >> C_2 and R_{OUT} >> R_1 up to $F_{SW}/2$, is:

$$G_{LOOP}(s) = \alpha(s)G_C(s)F_p(s)F_h(s) \tag{27}$$

$$G_{LOOP}(s) = \alpha(0)\frac{1 + R_{fb1}C_{fb}s}{1 + \alpha(0)R_{fb1}C_{fb}s} g_m R_{OUT} \frac{1 + R_1C_1s}{(1 + R_{OUT}C_1s)(1 + R_1C_2s)} \frac{R_L}{R_i} \frac{1}{1 + \frac{R_L T_{SW}}{L}[m_c(1-D) - 05]} \frac{1 + R_C C_O s}{1 + \frac{s}{\omega_p}} \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}}$$

$$G_{LOOP}(s) = G_{LOOP}(0)\frac{1 + R_{fb1}C_{fb}s}{1 + \alpha(0)R_{fb1}C_{fb}s} \frac{1 + R_1C_1s}{(1 + R_{OUT}C_1s)(1 + R_1C_2s)} \frac{1 + R_C C_O s}{1 + \frac{s}{\omega_p}} \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}} \tag{28}$$

where:

$$G_{LOOP}(0) = g_m \alpha(0) \frac{R_{OUT}R_L}{R_i} \frac{1}{1 + \frac{R_L T_{SW}}{L}[m_c(1-D) - 05]}$$

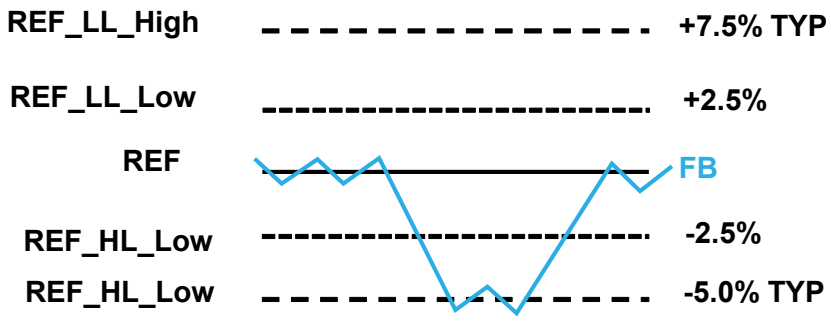
$$\alpha(0) = \frac{R_{fb2}}{R_{fb1} + R_{fb2}} \tag{29}$$

7.4 Fast load transient response

When fast load transient is applied to the output, the device is able to reacts very quickly in order to limit output voltage overshoot or undershoot. This feature is the combination of a fast error amplifier response and a proper control logic scheme that is driven by the use of two fast comparators, called HL (high load) and LL (low load).

When the FB voltage goes below the REF_HL, the HL comparator force ON-time period turning on the power switch. Typically, REF_HL level is -5% below the nominal voltage loop reference of 800 mV. HL comparator output is latched to high level voltage till overcurrent protection occurs or the output voltage goes back again the regulation voltage level. So, a proper voltage hysteresis is implemented: the comparator output goes low when the feedback goes back again to -2.5% of the regulation threshold (see figure below). If during the ON phase current limit is reached minimum OFF time period around 200 ns is applied.

Figure 8. **Fast load transient response**



Propagation delay time of the comparator has to be minimized to speed up the device reaction to a fast step load, but once ON phase is triggered, the faster is the coil ramp current slope the lower is output voltage drop. For this reason the lower inductance coil is suggested, for instance 0.8 µH is suggested.

In opposite, when the load current quickly decreases, the FB voltage can show an overshoot. The LL comparator output goes high when the FB goes above the REF_LL voltage (typically +7% above the nominal 800 mV reference) and an OFF-time is forced. The OFF-time is kept till or the FB goes again back to the hysteresis threshold (typically +2.5%) or negative inductor current threshold is reached. In fact, the device naturally works in full PWM mode, but when fast negative step loads the current on the coil can quickly go below zero. So, zero-crossing comparator, whose typical threshold of -1.5 A, is implemented to avoid the inductor coil goes deeply below zero. When the zero-crossing threshold is reached, switching activity is stopped and the power stage is forced in open loop condition (LX is in high impedance).

The two comparators are not enough to speed the loop response, but as mentioned above, also the error amplifier must be able to speed up the transient response. A fast error amplifier with dynamic bias has been designed in order to improve the load-transient response. In practice the error amplifier must be able to quickly charge or discharge the compensation capacitor (on the COMP pin) changing its output in non-linear shape at a step change in the input of the error amplifier itself. So, when one of the two comparators drives ON or OFF, time phase in parallel bandwidth and the large signal current capability (so the large signal current gain) of the error amplifier are increased as well.

Finally, this solution allows a fast load transient response with a lower output capacitance with a smaller output voltage drop.

7.5 Slope compensation

As well-known and documented in literature, the current-mode control can produce sub-harmonic oscillations when $d \geq 50\%$ (duty cycle). Any perturbation in the inductor current, due to fluctuations in the control loop, can persist if the converter works at a duty cycle greater than 50%. To overcome this issue, an additional ramp is usually added to the sensed one in order to over-dump the current loop and make the regulator stable. This feature is present in the RHRPMPOL01 for maximum design flexibility. In order to let the RHRPMPOL01 control loop work properly in case of $d \geq 50\%$, a current slope can be programmed by the user. Adding this current slope to the sensing current ramp makes the regulator stable in this condition too.

The slope compensation ramp is programmed by connecting an external R_{SLOPE} resistor between SLOPE pin and GND.

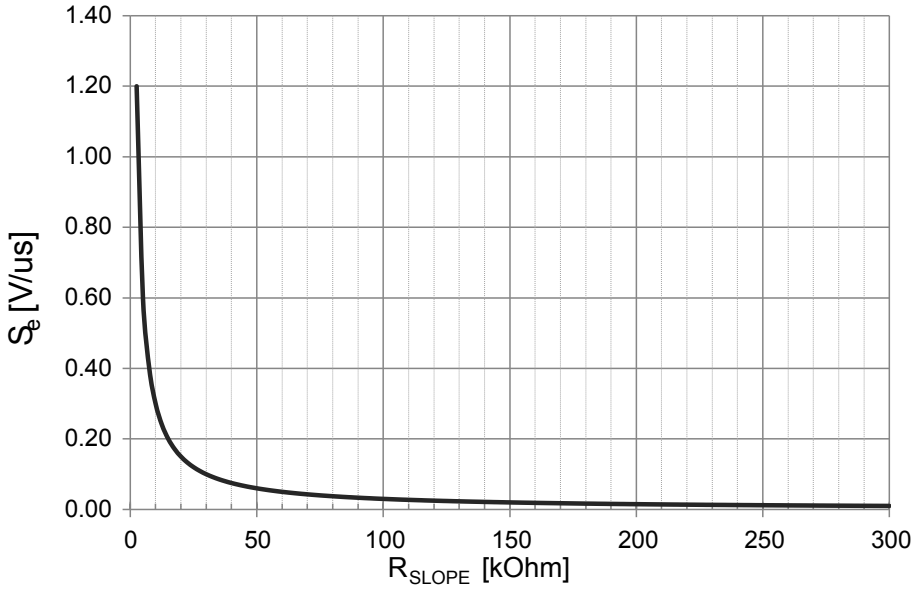
A default internal slope compensation is also implemented and it can be enabled by pulling up the voltage on SLOPE pin to VDD by a resistor or simply by a short.

A compact formula can be used to set the slope compensation ramp. If V_{SL_PK} is the peak value of the wanted voltage slope at the switching period T_S, the external resistor can be set as below:

$$R_{SLOPE} = \frac{3 \cdot 10e3 \cdot T_S[\mu s]}{V_{SL\_PK}[V]} = \frac{3 \cdot 10e3}{S_e\left[\frac{V}{\mu s}\right]} \quad (30)$$

where R_{SLOPE}, T_S and the voltage slope S_e are, respectively, expressed in kΩ, µs and Volt. Here below, for instance, a graph of the voltage slope ramp versus the SLOPE pin resistor is shown, in case of a typical frequency of 500 kHz and duty cycle supposed to be 50%.

Figure 9. **Slope compensation ramp versus R_{SLOPE}, 500 kHz, d=50%**



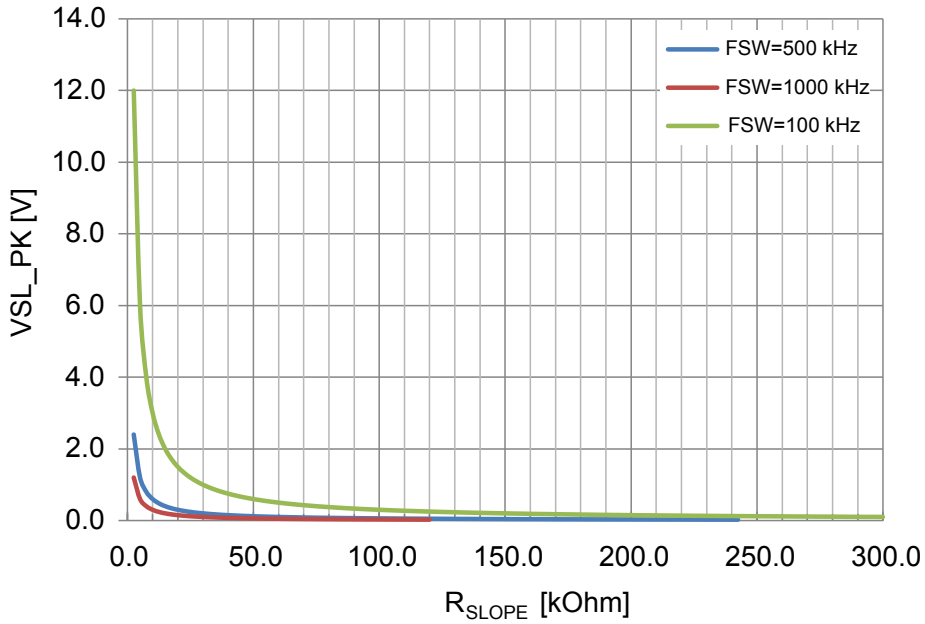
The user can, therefore, have maximum design flexibility. For instance, the following table summarizes the SLOPE pin programmability through the external resistor if the switching frequency is set from 100 kHz up to 1 MHz.

Table 9. **Slope compensation programmability**

Parameter	Description	Conditions	@ T_{amb}		Unit
Slope compensation programming			**Min.**	**Max.**	
V_SLOPE	Programmable slope peak voltage at T_s		0.1	1.2	V
R_{SLOPE}	External resistor range	F_{SW}=100 kHz	25	300	kΩ
		F_{SW}=500 kHz	5	60	
		F_{SW}= 1 MHz	2.5	30	
		F_{SW}= 100 kHz	10	120	mV/µs
Se	Programmable slope	F_{SW}=500 kHz	50	600	
		F_{SW}=1 MHz	100	1200	

Here below, for instance, a graph of the voltage slope ramp peak over the SLOPE pin resistor, for three typical frequency values and duty cycle supposed to be 50%.

Figure 10. **Slope compensation voltage peak versus R_{SLOPE}, d=50%**



Concerning the default ramp, here is a compact formula as a function of the switching frequency:

$$S_{e\_DEFAULT} = V_{SL\_PK} \cdot f_{SW} = 145e + 3 \quad (31)$$

So, in the work case of lower frequency of 100 kHz and maximum duty cycle, the maximum voltage peak on the ramp voltage due to the extra slope is supposed to be below 1.45 V.

7.6 Switching frequency programming

The regulator switching frequency can be programmed by connecting an external resistor between FSW pin and GND.

A voltage of 1 V is present on the FSW pin, so a current of 1 V/R_{FSW} is set on the resistor. This current is used to charge an internal capacitor (~20 pF). The switching frequency range of 100 kHz to 1 MHz, as summarized in the table below,R_{FSW} choice is obtained, by using the following equation:

$$f_{FSW}[MHz] = \frac{1}{2 \cdot R_{SW} \cdot 20pF} = \frac{2.5 \times 10^{10}}{R_{SW}} \quad (32)$$

If the FSW pin is connected to VDD, the external programmability is turned off and the internal default frequency, tuned at 500 kHz, is enabled. Both the programmable and the default frequency are trimmed by OTP.

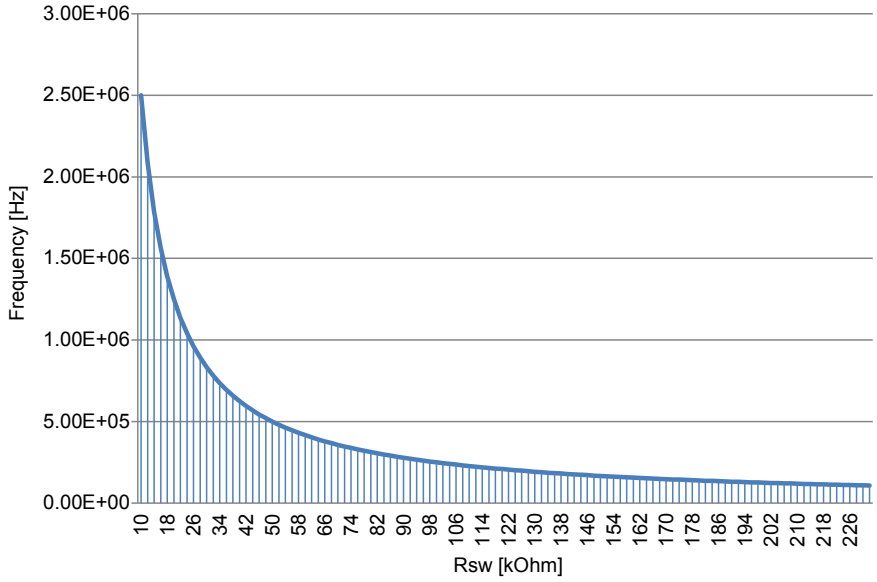
Table 10. **R_{FSW} choice**

R_{FSW} [kΩ]	F_{SW} [kHz]
50 to 500	100 to 1000
V_{FSW} = VDD	500

To set “slave mode” configuration, FSW pin must be shorted to ground (refer to for details on master/slave working mode). The internal clock is normally present to the SYNC pin with 180° phase shifting. If the device works as “MASTER”, this clock is used to synchronize other devices working as slave. In opposition, if the device is set as “SLAVE” (FSW pin shorted-to-ground) the SYNC pin is used as input pin for an external clock signal, coming, for instance, from another point of load used as master.

Here below, for instance, a graph and the equation of the programmed frequency F_{SW} over the R_{FSW} resistor connected between FSW pin and GND.

Figure 11. **Programmed switching frequency R_{FSW}**



7.7 Start-up and soft-start

The RHRPMPOL01 monitors the supply voltage on VCC pin. Once V_{CC} voltage is above the UVLO (undervoltage lockout) rising threshold, the device waits for enable pin (EN) assertion and then begins the soft-start.

The RHRPMPOL01 enable pin has two thresholds, in order to add flexibility to turn-on management:

- If the EN pin is kept below the PRE_EN rising threshold (0.7 V typ. with 100 mV hysteresis), the IC is fully off and the current consumption is typically 400 µA
- If the EN pin is forced above the UVLO_EN rising threshold (1.24 V typ. with 200 mV hysteresis) the regulator starts switching, after the SSDEL time elapses
- If the EN pin is kept between the two above mentioned thresholds, the regulator main blocks are turned on (voltage reference, bias and programming currents) and the RHRPMPOL01 is ready to turn on

The filtering capacitors, mounted among function programming pins (FSW, ILIM and SLOPE) and GND, as shown in Figure 3. Typical application circuit, have a direct impact on the IC wake-up timing.

For this reason, to be sure that the soft-start sequence starts when the function programming pin voltage is stable only, the soft-start delay has been added.

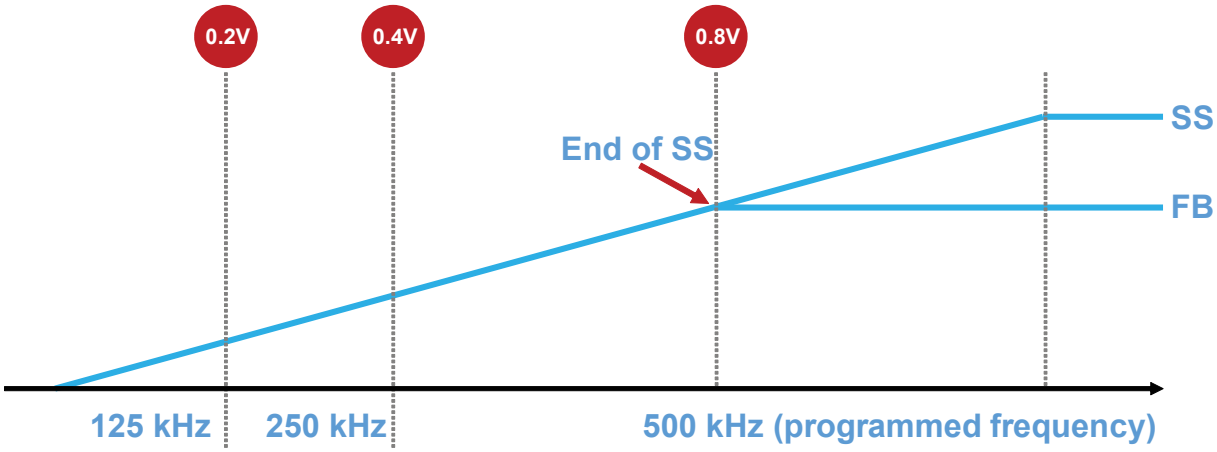
When the EN pin voltage level is above the PRE_EN threshold, a DC current (100 µA typ.) is forced on the SSDEL pin, so charging the soft-start delay capacitor connected between SSDEL and GND.

Once the input voltage supply is above the VCC_UVLO rising threshold (2.7 V typ.), EN pin is forced above UVLO_EN threshold and SSDEL has reached the threshold (1 V typ.), the RHRPMPOL01 can finally start switching.

After SSDEL pin voltage reaches 1 V, the soft-start phase begins. According with the capacitor value on SS pin, the internal loop reference increases slowly until 0.8 V, and consequently the VOUT voltage reaches the regulation value.

During start-up phase (to prevent in-rush current when the VOUT voltage is too low) two switching frequency changes are implemented. As long as SS voltage value is below 0.2 V, the switching frequency is a quarter of programmed frequency. When SS value is between 0.2 V and 0.4 V, the switching frequency is half of the programmed frequency. After SS reaches 0.4 V, the switching frequency nominally reaches the programmed one.

Figure 12. **Soft-start sequence**



The UVLO-EN threshold can also be exploited in order to program a higher VIN turn-on level. This feature is simply implemented by connecting EN pin to the central tap of a resistor divider between VIN and GND. So doing, the programmed VIN turn-on threshold is given by UVLO_EN threshold multiplied by the VIN divider ratio.

Here below the complete flow chart of start-up sequence.

Figure 13. **Flow chart of start-up sequence**

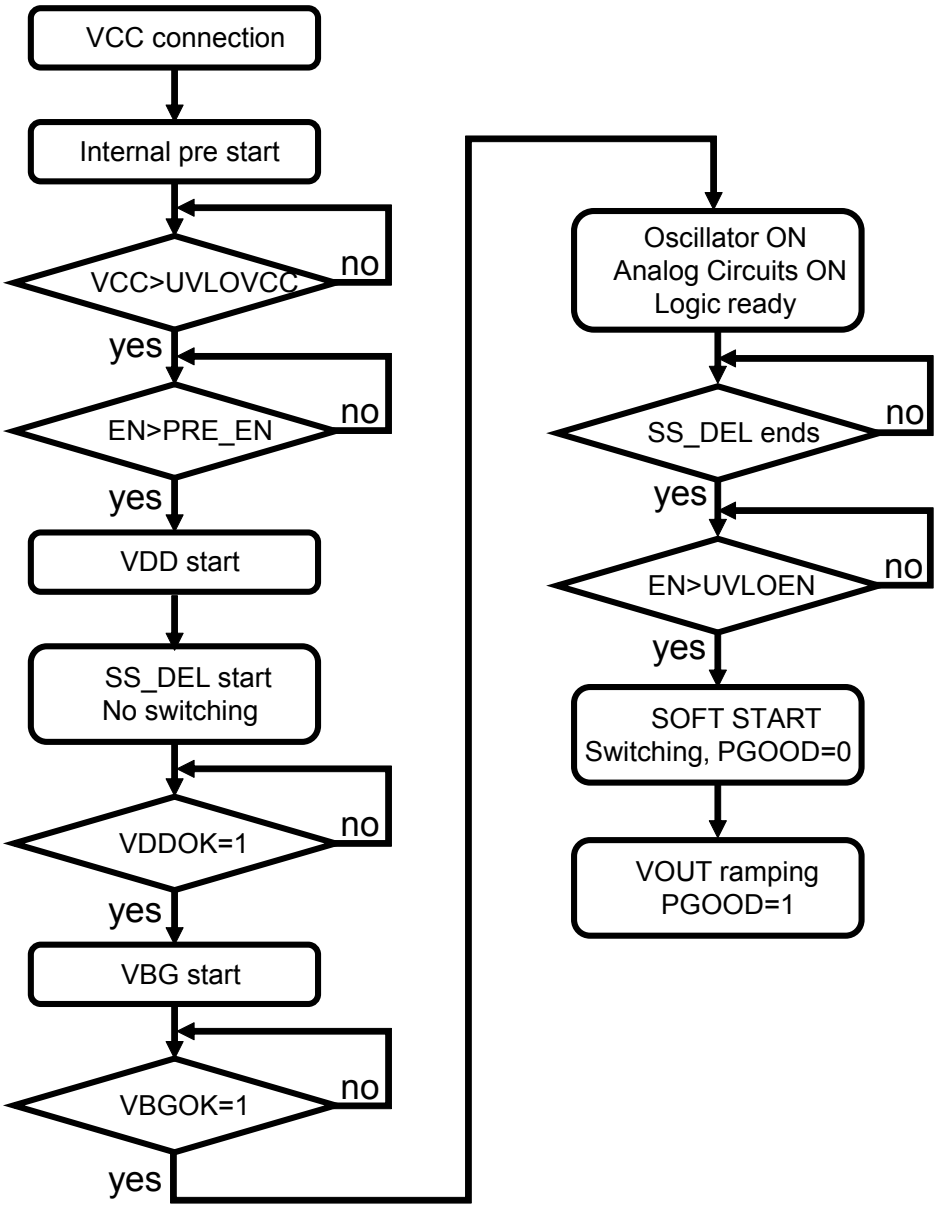
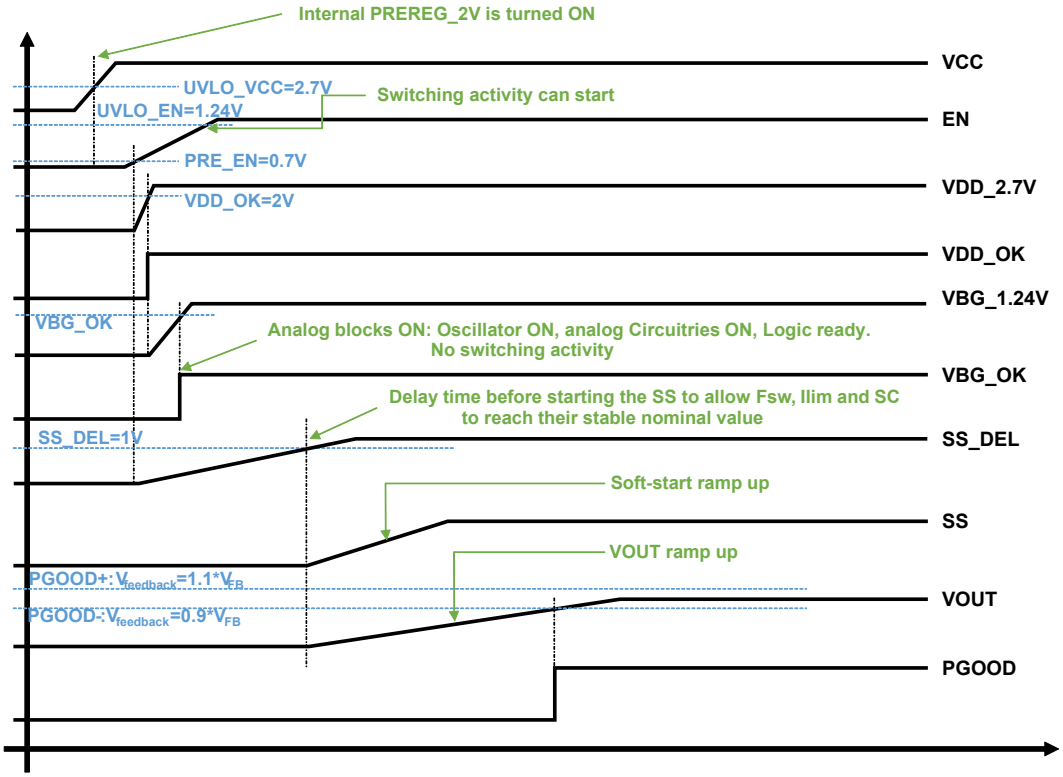


Figure 14. **RHRPMPOL01 start-up sequence**



The output soft-start function is achieved by ramping up the SS pin voltage with a constant slew rate dV/dt. When the switching section is enabled, the SS pin charges at a constant current the capacitor connected between SS and GND pins. The SS voltage is used as a reference of the switching regulator and the output voltage of the converter follows the ramp of the SS voltage. When the SS pin voltage is higher than 0.8 V typ., the error amplifier switches to the internal 0.8 V reference and regulates the output voltage.

During SS period and until voltage at pin SS reaches 0.9 V, OVP is masked, PGOOD is asserted low and a negative current protection on low-side MOS (LS_OCP) is turned ON. If a negative current is detected during the soft-start phase or in a very low load condition, the LS_OCP detects it and we force the low-side OFF. This function is also called “zero-crossing detection”, because the current in the coil crosses the zero passing from positive (from GND versus the load) to negative (from load versus the GND).

When feedback voltage enters the V_{FB}±10% power good window, the PGOOD pin is released (floating, PGOOD=high).

7.8 Turn-off

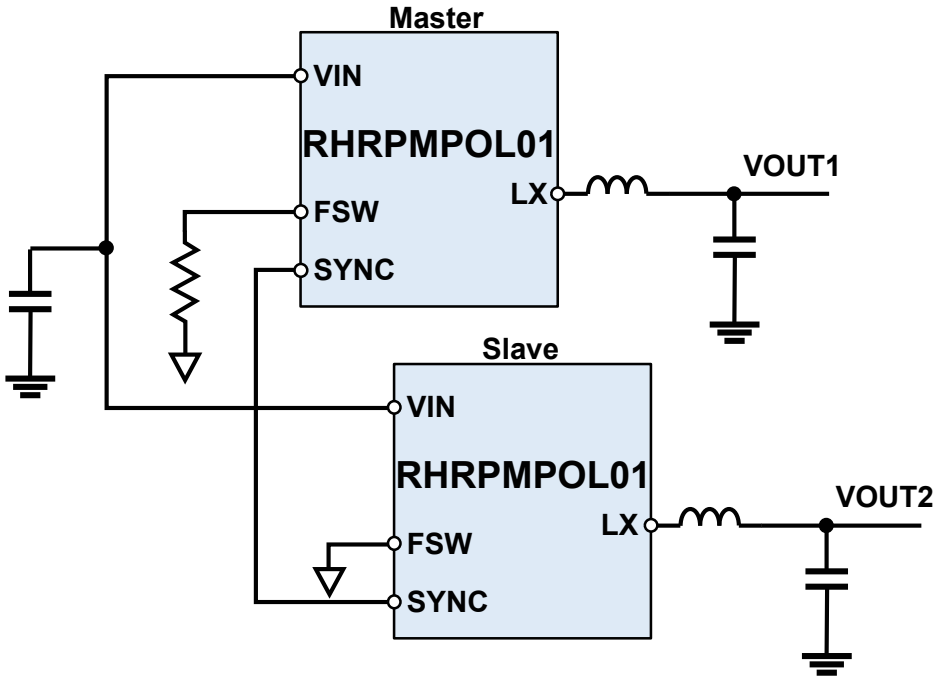
When the enable signal is forced below the UVLO_EN falling threshold (1.04 V typ.), the PGOOD signal is pulled-low, the device stops switching and the power MOSFETs are set at high impedance.

The output capacitor is discharged via the output load. If V_{CC} goes below the V_{CC_UVLO} threshold, the device is switched off.

7.9 Synchronization

The RHRPMPOL01 can work in a two synchronized ICs configuration. The clock synchronization is performed in case one IC is configured as master (FSW connected to GND through a switching frequency programming resistor) and the second one configured as slave (FSW pin shorted to GND). The main benefit of this configuration is the reduction of the input capacitor current ripple, when the two devices work in interleaved configuration.

Figure 15. **Synchronized ICs**



When two RHRPMPOL01 are synchronized together, they act as follows:

- Master IC

The SYNC pin is configured as clock output. The device provides, on the SYNC pin, its internal switching clock information with a 180 ° time shifting.

- Slave IC

The SYNC pin is configured as clock input. The device uses the clock information received on the SYNC pin to synchronize its internal switching clock. Care must be taken to properly route the SYNC trace on the application PCB to avoid coupling with the power switching traces (e.g. LX) that might generate jitter.

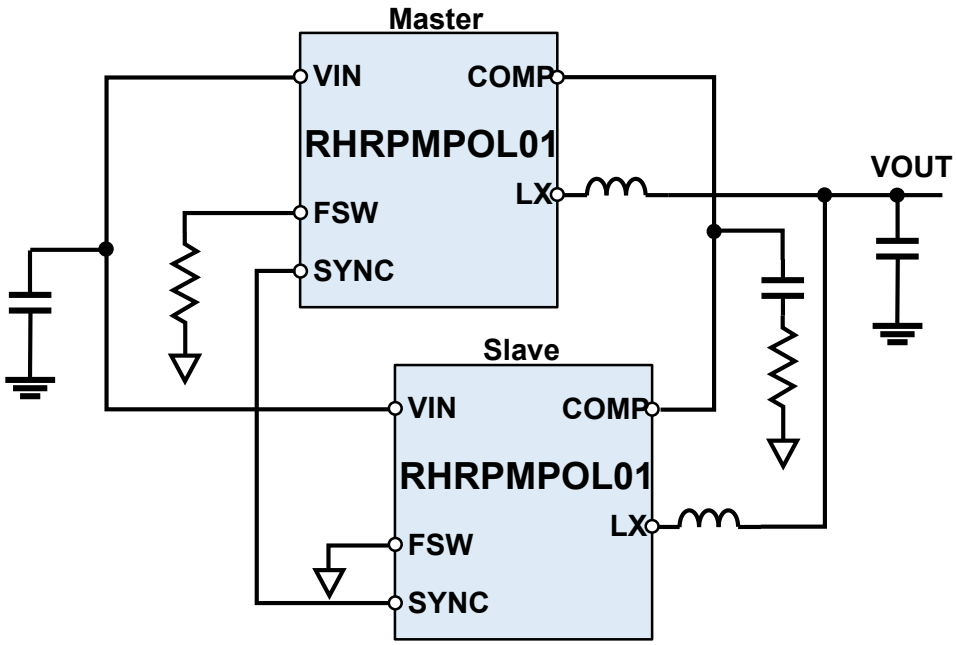
7.10 Interleaving

The RHRPMPOL01 can work in a two interleaved ICs configuration, in order to provide up to 14 A maximum load.

The ICs interleaving (or parallelization) is performed in case that IC is configured as master (FSW pin connected to GND through a switching frequency programming resistor R_{FSW}) and the second one configured as slave (FSW pin forced to a voltage lower than 0.1 V). The two SYNC pins must be shorted together and the compensation network must be shared by the two ICs.

The main benefits of this configuration are the doubled available output current and the reduction of the output and input capacitor current ripple

Figure 16. **Interleaved ICs**



When two RHRPMPOL01 are interleaved, they act as follows:

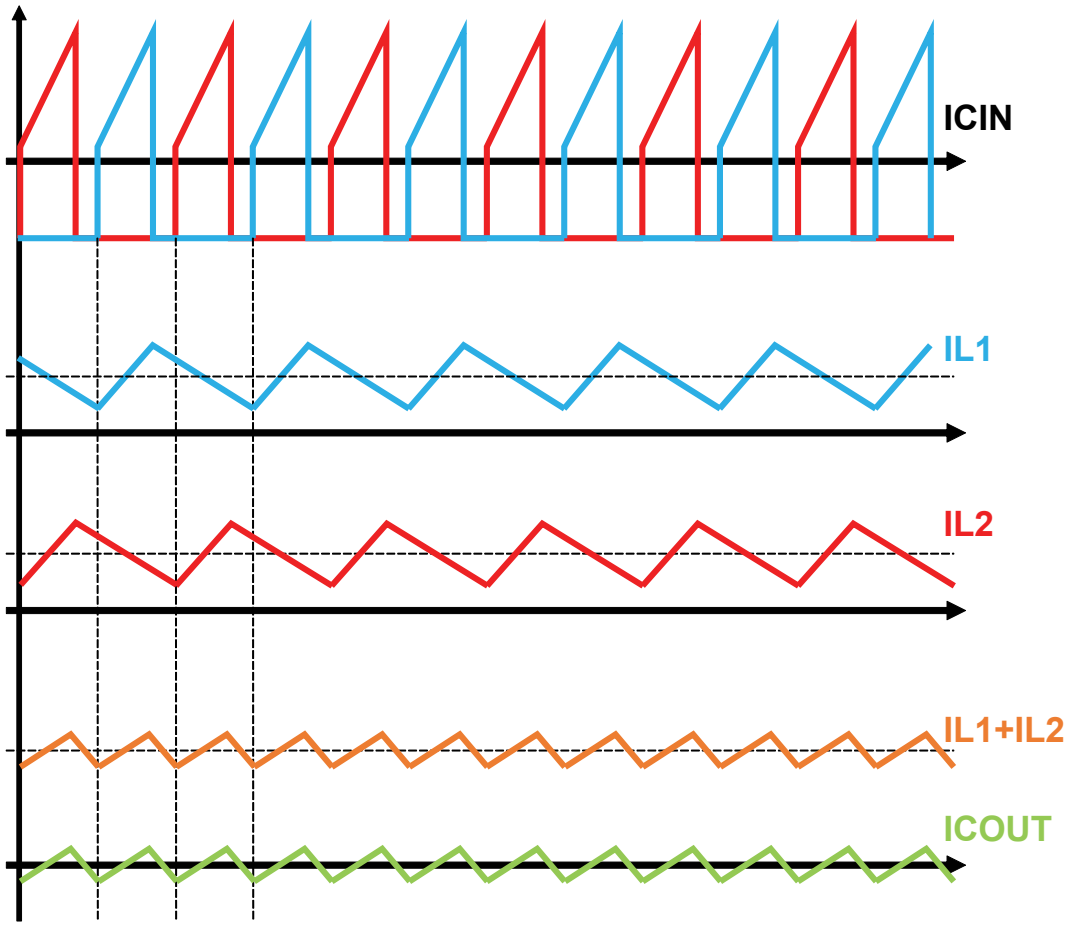
- Master IC

The SYNC pin is configured as clock output. The device provides, on the SYNC pin, its internal switching clock information with a 180 ° time shifting.

- Slave IC

The SYNC pin is configured as clock input. The device uses the clock information received on the SYNC pin to synchronize its internal switching clock. An example of the typical inductor and input/output current waveforms is shown below.

Figure 17. **Interleaved ICs current**



7.11 Fault management

The RHRPMPOL01 provides the following input and output voltage protections and monitoring features.

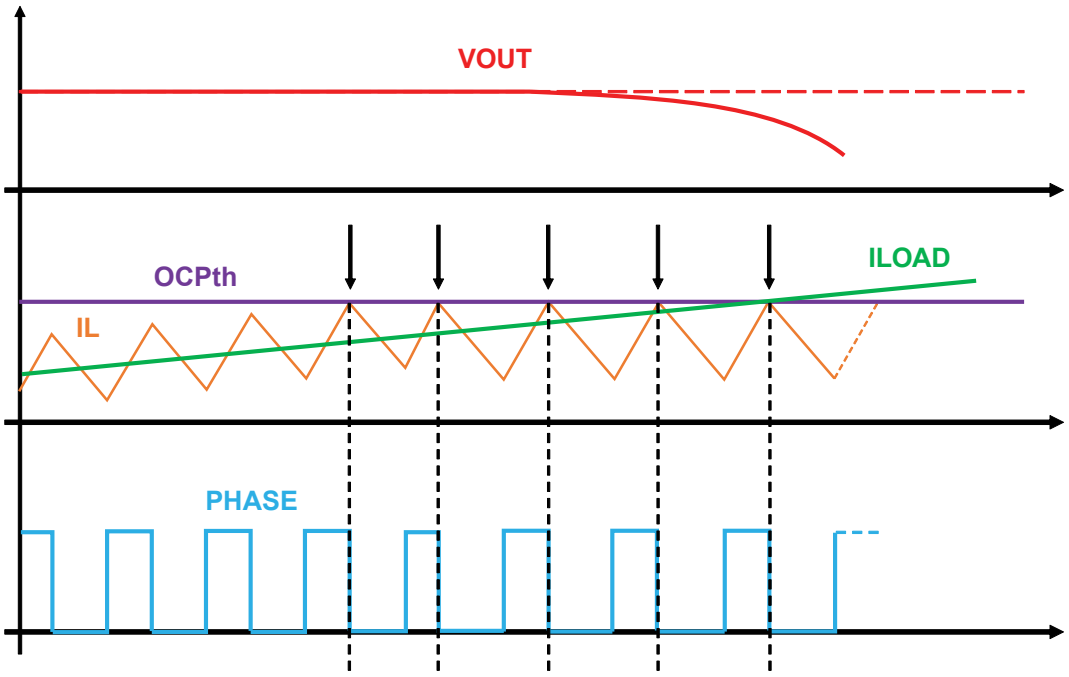
7.12 Power Good (PGOOD)

The Power Good pin (PGOOD) is an open drain output, which is left floating if the output voltage is in the ±10% regulation window. During start-up, turn-off and fault detection, the PGOOD pin is forced low.

7.13 Overcurrent protection (OCP)

The RHRPMPOL01 is able to monitor, cycle-by-cycle, the HS MOS current. If the measured current reaches the first level overcurrent limit threshold (I_{LIM1}) the high-side MOS is immediately turned-off and the low-side MOS is turned-on, until a new clock pulse is generated. The PGOOD signal is not affected and it stays in high impedance (high level).

Figure 18. **Peak current protection (OCP1)**

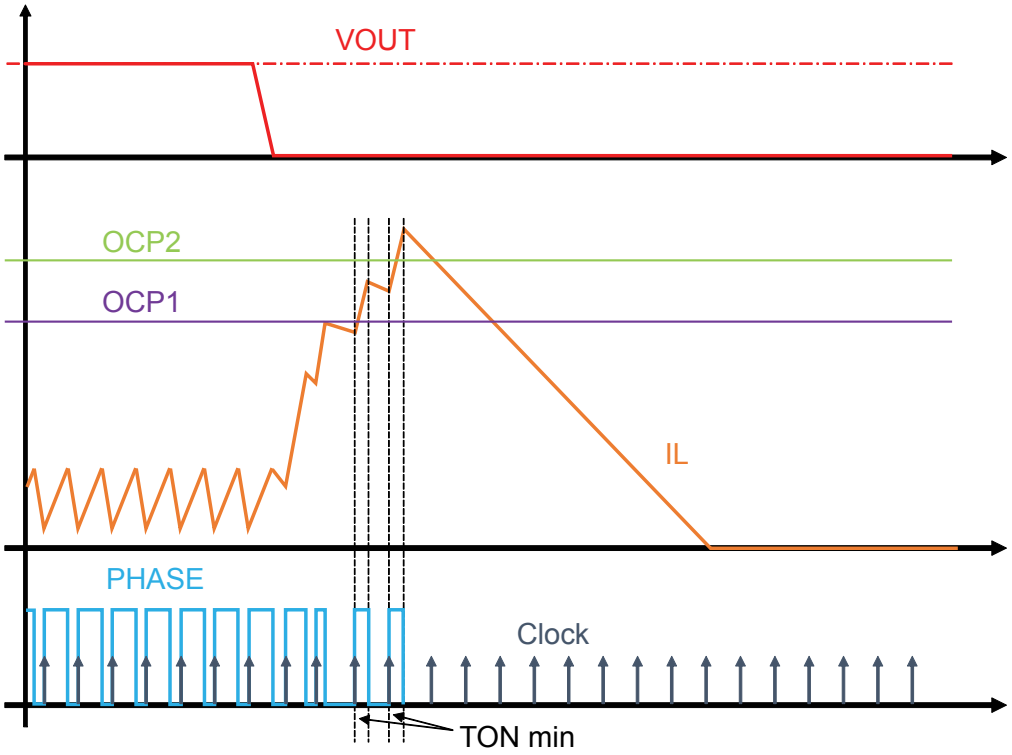


The peak current protection described above can meet some limitations in case of output voltage short versus GND.

In this case, the minimum HS MOS on-time, required for a precise current sensing, could lead to a current increase above the OCP1 limit. In fact, since in this case the output voltage is almost zero, the inductor current cannot decrease during the LS MOS on-time.

To overcome this problem, the RHRPMPOL01 implements a second order overcurrent threshold (OCP2, refer to Figure 19. Second level overcurrent protection (OCP2)). In case the sensed HS MOS current reaches the second level threshold (I_{LIM2}), the switching regulator immediately turns off and the MOSFETs are set at high impedance. The PGOOD pin is asserted low and the SS capacitor is discharged. For more details about alarm s/faults handling, please refer to Section 7.16 Alarm description.

Figure 19. **Second level overcurrent protection (OCP2)**

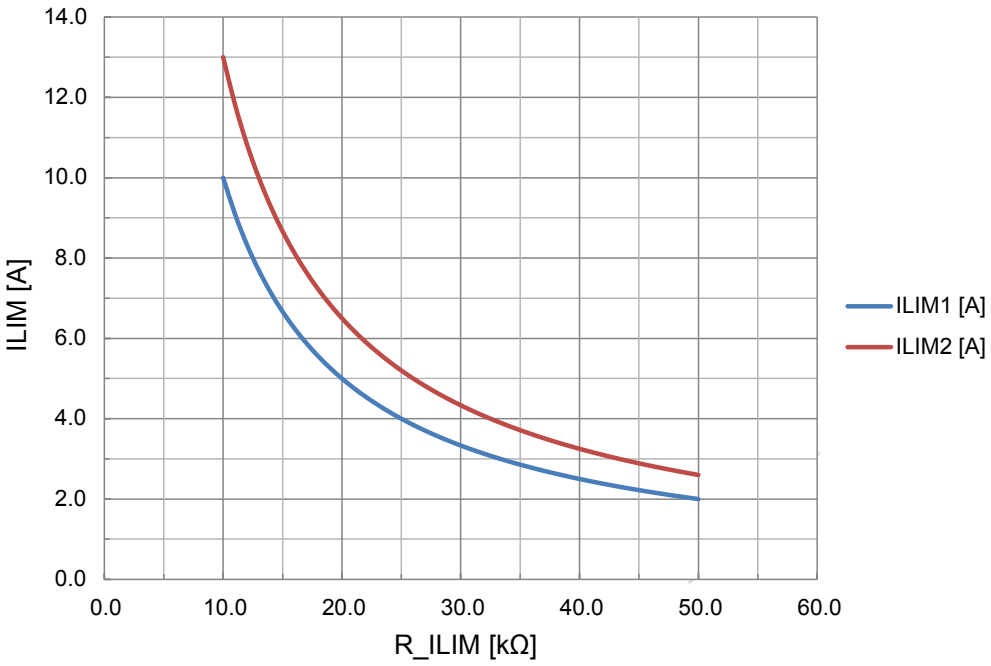


The default value for the overcurrent threshold is 10 A, with a second level OCP of 13 A (ILIM pin pulled up to V_{DD}).

If a resistor (R_{ILIM}) is connected between ILIM pin and GND the I_{LIM1} threshold can be set at a lower value, and the I_{LIM2} isconsequently set at 1.3 x I_{LIM1}.

Here below a graph of both programmable current limitation (I_{LIM1}, I_{LIM2}) versus the resistor R_{ILIM} connected on ILIM pin.

Figure 20. **Overcurrent protections vs R_{ILIM}**



7.14 Overvoltage protection

If the output voltage exceeds +25% of the nominal value (VFB=1 V), the internal signal OVP is asserted high. The driver stops switching and the bridge is forced in high impedance (both low and high-side MOS are turned OFF). The energy stored in the coil is discharged into VIN power supply. The whole power bridge stays in high impedance until VFB<0.85 V again.

7.15 Overtemperature protection

It is recommended to never let the device exceed the maximum allowable junction temperature. This temperature increase is mainly caused by the total power dissipated by the integrated power MOSFETs.

To avoid any damage to the device when reaching high temperature, the RHRPMPOL01 implements a thermal shutdown feature: when the junction temperature reaches 155 °C, the device turns off both MOSFETs and the PGOOD pin is forced low.

When the junction temperature drops again to around 135 °C, the overtemperature fault condition is cleared and the PGOOD open drain pin goes again to high impedance.

Refer to Section 7.16 Alarm description for more details about restart sequence and alarm handling.

7.16 Alarm description

When a fault condition occurs (thermal shutdown or the 2nd level overcurrent protection), the capacitor connected to the AL pin (typ. 1 µF) is discharged and charged with a constant current (typ. 20 uA); this is used to generate a “cooling” and a “watching” time cycle.

For the “cooling” time frame $\Delta t_{cooling}$ = 16 *t_{AL} while for the “watching” time frame: $\Delta t_{watching}$ ~ 3 * $\Delta t_{cooling}$

Where t_{AL}=C_{AL}*K/20 uA and K=3.1 V

In case of thermal shutdown the cooling time is incremented by Δtf_{ault} (time required to make the device exit fault condition – the junction temperature must decrease to T_{OTP} minus hysteresis). Δt_{fault} is negligible in case of 2nd level overcurrent protection.

The device cools down during the first window Δt_{fault}+$\Delta t_{cooling}$ (switching is stopped, LX is set to high impedance, SS pin is discharged/pulled down to GND) and then restarts with a soft-start sequence at the beginning of the “watching” time frame during which the logic starts monitoring for a possible consecutive fault.

After a first alarm is raised, an internal counter is incremented and two different scenarios can be generated:

1. No consequent alarm is raised during the “watching” time frame: in this case, the internal counter is reset and the device continues regulating. If a new alarm is raised after the watching window is over, the cycle is repeated. This mode of operation is called "Hiccup" mode.
2. Another alarm is raised during “watching” window. In this case the “cooling” + “watching” time cycle is restarted and internal counter is incremented. If 16 total consecutive alarms happen during the watching window, the device is latched and the regulation is stopped. To exit from latched condition an enable cycle has to be externally provided. This mode of operation is called "Latched" mode

The table below indicates what happens in different alarm conditions.

Table 11. Alarm summary

Event	Description	PGOOD
OVP	Overvoltage protection: if FB>1 V, POL stops switching until FB<0.85 V. Both bridge powers are OFF	low
OTP	Overtemperature protection: if T_j > 155 °C, POL stops switching (both bridge powers are OFF) for $\Delta t_{fault}+\Delta t_{cooling}$. After this time the device restarts in soft-start. If this event is repeated for 16 times within the watching window, the info is latched and the device can be restarted only by cycling the EN pin	low
OCP1	Overcurrent protection 1: it is externally programmable by a resistance on pin ILIM. This signal is used only internally to limit the coil current (stopping T_{on} time). No alarm is given and the bridge continues to switch	high
OCP2	Overcurrent protection 2: this threshold is about 1.3*OCP1. When this threshold is crossed, the RHRPMPOL01 stops switching (both bridge powers are OFF) for a time of $\Delta t_{fault}+\Delta t_{cooling}$. After this time the device restarts in soft-start. If this event is repeated for 16 times within the watching window, the info is latched and the device can be restarted only by cycling the EN pin	low

7.17 Hiccup and latched mode configuration

The entry in hiccup or latched mode described in the previous section depends on several factors:

- Watching window duration - f(C_{AL})
- Soft-start time – f(C_{SS})
- Thermal performance of the application
- Alarm type (thermal or OCP2)
- Voltage at AL pin

Regarding to thermal alarms, if a latched mode operation is required, the user must select a watching window duration longer than the time required by the device to trigger the thermal protection after the cooling time. This makes the alarm event counter increment without being reset leading to a latched behavior after 16 events.

If a hiccup mode operation is required, the user must select a watching window duration shorter than the time required by the device to trigger the thermal protection after the cooling time. This selection results in a reset of the event counter after each fault and the stop/restart sequence continues in an infinite loop.

Considering that the thermal performance of the device is strongly dependent on the application conditions (PCB layout, ambient temperature, etc.) the value of C_{AL} must be carefully evaluated in order to have the desired cooling/watching time and response to thermal alarms.

In case of OCP2 alarms, the entry in hiccup or latched mode is strictly linked to the soft-start time. Similarly to thermal events, in order to have a latched response to an OCP2 event, the programmed soft-start time must be shorter than the watching window duration. If a hiccup response is desired, the soft-start time must be longer than the watching window duration.

The considerations above imply that the value of both C_{SS} and C_{AL} must be chosen to fit the application conditions and get the desired response bearing in mind that the value of C_{AL} has impact on the response to both thermal and OCP2 events.

If the user prefers a simpler approach to alarms, the behavior of the device in case of thermal or OCP2 events can be forced by driving the AL pin to the right voltage:

- Forced hiccup mode: V_{AL} = 0
- Forced latched mode: V_{AL} >0.2 V

7.18 Typical performance characteristics

Figure 21. LX rise time, V_{IN}=7 V, V_{OUT}=2.5 V, I_{OUT}=2 A

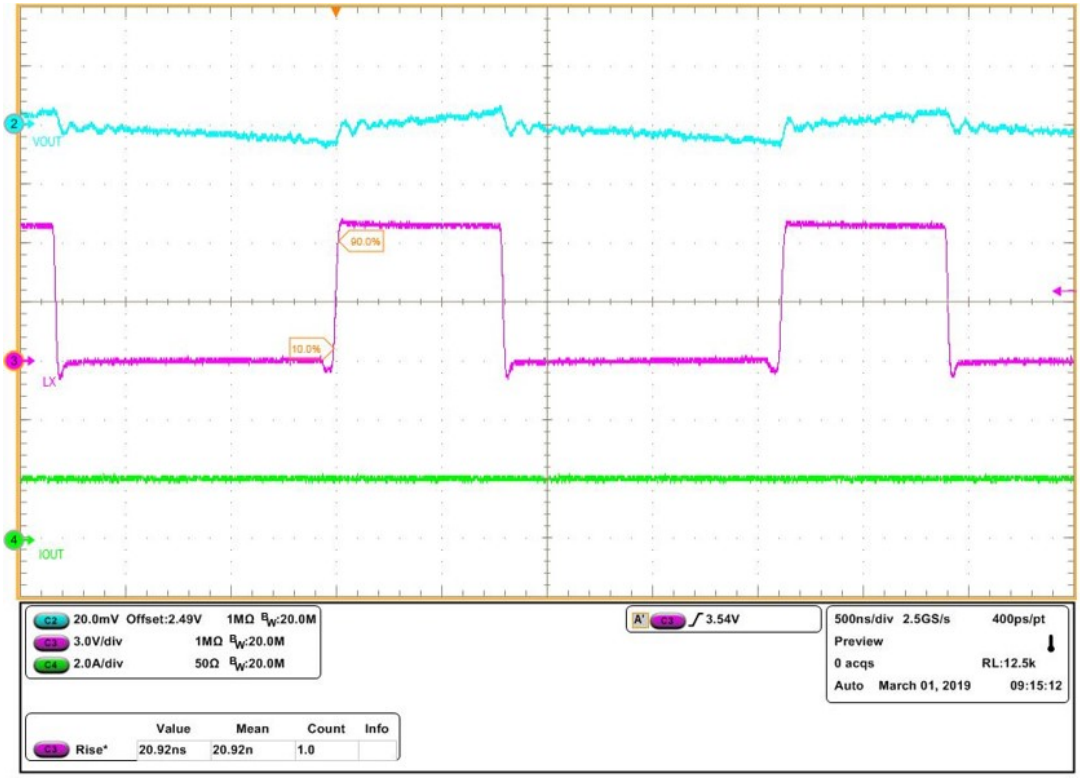


Figure 22. LX fall time, V_{IN}=7 V, V_{OUT}=2.5 V, I_{OUT}=2 A

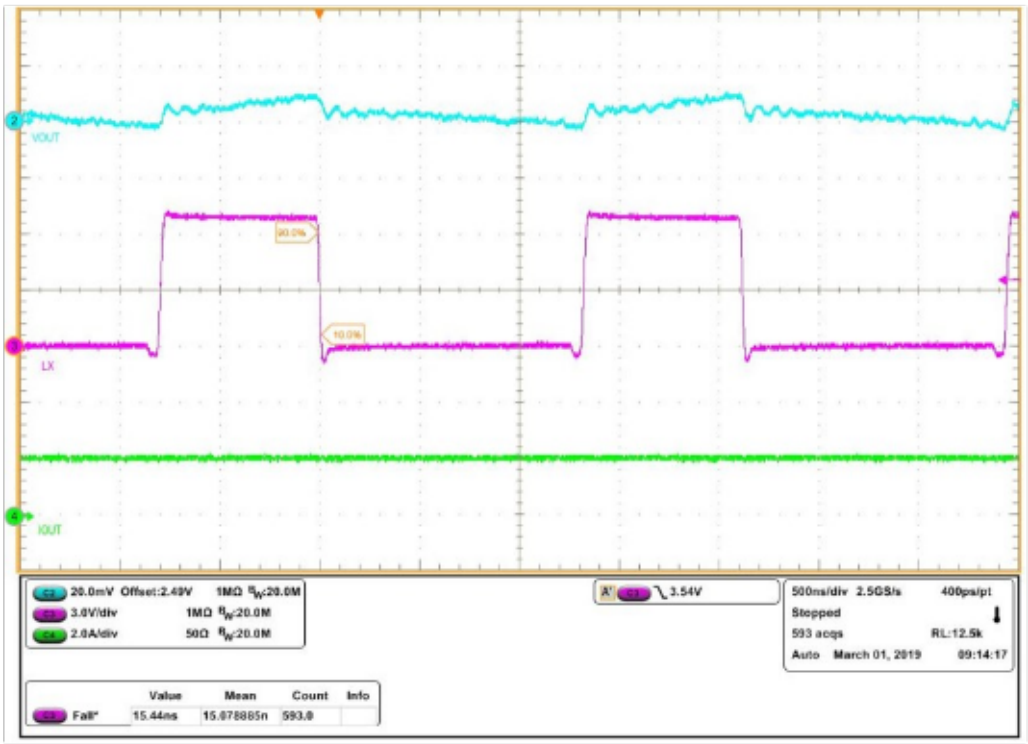


Figure 23. LX rise time, V_{IN}=7 V, V_{OUT}=2.5 V, I_{OUT}=7 A

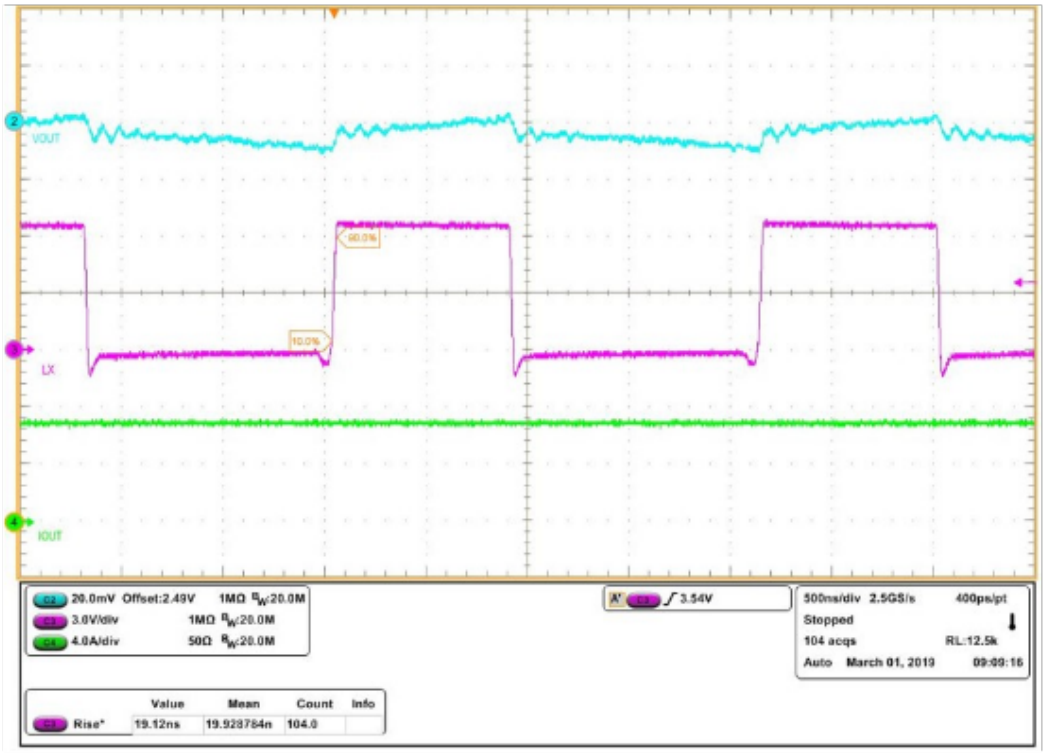


Figure 24. LX fall time, V_{IN}=7 V, V_{OUT}=2.5 V, I_{OUT}=7 A

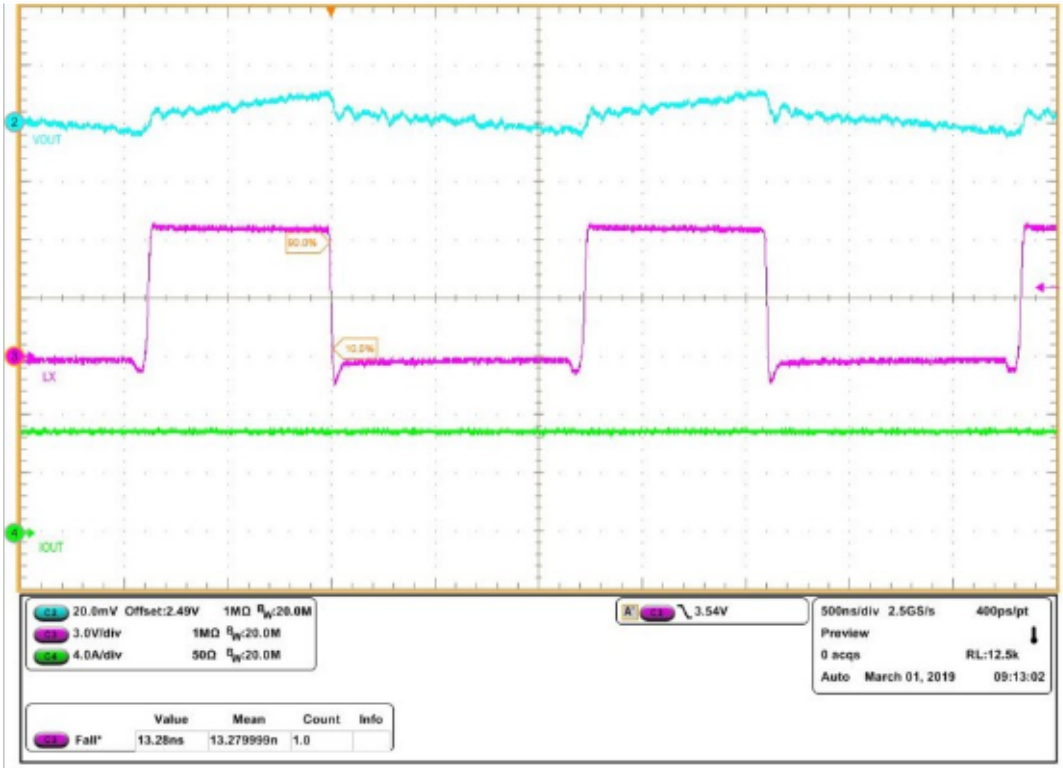


Figure 25. **Efficiency@Vin=5 V, fsw=200 kHz- coil 4.7 uH**

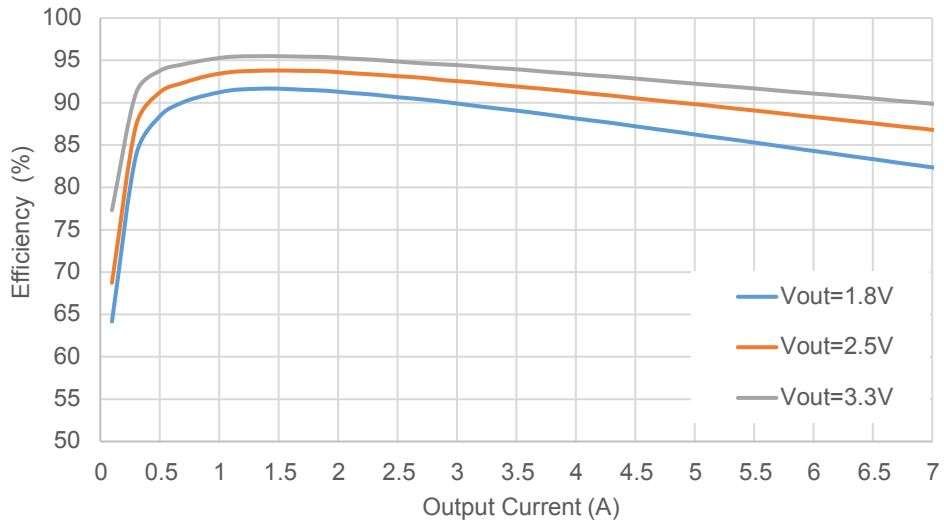


Figure 26. **Efficiency@Vin=5 V, fsw=500 kHz- coil 2.2 uH**

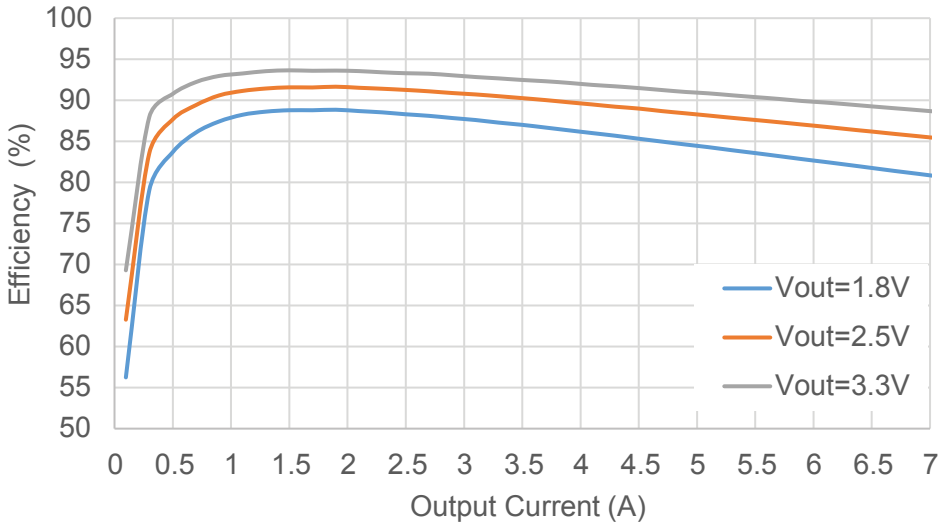


Figure 27. **Voltage reference vs. temperature**

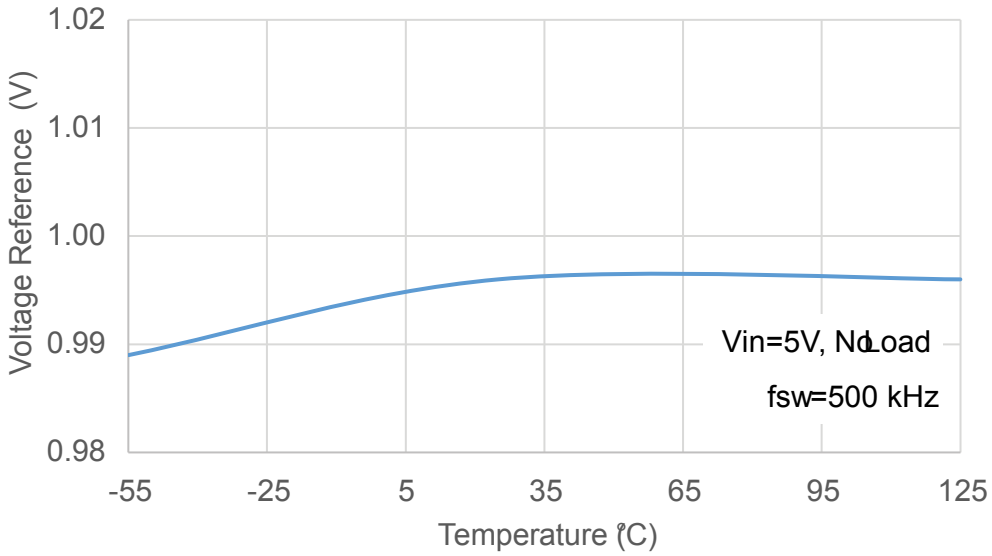


Figure 28. **UVLO_H vs. temperature**

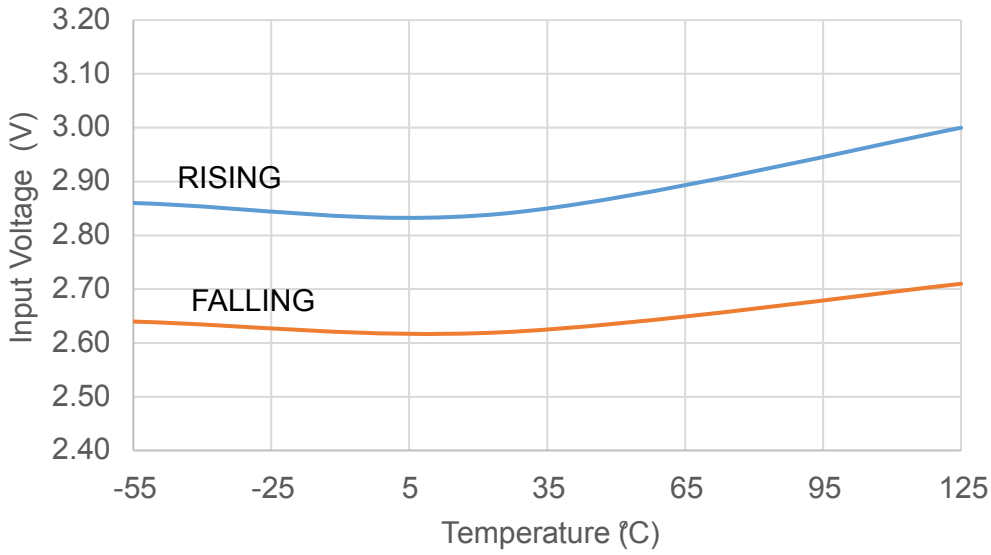


Figure 29. **Shutdown current vs. temperature**

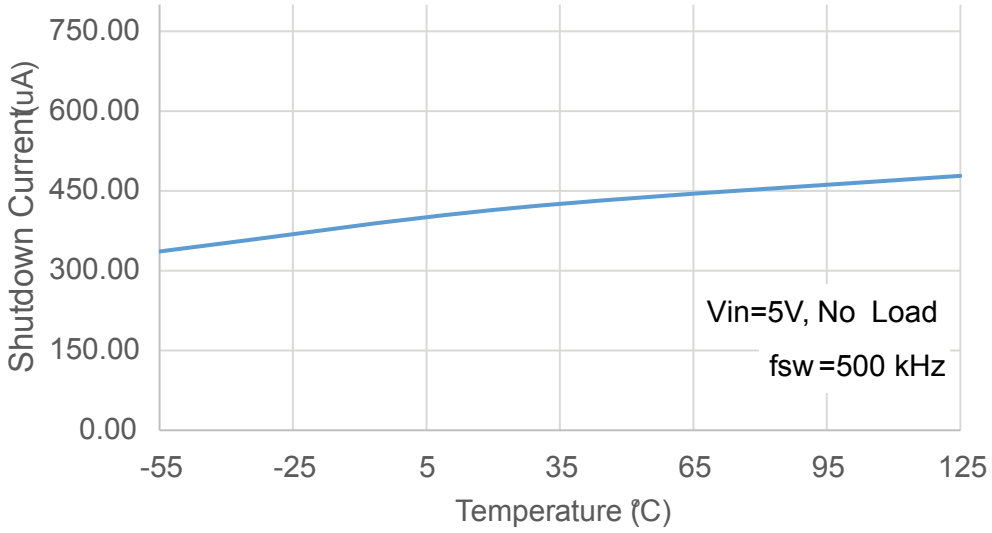


Figure 30. **Quiescent current vs. temperature**

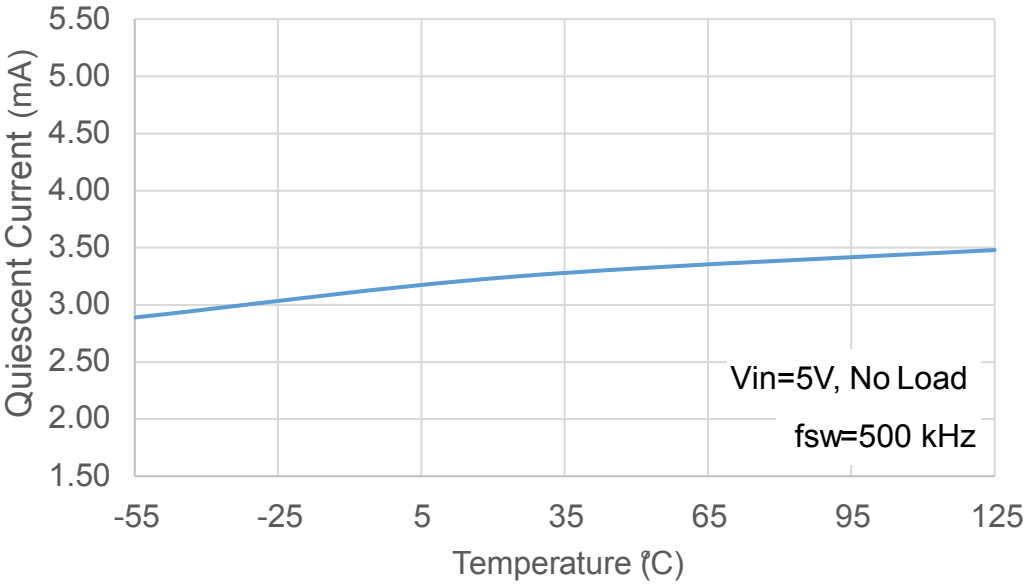
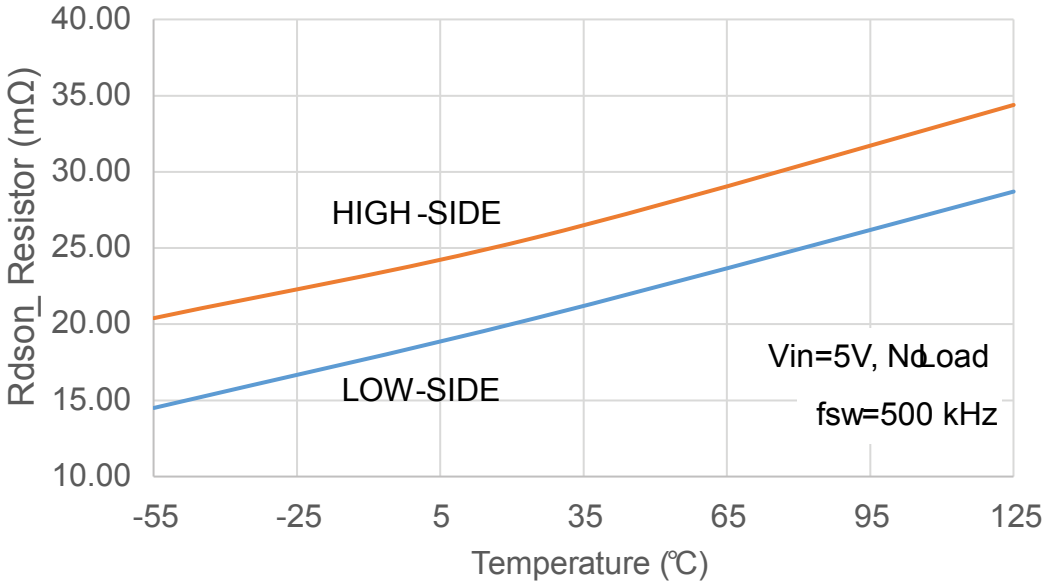


Figure 31. $R_{DS(on)}$ vs. temperature



8 Bill of material list

Figure 32. **Typical application diagram**

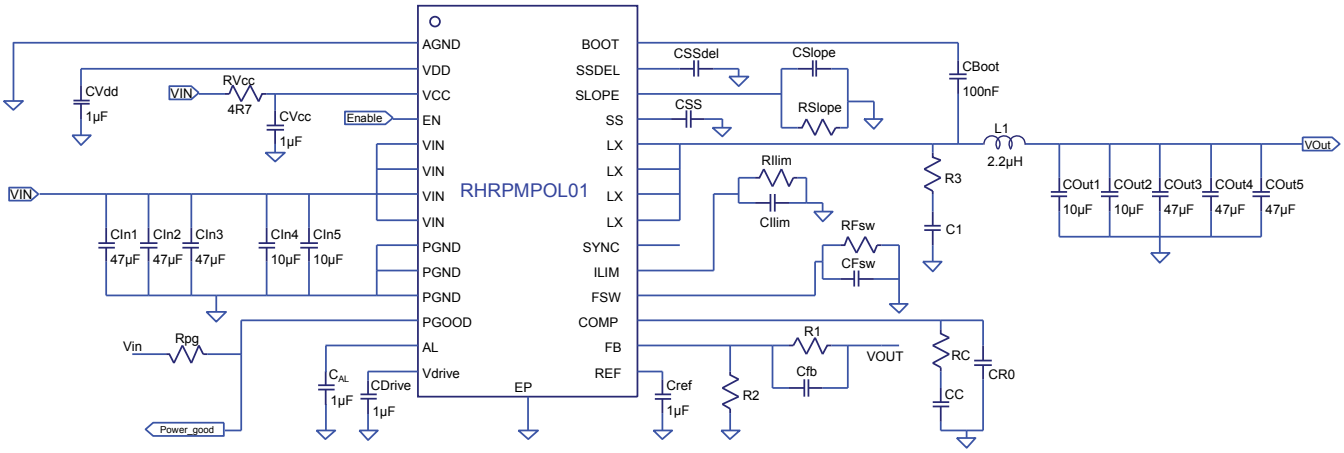


Table 12. **External components**

Reference	Description	Suggested P/N
L1	Inductance, 2.2 µH, low DCR	
C_{in1}, C_{in2}, C_{in3}	Capacitor, 47 µF, 25 V, ceramic low ESR	
C_{in4}, C_{in5}	Capacitor, 10 µF, 25 V , ceramic low ESR	
C_{out1}, C_{out2}	Capacitor, 10 µF, 25 V, ceramic low ESR	GRM32ER71H106KA12L
C_{out3}, C_{out4}, C_{out5}	Capacitor, 47 µF, 25 V, ceramic low ESR	GRM32ER61C476KE15L
C_{drive}, C_{Vdd}	Capacitor, 1 µF, 6.3V, ceramic low ESR	
C_{Vcc}	Capacitor, 1 µF, 25 V , ceramic low ESR	
C_{SSdel}, C_{SS}	Capacitor, 10 nF-1 µF , 6.3 V , ceramic	
C_{Slope}	Capacitor,1 nF or less, 6.3 V,ceramic (optional)	
C_{Ilim}	Capacitor, 1 nF or less, 6.3 V , ceramic (optional)	
C_{Fsw}	Capacitor, 1 nF or less, 6.3 V , ceramic (optional)	
C_{fb}	Capacitor, 100 pF-10 nF, 25 V, ceramic	
C_{ref}	Capacitor, 1 µF, 6.3 V, ceramic	
C_{boot}	Capacitor, 1 µF, 6.3 V, ceramic	
C_1	Capacitor, 1 nF, 16 V, ceramic (optional)	
C_C	Capacitor, 4.7 nF, 6.3 V, ceramic	
C_{R0}	Capacitor, 10 pF, 6.3 V, ceramic (optional)	
R_{Vcc}	Resistor, 4.7 Ω, 1/4 W, 5%	
R_{PG}	Resistor, > 4.7 kΩ, 1/4 W, 10%	
R_{SLOPE}	Resistor, 15 kΩ, 1/4 W, 5%	

Reference	Description	Suggested P/N
R_{Ilim}	Resistor, 1/4 W, 5% or less	
R_{Fsw}	Resistor, 1/4 W, 5% or less	
R_1	Resistor, 1/4 W, 5% or less	
R_2	Resistor, 1/4 W, 5% or less	
R_3	Resistor, 10 Ω, 1/2 W, 10% (optional)	
R_C	Resistor, 500 Ω, 1/4 W, 5% or less	

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 FLAT PACK 28 leads ceramic package information

Figure 33. **FLAT PACK 28 package outline**

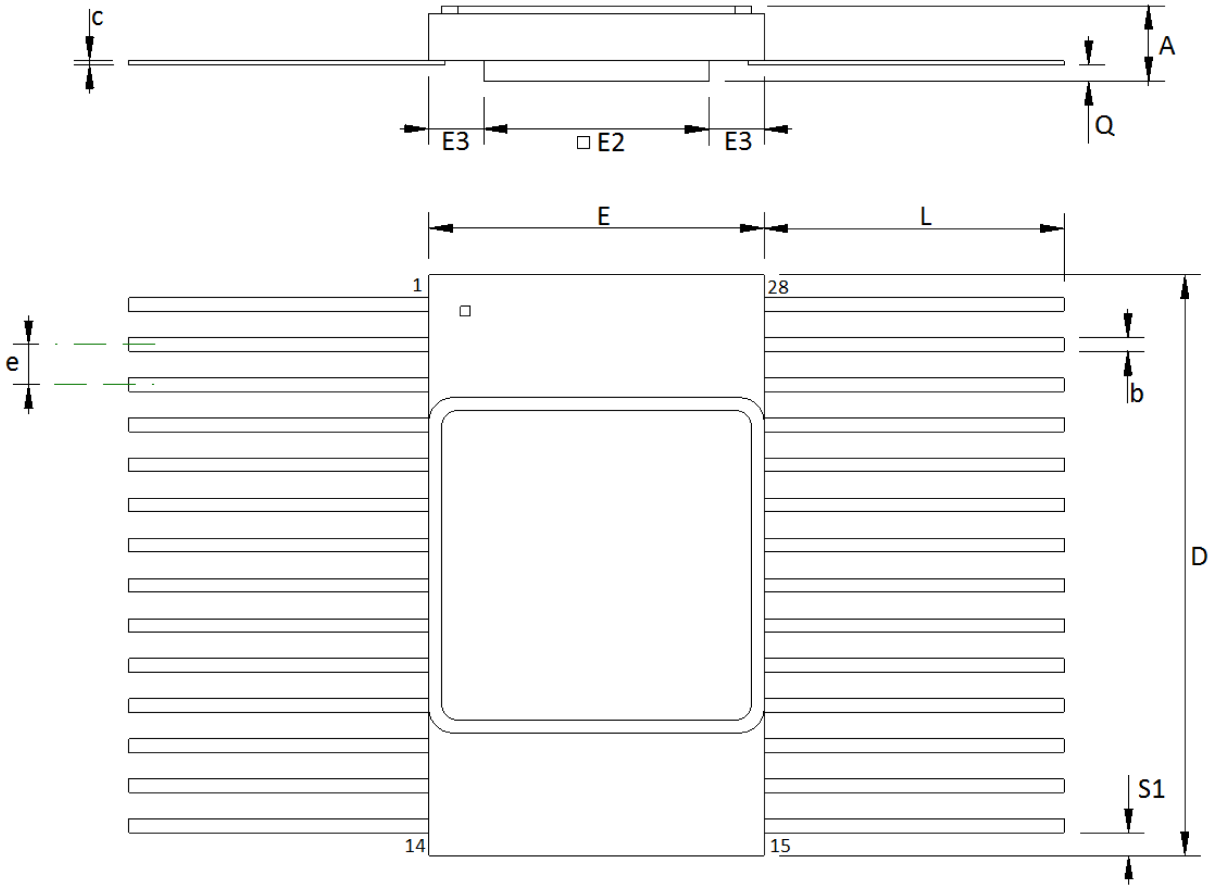


Table 13. **FLAT PACK 28 mechanical data**

Symbol	Milimeters		
	Min.	Typ.	Max.
A	2.5		3
b	0.38		0.48
c	0.125		0.175
D	18.21		18.57
E	10.48		10.74
E2	7.02		7.28
E3		1.73	
e		1.27	
L	6.35		9.4
Q	0.66		
S1	0.13		

10 Ordering information

Table 14. Ordering information

Part number	SMD pin	Qualitylevel	Package	Lead finish	Marking(1)	Packing
RH-PMPOL01KPX	-	Evaluation model	FLAT PACK 28 hermetic	Gold	RH-PMPOL01KPX	Strip pack
RH-PMPOL01KP1	-	Engineering model	FLAT PACK 28 hermetic	Gold	RH-PMPOL01KP1	Strip pack
RHRPMPOL01K01V	5962R2020801VXC	QML-V flight	FLAT PACK 28 hermetic	Gold	5962R2020801VXC	Strip pack
RHRPMPOL01K02V	5962R2020801VXA	QML-V flight	FLAT PACK 28 hermetic	Tin	5962R2020801VXA	Strip pack
RHRPMPOL01D2S	-	Engineering model	Die version	-	-	-
RHRPMPOL01D2V	5962R2020801V9A	QML-V flight	Die version	-	-	-
EVAL-RHRPMPOL01	Evaluation board					

1. *Specific marking only. The full marking includes in addition:*
   - *for the engineering models : ST logo, date code, country of origin (FR)*
   - *for QML flight parts : ST logo, date code, country of origin (FR), manufacturer code (CSTM), serial number of the part within the assembly lot.*

Contact ST sales office for information about the specific conditions for:

1. Products in die form
2. Other quality levels
3. Tape and reel packing

10.1 Traceability information

Datecode information is structured as described below:

Table 15. Date code

Model	Datecode
EvM – evaluation model	
EM – engineering model	3yywwN
QML flight	yywwN

where:

- yy = year
- ww = week number
- N = lot index in the week

10.2 Documentation

The table below gives a summary of the documentation provided with each type of products:

Table 16. Table of documentation by product

Quality level	Documentation
Evaluation model	-
Engineering model	-
QML-V flight	Certificate of conformance (including group C and D reference) precap report (100% high and low magnification) SEM report screening summary Group A summary (quality conformance inspection of electrical tests) Group B summary (quality conformance inspection of mechanical tests) Group E (quality conformance inspection of wafer lot radiation verification test)

Revision history

Table 17. **Document revision history**

Date	Version	Changes
01-Oct-2019	1	Initial release.
16-Feb-2021	2	Updated the cover page. Updated Figure 1. Block diagram. Added Section 4.1 Output voltage setting, Section 4.2 Inductor selection, Section 4.3 Input capacitor selection, Section 6 Radiations, Section 6.1 Total ionizing dose (MIL-STD-883 test method 1019), Section 6.2 Single event effect, Section 6.2.1 Single event upset and single event functional interrupt, Section 6.2.2 Proton test, Section 10.1 Traceability information and Section 10.2 Documentation. Added Figure 25. Efficiency@Vin=5 V, fsw=200 kHz- coil 4.7 uH , Figure 26. Efficiency@Vin=5 V, fsw=500 kHz- coil 2.2 uH , Figure 27. Voltage reference vs. temperature, Figure 28. UVLO_H vs. temperature, Figure 29. Shutdown current vs. temperature, Figure 30. Quiescent current vs. temperature and Figure 31. $R_{DS(on)}$ vs. temperature. Updated Section 10 Ordering information, Table 8. Test results.

Contents

List of tables

List of figures

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