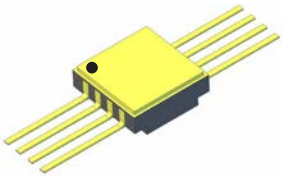
RHR61, RHR64

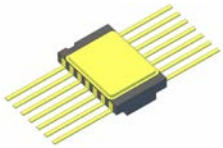
Rad-hard, low-power, rail-to-rail CMOS operational amplifiers

Datasheet - production data

Ceramic Flat-8
RHR61



Ceramic Flat-14
RHR64



Features

- Single and quad CMOS operational amplifiers (op amp)
- Unity gain stable on 100 pF load
- Very low power supply: 1.5 V to 5.5 V
- Very low consumption: 60 µA max
- Low offset voltage: 1 mV max
- Low input bias: 1 pA
- Input and output rail-to-rail
- 100 krad TID (high-dose rate)
- SEL immune at 120 MeV.cm²/mg
- SET characterized

Description

The RHR61 and RHR64 devices are pure CMOS single and quad op amps respectively. The RHR61 is packaged in a flat hermetic 8-lead and the RHR64 in a flat hermetic 14-lead. Both devices are guaranteed in radiation and over the temperature range -55 °C to 125 °C. They are for general use in any space application.

Table 1: Device summary

Parameter	RHR61K1	RHR64K1	RHR61K01V	RHR64K01V
SMD (1)	—		5962R1620401VXC	5962R1620501VXC
Quality level	Engineering model		QML-V flight model	
Package, mass	Flat-8, 0.50 g	Flat-14, 0.70 g	Flat-8, 0.50 g	Flat-14, 0.70 g
EPPL (2)	—			
Temp. range	-55 °C to 125 °C			

Notes:

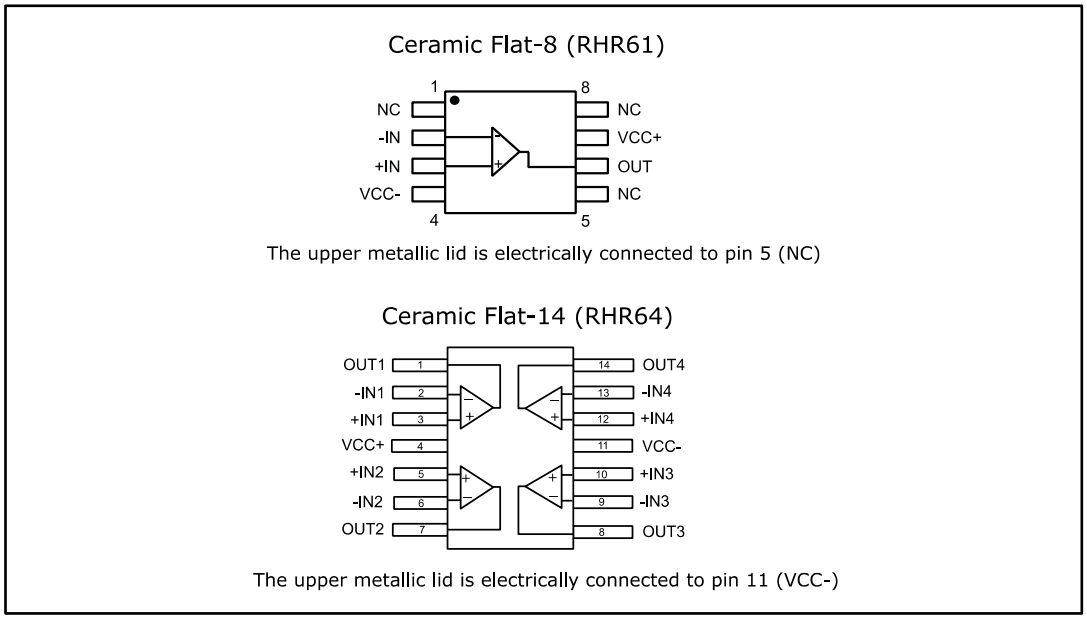
(1)SMD: standard microcircuit drawing

(2)EPPL = European preferred part list

Contents

1 Pin description

Figure 1: Pin connections of Ceramic Flat-8 and Ceramic Flat-14 (top view)



2 Absolute maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 2: Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{id}	Differential input voltage (2)		$\pm V_{CC}$	
V_{in}	Input voltage (3)		(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction-to-ambient (4)(5)	Ceramic Flat-8	125	°C/W
		Ceramic Flat-14	120	
R_{thjc}	Thermal resistance junction-to-case (4)(5)	Ceramic Flat-8	40	
		Ceramic Flat-14	22	
ESD	HBM: human body model (6)		4	kV
	MM: machine model (7)		300	V
	CDM: charged device model (8)	RHR61	700	
		RHR64	1300	
	Latch-up immunity		200	mA

Notes:

(1)All voltage values, except differential voltage are measured with respect to network ground terminal

(2)Differential voltages are the non-inverting input terminal with respect to the inverting input terminal

(3)V_{CC} - V_{in} must not exceed 6 V

(4)Short circuits can cause excessive heating and destructive dissipation

(5)R_{th} are typical values

(6)Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

(7)Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

(8)Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.

Table 3: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common-mode input voltage	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	
T_{amb}	Operating free-air temperature range	-55 to 125	°C

3 Electrical characteristics

Table 4: VCC+ = 1.8 V, VCC- = 0 V, Vicm = 0.9 V, Tamb = 25 °C, and load (RL) connected to 0.9 V (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage				1	mV
		-55 °C < T_{amb} < 125 °C			3	
DV_{io}	Input offset voltage drift			4		µV/°C
I_{io}	Input offset current (V_{out} = 0.9 V)			1	70	pA
		-55 °C < T_{amb} < 125 °C		1	150	
I_{ib}	Input bias current (V_{out} = 0.9 V)			1	70	
		-55 °C < T_{amb} < 125 °C		1	150	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 0.9 V, V_{out} = 0.9 V	70	74		dB
		-55 °C < T_{amb} < 125 °C	67			
		0 V to 1.8 V, V_{out} = 0.9 V	56			
		-55 °C < T_{amb} < 125 °C	53			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 1.3 V	83	95		
		-55 °C < T_{amb} < 125 °C	78			
V_{OH}	High-level output voltage	R_L = 10 kΩ	35	5		mV
		-55 °C < T_{amb} < 125 °C	50			
V_{OL}	Low-level output voltage	R_L = 10 kΩ		4	35	
		-55 °C < T_{amb} < 125 °C			50	
I_{out}	I_{sink}	V_o = 1.8 V	6	12		mA
		-55 °C < T_{amb} < 125 °C	4			
	I_{source}	V_o = 0 V		-10	-6	
		-55 °C < T_{amb} < 125 °C			-4	
I_{CC}	Supply current (per channel)	No load, V_{out} = 0.9 V		50	60	µA
		-55 °C < T_{amb} < 125 °C			62	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF	600	740		kHz
		-55 °C < T_{amb} < 125 °C	300			
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		48		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF		11		dB
SR	Slew rate	V_{IN} = 0.5 V to V_{CC} -0.5V, 10 % to 90 %, R_L = 2 kΩ, C_L = 100 pF, Av = 1	0.2	0.27		V/µs
		-55 °C < T_{amb} < 125 °C	0.15			
e_n	Equivalent input noise voltage	f = 1 kHz		65		nV/√Hz
		f = 10 kHz		50		

Table 5: VCC+ = 3.3 V, VCC- = 0 V, Vicm = 1.65 V, Tamb = 25 °C, and load (RL) connected to 1.65 V (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage				1	mV
		-55 °C < T_{amb} < 125 °C			3	
DV_{io}	Input offset voltage drift			4		µV/°C
I_{io}	Input offset current			1	70	pA
		-55 °C < T_{amb} < 125 °C		1	150	
I_{ib}	Input bias current			1	70	
		-55 °C < T_{amb} < 125 °C		1	150	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 1.65 V, V_{out} = 1.65 V	75	79		dB
		-55 °C < T_{amb} < 125 °C	72			
		0 V to 3.3 V, V_{out} = 1.65 V	60			
		-55 °C < T_{amb} < 125 °C	56			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 2.8 V	87	98		
		-55 °C < T_{amb} < 125 °C	82			
V_{OH}	High-level output voltage	R_L = 10 kΩ	35	6		mV
		-55 °C < T_{amb} < 125 °C	50			
V_{OL}	Low-level output voltage	R_L = 10 kΩ		7	35	
		-55 °C < T_{amb} < 125 °C			50	
I_{out}	I_{sink}	V_o = 3.3 V	30	45		mA
		-55 °C < T_{amb} < 125 °C	25			
	I_{source}	V_o = 0 V		-45	-30	
		-55 °C < T_{amb} < 125 °C			-25	
I_{CC}	Supply current (per channel)	No load, V_{out} = 1.75 V		55	64	µA
		-55 °C < T_{amb} < 125 °C			66	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF	610	820		kHz
		-55 °C < T_{amb} < 125 °C	310			
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		50		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF		11		dB
SR	Slew rate	V_{IN} = 0.5 V to V_{CC} -0.5V, 10 % to 90 %, R_L = 2 kΩ, C_L = 100 pF, Av = 1	0.22	0.29		V/µs
		-55 °C < T_{amb} < 125 °C	0.17			
e_n	Equivalent input noise voltage	f = 1 kHz		65		nV/√Hz
		f = 10 kHz		50		

Table 6: VCC+ = 5 V, VCC- = 0 V, Vicm = 2.5 V, Tamb = 25 °C, and RL connected to 2.5 V (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage				1	mV
		-55 °C < T_{amb} < 125 °C			3	
DV_{io}	Input offset voltage drift			4		µV/°C
I_{io}	Input offset current (V_{out} = 2.5 V)			1	70	pA
		-55 °C < T_{amb} < 125 °C		1	150	
I_{ib}	Input bias current (V_{out} = 2.5 V)			1	70	
		-55 °C < T_{amb} < 125 °C		1	150	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 2.5 V, V_{out} = 2.5 V	77	83		dB
		-55 °C < T_{amb} < 125 °C	74			
		0 V to 5.0 V, V_{out} = 2.5 V	63			
		-55 °C < T_{amb} < 125 °C	58			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 1.8 to 5 V	75	102		
		-55 °C < T_{amb} < 125 °C	70			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 4.5 V	88	98		
		-55 °C < T_{amb} < 125 °C	83			
V_{OH}	High-level output voltage	R_L = 10 kΩ	35	7		mV
		-55 °C < T_{amb} < 125 °C	50			
V_{OL}	Low-level output voltage	R_L = 10 kΩ		6	35	
		-55 °C < T_{amb} < 125 °C			50	
I_{out}	I_{sink}	V_o = 5 V	40	69		mA
		-55 °C < T_{amb} < 125 °C	35			
	I_{source}	V_o = 0 V		-69	-40	
		T_{min} < T_{amb} < T_{max}			-35	
I_{CC}	Supply current (per channel)	No load, V_{out} = 2.5 V		59	69	µA
		-55 °C < T_{amb} < 125 °C			72	
AC performance						
GBP	Gain bandwidth product	R_L= 2 kΩ, C_L= 100 pF	630	920		kHz
		-55 °C < T_{amb} < 125 °C	330			
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		50		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF		12		dB
SR	Slew rate	V_{IN} = 0.5 V to V_{CC} -0.5V, 10 % to 90 %, R_L = 2 kΩ, C_L = 100 pF, Av = 1	0.25	0.34		V/µs
		-55 °C < T_{amb} < 125 °C	0.20			
e_n	Equivalent input noise voltage	f = 1 kHz		65		nV/√Hz
		f = 10 kHz		50		
THD+e_n	Total harmonic distortion	G = 1, f = 1 kHz, R_L = 100 kΩ, V_{out} = 2 V_{pp}		0.002		%

Table 7: Electrical characteristics after 100 krad, VCC+ = 1.8 V, VCC- = 0 V, Vicm = 0.9 V, Tamb = 25 °C, and load (RL) connected to VCC/2 (unless otherwise specified). Min. and max. values obtained on a sample size of 10 parts from 2 different lots (2x5). Non listed parameters are not impacted by the dose.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Output voltage			—	1.7	mV
CMR (1)	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 1.8 V, V_{out} = 0.9 V	51			dB
		0 V to 0.9 V, Vout = 0.9 V	61			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 1.3 V	81			
I_{source}	Output source current	V_O = 0 V			-1.5	mA
I_{CC}	Supply current (per channel)	No load, V_{out} = 0.9 V			110	µA

Notes:

(1)The CMR from 0 V to V_{CC}/2 has not been characterized in radiation

Table 8: Electrical characteristics after 100 krad, VCC+ = 5 V, VCC- = 0 V, Vicm = 2.5 V, Tamb = 25 °C, and load (RL) connected to VCC/2 (unless otherwise specified). Min. and max. values obtained on a sample size of 10 parts from 2 different lots (2x5). Non listed parameters are not impacted by the dose.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Output voltage			—	1.5	mV
I_{ib}	Input bias current	Vout = 2.5 V	220			pA
CMR (1)	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 5 V, V_{out} = 2.5 V	62			dB
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 1.8 V to 5 V	71			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 4.5 V	87			
I_{sink}	Output sink current	V_O = 5 V	35			mA
I_{source}	Output source current	V_O = 0 V			-32	
I_{CC}	Supply current (per channel)	No load, V_{out} = 2.5 V			150	µA

Notes:

(1)The CMR from 0 V to V_{CC}/2 has not been characterized in radiation

4 Electrical characteristic curves

Figure 2: Supply current vs supply voltage

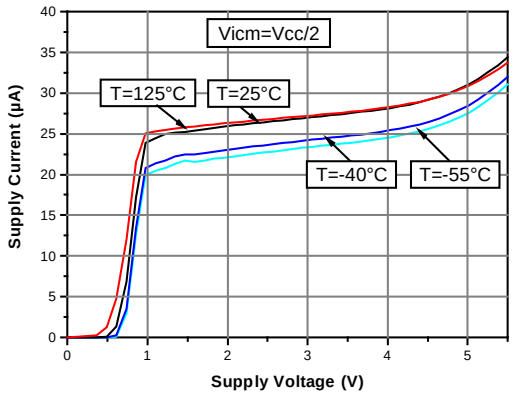


Figure 3: Input offset voltage vs input common-mode voltage at VCC = 1.5 V

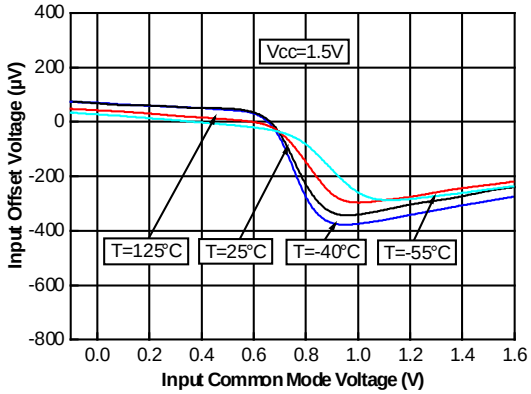


Figure 4: Input offset voltage vs input common-mode voltage at VCC = 5 V

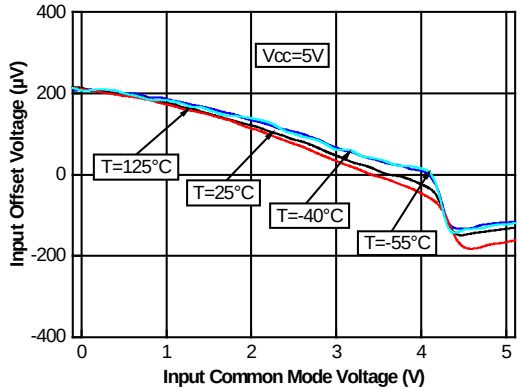


Figure 5: Input offset voltage vs output voltage at VCC = 1.5 V

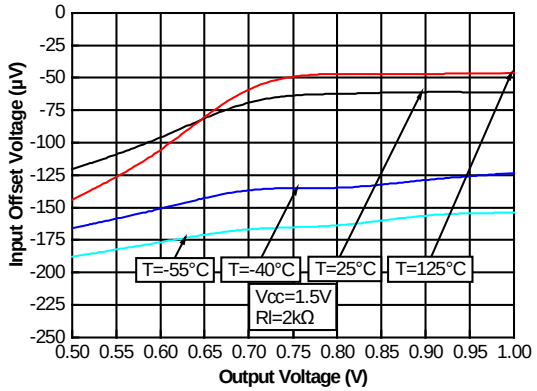


Figure 6: Input offset voltage vs output voltage at VCC = 5 V

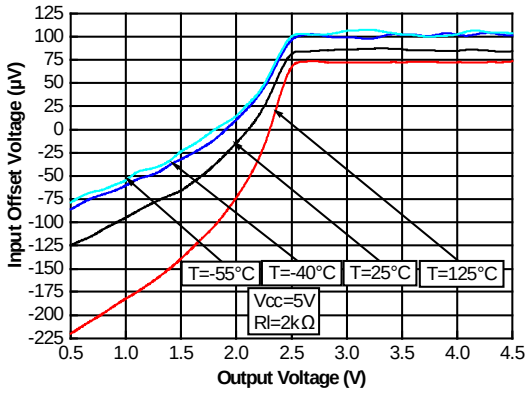


Figure 7: VOH vs supply voltage

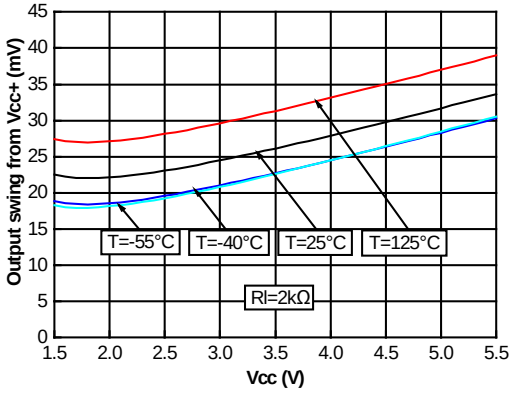


Figure 8: VOL vs supply voltage

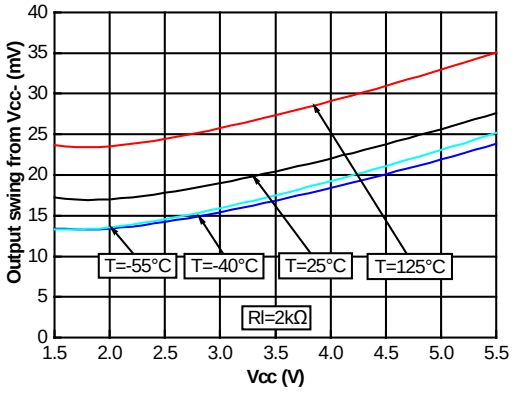


Figure 9: Output current vs output voltage at VCC = 5 V

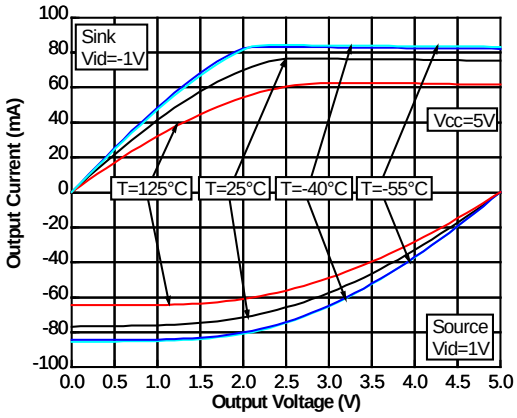


Figure 10: Bode diagram at VCC = 1.5 V

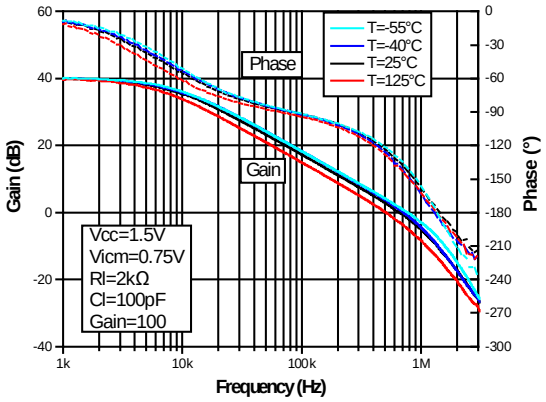


Figure 11: Bode diagram at VCC = 5 V

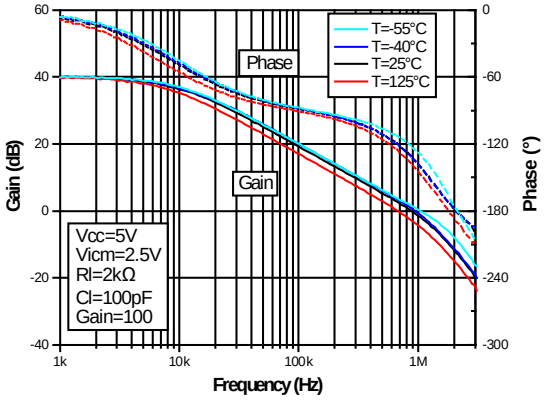


Figure 12: Slew rate vs supply voltage

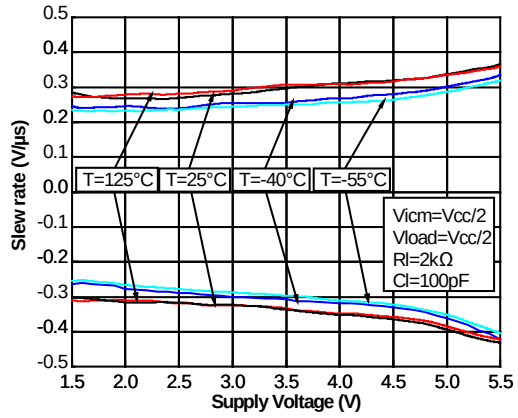


Figure 13: Negative slew rate vs supply voltage

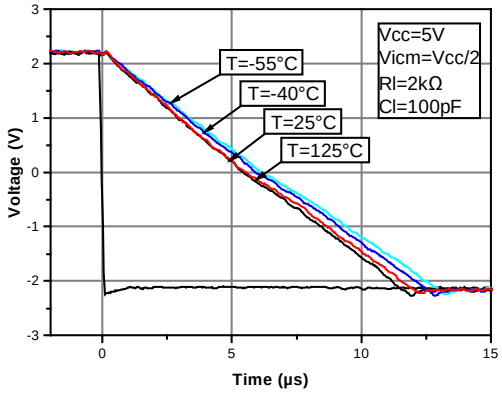


Figure 14: Positive slew rate vs supply voltage

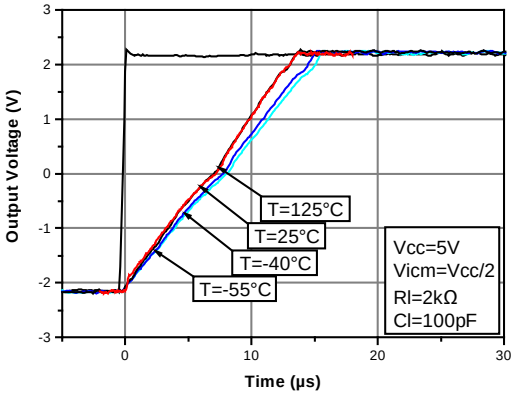


Figure 15: Phase margin vs output current at VCC = 1.5 V

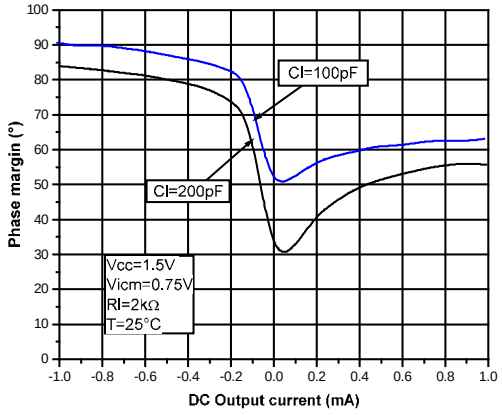


Figure 16: Phase margin vs output current at VCC = 5 V

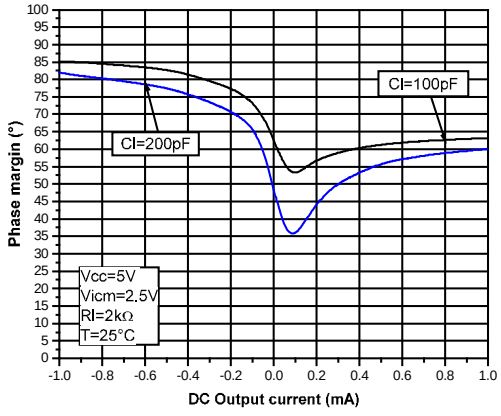


Figure 17: Noise vs frequency

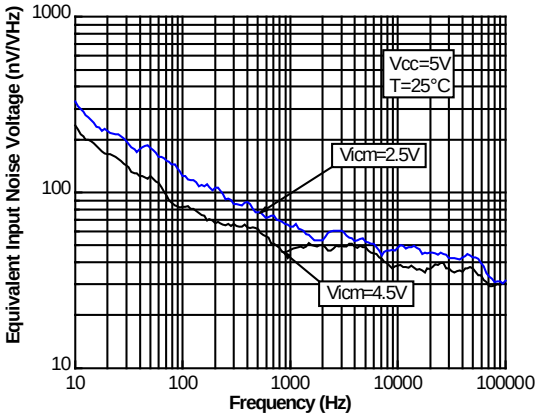


Figure 18: Small step

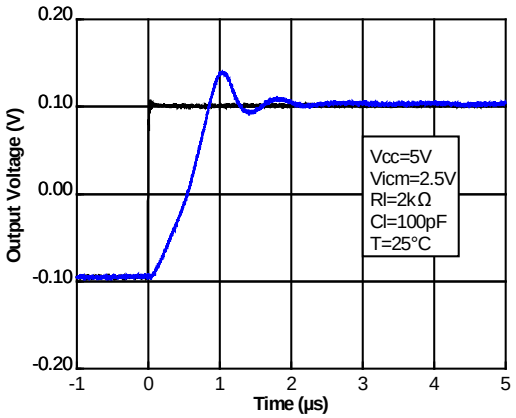


Figure 19: Power supply rejection ratio vs frequency

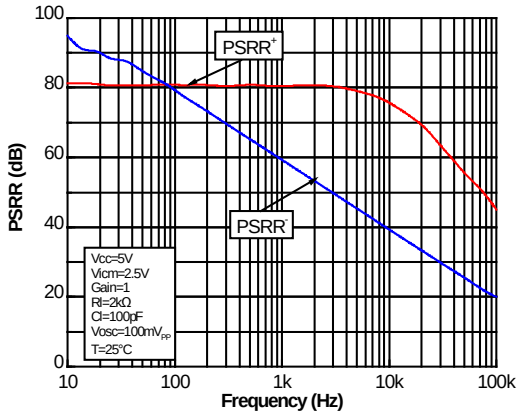


Figure 20: Total harmonic distortion and noise vs frequency and Rload

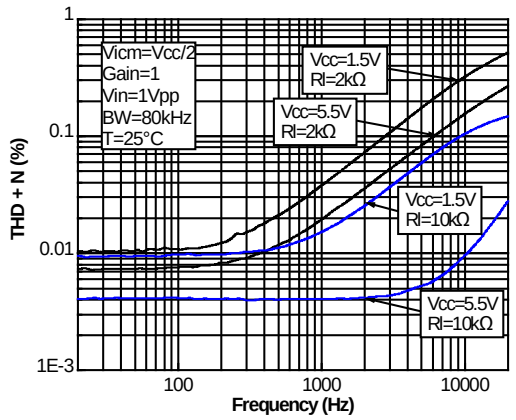


Figure 21: Total harmonic distortion and noise vs frequency and input voltage

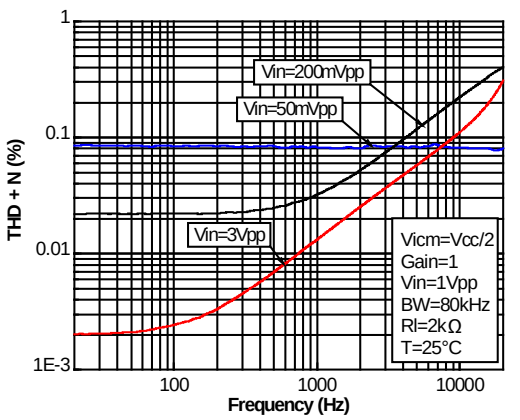


Figure 22: Total harmonic distortion and noise vs output voltage at Rload = 2 kΩ

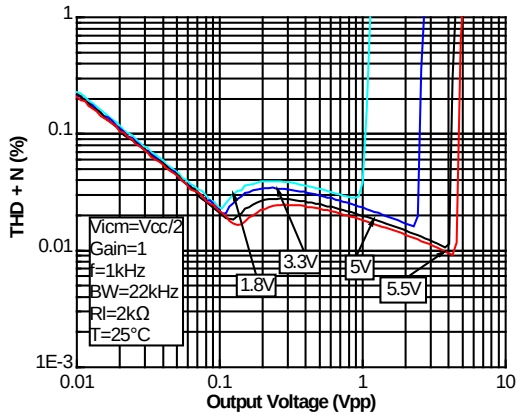
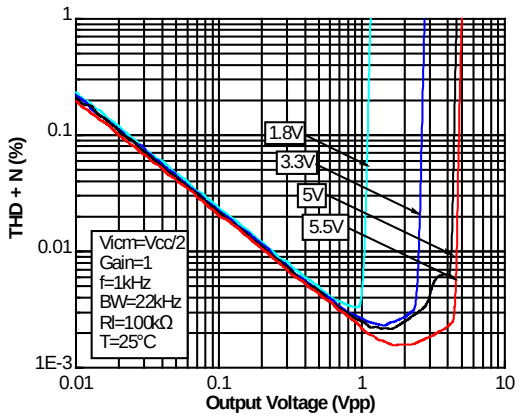


Figure 23: Total harmonic distortion and noise vs output voltage at Rload = 100 kΩ



5 Radiations

Total ionizing dose (MIL-STD-883 TM 1019)

The products guaranteed by radiation within the RHA QML-V system, fully comply with the MIL-STD-883 TM 1019 specification.

The RHR61 and RHR64 are RHA QML-V tested and characterized in full compliance with the MIL-STD-883 specification, condition B (between 10 and 100 mrad/s).

All parameters provided in *Table 4*, *Table 5*, and *Table 6* apply to pre-irradiation, *Table 7* and *Table 8* apply to post-irradiation as follows:

- All tests are performed in accordance with MIL-PRF-38535 and the test method 1019 of the MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy ions

The behavior of the product when submitted to heavy ions is not tested in production. Heavy ion trials are performed on qualification lots only.

Table 9: Radiations

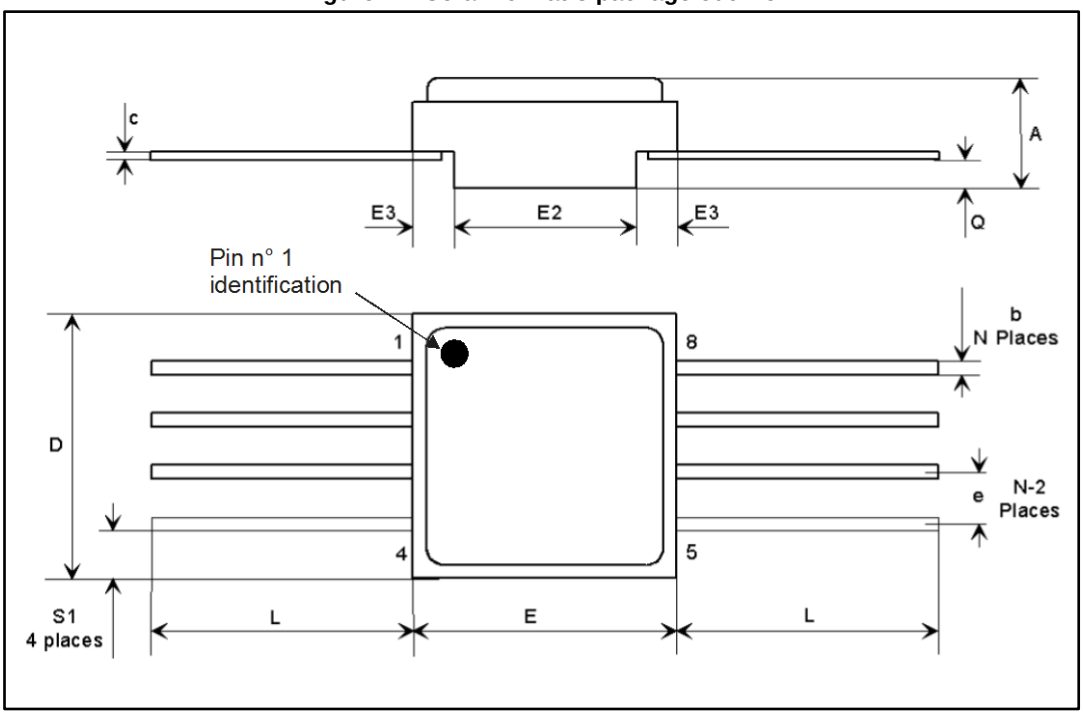
Type	Characteristics	Value	Unit
TID	Low-dose rate (36 to 360 rad/h) up to:	100	krad
Heavy ions	SEL immunity up to: (with a particle angle of 60 ° at 125 °C)	120	MeV.cm²/mg
	SEL immunity up to: (with a particle angle of 0 ° at 125 °C)	60	
	SET immunity (at 25 °C)	Characterized	

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

6.1 Ceramic Flat-8 package information

Figure 24: Ceramic Flat-8 package outline



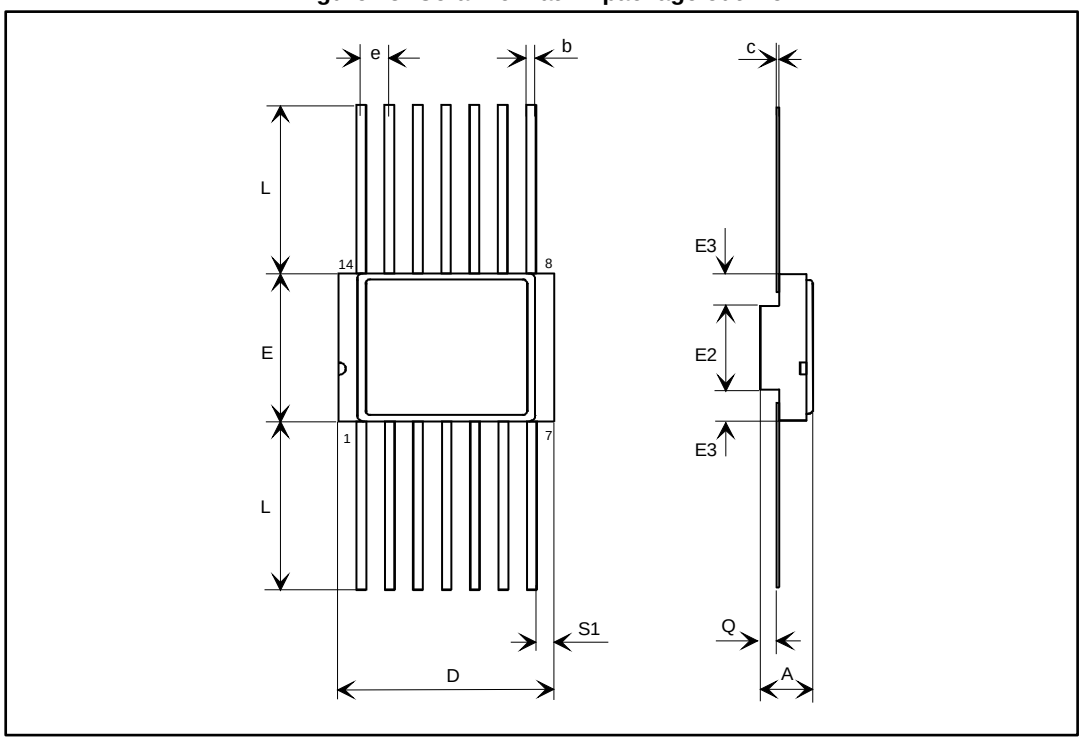
The upper metallic lid is electrically connected to pin 5. No other pin is electrically connected to the metallic lid nor to the IC die inside the package.

Table 10: Ceramic Flat-8 package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L	6.51		7.38	0.256		0.291
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

6.2 Ceramic Flat-14 package information

Figure 25: Ceramic Flat-14 package outline



The upper metallic lid is electrically connected to pin 11 (VCC-) only.

Table 11: Ceramic Flat-14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.31		2.72	0.091		0.107
b	0.38		0.48	0.015		0.019
c	0.10		0.18	0.004		0.007
D	9.27		9.73	0.365		0.383
E	6.19		6.50	0.244		0.256
E2		3.68			0.145	
E3	0.76			0.030		
e		1.27			0.050	
L	6.86		7.62	0.250		0.300
Q	0.66		1.14	0.026		0.045
S1	0.13			0.005		

7 Ordering information

Table 12: Order codes

Order code	Description	Temperature range	Package	Marking (1)	Packing
RHR61K1	Engineering model	-55 °C to 125 °C	Ceramic Flat-8	RHR61K1	Strip pack
RHR64K1			Ceramic Flat-14	RHR64K1	
RHR61K01V	QML-V flight model		Ceramic Flat-8	5962R1620401 VXC	
RHR64K01V			Ceramic Flat-14	5962R1620501 VXC	

Notes:

(1)Specific marking only. Complete marking includes the following: ST logo, Date code (date the package was sealed) in YYWWA (year, week, and lot index of week), Country of origin (FR = France).

8 Shipping information

Date code

The date code is structured as shown below:

- EM xyywwz

where:

- x (EM only) = 3 and the assembly location is Rennes, France
- yy = last two digits of the year
- ww = week digits
- z = lot index in the week

9 Revision history

Table 13: Document revision history

Date	Revision	Changes
11-May-2016	1	Initial release
21-Apr-2017	2	Removed pinout diagrams from cover image to Section 1: "Pin description", updated footnotes. Description: added order codes RHR61K01V and RHR64K01V, updated EPPL abbreviation. Table 2: "Absolute maximum ratings": updated Rthjc value for Ceramic Flat-14. Table 4, Table 5, and Table 6: updated Isource values Table 7 and Table 8: updated Isource and ICC values Table 12: "Order codes": updated table title and added order codes RHR61K01V and RHR64K01V.
05-Oct-2017	3	Updated *Table 7* and *Table 8.*

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