SN74AUP1T34 1 位单向电压电平转换器

1 特性

- 0.9V 至 3.6V 的宽运行 VCC 范围
- 均衡的传播延迟：$t_{PLH} = t_{PHL}$ （1.8V 至 3.3V 转换时的典型值）
- 低静态功耗：最大 5μA ICC
- ±6mA 输出驱动（电压为 3V 时）
- I_{off} 支持部分掉电模式运行
- VCC 隔离特性 – 如果 V_{CCA} 输入接地，则 B 端口处于高阻态
- 输入滞后可实现输入转换和输入上更好的开关噪声抗扰度
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
- 5000V 人体放电模式 (A114-A)
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 企业
- 工业
- 个人电子产品
- 电信

3 说明

SN74AUP1T34 器件是一款 1 位非反向转换器，使用两条独立的可配置电源轨。它是一个从 A 至 B 的单向转换器。A 端口设计用来跟踪 V_{CCA}。V_{CCA}可接受从 0.9V 到 3.6V 范围内的电源电压。B 端口设计用于跟踪 V_{CCB}。V_{CCB}可接受从 0.9V 至 3.6V 间的电源电压值。这可实现 1V，1.2V，1.5V，1.8V，2.5V 和 3.3V 电压节点间的低压转换。此外，SN74AUP1T34 完全 适用于 使用 I_{off} 的局部掉电应用。I_{off} 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。

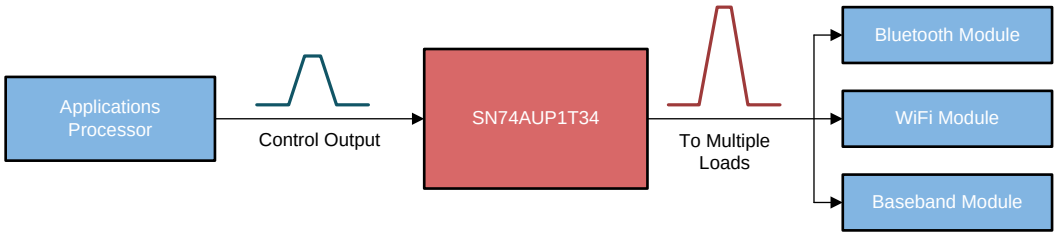
VCC 隔离特性确保了在 V_{CCA}输入在 GND 上时，B 端口处于高阻抗状态。如果 V_{CCB}输入在 GND 上，到 A 侧的任一输入都不会导致泄漏电流，即使在悬空状态时也是如此。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74AUP1T34DCK	SC70 (5)	2.00mm × 1.25mm
SN74AUP1T34DRY	SON (6)	1.45mm x 1.00mm
SN74AUP1T34DSF	SON (6)	1.00mm x 1.00mm

(1) 要了解所有可用封装，参阅数据表末尾的可订购产品附录。

示例应用



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (June 2016) to Revision F **Page**

- Added operating junction temperature to *Absolute Maximum Ratings* table ... 5
- Updated *Recommended Operating Conditions* table ... 6
- Updated the V_{CCB} value for the parameter 'high-level input voltage' in the *Recommended Operating Conditions* table ... 6
- Updated the V_{CCB} value for the parameter 'low-level input voltage' in the *Recommended Operating Conditions* table ... 6
- Added *Electrical Characteristics: DC* table ... 7

Changes from Revision D (April 2016) to Revision E **Page**

- Changed pin A number From: 3 To: 2 and GND From: 2 To: 3 for the SC70 package in the *Pin Configuration and Functions* section ... 4

Changes from Revision C (May 2013) to Revision D **Page**

- 添加了 *ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1
- 已删除*订购信息*表 ... 1

Changes from Revision B (July 2012) to Revision C **Page**

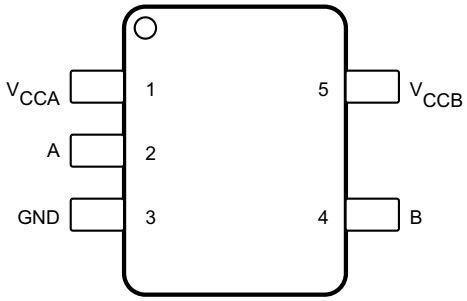
- 已添加特性：VCC 隔离特性 – 如果 V_{CCA} 输入接地，则 B 端口处于高阻态。 ... 1
- Updated *Pin Functions* table. ... 4
- Deleted I_{OZ} PARAMETER from RECOMMENDED OPERATION CONDITIONS. ... 6
- Added V_{MI} and V_{MO} equations to Wavefrom 1 graphic. ... 10
- 已添加 FUNCTION TABLE. ... 12

Changes from Revision A (June 2012) to Revision B **Page**

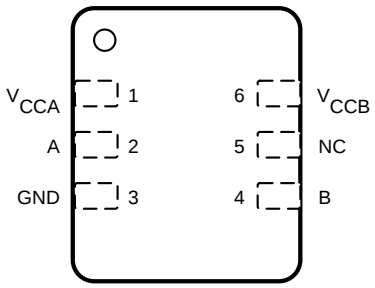
- 已删除特性：输出使能特性方便用户禁用输出，从而降低功耗。 1

5 Pin Configuration and Functions

DCK Package
5-Pin SC70
Top View



DRY or DSF Package
6-Pin SON
Top Through View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SC70	SON		
A	2	2	I	Input Port
B	4	4	O	Output Port
GND	3	3	—	Ground
V_{CCA}	1	1	—	Input Port DC Power Supply
V_{CCB}	5	6	—	Output Port DC Power Supply
NC	—	5	—	No Connect. Leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CCA} and V_{CCB}		–0.3	4	V
Input voltage, V_I		–0.5	4.6	V
		–0.5	4.6	
		–0.5	4.6	
Voltage applied to any output in the high-impedance or power-off state, V_O		–0.5	4.6	V
		–0.5	4.6	
Voltage applied to any output in the high or low state, V_O		–0.5	4.6	V
		–0.5	4.6	
Input clamp current, I_{IK}	V_I < 0 V		–50	mA
Output clamp current, I_{OK}	V_O < 0 V		–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CCA} or GND			±100	mA
Storage temperature, T_{stg}		–65	150	°C
Operating junction temperature, T_J			150	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage			0.9		3.6	V
V_{CCB}	Supply voltage			0.9		3.6	V
V_{IH}	High-level input voltage	V_{CCA} = 0.9 V to 1.95 V	V_{CCB} = 0.9 V to 3.6 V	0.65 × V_{CCA}			V
		V_{CCA} = 2.3 V to 2.7 V	V_{CCB} = 0.9 V to 3.6 V	1.6			
		V_{CCA} = 3 V to 3.6 V	V_{CCB} = 0.9 V to 3.6 V	2			
V_{IH}	Low-level input voltage	V_{CCA} = 0.9 V	V_{CCB} = 0.9 V to 3.6 V			0.3 × V_{CCA}	V
		V_{CCA} = 1 V to 1.95 V	V_{CCB} = 0.9 V to 3.6 V			0.35 × V_{CCA}	
		V_{CCA} = 2.3 V to 2.7 V	V_{CCB} = 0.9 V to 3.6 V			0.7	
		V_{CCA} = 3 V to 3.6 V	V_{CCB} = 0.9 V to 3.6 V			0.9	
Δt/Δv	Input transition rise or fall rate	V_{CCA} = 3 V to 3.6 V	V_{CCB} = 0.9 V to 3.6 V			200	ns/V
T_A	Operating free-air temperature			–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74AUP1T34			UNIT
		DCK (SC70)	DRY (SON)	DSF (SON)	
		5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	300.8	338.5	367.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	141.3	240.4	188.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.3	224.6	274.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.6	86.8	24.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.5	221.4	273.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: DC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = –100 µA	0.9 V to 3.6 V	0.9 V to 3.6 V	V_{CCB} – 0.2		V
			I_{OH} = –0.25 mA	0.9 V to 1 V	0.9 V to 1 V	0.75 × V_{CCB}		
			I_{OH} = –1.5 mA	1.2 V	1.2 V	1		
			I_{OH} = –2 mA	1.65 V	1.65 V	1.32		
			I_{OH} = –3 mA	2.3 V	2.3 V	1.9		
			I_{OH} = –6 mA	3 V	3 V	2.72		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.9 V to 3.6 V	0.9 V to 3.6 V		0.1	V
			I_{OL} = 0.25 mA	0.9 V to 1 V	0.9 V to 1 V		0.1	
			I_{OL} = 1.5 mA	1.2 V	1.2 V		0.3 × V_{CCB}	
			I_{OL} = 2 mA	1.65 V	1.65 V		0.31	
			I_{OL} = 3 mA	2.3 V	2.3 V		0.31	
			I_{OL} = 6 mA	3 V	3 V		0.31	
I_I	Input leakage current	V_I = VCCA or GND		0.9 V to 3.6 V	0.9 V to 3.6 V		±1	µA
I_{off}	Off-state current	A or B port: V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±5	µA
				0 V to 3.6 V	0 V		±5	
I_{CCA}	V_{CCA} supply current	V_I = VCCI or GND, I_O = 0 mA		0.9 V to 3.6 V	0.9 V to 3.6 V		5	µA
				0.9 V to 3.6 V	V_{CCA}		2	
				0 V	0 V to 3.6 V		1	
				0 V to 3.6 V	0 V		1	
I_{CCB}	V_{CCB} supply current	V_I = VCCI or GND, I_O = 0 mA		0.9 V to 3.6 V	0.9 V to 3.6 V		5	µA
				0.9 V to 3.6 V	V_{CCA}		2	
				0 V	0 V to 3.6 V		1	
				0 V to 3.6 V	0 V		1	
I_{CCA} + I_{CCB}	Combined supply current	V_I = VCCI or GND, I_O = 0 mA		0.9 V to 3.6 V	0.9 V to 3.6 V		5.2	µA
C_I	Input capacitance	V_I = 3.3 V or GND		3.3 V	3.3 V		4	pF
$C_{I/O}$	Input-to-output internal capacitance	A or B port: V_O = 3.3 V or GND		0 V	3.3 V		7	pF

6.6 Electrical Characteristics: AC

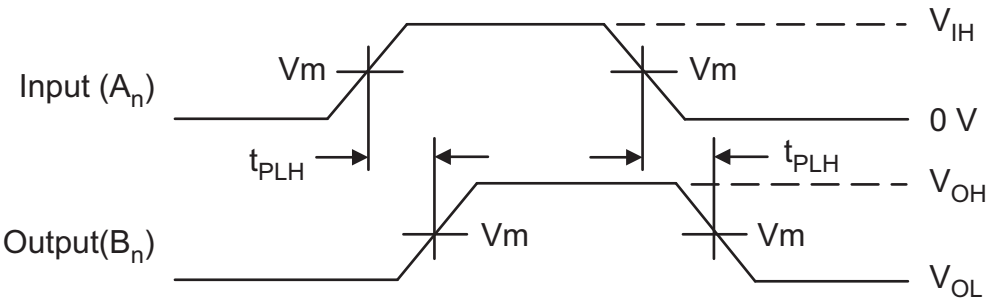
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}/t_{PHL}	Propagation delay time low-to-high output / high-to-low output	C_L = 5 pF	0.9 V	0.9 V		25		ns
				1.2 V		18		
				1.65 V		16.2		
				2.3 V		16.3		
				3 V		16.8		
		C_L = 5 pF	1.2 V	0.9 V			42.5	
				1.2 V			24.9	
				1.65 V			23.2	
				2.3 V			22.6	
				3 V			22.5	
		C_L = 5 pF	1.65 V	0.9 V			40	
				1.2 V			10.7	
				1.65 V			8.84	
				2.3 V			8.08	
				3 V			7.88	
		C_L = 5 pF	2.3 V	0.9 V			41.3	
				1.2 V			8.02	
				1.65 V			5.73	
				2.3 V			4.92	
				3 V			4.2	
		C_L = 5 pF	3 V	0.9 V			42.5	
				1.2 V			7.61	
				1.65 V			4.5	
				2.3 V			3.65	
				3 V			3.39	
t_{PLH}/t_{PHL}	Propagation delay time low-to-high output / high-to-low output	C_L = 10 pF	0.9 V	0.9 V		28.9		ns
				1.2 V		19.8		
				1.65 V		17.9		
				2.3 V		18		
				3 V		18.5		
		C_L = 10 pF	1.2 V	0.9 V			43.22	
				1.2 V			12.33	
				1.65 V			9.57	
				2.3 V			8.81	
				3 V			8.61	
		C_L = 10 pF	1.65 V	0.9 V			40.44	
				1.2 V			9.21	
				1.65 V			6.57	
				2.3 V			5.5	
				3 V			4.73	
		C_L = 10 pF	2.3 V	0.9 V			41.56	
				1.2 V			8.3	
				1.65 V			5.54	
				2.3 V			4.42	
				3 V			4.01	
		C_L = 10 pF	3 V	0.9 V			42.81	
				1.2 V			7.87	
				1.65 V			4.55	
				2.3 V			3.8	
				3 V			3.36	

Electrical Characteristics: AC (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}/t_{PHL}	Propagation delay time low-to-high output / high-to-low output	C_L = 15 pF	0.9 V	0.9 V		30.6		ns
				1.2 V		21.6		
				1.65 V		19.6		
				2.3 V		19.7		
				3 V		20.3		
		C_L = 15 pF	1.2 V	0.9 V			43.87	
				1.2 V			12.98	
				1.65 V			10.3	
				2.3 V			9.54	
				3 V			9.34	
		C_L = 15 pF	1.65 V	0.9 V			40.78	
				1.2 V			9.59	
				1.65 V			6.95	
				2.3 V			5.87	
				3 V			5.07	
		C_L = 15 pF	2.3 V	0.9 V			41.79	
				1.2 V			8.55	
				1.65 V			5.8	
				2.3 V			4.68	
				3 V			4.27	
		C_L = 15 pF	3 V	0.9 V			43.09	
				1.2 V			8.16	
				1.65 V			4.84	
				2.3 V			4.09	
				3 V			3.65	
t_{PLH}/t_{PHL}	Propagation delay time low-to-high output / high-to-low output	C_L = 30 pF	0.9 V	0.9 V		32.1		ns
				1.2 V		21.3		
				1.65 V		18.7		
				2.3 V		18		
				3 V		18.3		
		C_L = 30 pF	1.2 V	0.9 V			45.65	
				1.2 V			14.76	
				1.65 V			12.37	
				2.3 V			11.61	
				3 V			11.41	
		C_L = 30 pF	1.65 V	0.9 V			41.72	
				1.2 V			10.65	
				1.65 V			8.01	
				2.3 V			6.94	
				3 V			5.99	
		C_L = 30 pF	2.3 V	0.9 V			42.44	
				1.2 V			9.26	
				1.65 V			6.51	
				2.3 V			5.39	
				3 V			4.97	
		C_L = 30 pF	3 V	0.9 V			43.69	
				1.2 V			8.8	
				1.65 V			5.48	
				2.3 V			4.72	
				3 V			4.28	



V_{MI} =V_{IH}/2; V_{MO}= V_{CCB}/2

t_R = t_F = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 1. Waveform 1 – Propagation Delays

6.7 Typical Characteristics

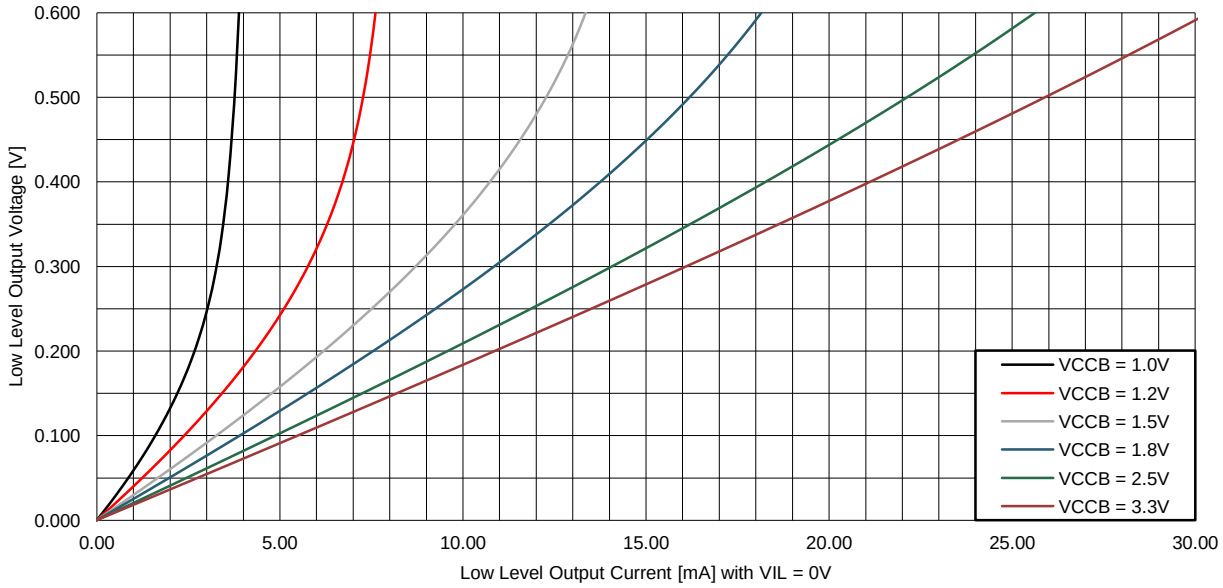
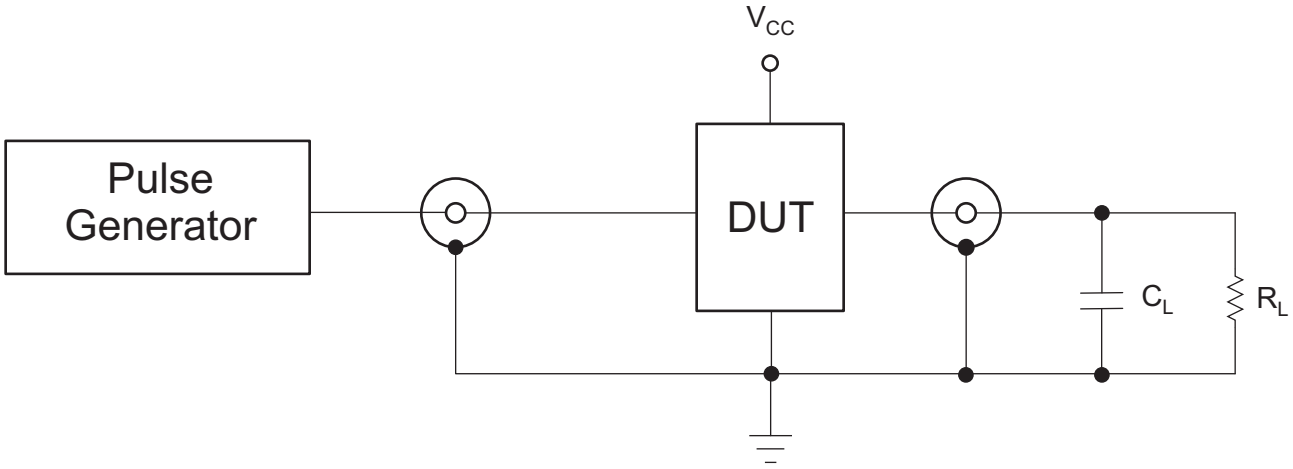


图 2. Low Level Output Voltage vs Low Level Output Current

7 Parameter Measurement Information



TEST

t_{PLH}, t_{PHL}

C_L = 5 pF, 10 pF, 15 pF, 30 pF or equivalent (includes probe and jig capacitance)

R_L = 1 MΩ or equivalent

Z_{OUT} of pulse generator = 50 Ω

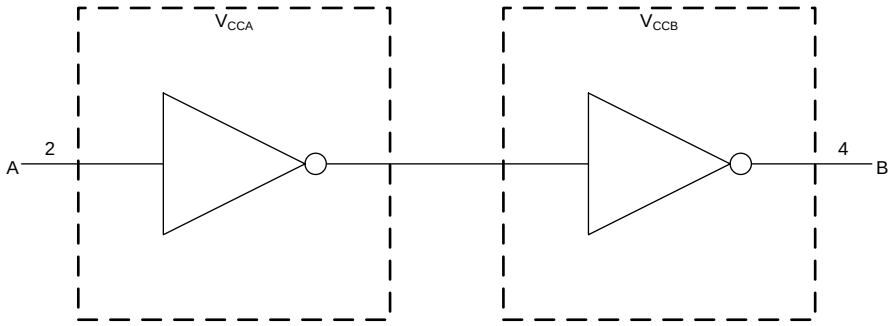
图 3. AC (Propagation Delay) Test Circuit

8 Detailed Description

8.1 Overview

The SN74AUP1T34 is a unidirectional, single-bit, dual-supply, noninverting voltage-level translator. Pin A, which is referenced to V_{CCA}, receives the signal that is to be level translated. Pin B, which is referenced to V_{CCB}, transmits the level translated signal. Both supply pins V_{CCA} and V_{CCB} support a voltage range from 0.9 V to 3.6 V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 0.9 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (1 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Partial-Power-Down Mode Operation

I_{off} circuitry disables the outputs, preventing damaging current backflow through the SN74AUP1T34 when it is powered down. This can occur in applications where subsections of a system are powered down (partial-power-down) to reduce power consumption.

8.3.3 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND (or < 0.4 V), both ports A and B are set to a high-impedance state, preventing false logic levels from being presented to either bus.

8.3.4 Input Hysteresis

Input hysteresis allows the input to support slew rates as slow as 200 ns/V, improving switching noise immunity.

8.4 Device Functional Modes

表 1 lists the functional modes of the SN74AUP1T34.

表 1. Function Table

INPUT	OUTPUT
A PORT	**B PORT**
L	L
H	H

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AUP1T34 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

9.2 Typical Application

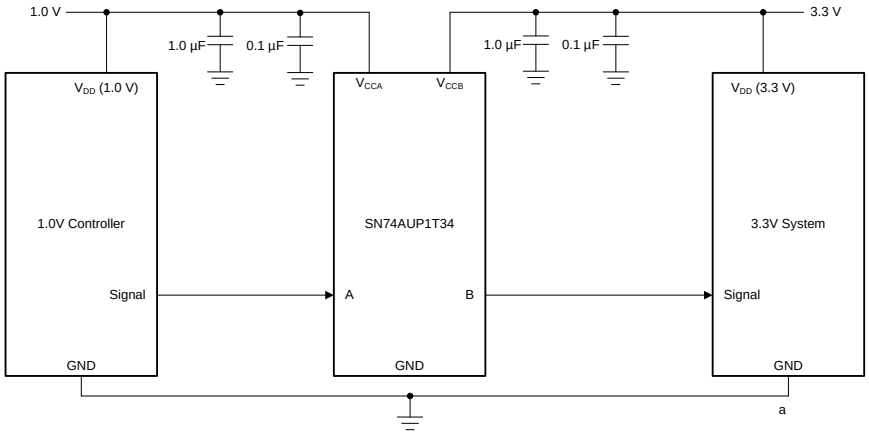


图 4. Typical Application Example

9.2.1 Design Requirements

表 2 lists the design requirements of the SN74AUP1T34.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0.9 V to 3.6 V
Output Voltage Range	0.9 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AUP1T34 device to determine the input voltage range. For a valid logic-high, the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AUP1T34 device is driving to determine the output voltage range.

9.2.3 Application Curve

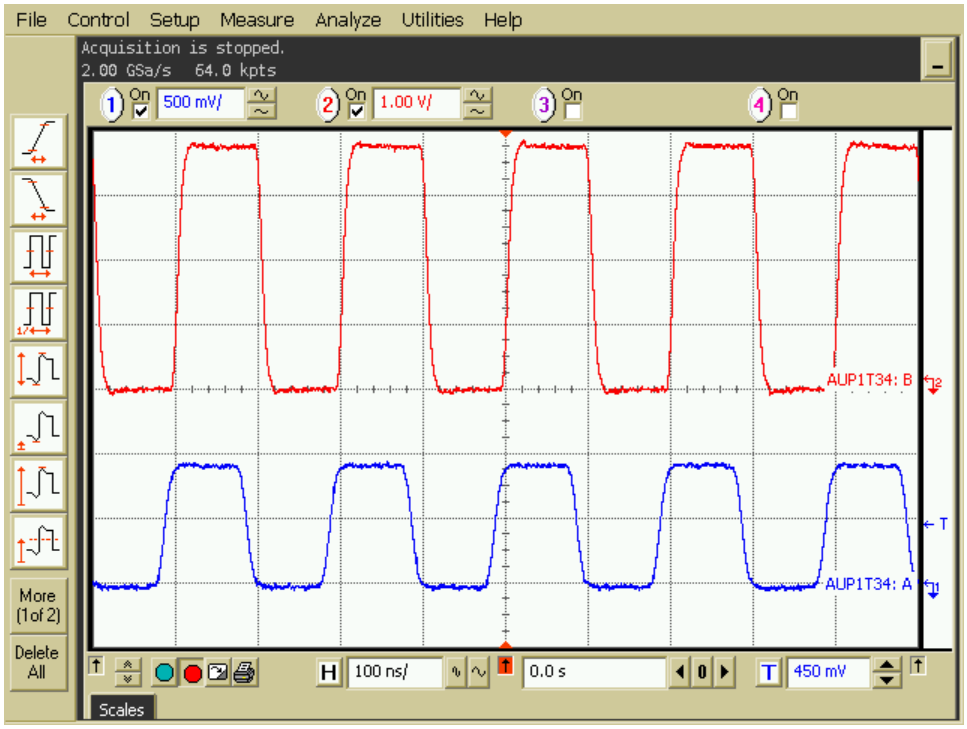


图 5. 10-MHz Up Translation (0.9 V to 3.6 V)

10 Power Supply Recommendations

Connect ground before applying either V_{CCA} or V_{CCB}. There is no specific power sequence requirement for the SN74AUP1T34. V_{CCA} or V_{CCB} may be powered up first, and V_{CCA} or V_{CCB} may be powered down first.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

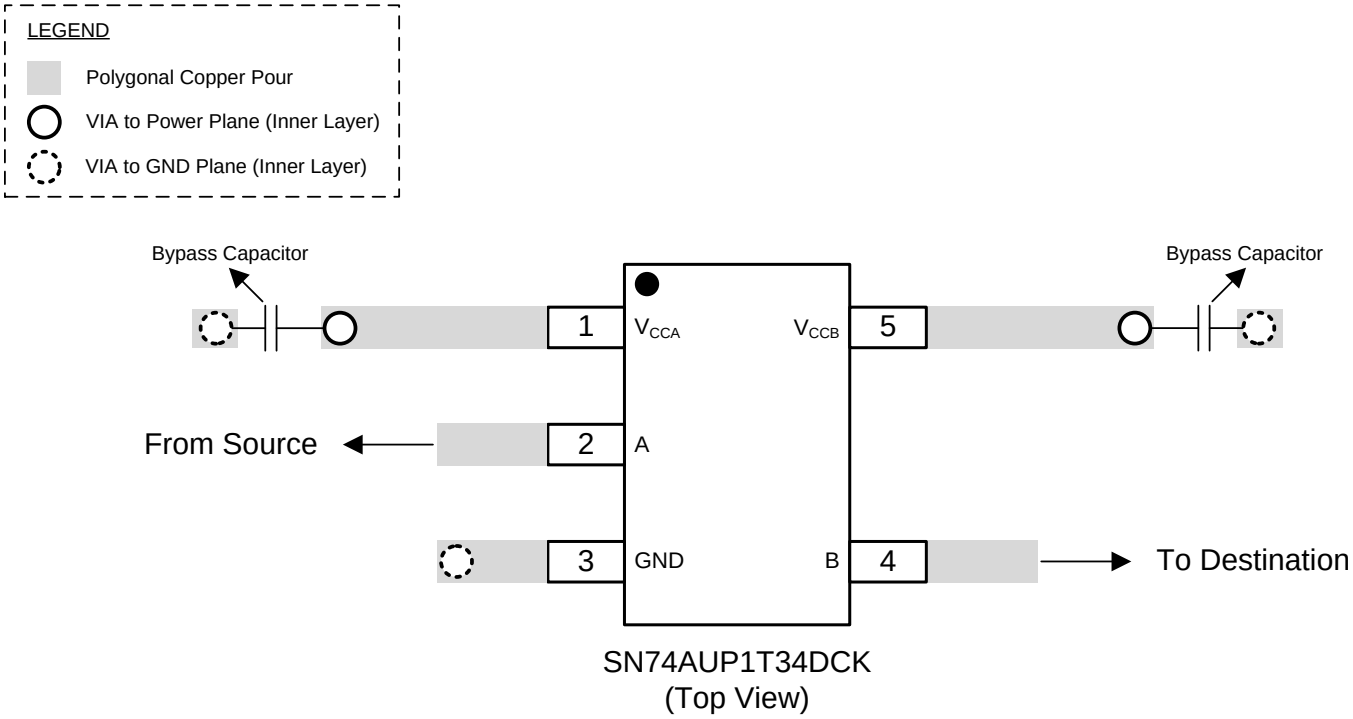


图 6. Example Layout

12 器件和文档支持

12.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T34DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U2E	Samples
SN74AUP1T34DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U2	Samples
SN74AUP1T34DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AUP1T34 :

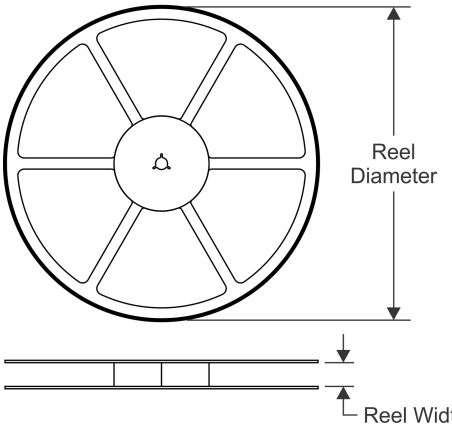
- Automotive : SN74AUP1T34-Q1

NOTE: Qualified Version Definitions:

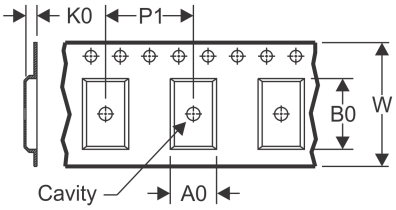
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

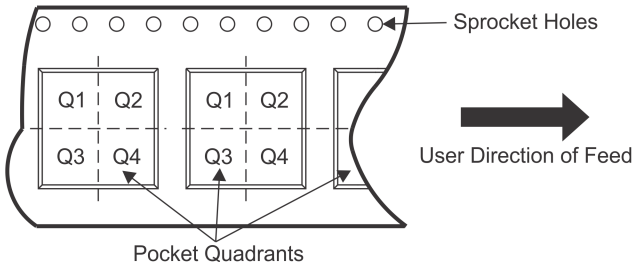


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

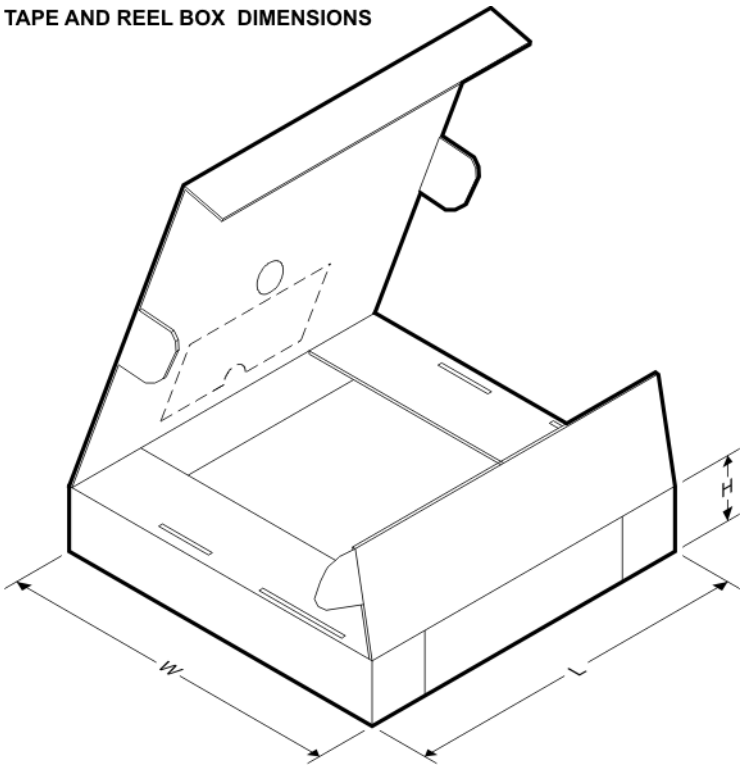
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T34DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP1T34DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1T34DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

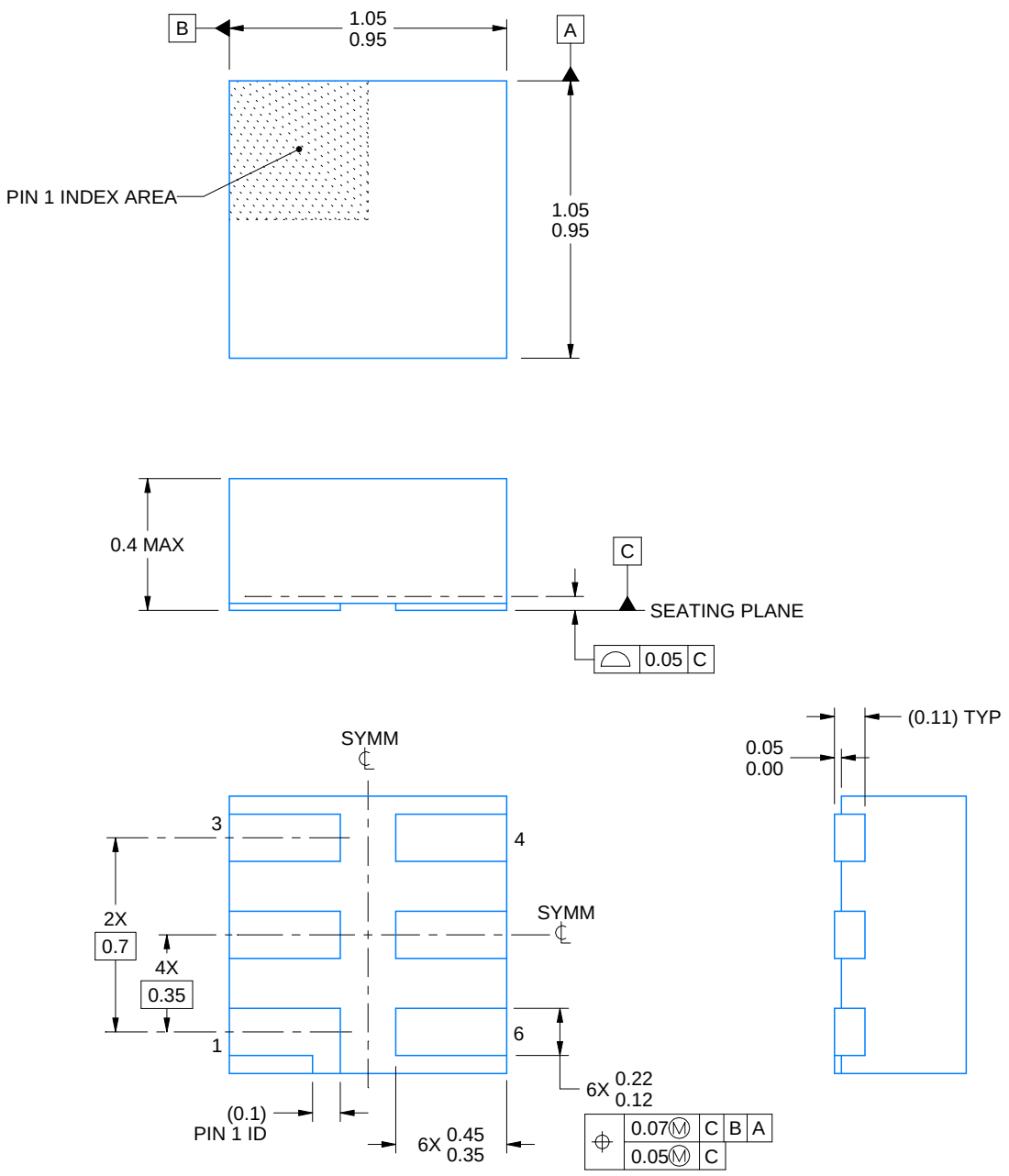
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T34DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1T34DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1T34DSFR	SON	DSF	6	5000	184.0	184.0	19.0

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

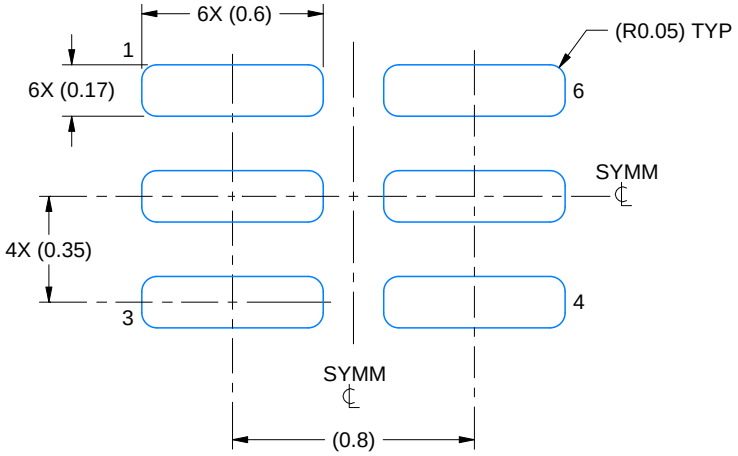
PLASTIC SMALL OUTLINE - NO LEAD



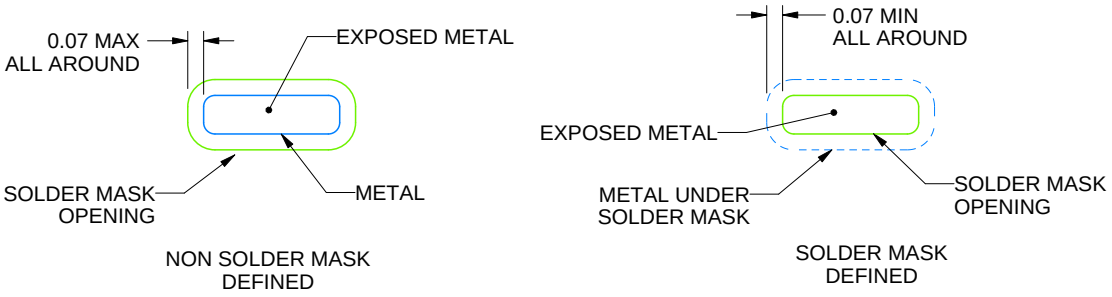
4220597/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

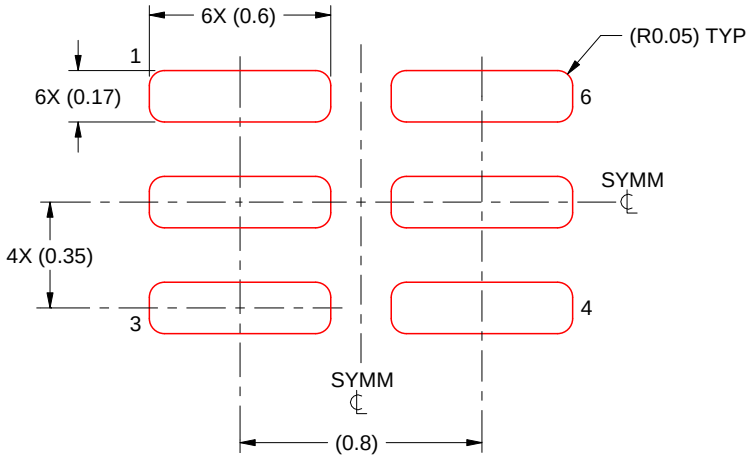
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



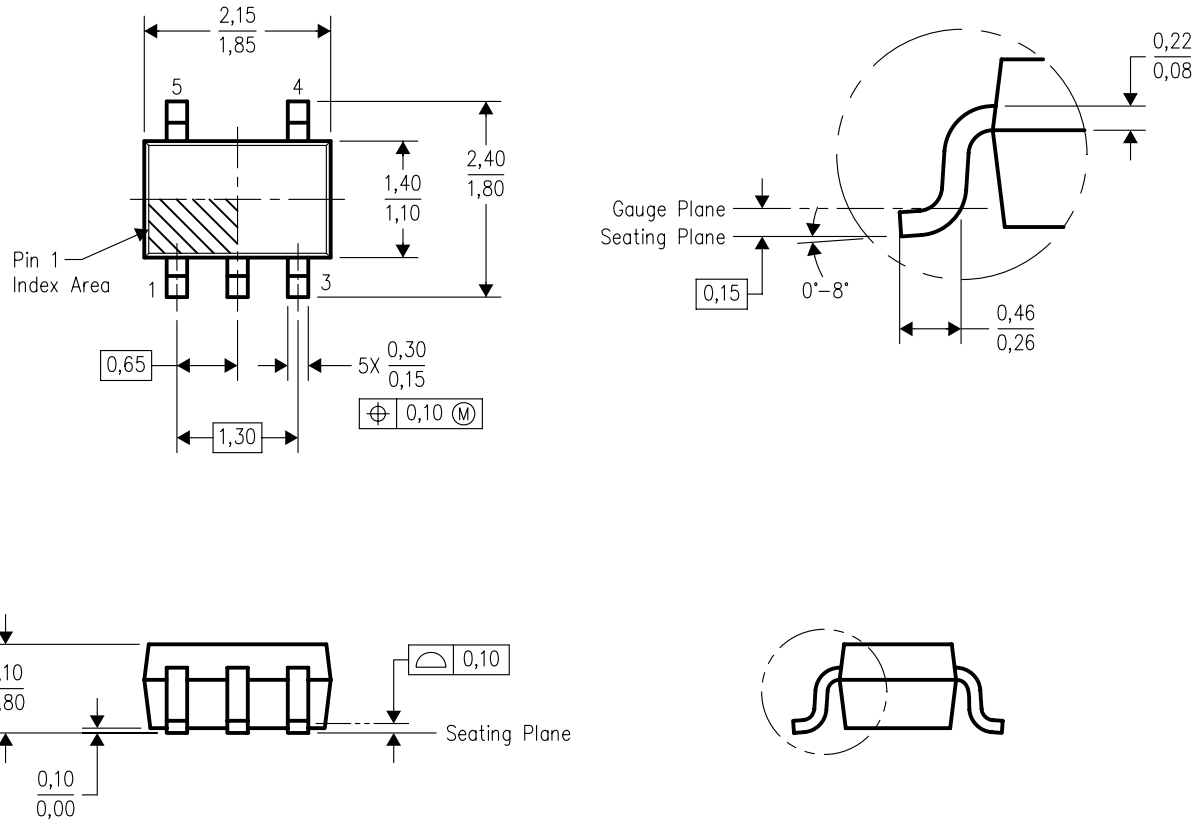
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

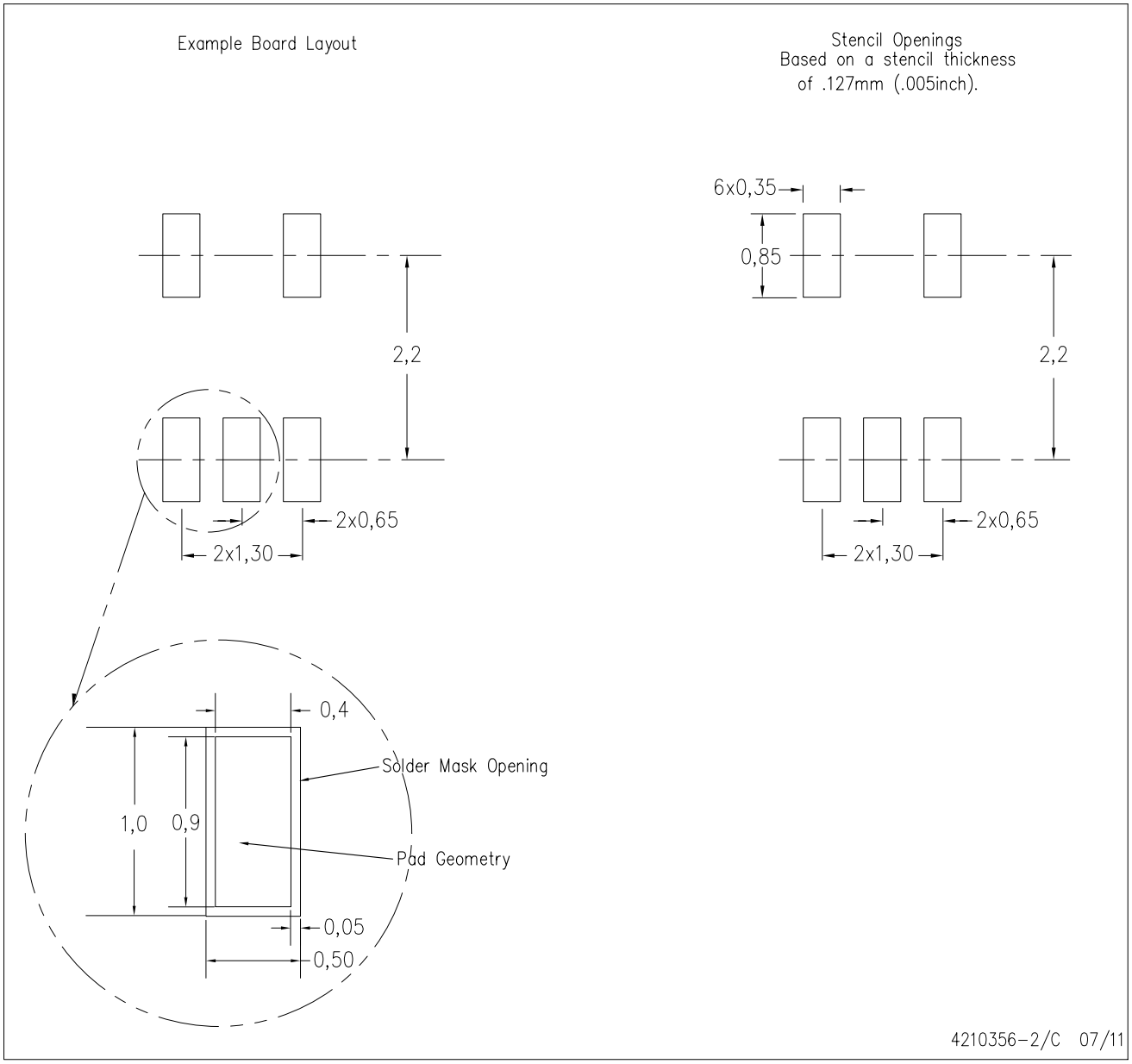
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



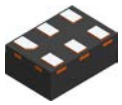
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

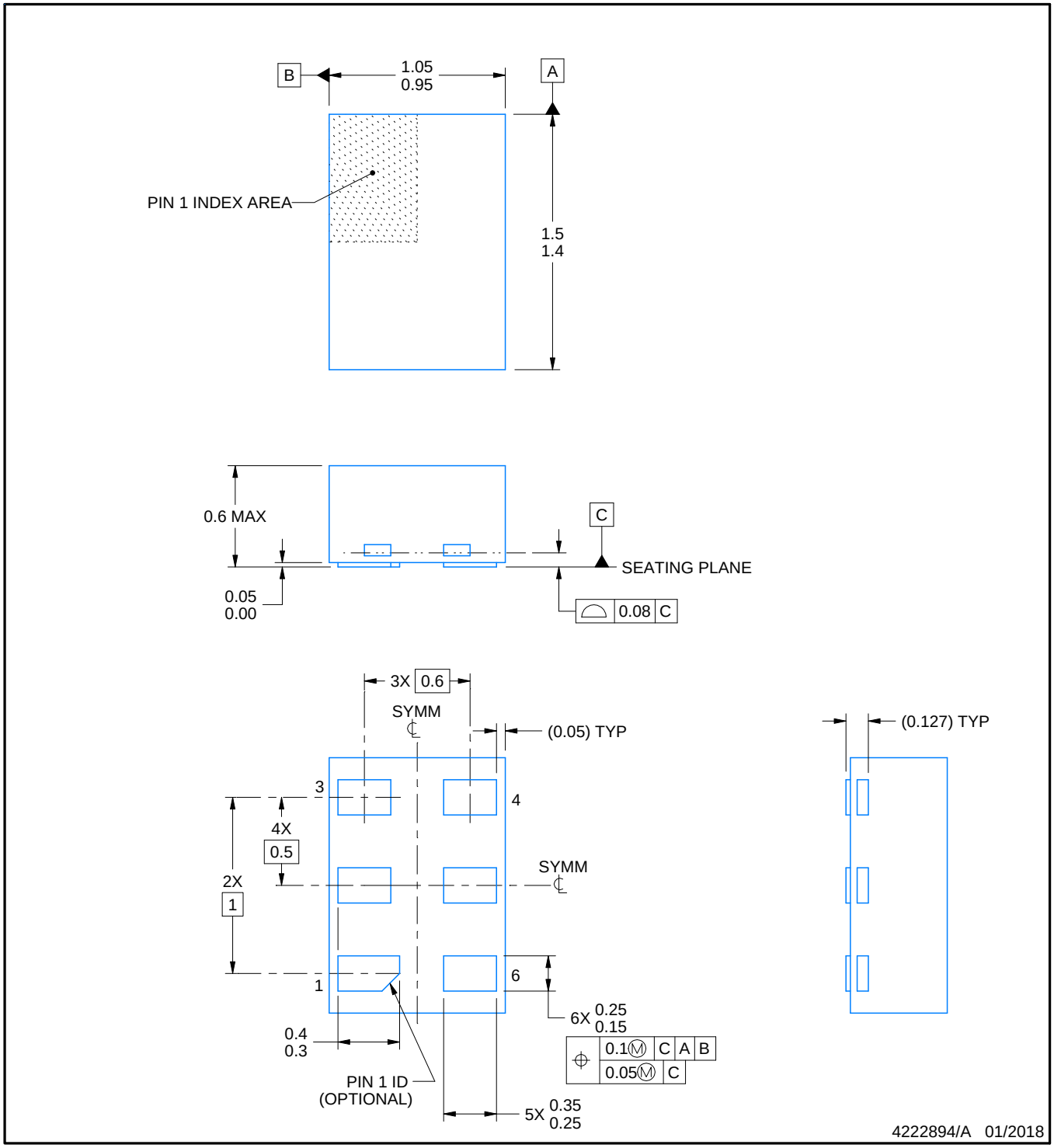
DRY0006A



PACKAGE OUTLINE

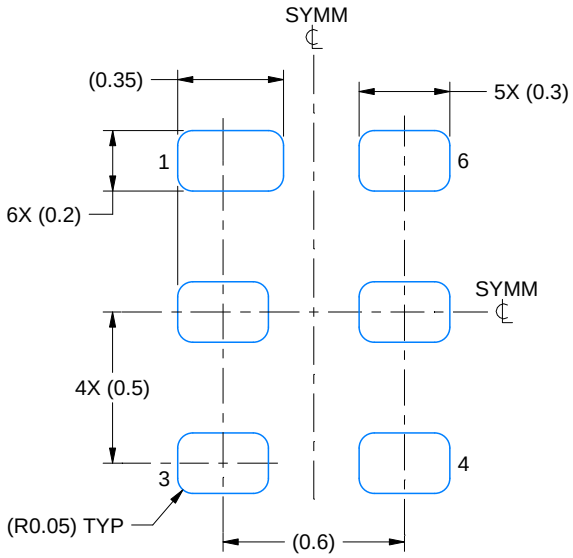
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

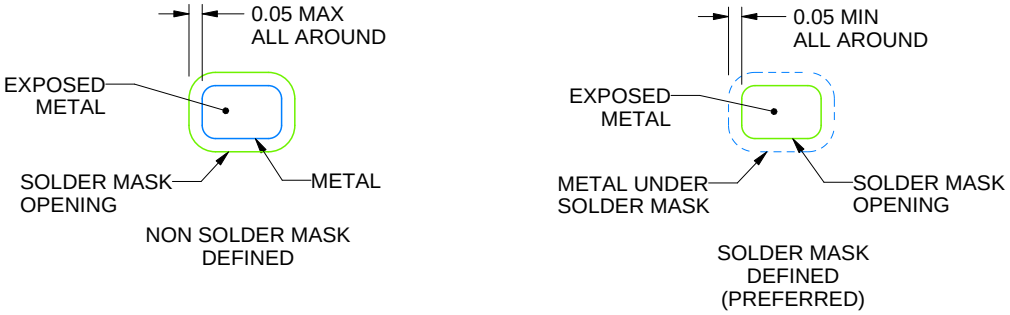


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

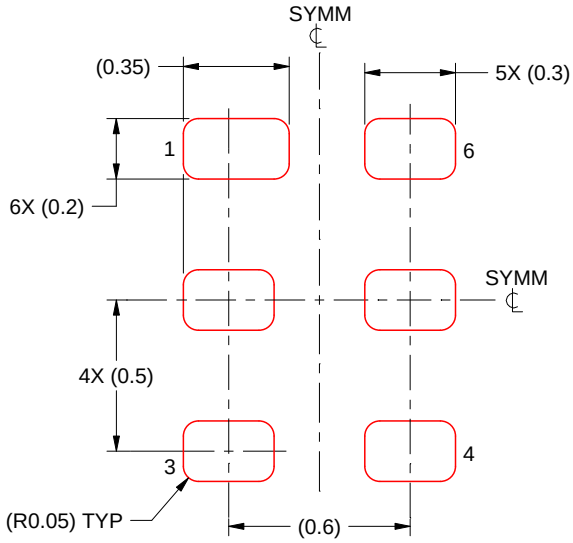
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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