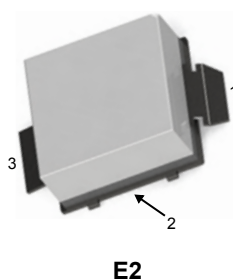


20 W, 28 V, 0.7 to 3.6 GHz RF power LDMOS transistor



Pin connection	
Pin	Connection
1	Drain
2	Source (bottom side)
3	Gate

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
ST36015	3450 MHz	28 V	20 W	12.4 dB	42%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internal input matching for ease of use
- Large positive and negative gate/source voltage range
- In compliance with the European Directive 2002/95/EC

Applications

- Telecom and wideband communication
- Industrial, scientific and medical (ISM)

Description

The ST36015 is a 20 W internally matched LDMOS transistor designed for cellular base stations and ISM applications at frequencies from 0.7 to 3.6 GHz.

Product status link
ST36015

Product summary	
Order code	ST36015
Marking	ST36015
Package	E2
Packing	Tape and reel 13"
Base / Bulk qty	300 / 300

1 Electrical ratings

Table 1. Absolute maximum ratings (+25 °C)

Symbol	Parameter	Value	Unit
B _{VDSS}	Drain-source voltage	65	V
V _{GS}	Gate-source voltage	-6/+10	V
V _{DD}	Drain supply voltage	32	V
T _{STG}	Storage temperature range	-65 to +150	°C
T _J	Junction temperature	+200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Junction-case thermal resistance T _{CASE} = +80 °C , T _J = +200 °C, DC test	2	°C/W

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to JESD22-A114)	2

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static (per side)

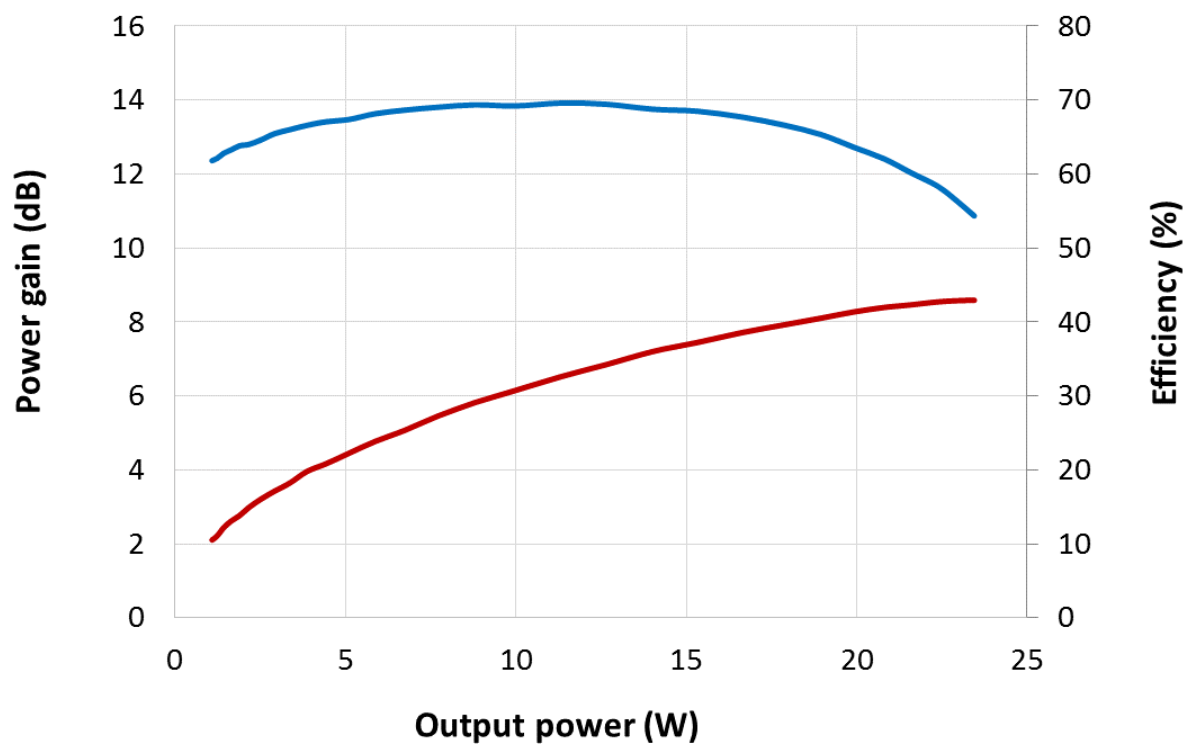
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 100\text{ }\mu\text{A}$	65			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 28\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$			1	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = 10\text{ V}$			1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 28\text{ V}$, $I_D = 600\text{ }\mu\text{A}$	1.5		2.5	V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}$, $I_D = 200\text{ mA}$			0.25	V
C_{ISS}	Common source input capacitance	$V_{GS} = 0\text{ V}$, $V_{DD} = 28\text{ V}$, $f = 1\text{ MHz}$		37		pF
C_{RSS}	Common source feedback capacitance			0.3		pF
C_{OSS}	Common source output capacitance			8.4		pF

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	$V_{DD} = 28\text{ V}$, $I_{DQ} = 10\text{ mA}$, $f = 3450\text{ MHz}$, $PW = 10\text{ }\mu\text{s}$, $DC = 10\%$	-	20	-	W
Gain	Power gain		-	12.4	-	dB
Efficiency	Drain efficiency		-	42	-	%
VSWR	Load mismatch	$P_{OUT} = 20\text{ W}$, all phases	-	10:1	-	

2.1 Electrical characteristics (curves)

Figure 1. Power gain and drain efficiency vs output power at 3450 MHz



GADG070920181048IG

3 Circuit layout

Figure 2. Circuit layout

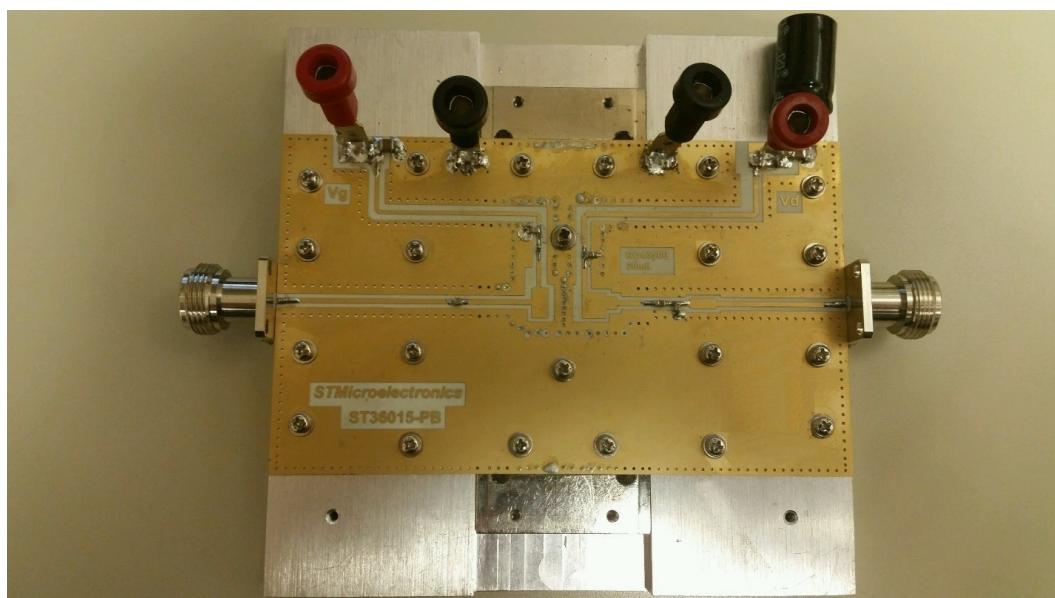
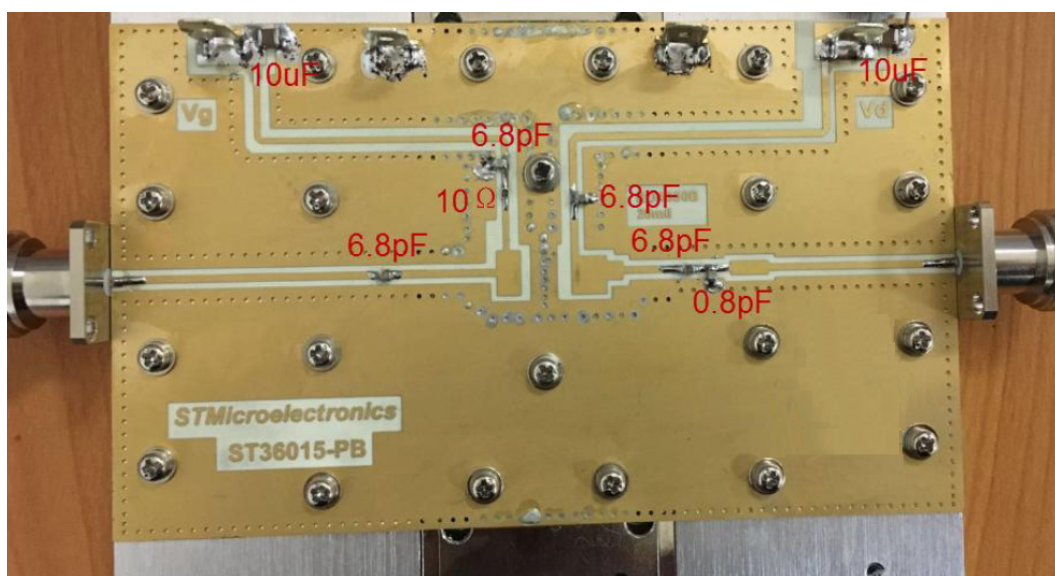


Figure 3. Component list

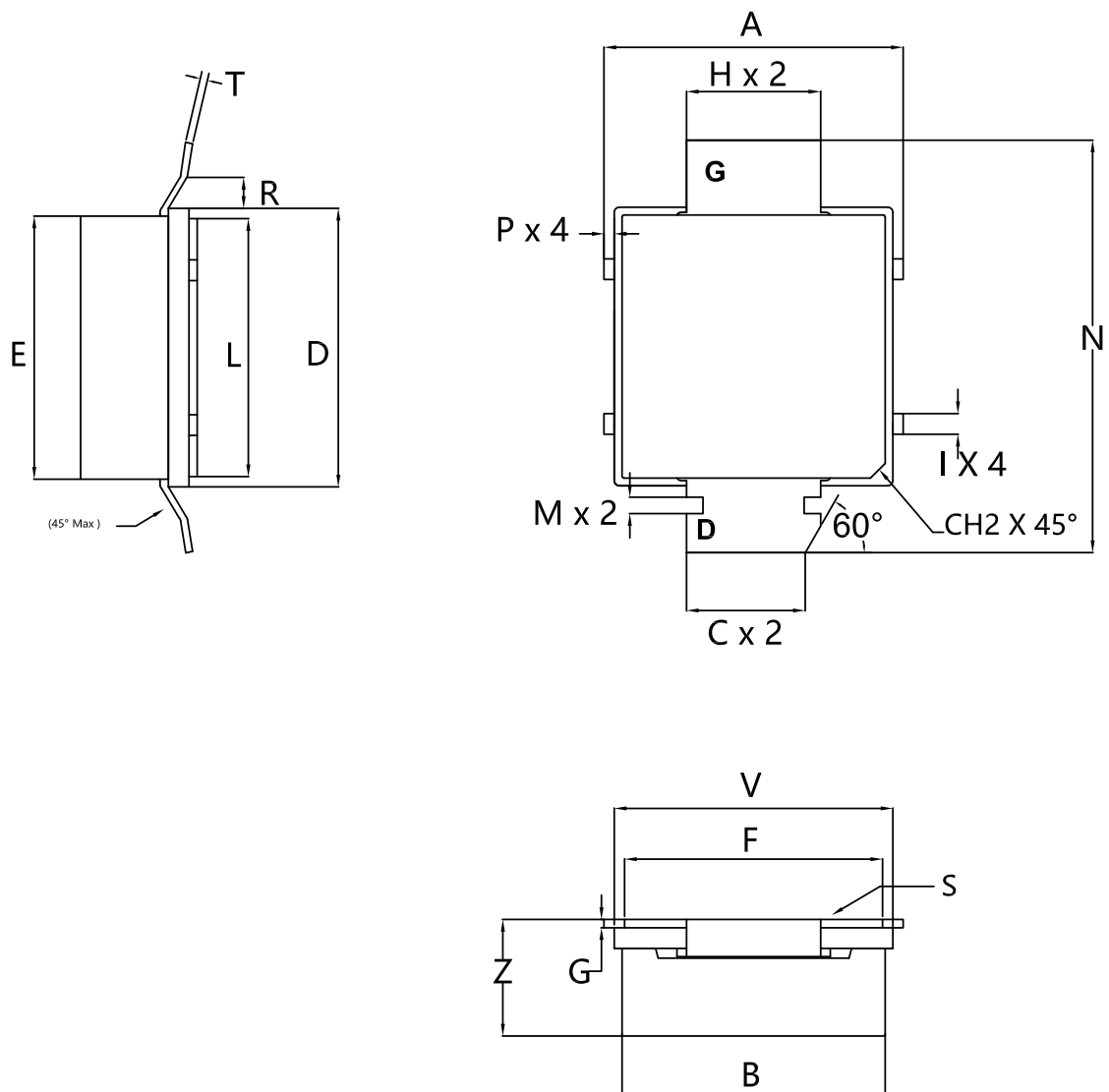


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 E2 package information

Figure 4. E2 package outline



00418523_4

Table 6. E2 mechanical data

Symbol	Millimetres		
	Min.	Typ.	Max.
A			7.37
B	6.35	6.48	6.60
C	2.84	2.92	3.0
D	6.78	6.86	6.94
E	6.35	6.48	6.61
F	6.10	6.35	6.60
G	0.18	0.20	0.23
H	3.23	3.30	3.38
I	0.43	0.51	0.59
L	6.27	6.35	6.43
M	0.33	0.41	0.49
N	10.03	10.16	10.29
P			0.25
R	0.76		1.02
T	0.13	0.18	0.23
V	6.78	6.86	6.94
Z	2.49	2.87	3.25
CH2		0.51	

Revision history

Table 7. Document revision history

Date	Version	Changes
12-Sep-2018	1	Initial release
02-Oct-2018	2	Added Section 3 Circuit layout
08-Sep-2020	3	Updated Section Product status / summary , Table 5 and Section 4.1 E2 package information.

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