UCC21521 具有使能功能的 4A/6A、5.7 kV$_{RMS}$ 隔离式双通道栅极驱动器

1 特性

- 通用：双路低侧、双路高侧或半桥驱动器
- 工作温度范围：–40°C 至 +125°C
- 开关参数：
  - 19ns 典型传播延迟
  - 10ns 最小脉冲宽度
  - 5ns 最大延迟匹配度
  - 5ns 最大脉宽失真度
- 共模瞬态抗扰度 (CMTI) 大于 100 V/ns
- 浪涌抗扰度高达 12.8kV
- 隔离栅寿命 > 40 年
- 4A 峰值拉电流，6A 峰值灌电流输出
- TTL 和 CMOS 兼容输入
- 3V 至 18V 输入 VCCI 范围，可连接数字和模拟控制器
- 高达 25V 的 VDD 输出驱动电源
  - 5V、8V、12V VDD UVLO 选项
- 可通过编程的重叠和死区时间
- 抑制短于 5ns 的输入脉冲和瞬态噪声
- 可针对电源排序快速使能
- 宽体小外形尺寸集成电路 (SOIC)-16 (DW) 封装
- 安全相关及管理批准：
  - 8000 V$_{PK}$ 隔离，符合 DIN V VDE V 0884-10 (VDE V0884-10):2006-12 标准
  - 符合 UL 1577 标准且长达 1 分钟的 5700 V$_{RMS}$ 隔离
  - CSA 组件验收通知 5A，IEC 60950-1 和 IEC 60601-1 终端设备标准（计划）
  - 通过 GB4943.1-2011 CQC 认证（计划）

2 应用

- 离线交流-直流电源中的隔离式转换器
- 服务器、电信、IT 和工业基础设施
- 电机驱动和直流-交流太阳能逆变器
- LED 照明
- 感应加热
- 不间断电源 (UPS)
- HEV 和 BEV 电池充电器

3 说明

UCC21521 是一款隔离式双通道栅极驱动器，具有 4A 峰值拉电流和 6A 峰值灌电流。该器件设计用于驱动高达 5MHz 的功率 MOSFET、IGBT 和 SiC MOSFET，具有一流的传播延迟和脉宽失真度。

输入侧通过一个 5.7 kV$_{RMS}$ 增强型隔离栅与两个输出驱动器隔离，共模瞬态抗扰度 (CMTI) 的最小值为 100V/ns。两个二次侧驱动器之间采用内部功能隔离，支持高达 1500 V$_{DC}$ 的工作电压。

该驱动器可配置为两个低侧驱动器、两个高侧驱动器或一个死区时间 (DT) 可编程的半桥驱动器。EN 引脚拉低时会同时关闭两个输出，悬空或拉高时可使器件恢复正常运行。作为一种故障安全机制，一次侧逻辑故障会强制两个输出为低电平。

此器件接受高达 25V 的 VDD 电源电压。3V 到 18V 的宽输入电压 VCCI 范围使得该驱动器适用于连接数字和模拟控制器。所有电源电压引脚均具有欠压闭锁 (UVLO) 保护。

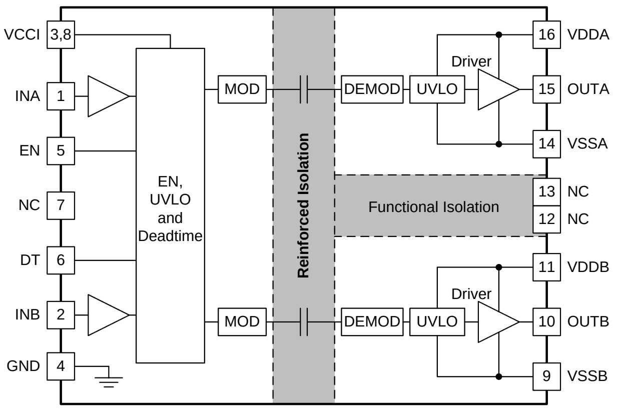
凭借上述所有高级 特性，UCC21521 能够满足各类电源应用中对于高效率、高电源密度和稳健性的 要求。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
UCC21521ADW	DW SOIC (16)	10.30mm x 7.50mm
UCC21521DW	DW SOIC (16)	10.30mm x 7.50mm
UCC21521CDW	DW SOIC (16)	10.30mm x 7.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

功能框图



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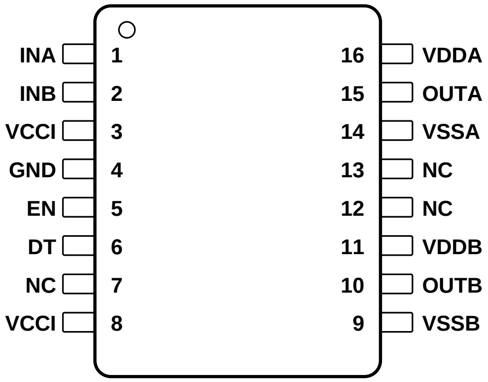
4 修订历史

日期	修订版本	注释
2016 年 10 月	*	最初发布版本

5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
DT	6	I	Programmable dead time function. Tying DT to VCCI allows the outputs to overlap. Leaving DT open sets the dead time to <15 ns. Placing a 500-Ω to 500-kΩ resistor (R_{DT}) between DT and GND adjusts dead time according to: DT (in ns) = 10 x R_{DT} (in kΩ). It is recommended to parallel a ceramic capacitor, 2.2nF or above, with R_{DT} to achieve better noise immunity.
EN	5	I	Enable both driver outputs if asserted high or left open, disable the output if set low. This pin is pulled high internally if left open. It is recommended to tie this pin to VCCI if not used to achieve better noise immunity.
GND	4	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
INA	1	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
INB	2	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
NC	7	–	No connection.
NC	12	–	No connection.
NC	13	–	No connection.
OUTA	15	O	Output of driver A. Connect to the gate of the A channel FET or IGBT.
OUTB	10	O	Output of driver B. Connect to the gate of the B channel FET or IGBT.
VCCI	3	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
VCCI	8	P	Primary-side supply voltage. This pin is internally shorted to pin 3.
VDDA	16	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.
VDDB	11	P	Secondary-side power for driver B. Locally decoupled to VSSB using low ESR/ESL capacitor located as close to the device as possible.
VSSA	14	P	Ground for secondary-side driver A. Ground reference for secondary side A channel.
VSSB	9	P	Ground for secondary-side driver B. Ground reference for secondary side B channel.

[1] P =Power, G= Ground, I= Input, O= Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input bias pin supply voltage	VCCI to GND	–0.3	20	V
Driver bias supply	VDDA-VSSA, VDDB-VSSB	–0.3	30	V
Output signal voltage	OUTA to VSSA, OUTB to VSSB	–0.3	V_{VDDA}+0.3, V_{VDDB}+0.3	V
	OUTA to VSSA, OUTB to VSSB, Transient for 200 ns	–2	V_{VDDA}+0.3, V_{VDDB}+0.3	V
Input signal voltage	INA, INB, EN, DT to GND	–0.3	V_{VCCI}+0.3	V
	INA, INB Transient for 50ns	–5	V_{VCCI}+0.3	V
Channel to channel voltage	VSSA-VSSB, VSSB-VSSA		1500	V
Junction temperature, T_J (2)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To maintain the recommended operating conditions for T_J, see the Thermal Information.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
VCCI	VCCI Input supply voltage		3	18	V
VDDA, VDDB	Driver output bias supply	5-V UVLO version - UCC21521ADW	6.5	25	V
		8-V UVLO version - UCC21521DW	9.2	25	V
		12-V UVLO version - UCC21521CDW	14.7	25	V
T_A	Ambient Temperature		–40	125	°C
T_J	Junction Temperature		–40	130	°C

6.4 Thermal Information

THERMAL METRIC[1]		UCC21521	UNIT
		DW-16 (SOIC)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Power Ratings

			VALUE	UNIT
P_D	Power dissipation by UCC21521	VCCI = 18 V, VDDA/B = 12 V, INA/B = 3.3 V, 3 MHz 50% duty cycle square wave 1-nF load	1.05	W
P_{DI}	Power dissipation by transmitter side of UCC21521		0.05	W
P_{DA}, P_{DB}	Power dissipation by each driver side of UCC21521		0.5	W

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest terminal to terminal distance through air	> 8	mm
CPG	External creepage[1]	Shortest terminal to terminal distance across the package surface	> 8	mm
DTI	Distance through insulation	Distance through internal isolation (internal clearance)	>21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE 0884-10 (VDE V 0884-10): 2006-2012[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	Time dependent dielectric breakdown (TDDB) test, (See 图 1)	1500	V_{RMS}
			2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t = 1 sec (100% production)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After Input/Output safety test subgroup 2/3. $V_{ini} = V_{IOTM}$, $t_{ini} = 60s$; $V_{pd(m)} = 1.2\ X\ V_{IORM} = 2545\ V_{PK}$, $t_m = 10s$	<5	pC
		Method a, After environmental tests subgroup 1. $V_{ini} = V_{IOTM}$, $t_{ini} = 60s$; $V_{pd(m)} = 1.6\ X\ V_{IORM} = 3394\ V_{PK}$, $t_m = 10s$	<5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$; $t_{ini} = 1s$; $V_{pd(m)} = 1.875 * V_{IORM} = 3977\ V_{PK}$, $t_m = 1s$	<5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \sin(2\pi ft)$, f =1 MHz	1.2	pF
R_{IO}	Isolation resistance, input to output	V_{IO} = 500 V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S =150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 sec. (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6840V_{RMS}$, t = 1 sec (100% production)	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC
Certified according to DIN VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011
Reinforced Insulation Maximum Transient Isolation voltage, 8000 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 2121 V_{PK}; Maximum Surge Isolation Voltage, 8000 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.	Single protection, 5700 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate
Certification number: 40040142	Agency Qualification Planned	File number: E181974	Agency Qualification Planned

6.8 Safety-Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	$R_{\theta JA}$ = 78.1ºC/W, VDDA/B = 12 V$^{(1)}$, T_A = 25°C, T_J = 150°C See 图 2	DRIVER A, DRIVER B			64	mA
		$R_{\theta JA}$ = 78.1ºC/W, VDDA/B = 25 V$^{(1)}$, T_A = 25°C, T_J = 150°C	DRIVER A, DRIVER B			31	mA
P_S	Safety supply power	$R_{\theta JA}$ = 78.1ºC/W, T_A = 25°C, T_J = 150°C See 图 3	INPUT			50	mW
			DRIVER A			775	
			DRIVER B			775	
			TOTAL			1600	
T_S	Safety temperature					150	°C

(1) VDDA=VDDB=12V is used for the test condition of 5V and 8V UVLO, and VDDA=VDDB=25V is used for 12V UVLO.

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K test board for leaded surface mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics

V_{VCCI} = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V or 15V(1), 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCCI}	VCCI quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.5	2.0	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.0	1.8	mA
I_{VCCI}	VCCI per channel operating current	f = 500 kHz, C_{OUT} = 100 pF		2.0		mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB operating current	f = 500 kHz, C_{OUT} = 100 pF, VDD=12V		2.5		mA
		f = 500 kHz, C_{OUT} = 100 pF, VDD=15V		3.0		mA
SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VCCI_ON}	Rising threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	Falling threshold VCCI_OFF		2.35	2.5	2.65	V
V_{VCCI_HYS}	Threshold hysteresis			0.2		V
UCC21521ADW UVLO THRESHOLDS (5-V UVLO VERSION)						
V_{VDDA_ON}, V_{VDDB_ON}	Rising threshold VDDA_ON, VDDB_ON		5.2	5.8	6.3	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling threshold VDDA_OFF, VDDB_OFF		4.9	5.5	6	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold hysteresis			0.3		V
UCC21521DW UVLO THRESHOLDS (8-V UVLO VERSION)						
V_{VDDA_ON}, V_{VDDB_ON}	Rising threshold VDDA_ON, VDDB_ON		8	8.5	9	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling threshold VDDA_OFF, VDDB_OFF		7.5	8	8.5	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold hysteresis			0.5		V
UCC21521CDW UVLO THRESHOLDS (12-V UVLO VERSION)						
V_{VDDA_ON}, V_{VDDB_ON}	Rising threshold VDDA_ON, VDDB_ON		12.5	13.5	14.5	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling threshold VDDA_OFF, VDDB_OFF		11.5	12.5	13.5	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold hysteresis			1.0		V
INA and INB						
V_{INAH}, V_{INBH}	Input high threshold voltage		1.6	1.8	2	V
V_{INAL}, V_{INBL}	Input low threshold voltage		0.8	1	1.2	V
V_{INA_HYS}, V_{INB_HYS}	Input threshold hysteresis			0.8		V
V_{INA}, V_{INB}	Negative transient, ref to GND, 50 ns pulse	Not production tested, bench test only	–5			V
EN THRESHOLDS						
V_{ENH}	Enable high voltage		2.0			V
V_{ENL}	Enable low voltage				0.8	V

(1) VDDA=VDDB=12V is used for the test condition of 5V and 8V UVLO, and VDDA=VDDB=15V is used for 12V UVLO.

Electrical Characteristics (continued)

V_{VCCI} = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V or 15V(1), 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
I_{OA+}, I_{OB+}	Peak output source current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		4		A
I_{OA-}, I_{OB-}	Peak output sink current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		6		A
R_{OHA}, R_{OHB}	Output resistance at high state	I_{OUT} = –10 mA, T_A = 25°C, R_{OHA}, R_{OHB} do not represent drive pull-up performance. See t_{RISE} in Switching Characteristics and Output Stage for details.		5		Ω
R_{OLA}, R_{OLB}	Output resistance at low state	I_{OUT} = 10 mA, T_A = 25°C		0.55		Ω
V_{OHA}, V_{OHB}	Output voltage at high state	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = –10 mA, T_A = 25°C		11.95		V
V_{OLA}, V_{OLB}	Output voltage at low state	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = 10 mA, T_A = 25°C		5.5		mV
DEADTIME AND OVERLAP PROGRAMMING						
Dead time		Pull DT pin to VCCI	Overlap determined by INA INB			-
		DT pin is left open, min spec characterized only, tested for outliers	0	8	15	ns
		R_{DT} = 20 kΩ	160	200	240	ns

6.10 Switching Characteristics

V_{VCCI} = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V or 15V(1), 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_A = –40°C to +125°C, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise time, 20% to 80% measured points	C_{OUT} = 1.8 nF		6	16	ns
t_{FALL}	Output fall time, 90% to 10% measured points	C_{OUT} = 1.8 nF		7	12	ns
t_{PWmin}	Minimum pulse width	Output off for less than minimum, C_{OUT} = 0 pF			20	ns
t_{PDHL}	Propagation delay from INx to OUTx falling edges			19	30	ns
t_{PDLH}	Propagation delay from INx to OUTx rising edges			19	30	ns
t_{PWD}	Pulse width distortion $\lvert t_{PDLH} – t_{PDHL} \rvert$				5	ns
t_{DM}	Propagation delays matching between VOUTA, VOUTB	f = 100 kHz			5	ns
CMTI	Static common-mode transient immunity (See CMTI Testing)	Slew rate of GND versus VSSA and VSSB, INA and INB both tied to GND or VCCI	100			V/ns

(1) VDDA=VDDB=12V is used for the test condition of 5V and 8V UVLO, and VDDA=VDDB=15V is used for 12V UVLO.

6.11 Insulation Characteristics Curves

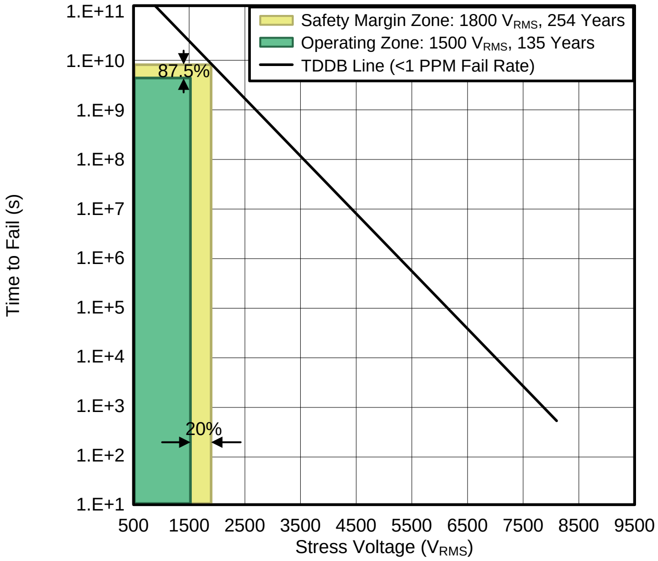


图 1. Reinforced Isolation Capacitor Life Time Projection

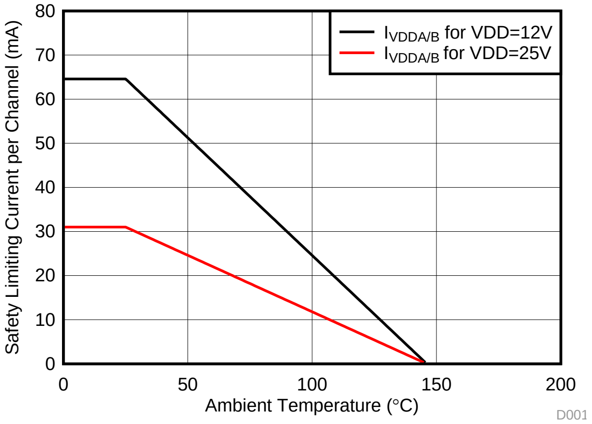


图 2. Thermal Derating Curve for Safety-Related Limiting Current (Current in Each Channel with Both Channels Running Simultaneously)

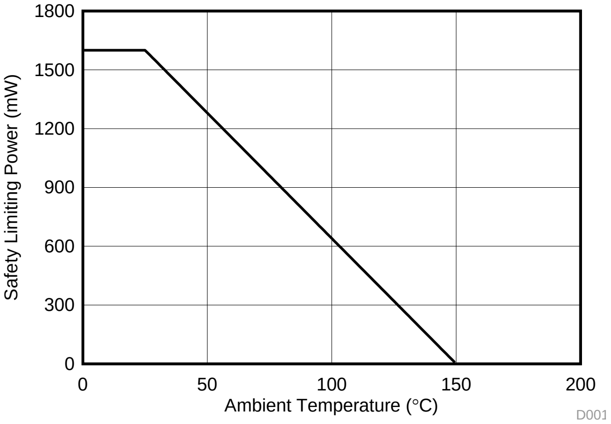


图 3. Thermal Derating Curve for Safety-Related Limiting Power

6.12 Typical Characteristics

VDD = 12 V for 5V and 8V UVLO, VDDA = 15 V for 12V UVLO, VCCI = 3.3 V, T_A = 25°C, No load. (unless otherwise noted)

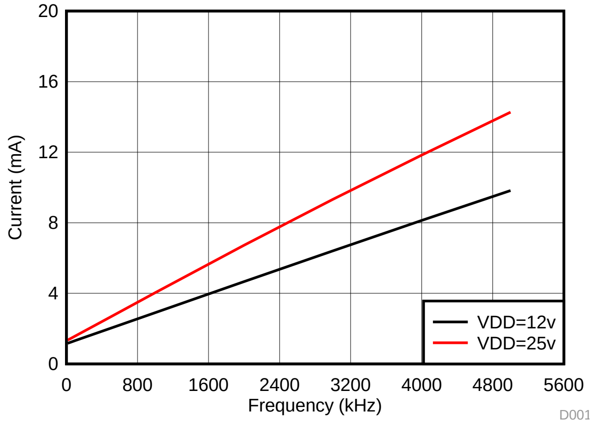


图 4. Per Channel Current Consumption vs. Frequency (No Load, VDD = 12 V or 25 V)

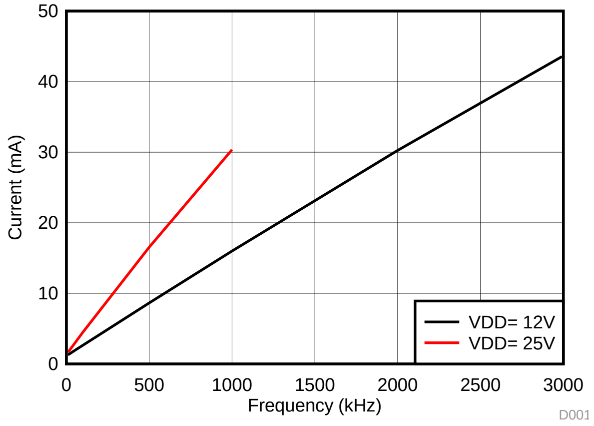


图 5. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency (1-nF Load, VDD = 12 V or 25 V)

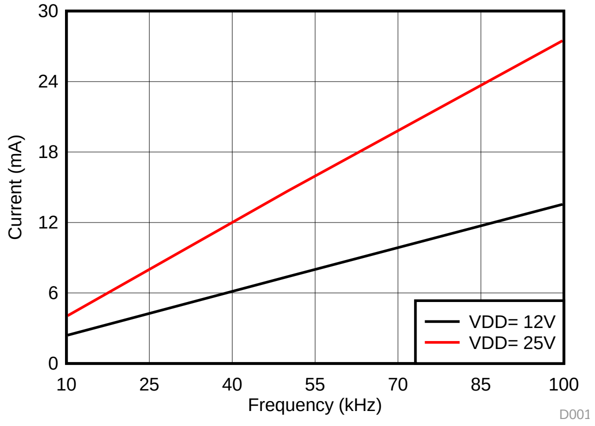


图 6. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency (10-nF Load, VDD = 12 V or 25 V)

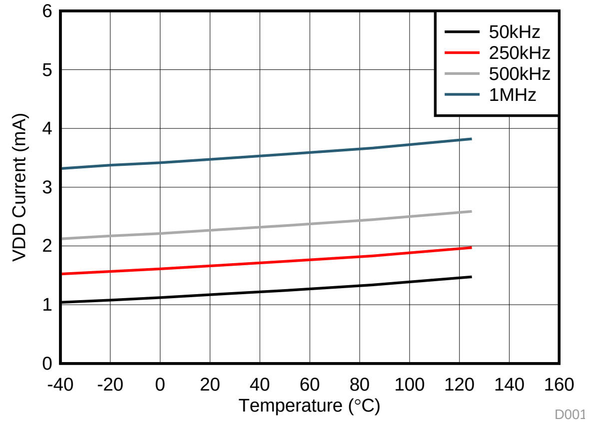


图 7. Per Channel ($I_{VDDA/B}$) Supply Current Vs. Temperature (VDD=12V, No Load, Different Switching Frequencies)

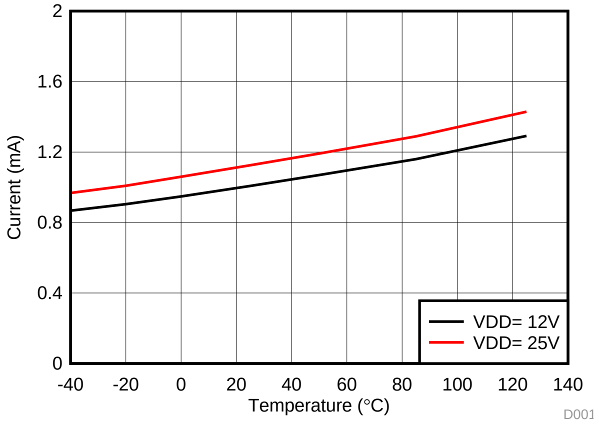


图 8. Per Channel ($I_{VDDA/B}$) Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)

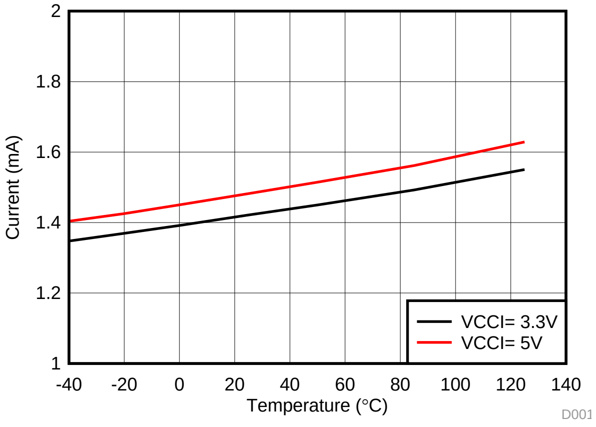


图 9. I_{VCCI} Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)

Typical Characteristics (接下页)

VDD = 12 V for 5V and 8V UVLO, VDDA = 15 V for 12V UVLO, VCCI = 3.3 V, T_A = 25°C, No load. (unless otherwise noted)

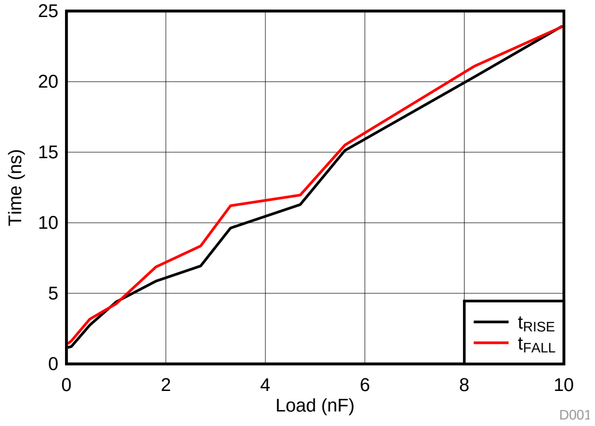


图 10. UCC21521ADW and UCC21521DW Rising and Falling Times vs. Load (VDD = 12 V)

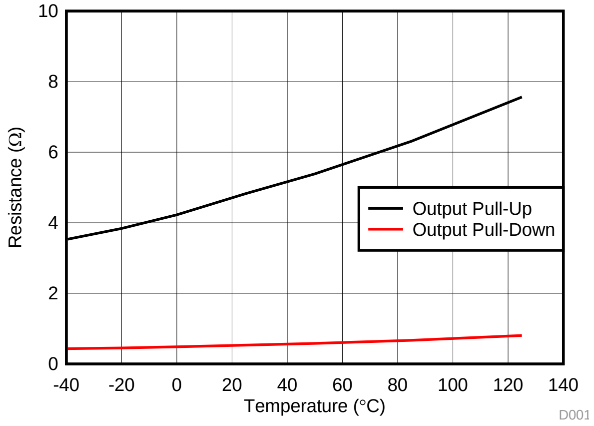


图 11. Output Resistance vs. Temperature

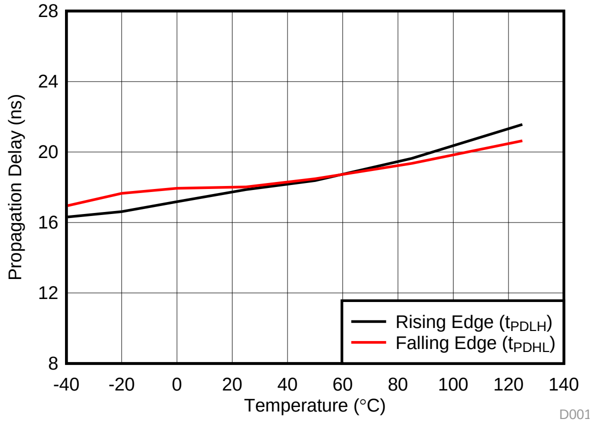


图 12. Propagation Delay vs. Temperature

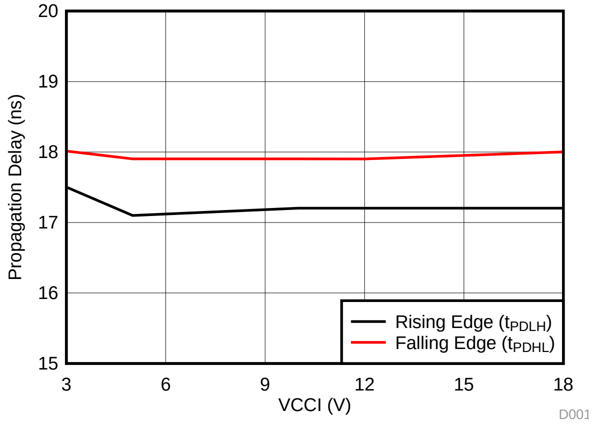


图 13. Propagation Delay vs. VCCI

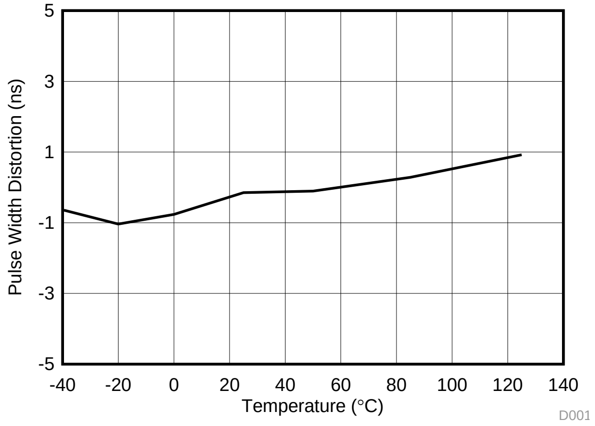


图 14. Pulse Width Distortion vs. Temperature

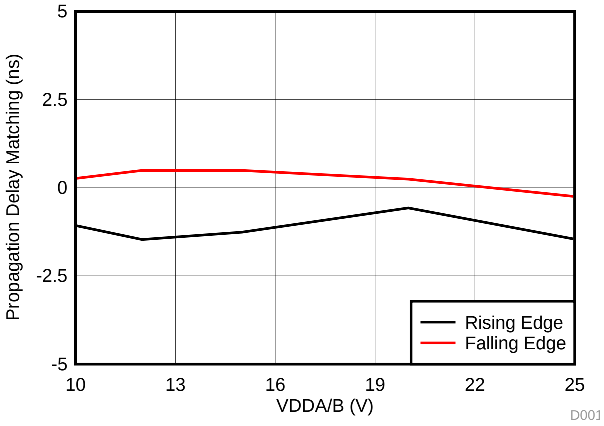


图 15. Propagation Delay Matching (t_{DM}) vs. VDD

Typical Characteristics (接下页)

VDD = 12 V for 5V and 8V UVLO, VDDA = 15 V for 12V UVLO, VCCI = 3.3 V, T_A = 25°C, No load. (unless otherwise noted)

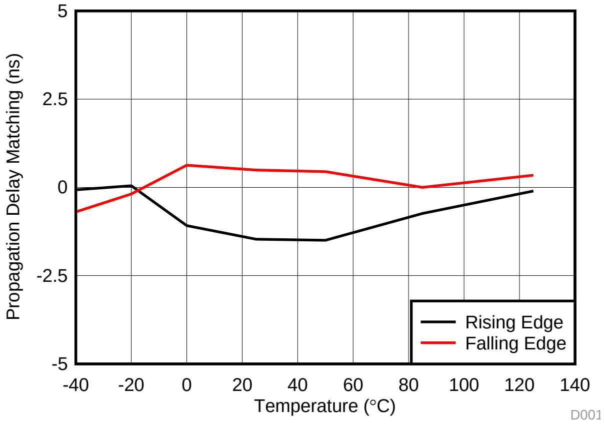


图 16. Propagation Delay Matching (t_{DM}) vs. Temperature

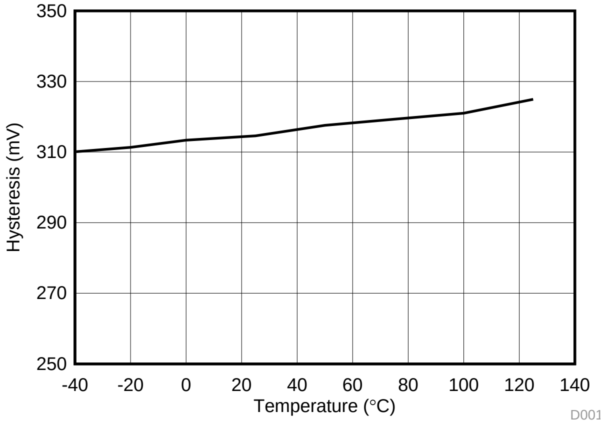


图 17. UCC21521ADW UVLO Hysteresis vs. Temperature

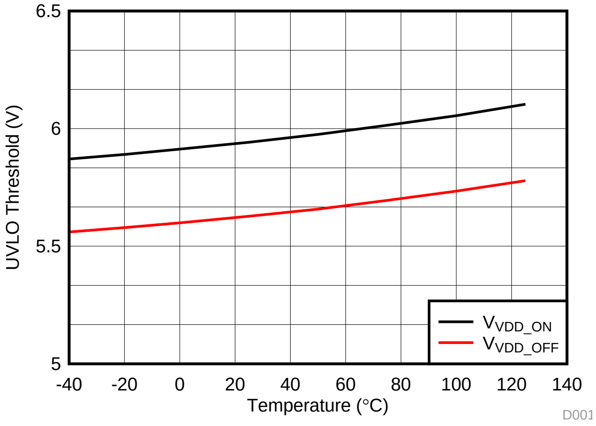


图 18. UCC21521ADW UVLO Threshold vs. Temperature

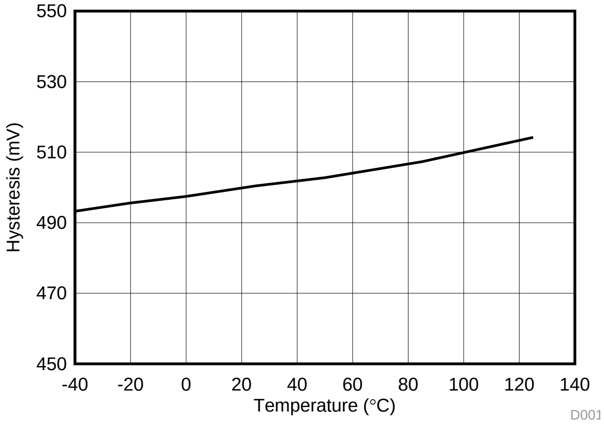


图 19. UCC21521DW UVLO Hysteresis vs. Temperature

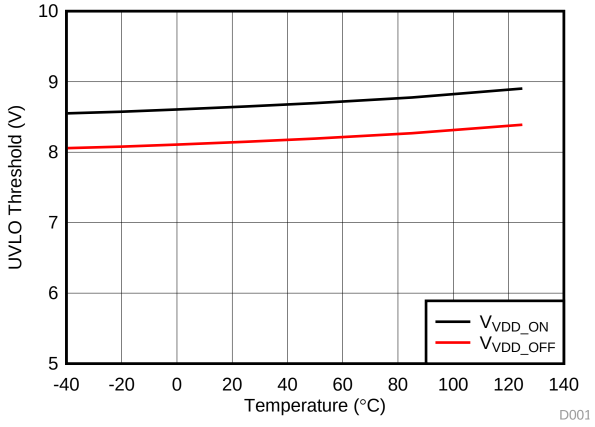


图 20. UCC21521DW UVLO Threshold vs. Temperature

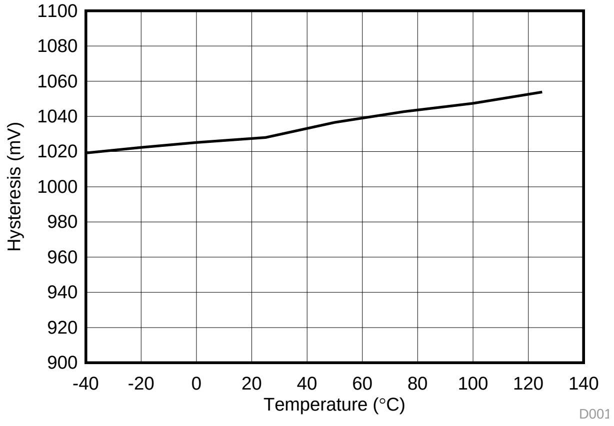


图 21. UCC21521CDW UVLO Hysteresis vs. Temperature

Typical Characteristics (接下页)

VDD = 12 V for 5V and 8V UVLO, VDDA = 15 V for 12V UVLO, VCCI = 3.3 V, T_A = 25°C, No load. (unless otherwise noted)

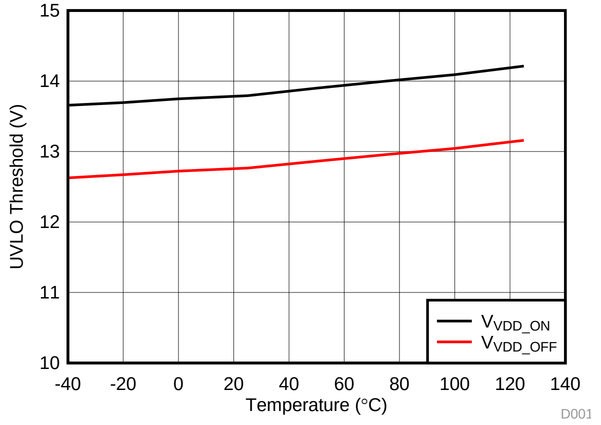


图 22. UCC21521CDW UVLO Threshold vs. Temperature

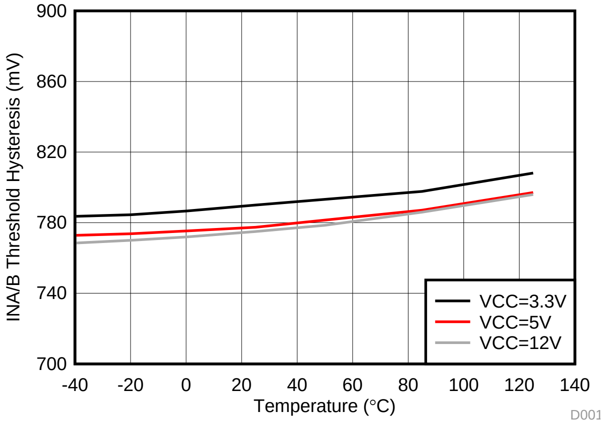


图 23. INA/B Hysteresis vs. Temperature

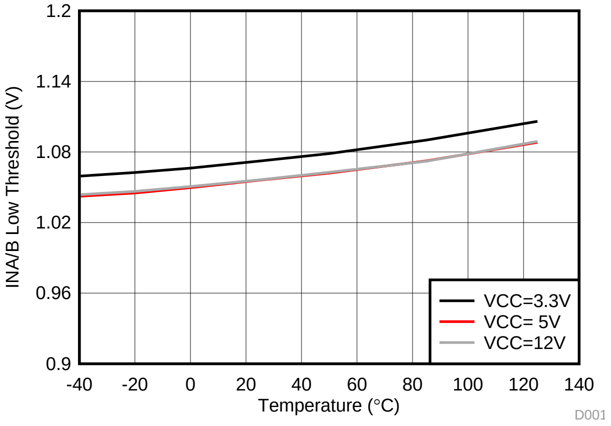


图 24. INA/B Low Threshold

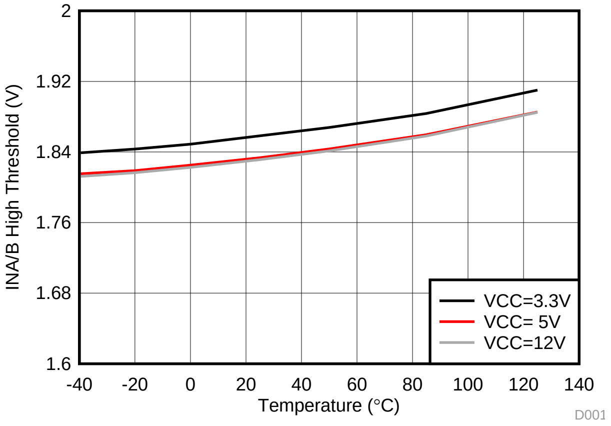


图 25. INA/B High Threshold

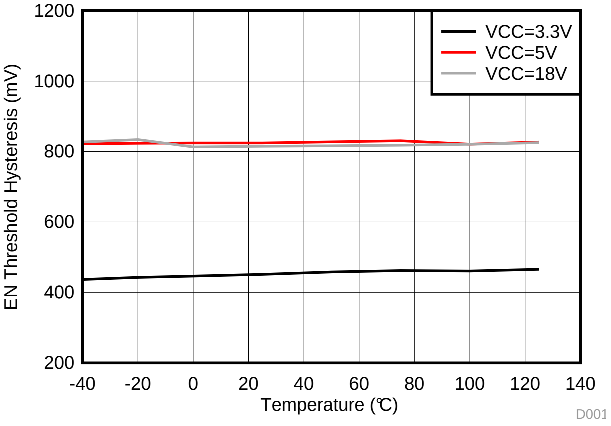


图 26. EN Threshold Hysteresis vs. Temperature

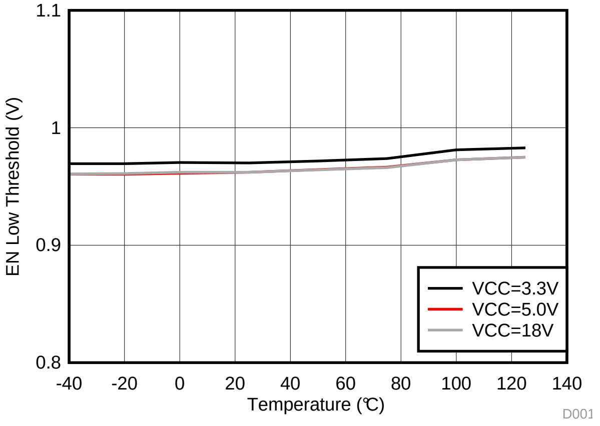


图 27. EN Low Threshold

Typical Characteristics (接下页)

VDD = 12 V for 5V and 8V UVLO, VDDA = 15 V for 12V UVLO, VCCI = 3.3 V, T_A = 25°C, No load. (unless otherwise noted)

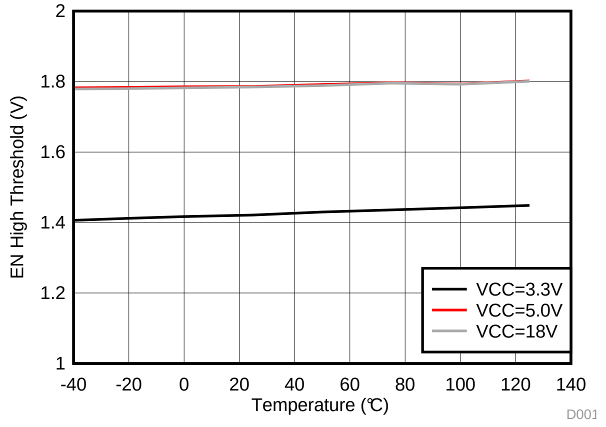


图 28. EN High Threshold

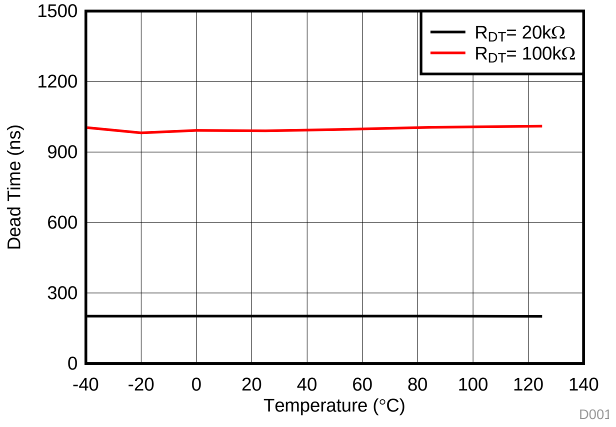


图 29. Dead Time vs. Temperature (with R_{DT} = 20 kΩ and 100 kΩ)

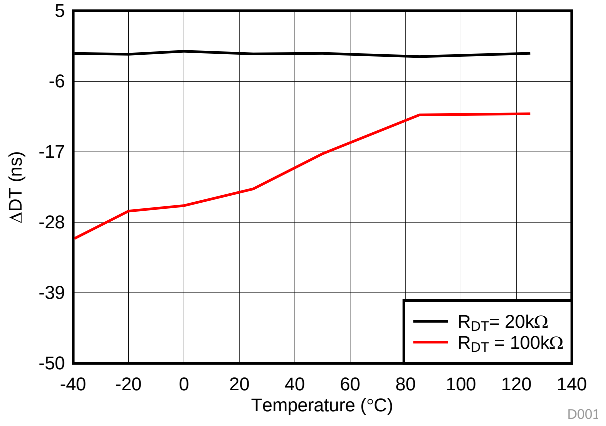


图 30. Dead Time Matching vs. Temperature (with R_{DT} = 20 kΩ and 100 kΩ)

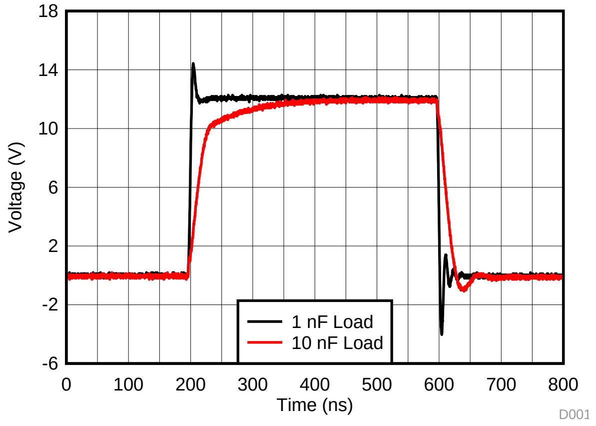


图 31. Typical Output Waveforms (VDD=12V)

7 Parameter Measurement Information

7.1 Propagation Delay and Pulse Width Distortion

图 32 shows how one calculates pulse width distortion (t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase and disabling the dead time function by shorting the DT Pin to VCC.

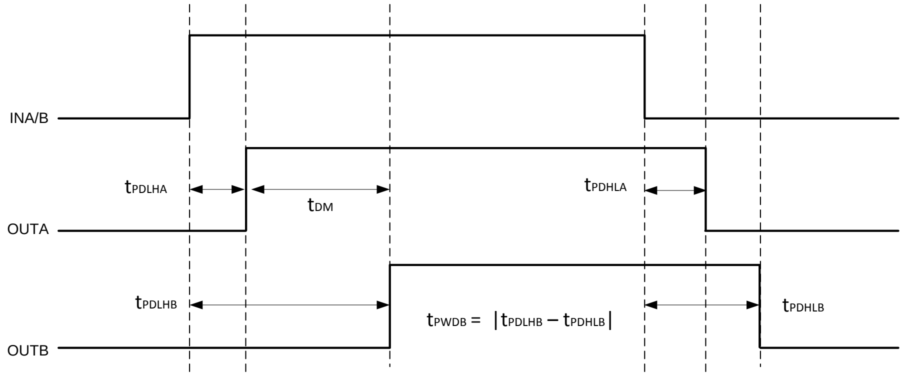


图 32. Overlapping Inputs, Dead Time Disabled

7.2 Rising and Falling Time

图 33 shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) times. For more information on how short rising and falling times are achieved see Output Stage

图 33. Rising and Falling Time Criteria

7.3 Input and Enable Response Time

图 34 shows the response time of the enable function. For more information, see Enable Pin .

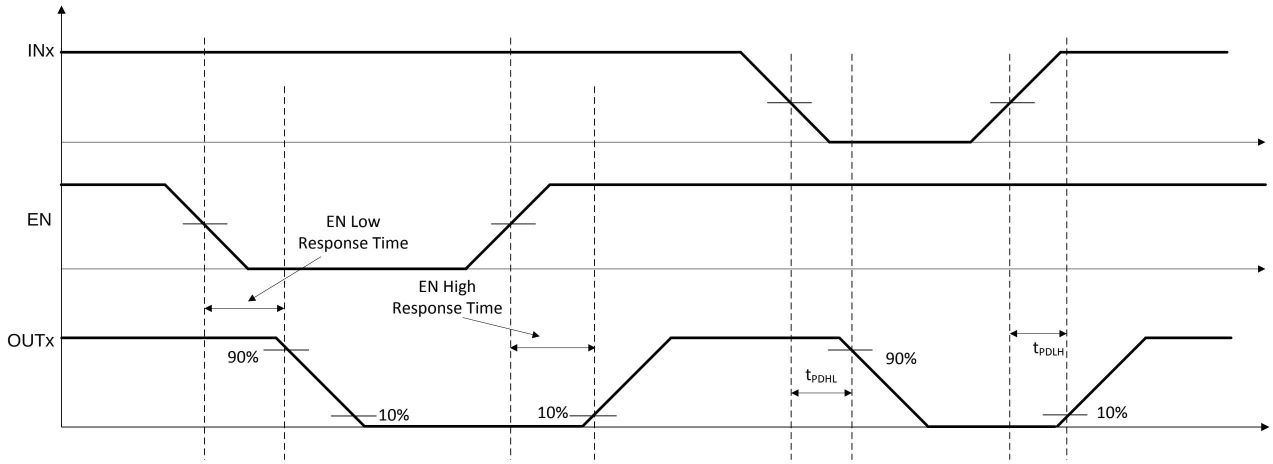


图 34. Enable Pin Timing

7.4 Programable Dead Time

Leaving the DT pin open or tying it to GND through an appropriate resistor (R_{DT}) sets a dead-time interval. For more details on dead time, refer to Programmable Dead Time (DT) Pin .

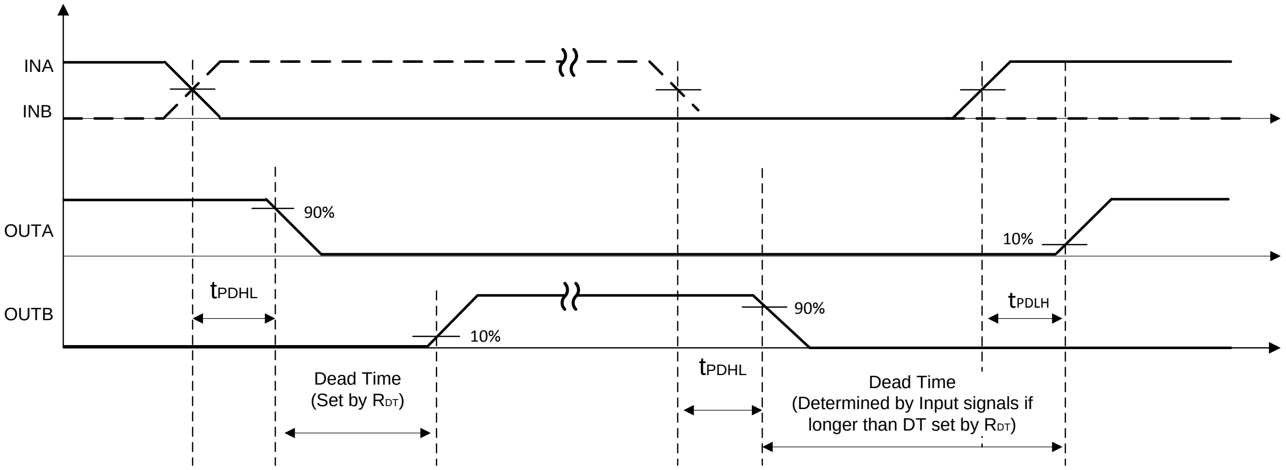


图 35. Dead-Time Switching Parameters

7.5 CMTI Testing

图 36 is a simplified diagram of the CMTI testing configuration.

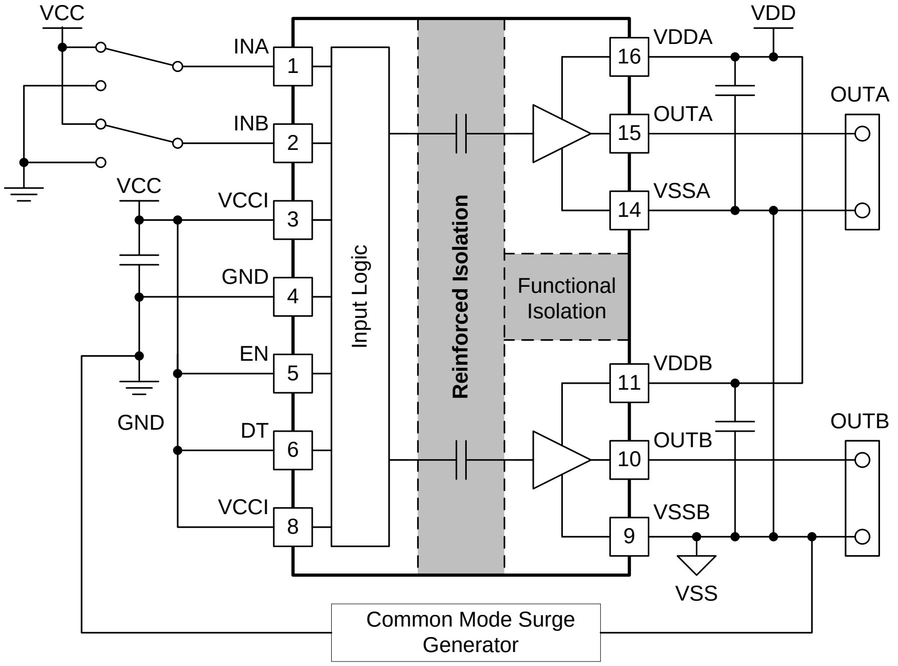


图 36. Simplified CMTI Testing Setup

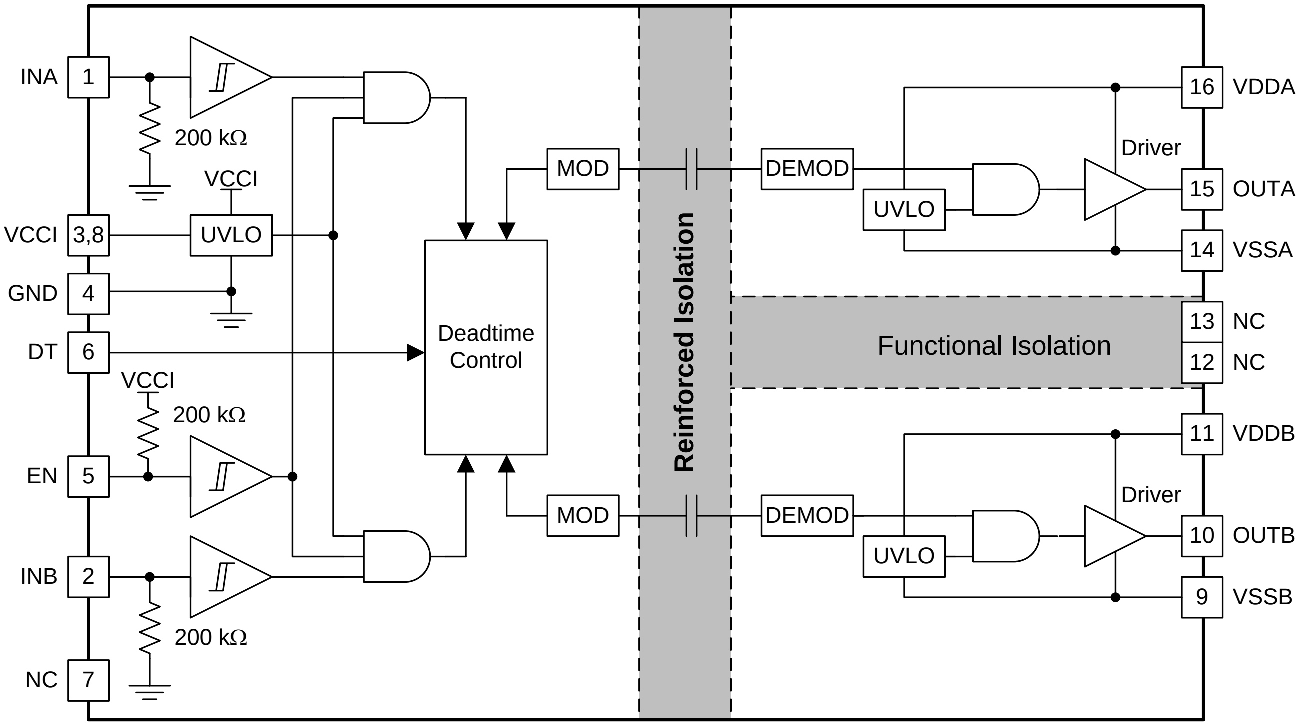
8 Detailed Description

8.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21521 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors, including SiC MOSFETs. UCC21521 has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, an EN pin, and under voltage lock out (UVLO) for both input and output voltages. The UCC21521 also holds its outputs low when the inputs are left open or when the input pulse is not wide enough. The driver inputs are CMOS and TTL compatible for interfacing to digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The UCC21521 has an internal under voltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the effected output low, regardless of the status of the input pins (INA and INB).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in 图 37). In this condition, the upper PMOS is resistively held off by $R_{Hi\text{-}Z}$ while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically less than 1.5V, when no bias power is available.

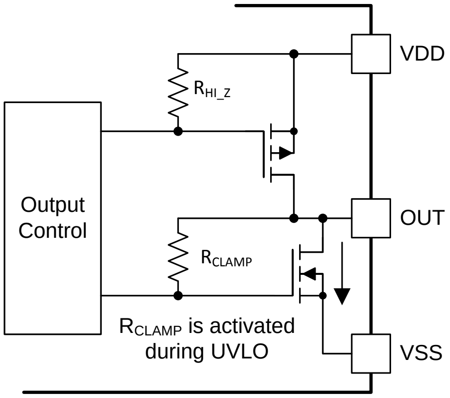


图 37. Simplified Representation of Active Pull Down Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC21521 also has an internal under voltage lock out (UVLO) protection feature. The device isn't active unless the voltage, VCCI, is going to exceed V_{VCCI_ON} on start up. And a signal will cease to be delivered when that pin receives a voltage less than V_{VCCI_OFF}. And, just like the UVLO for VDD, there is hystersis (V_{VCCI_HYS}) to ensure stable operation.

Feature Description (接下页)

All versions of the UCC21521 can withstand an absolute maximum of 30 V for VDD, and 20 V for VCCI.

表 1. UCC21521 VCCI UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

表 2. UCC21521 VDD UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L	L

8.3.2 Input and Output Logic Table

Assume VCCI, VDDA, VDDB are powered up. See VDD, VCCI, and Under Voltage Lock Out (UVLO) for more information on UVLO operation modes.

表 3. INPUT/OUTPUT Logic Table(1)

INPUTS		EN	OUTPUTS		NOTE
INA	**INB**		**OUTA**	**OUTB**	
L	L	H or Left Open	L	L	If Dead Time function is used, output transitions occur after the dead time expires. See Programmable Dead Time (DT) Pin
L	H	H or Left Open	L	H	
H	L	H or Left Open	H	L	
H	H	H or Left Open	L	L	DT is left open or programmed with R_{DT}
H	H	H or Left Open	H	H	DT pin pulled to VCCI
Left Open	Left Open	H or Left Open	L	L	-
X	X	L	L	L	-

(1) "X" means L, H or left open.

8.3.3 Input Stage

The input signal pins (INA and INB) of UCC21521 are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (Such as those from 3.3-V micro-controllers), since UCC21521 has a typical high threshold ($V_{INA/BH}$) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature (see 图 24,图 25). A wide hysterisis (V_{INA/B_HYS}) of 0.8 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 200 kΩ (See Functional Block Diagram). However, it is still recommended to ground an input if it is not being used.

Since the input side of UCC21521 is isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn’t exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for their chosen gate. That said, the amplitude of any signal applied to INA or INB must *never* be at a voltage higher than VCCI.

8.3.4 Output Stage

The UCC21521’s output stages features a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 1.47 Ω when activated.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC21521 pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter. Therefore, the value of R_{OH} belies the fast nature of the UCC21521's turn-on time.

The pull-down structure in UCC21521 is simply composed of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC21521 are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

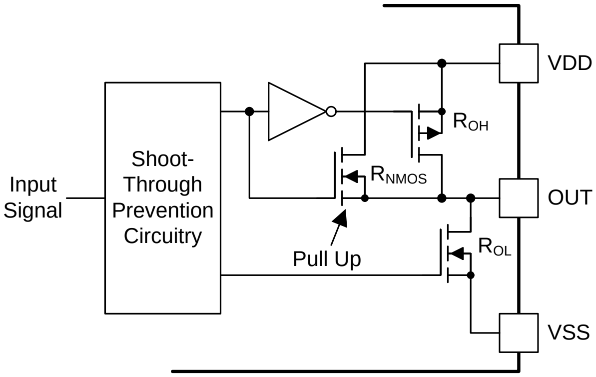


图 38. Output Stage

8.3.5 Diode Structure in UCC21521

图 39 illustrates the multiple diodes involved in the ESD protection components of the UCC21521. This provides a pictorial representation of the absolute maximum rating for the device.

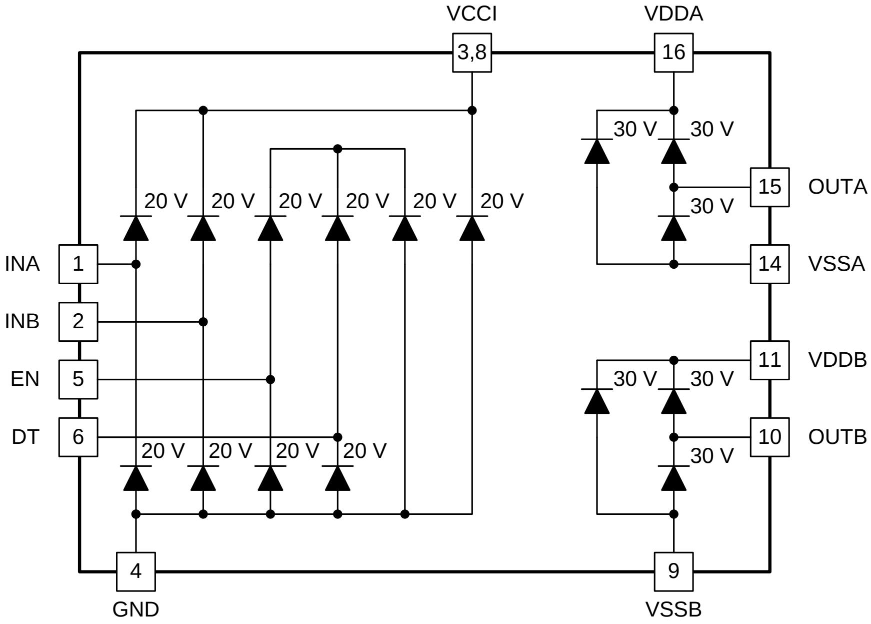


图 39. ESD Structure

8.4 Device Functional Modes

8.4.1 Enable Pin

Setting the EN pin low, i.e. V_{EN}≤0.8V, shuts down both outputs simultaneously. Pull the EN pin high (or left open), i.e. V_{EN}≥2.0V, allows UCC21521 to operate normally. The EN pin is quite responsive, as far as propagation delay and other switching parameters are concerned. The EN pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to VCCI if the EN pin is not used to achieve better noise immunity.

8.4.2 Programmable Dead Time (DT) Pin

UCC21521 allows the user to adjust dead time (DT) in the following ways:

8.4.2.1 Tying the DT Pin to VCC

Outputs completely match inputs, so no dead time is asserted. This allows outputs to overlap.

Device Functional Modes (接下页)

8.4.2.2 DT Pin Left Open or Connected to a Programming Resistor between DT and GND Pins

If the DT pin is left open, the dead time duration (t_{DT}) is set to <15 ns. One can program t_{DT} by placing a resistor, R_{DT}, between the DT pin and GND. The appropriate R_{DT} value can be determined from 公式 1, where R_{DT} is in kΩ and t_{DT} in ns:

$$t_{DT} \approx 10 \times R_{DT} \tag{1}$$

The steady state voltage at DT pin is around 0.8V, and the DT pin current will be less than 10uA when R_{DT}=100kΩ. Therefore, It is recommended to parallel a ceramic capacitor, 2.2nF or above, with R_{DT} to achieve better noise immunity and better deadtime matching between two channels, especially when the dead time is larger than 300ns. The major consideration is that the current through the R_{DT} is used to set the dead time, and this current decreases as R_{DT} increases.

An input signal's falling edge activates the programmed dead time for the other signal. The output signals' dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent shoot-through, and it doesn't affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in 图 40:

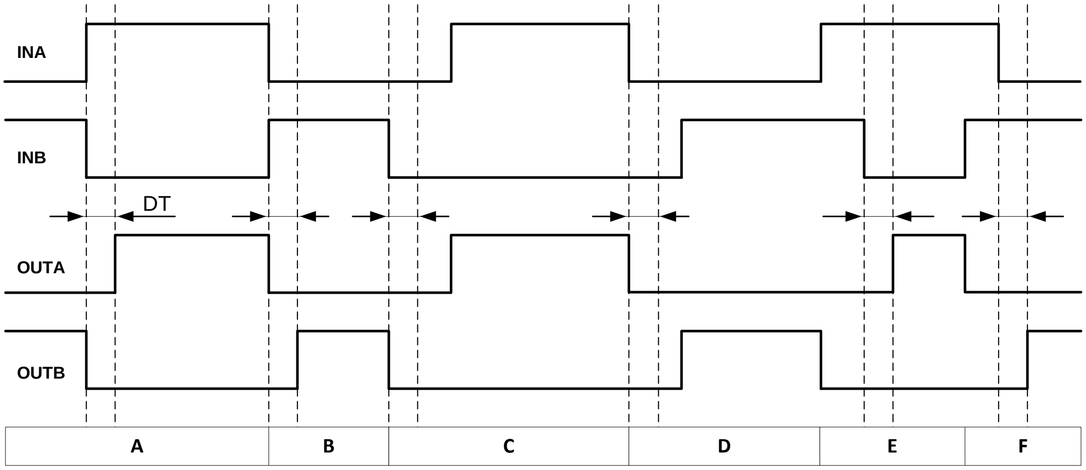


图 40. Input and Output Logic Relationship With Input Signals

Condition A: INB goes low, INA goes high. INB sets OUTB low immediately and assigns the programmed dead time to OUTA. OUTA is allowed to go high after the programmed dead time.

Condition B: INB goes high, INA goes low. Now INA sets OUTA low immediately and assigns the programmed dead time to OUTB. OUTB is allowed to go high after the programmed dead time.

Condition C: INB goes low, INA is still low. INB sets OUTB low immediately and assigns the programmed dead time for OUTA. In this case, the input signal's *own* dead time is longer than the programmed dead time. Thus, when INA goes high, it immediately sets OUTA high.

Condition D: INA goes low, INB is still low. INA sets OUTA low immediately and assigns the programmed dead time to OUTB. INB's *own* dead time is longer than the programmed dead time. Thus, when INB goes high, it immediately sets OUTB high.

Condition E: INA goes high, while INB and OUTB are still high. To avoid overshoot, INA immediately pulls OUTB low and keeps OUTA low. After some time OUTB goes low and assigns the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA is allowed to go high.

Condition F: INB goes high, while INA and OUTA are still high. To avoid overshoot, INB immediately pulls OUTA low and keeps OUTB low. After some time OUTA goes low and assigns the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB is allowed to go high.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC21521 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC21521 (with up to 18-V VCCI and 25-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or SiC MOSFETs. With integrated components, advanced protection features (UVLO, dead time, and enable) and optimized switching performance; the UCC21521 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

9.2 Typical Application

The circuit in 图 41 shows a reference design with UCC21521 driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

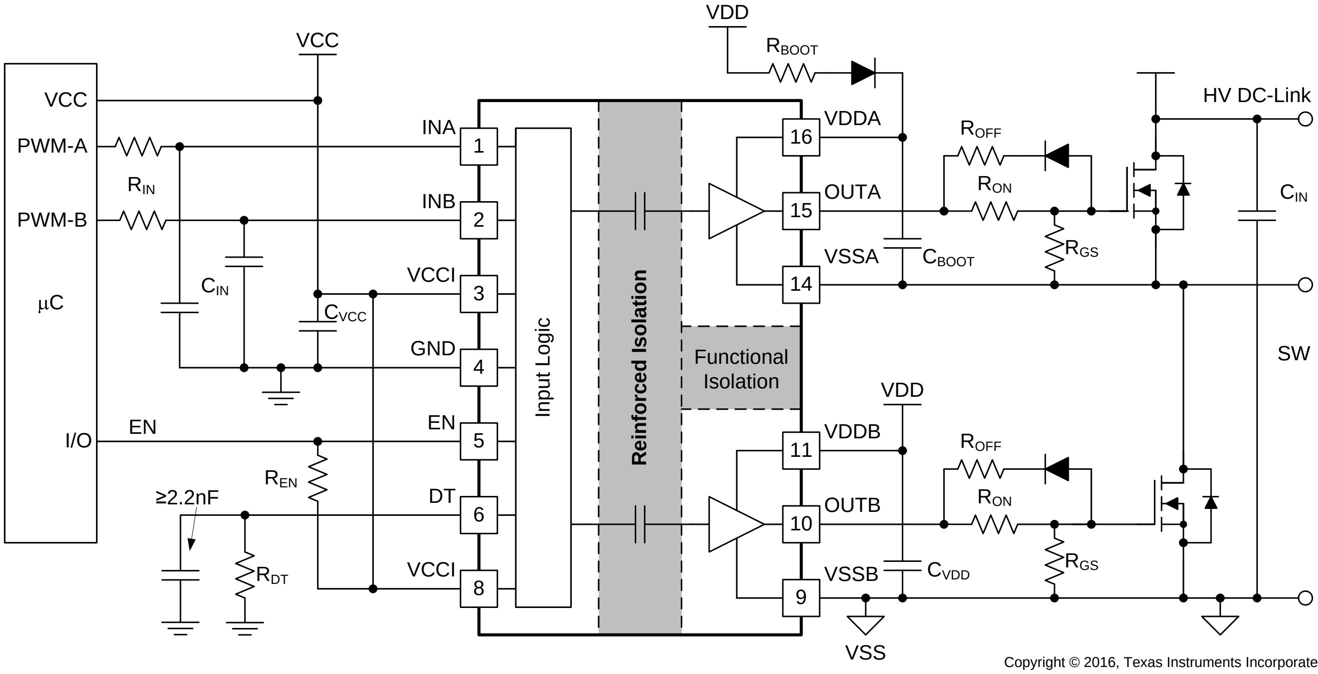


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图 41. Typical Application Schematic

Typical Application (接下页)

9.2.1 Design Requirements

表 4 lists reference design parameters for the example application: UCC21521 driving 1200-V SiC-MOSFETs in a high side-low side configuration.

表 4. UCC21521 Design Requirements

PARAMETER	VALUE	UNITS
Power transistor	C2M0080120D	-
VCC	5.0	V
VDD	20	V
Input signal amplitude	3.3	V
Switching frequency (f_S)	100	kHz
DC link voltage	800	V

9.2.2 Detailed Design Procedure

9.2.2.1 Designing INA/INB Input Filter

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input R_{IN}-C_{IN} filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an R_{IN} in the range of 0 Ω to 100 Ω and a C_{IN} between 10 pF and 100 pF. In the example, an R_{IN} = 51 Ω and a C_{IN} = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

9.2.2.2 Select External Bootstrap Diode and its Series Resistor

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode’s forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 800 V_{DC}. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 1200-V SiC diode, C4D02120E, is chosen in this example.

A bootstrap resistor, R_{BOOT}, is used to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle, especially when the VSSA(SW) pin has an excessive negative transient voltage. The recommended value for R_{BOOT} is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.2 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through D_{Boot} is,

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{20V - 2.5V}{2.2\Omega} \approx 8A$$

where

- V_{BDF} is the estimated bootstrap diode forward voltage drop at 8 A. (2)

9.2.2.3 Gate Driver Output Resistor

The external gate driver resistors, R_{ON}/R_{OFF}, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in Output Stage, the UCC21521 has a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \| R_{OH} + R_{ON} + R_{GFET\_Int}}\right)$$

$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \| R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \tag{3}$$

where

- R_{ON}: External turn-on resistance.
- R_{GFET_INT}: Power transistor internal gate resistance, found in the power transistor datasheet.
- I_{O+} = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance. (4)

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \| R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{20V - 0.8V}{1.47\Omega \| 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.4A \tag{5}$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \| R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{20V}{1.47\Omega \| 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.5A \tag{6}$$

Therefore, the high-side and low-side peak source current is 2.4 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \| R_{ON} + R_{GFET\_Int}}\right)$$

$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \| R_{ON} + R_{GFET\_Int}}\right) \tag{7}$$

where

- R_{OFF}: External turn-off resistance;
- V_{GDF}: The anti-parallel diode forward voltage drop which is in series with R_{OFF}. The diode in this example is an MSS1P4.
- I_{O-}: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance. (8)

In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{20V - 0.8V - 0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.6A \tag{9}$$

$$I_{OB-=} \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{20V\text{-}0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.7A \tag{10}$$

Therefore, the high-side and low-side peak sink current is 3.6 A and 3.7 A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

9.2.2.4 Estimate Gate Driver Power Loss

The total loss, P_G, in the gate driver subsystem includes the power losses of the UCC21521 (P_{GD}) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in P_G and not discussed in this section.

P_{GD} is the key power loss which determines the thermal safety-related limits of the UCC21521, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. P_{GDQ} is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. 图 4 shows the per output channel current consumption vs. operating frequency with no load. In this example, V_{VCCI} = 5 V and V_{VDD} = 20 V. The current on each power supply, with INA/INB switching from 0 V to 3.3 V at 100 kHz is measured to be I_{VCCI} = 2.5 mA, and I_{VDDA} = I_{VDDB} = 1.5 mA. Therefore, the P_{GDQ} can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} \approx 72mW \tag{11}$$

The second component is switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, P_{GSW}, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW}$$

where

- Q_G is the gate charge of the power transistor. (12)

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 20V \times 60nC \times 100kHz = 240mW \tag{13}$$

Q_G represents the total gate charge of the power transistor switching 800 V at 20 A, and is subject to change with different testing conditions. The UCC21521 gate driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} will be equal to P_{GSW} if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21521. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = P_{GSW} \times \left(\frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} \right) \tag{14}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21521 gate driver loss can be estimated with:

$$P_{GDO} = 240\text{mW} \times \left(\frac{5\Omega \,||\, 1.47\Omega}{5\Omega \,||\, 1.47\Omega + 2.2\Omega + 4.6\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 4.6\Omega} \right) \approx 60\text{mW} \tag{15}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = 2 \times f_{SW} \times \left[4A \times \int_0^{T_{R\_Sys}} \left(V_{DD} - V_{OUTA/B}(t) \right) dt + 6A \times \int_0^{T_{F\_Sys}} V_{OUTA/B}(t)\, dt \right]$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted. (16)

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the P_{GDO} will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21521, P_{GD}, is:

$$P_{GD} = P_{GDO} + P_{GDO} \tag{17}$$

which is equal to 127 mW in the design example.

9.2.2.5 Estimating Junction Temperature

The junction temperature (T_J) of the UCC21521 can be estimated with:

$$T_J = T_C + R_{\theta JC} \times P_{GD}$$

where

- T_C is the UCC21521 case-top temperature measured with a thermocouple or some other instrument, $R_{\theta JC}$ is the Junction-to-case-top thermal resistance from the Thermal Information table. Importantly, $R_{\theta JA}$, the junction to ambient thermal impedance provided in the Thermal Information table, is developed based on JEDEC standard PCB board and it is subject to change when the PCB board layout is different. (18)

9.2.2.6 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 V_{DC} is applied.

9.2.2.6.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

9.2.2.6.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{Total} = Q_G + \frac{I_{VDD}@100kHz\left(\text{No Load}\right)}{f_{SW}} = 60nC + \frac{1.5mA}{100kHz} = 75nC$$

where

- Q_G: Gate charge of the power transistor.
- I_{VDD}: The channel self-current consumption with no load at 100kHz.
- (19)

Therefore, the absolute minimum C_{Boot} requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{VDDA}} = \frac{75nC}{0.5V} = 150nF$$

where

- ΔV_{VDDA} is the voltage ripple at VDDA, which is 0.5 V in this example. (20)

In practice, the value of C_{Boot} is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the C_{Boot} value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

$$C_{Boot} = 1\mu F \tag{21}$$

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor with a low capacitance value, in this example a 100 nF, in parallel with C_{Boot} to optimize the transient performance.

注

Too large C_{BOOT} is not good. C_{BOOT} may not be charged within the first few cycles and V_{BOOT} could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial C_{BOOT} charging cycles, the bootstrap diode has highest reverse recovery current and losses.

9.2.2.6.3 Select a VDDB Capacitor

Chanel B has the same current requirements as Channel A, Therefore, a VDDB capacitor (Shown as C_{VDD} in 图 41) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for C_{VDD}. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor, with a value over 10 µF, should be used in parallel with CVDD.

9.2.2.7 Dead Time Setting Guidelines

For power converter topologies utilizing half-bridges, the dead time setting between the top and bottom transistor is important for preventing shoot-through during dynamic switching.

The UCC21521 dead time specification in the electrical table is defined as the time interval from 90% of one channel's falling edge to 10% of the other channel's rising edge (see 图 35). This definition ensures that the dead time setting is independent of the load condition, and guarantees linearity through manufacture testing. However, this dead time setting may not reflect the dead time in the power converter system, since the dead time setting is dependent on the external gate drive turn-on/off resistor, DC-Link switching voltage/current, as well as the input capacitance of the load transistor.

Here is a suggestion on how to select an appropriate dead time for UCC21521:

$$DT_{Setting} = DT_{Req} + T_{F\_Sys} + T_{R\_Sys} - T_{D(on)}$$

where

- $DT_{setting}$: UCC21521 dead time setting in ns, $DT_{Setting}$ = 10 × RDT(in kΩ).
- DT_{Req}: System required dead time between the real V_{GS} signal of the top and bottom switch with enough margin, or ZVS requirement.
- T_{F_Sys}: In-system gate turn-off falling time at worst case of load, voltage/current conditions.
- T_{R_Sys}: In-system gate turn-on rising time at worst case of load, voltage/current conditions.
- $T_{D(on)}$: Turn-on delay time, from 10% of the transistor gate signal to power transistor gate threshold. (22)

In the example, $DT_{Setting}$ is set to 250 ns.

It should be noted that the UCC21521 dead time setting is decided by the DT pin configuration (See Programmable Dead Time (DT) Pin), and it cannot automatically fine-tune the dead time based on system conditions. And it is recommended to parallel a ceramic capacitor, 2.2nF or above, with R_{DT} to achieve better noise immunity.

9.2.2.8 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

图 42 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, V_A, is equal to 25 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 25 V -– 5.1 V ≈ 20 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from R_Z.

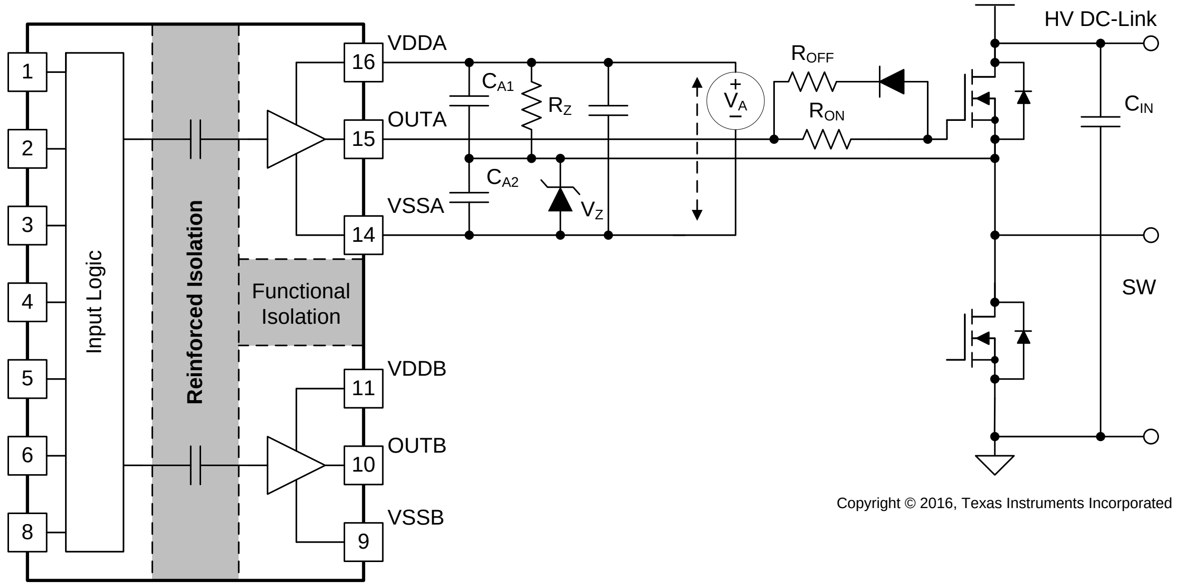

图 42. Negative Bias with Zener Diode on Iso-Bias Power Supply Output

图 43 shows another example which uses two supplies (or single-input-double-output power supply). Power supply V_{A+} determines the positive drive output voltage and $V_{A–}$ determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

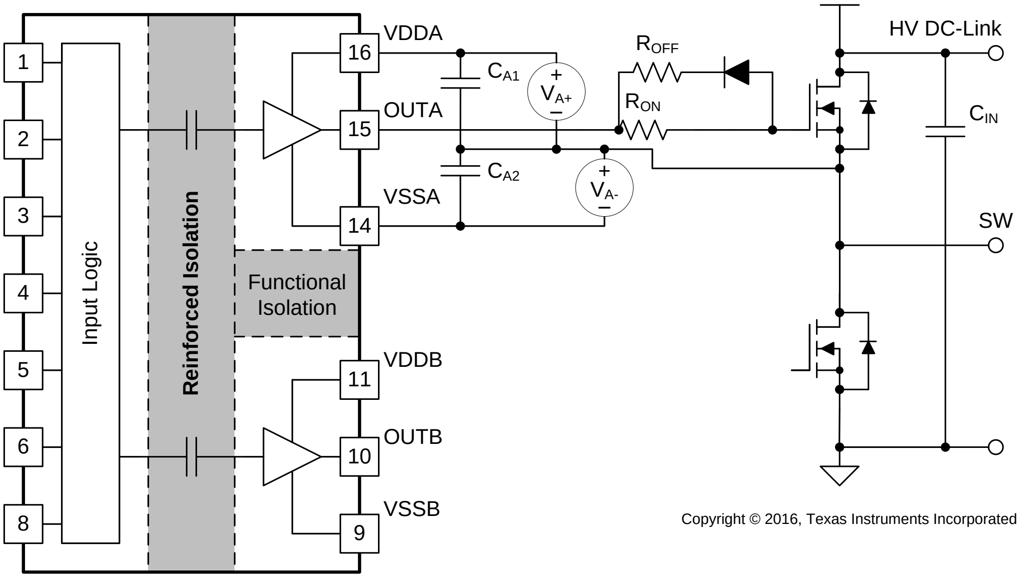

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图 43. Negative Bias with Two Iso-Bias Power Supplies

The last example, shown in 图 44, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors which favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

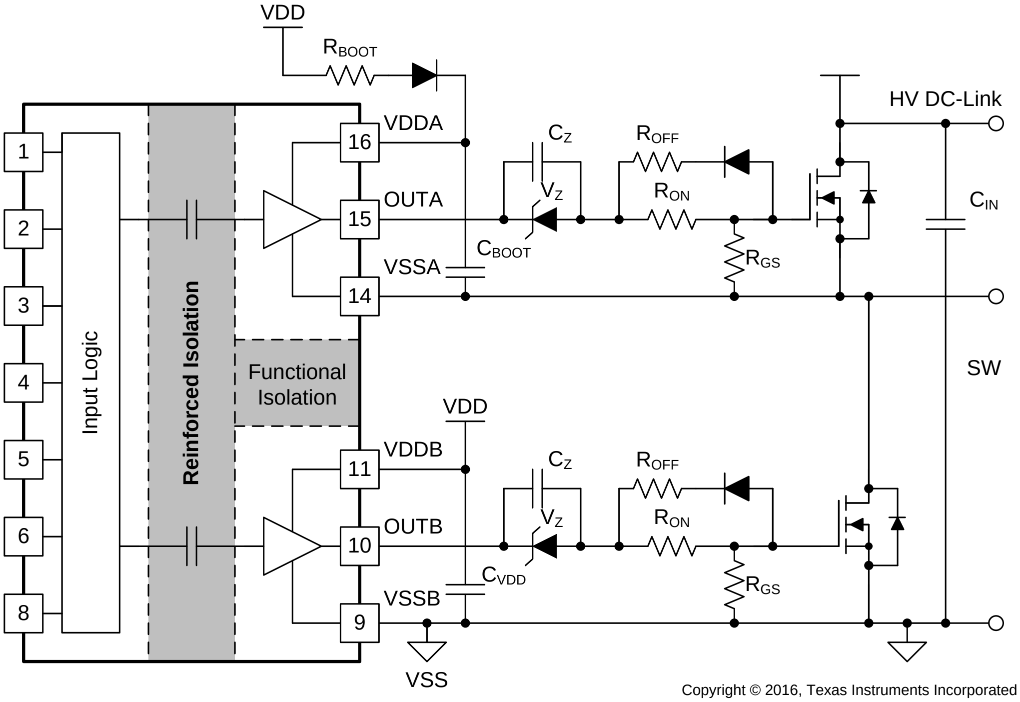


图 44. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

9.2.3 Application Curves

图 45 and 图 46 shows the bench test waveforms for the design example shown in 图 41 under these conditions: VCC = 5 V, VDD = 20 V, f_{SW} = 100 kHz, $V_{DC\text{-}Link}$ = 0 V.

Channel 1 (Yellow): UCC21521 INA pin signal.

Channel 2 (Blue): UCC21521 INB pin signal.

Channel 3 (Pink): Gate-source signal on the high side power transistor.

Channel 4 (Green): Gate-source signal on the low side power transistor.

In 图 45, INA and INB are sent complimentary 3.3-V, 50% duty-cycle signals. The gate drive signals on the power transistor have a 250-ns dead time, shown in the measurement section of 图 45.

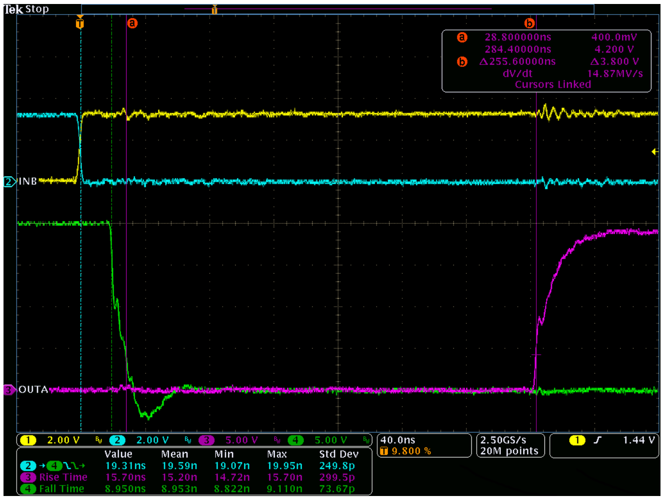
注

The dead-time matching is less than 1 ns with the 250-ns dead-time setting.

图 46 shows a zoomed-in version of the waveform of 图 45, with measurements for propagation delay and rising/falling time. Cursors are also used to measure dead time. Importantly, the output waveform is measured between the power transistors' gate and source pins, and is not measured directly from the driver OUTA and OUTB pins. Due to the split on and off resistors (R_{on},R_{off}) and different sink and source currents, different rising (16 ns) and falling time (9 ns) are observed in 图 46.

	Value	Mean	Min	Max	Std Dev
④→③	253.9ns	253.7n	253.1n	254.7n	341.2p
③→④	253.2ns	693.4n	252.3n	10.25µ	2.075µ
① Frequency	100.0kHz	1.056M	100.0k	28.96M	5.225M
② Frequency	100.0kHz	106.9k	100.0k	199.3k	25.16k

图 45. Bench Test Waveform for INA/B and OUTA/B



a	28.800000ns	400.0mV
	284.40000ns	4.200 V
b	Δ255.60000ns	Δ3.800 V
	dV/dt	14.87MV/s

Cursors Linked

	Value	Mean	Min	Max	Std Dev
②→④	19.31ns	19.59n	19.07n	19.95n	249.8p
③ Rise Time	15.70ns	15.20n	14.72n	15.70n	299.5p
④ Fall Time	8.950ns	8.953n	8.822n	9.110n	73.67p

图 46. Zoomed-In bench-test waveform

10 Power Supply Recommendations

The recommended input supply voltage (VCCI) for UCC21521 is between 3 V and 18 V. The output bias supply voltage (VDDA/VDDB) range depends on which version of UCC21521 one is using. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. One mustn't let VDD or VCCI fall below their respective UVLO thresholds (For more information on UVLO see VDD, VCCI, and Under Voltage Lock Out (UVLO)). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by UCC21521. All versions of UCC21521 have a recommended maximum VDDA/VDDB of 25 V.

A local bypass capacitor should be placed between the VDD and VSS pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested that one place two such capacitors: one with a value of between 220 nF and 10 µF for device biasing, and an additional 100-nF capacitor in parallel for high frequency filtering.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of UCC21521, this bypass capacitor has a minimum recommended value of 100 nF.

11 Layout

11.1 Layout Guidelines

One must pay close attention to PCB layout in order to achieve optimum performance for the UCC21521. Below are some key points.

Component Placement:

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

Grounding Considerations:

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

High-Voltage Considerations:

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC21521's isolation performance.
- For half-bridge, or high-side/low-side configurations, where the channel A and channel B drivers could operate with a DC-link voltage up to 1500 V_{DC}, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

Thermal Considerations:

- A large amount of power may be dissipated by the UCC21521 if the driving voltage is high, the load is heavy, or the switching frequency is high (Refer to Estimate Gate Driver Power Loss for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended (See 图 48 and 图 49). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. However, keep in mind that there shouldn't be any traces/coppers from different high voltage planes overlapping.

11.2 Layout Example

图 47 shows a 2-layer PCB layout example with the signals and key components labeled.

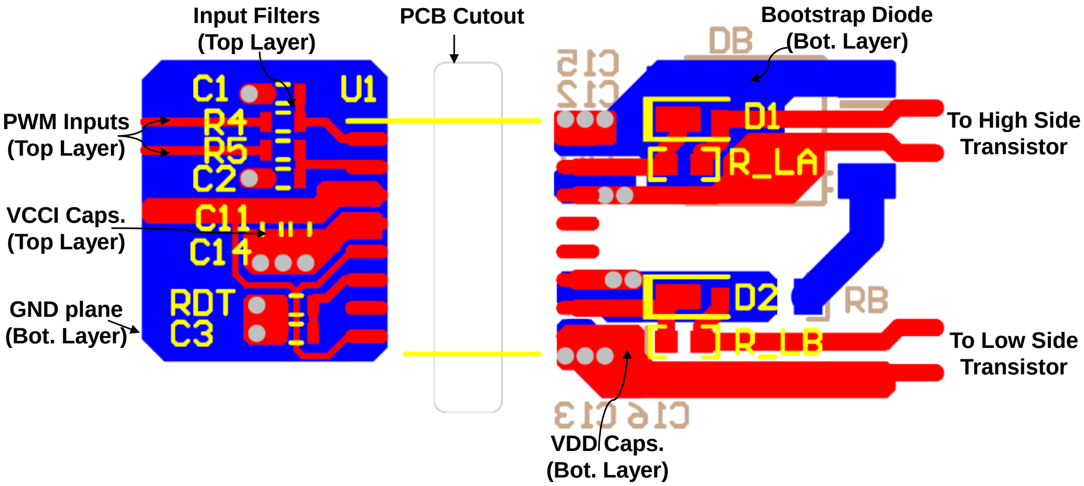


图 47. Layout Example

图 48 and 图 49 shows top and bottom layer traces and copper.

注

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

Layout Example (接下页)

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

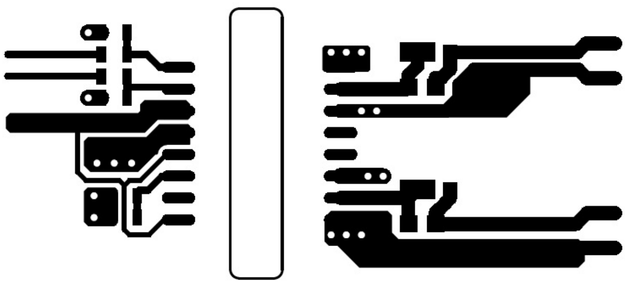


图 48. Top Layer Traces and Copper

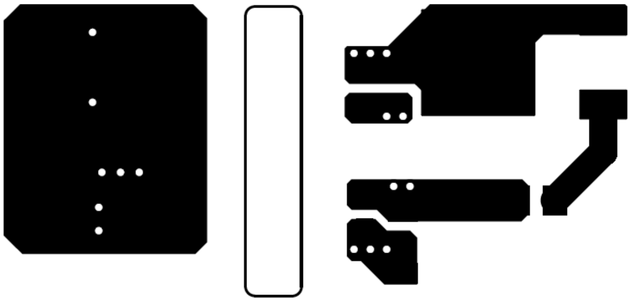


图 49. Bottom Layer Traces and Copper

图 50 and 图 51 are 3D layout pictures with top view and bottom views.

注

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

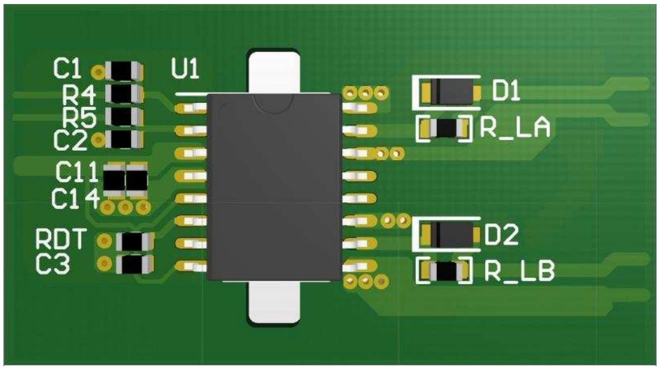


图 50. 3-D PCB Top View

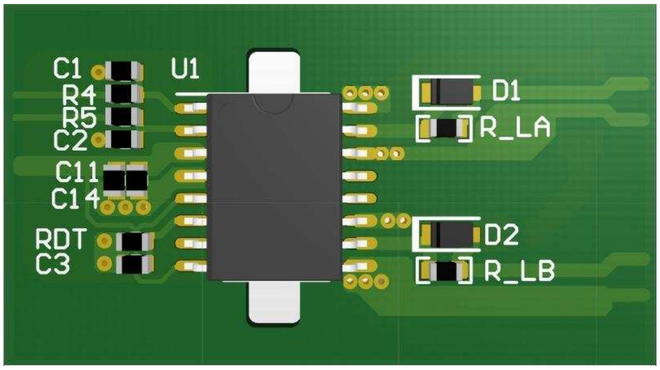


图 51. 3-D PCB Bottom View

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- 隔离相关术语

12.2 认证

UL 在线认证目录，*“FPPT2.E181974 非光学隔离器件 - 组件”*证书编号：20160516-E181974

VDE 在线认证目录，*“工厂监控符合性认证”*证书编号：40040142

12.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.6 静电放电警告

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC21521ADW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC21521A	Samples
UCC21521ADWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC21521A	Samples
UCC21521CDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC21521C	Samples
UCC21521CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC21521C	Samples
UCC21521DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC21521	Samples
UCC21521DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC21521	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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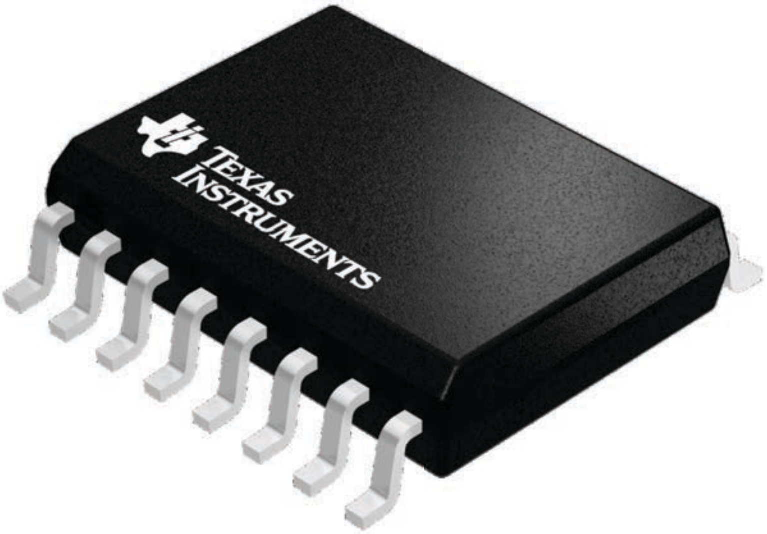
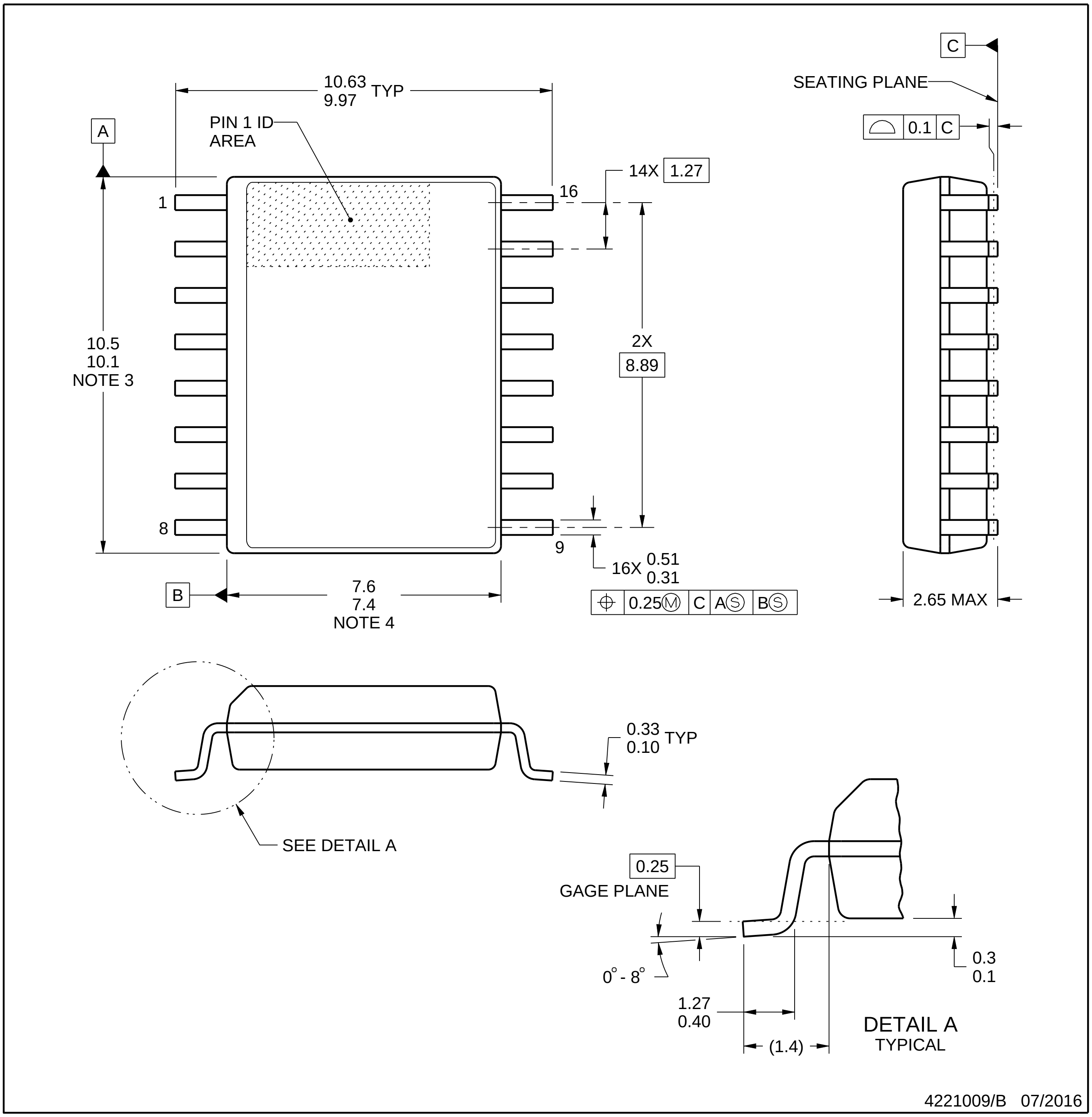
GENERIC PACKAGE VIEW

DW 16 **SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch SMALL OUTLINE INTEGRATED CIRCUIT

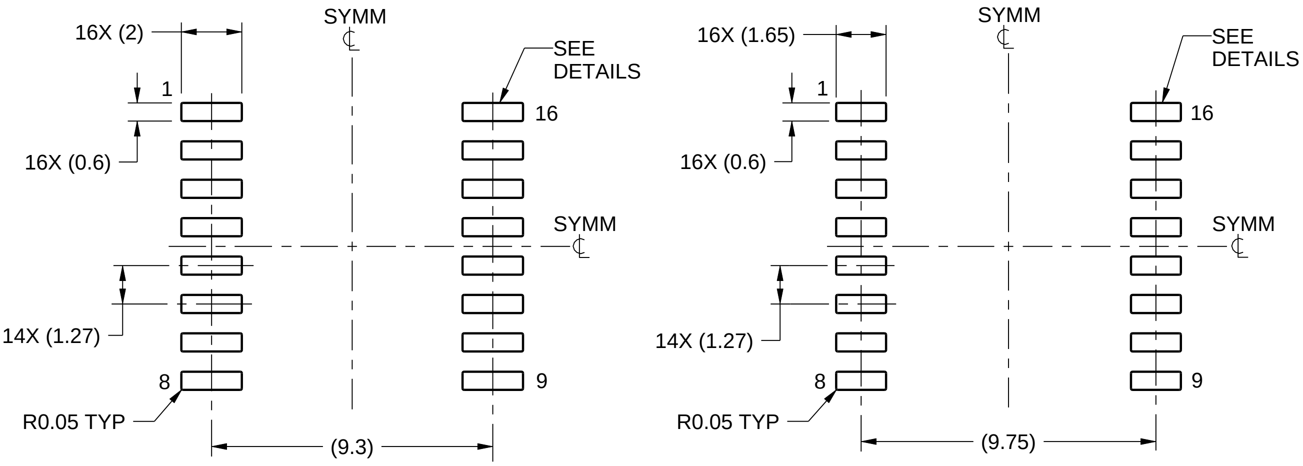
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





NOTES:

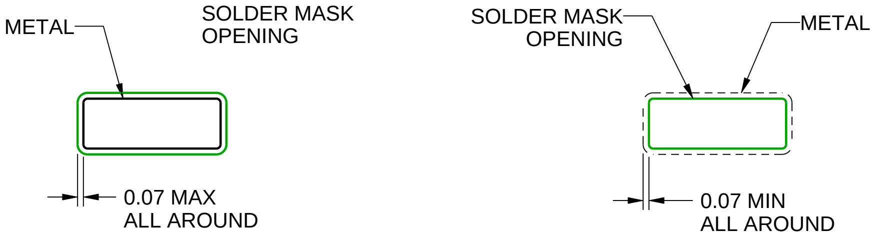
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK
DEFINED

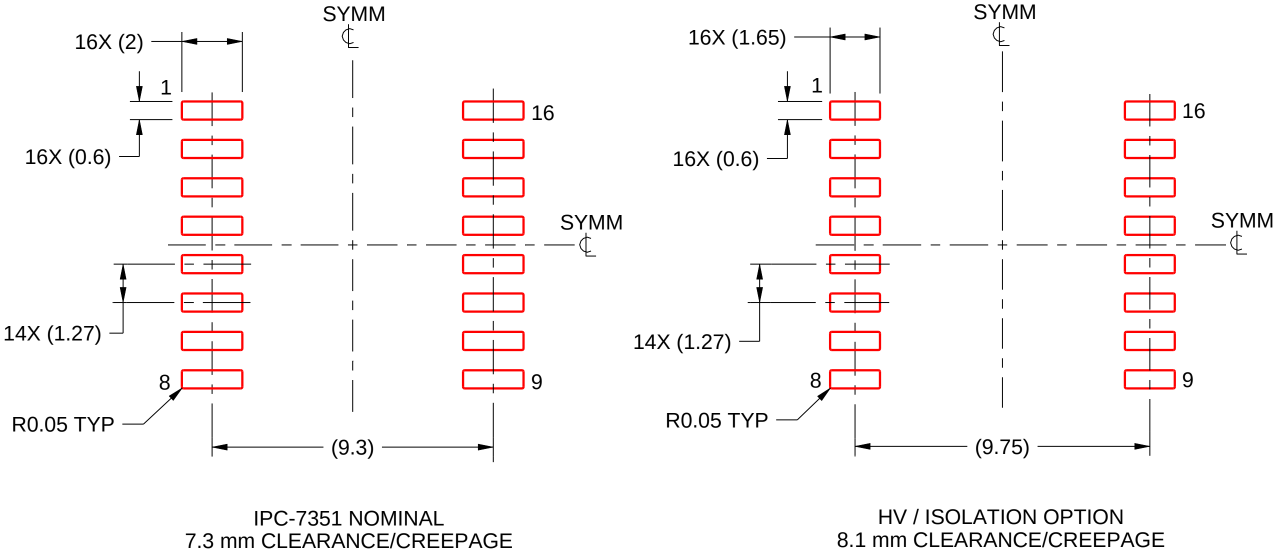
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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