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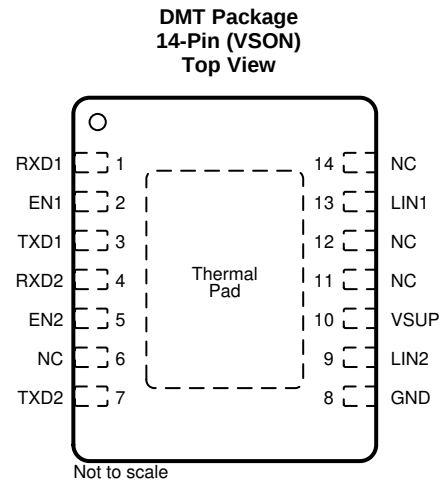
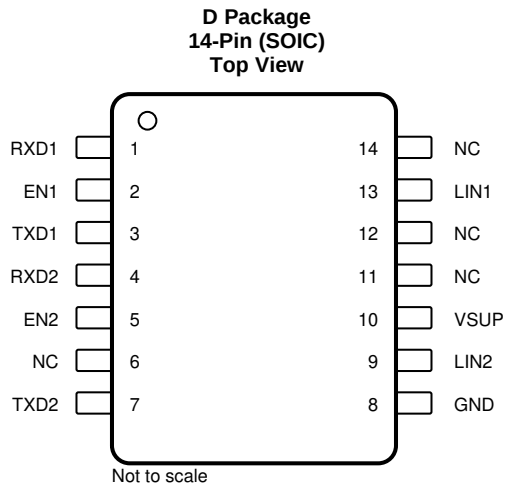
## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| <b>Changes from Revision A (January 2019) to Revision B</b>                                                                                             | <b>Page</b> |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • 将“特性”中的“ $\pm 58\text{V}$ LIN 总线故障保护”更改为“ $\pm 60\text{V}$ LIN 总线故障保护”                                                                                | <b>1</b>    |
| • 删除了 VSON (14) (DMT) 封装中的产品预发布                                                                                                                         | <b>1</b>    |
| • Changed $V_{\text{SUP}}$ from max = 58 V to max = 60 V in Absolute Maximum Ratings                                                                    | <b>4</b>    |
| • Changed $V_{\text{LIN}}$ from min = -58 V, max = 58 V to min = -60 V, max = 60 V in Absolute Maximum Ratings                                          | <b>4</b>    |
| • Changed $V_{\text{LOGIC}}$ from max = 5.5 V to: 6 V in Absolute Maximum Ratings                                                                       | <b>4</b>    |
| • Changed $C_{\text{LINPIN}}$ from max = 45 pF to max = 25 pF and added $V_{\text{SUP}} = 14\text{ V}$ for test condition in electrical characteristics | <b>6</b>    |

| <b>Changes from Original (December 2017) to Revision A</b> | <b>Page</b> |
|------------------------------------------------------------|-------------|
| • 将 VSON 尺寸从“3.00mm x 3.00mm”更改为“3.00mm x 4.50mm”          | <b>1</b>    |

## 5 Pin Configuration and Functions



### Pin Functions

| PIN           |      | Type   | DESCRIPTION                                                                                 |
|---------------|------|--------|---------------------------------------------------------------------------------------------|
| NO.           | NAME |        |                                                                                             |
| 1             | RXD1 | O      | Channel 1 RXD Output (open-drain) interface reporting state of LIN bus voltage              |
| 2             | EN1  | I      | Channel 1 Enable Input                                                                      |
| 3             | TXD1 | I      | Channel 1 TXD input interface to control state of LIN output                                |
| 4             | RXD2 | O      | Channel 2 RXD Output (open-drain) interface reporting state of LIN bus voltage              |
| 5             | EN2  | I      | Channel 2 Enable Input                                                                      |
| 7             | TXD2 | I      | Channel 2 TXD input interface to control state of LIN output                                |
| 8             | GND  | GND    | Ground                                                                                      |
| 9             | LIN2 | HV I/O | Channel 2 High voltage LIN bus single-wire transmitter and receiver                         |
| 10            | VSUP | Supply | Device Supply Voltage (connected to battery in series with external reverse blocking diode) |
| 13            | LIN1 | HV I/O | Channel 1 High voltage LIN bus single-wire transmitter and receiver                         |
| 6, 11, 12, 14 | NC   | –      | Not Connected                                                                               |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

| Symbol             | Parameter                                      | MIN  | MAX | UNIT |
|--------------------|------------------------------------------------|------|-----|------|
| V <sub>SUP</sub>   | Supply voltage range (ISO/DIS 17987 Param 10)  | −0.3 | 60  | V    |
| V <sub>LIN</sub>   | LIN Bus input voltage (ISO/DIS 17987 Param 82) | −60  | 60  | V    |
| V <sub>LOGIC</sub> | Logic Pin Voltage (RXD, TXD, EN)               | −0.3 | 6   | V    |
| T <sub>A</sub>     | Ambient temperature range                      | −40  | 125 | °C   |
| T <sub>J</sub>     | Junction Temp                                  | −55  | 150 | °C   |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

| ESD Ratings        |                         |                                                        | VALUE                                            | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------|--------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM) per AEC Q100-002 <sup>(1)</sup> | Pins RXD, RXD, EN <sup>(1)</sup>                 | ±4000 |
|                    |                         |                                                        | Pins LIN Bus <sup>(2)</sup> and V <sub>SUP</sub> | ±8000 |
|                    |                         | Charged device model (CDM), per AEC Q100-011           | All pins                                         | ±1500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) LIN bus a stressed with respect to GND.

### 6.3 ESD Ratings - IEC

| ESD and Surge Protection Ratings                                                                                       |                                                                        |                                                        | VALUE  | UNIT |
|------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------|--------------------------------------------------------|--------|------|
| V <sub>(ESD)</sub>                                                                                                     | IEC 61000-4-2 contact discharge electrostatic discharge <sup>(1)</sup> | LIN bus and V <sub>SUP</sub> pin to GND <sup>(2)</sup> | ±6000  | V    |
| V <sub>(ESD)</sub>                                                                                                     | IEC 61000-4-2 air-gap discharge electrostatic discharge <sup>(1)</sup> | LIN bus and V <sub>SUP</sub> pin to GND <sup>(2)</sup> | ±15000 |      |
| V <sub>(ESD)</sub>                                                                                                     | Powered ESD Performance, per SAEJ2962-1 <sup>(3)</sup>                 | contact discharge                                      | ±8000  | V    |
| V <sub>(ESD)</sub>                                                                                                     | Powered ESD Performance, per SAEJ2962-1 <sup>(3)</sup>                 | air-gap discharge                                      | ±15000 |      |
| ISO7637-2 <sup>(4)</sup> & IEC 62215-3 Transients according to IBEE LIN EMC test spec LIN bus pin and V <sub>SUP</sub> |                                                                        | Pulse 1                                                | −100   | V    |
|                                                                                                                        |                                                                        | Pulse 2                                                | 75     | V    |
| ISO7637-2 <sup>(4)</sup> & IEC 62215-3 Transients according to IBEE LIN EMC test spec LIN bus pin and V <sub>SUP</sub> |                                                                        | Pulse 3a                                               | −150   | V    |
|                                                                                                                        |                                                                        | Pulse 3b                                               | 100    | V    |

- (1) IEC 61000-4-2 is a system level ESD test. Results given here are specific to the IBEE LIN EMC Test specification conditions. Different system level configurations may lead to different results
- (2) Testing performed at 3rd party IBEE Zwickau test house, test report available upon request
- (3) SAEJ2962-1 Testing performed at 3rd party US3 approved EMC test facility, test report available upon request
- (4) ISO7637 is a system level transient test. Results given here are specific to the IBEE LIN EMC Test specification conditions. Different system level configurations may lead to different results.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                            | TLIN2022D-Q1 | TLIN2022DMT-Q1 | UNIT |
|-------------------------------|--------------------------------------------|--------------|----------------|------|
|                               |                                            | D (SOIC)     | DMT (VSON)     |      |
|                               |                                            | 14-PINS      | 14-PINS        |      |
| R <sub>ΘJA</sub>              | Junction-to-ambient thermal resistance     | 82.3         | 35.5           | °C/W |
| R <sub>ΘJC(top)</sub>         | Junction-to-case (top) thermal resistance  | 41.5         | 18.1           | °C/W |
| R <sub>ΘJB</sub>              | Junction-to-board thermal resistance       | 38.4         | 13.1           | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter | 8.9          | 0.6            | °C/W |

- (1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## Thermal Information (continued)

| THERMAL METRIC <sup>(1)</sup> |                                              | TLIN2022D-Q1 | TLIN2022DMT-Q1 | UNIT |
|-------------------------------|----------------------------------------------|--------------|----------------|------|
|                               |                                              | D (SOIC)     | DMT (VSON)     |      |
|                               |                                              | 14-PINS      | 14-PINS        |      |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 38.1         | 13.1           | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | n/a          | 2.5            | °C/W |

## 6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER - DEFINITION |                                  | MIN | NOM | MAX  | UNIT |
|------------------------|----------------------------------|-----|-----|------|------|
| $V_{SUP}$              | Supply voltage                   | 4   |     | 48   | V    |
| $V_{LIN}$              | LIN Bus input voltage            | 0   |     | 48   | V    |
| $V_{LOGIC}$            | Logic Pin Voltage (RXD, TXD, EN) | 0   |     | 5.25 | V    |
| TSD                    | Thermal shutdown edge            | 165 |     |      | °C   |
| TSD <sub>(HYS)</sub>   | Thermal shutdown hysteresis      |     | 15  |      | °C   |

## 6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                          |                                                                                                                                                               | TEST CONDITIONS                                                                                                                                                           | MIN  | TYP | MAX  | UNIT |
|------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|------|------|
| <b>Power Supply</b>                |                                                                                                                                                               |                                                                                                                                                                           |      |     |      |      |
| $V_{SUP}$                          | Operational supply voltage (ISO/DIS 17987 Param 10, 53)                                                                                                       | Device is operational beyond the LIN defined nominal supply voltage range See <a href="#">Fig 8</a> and <a href="#">Fig 9</a>                                             | 4    |     | 48   | V    |
| $V_{SUP}$                          | Nominal supply voltage (ISO/DIS 17987 Param 10, 53): Normal Mode: Ramp $V_{SUP}$ while LIN signal is a 10 kHz Square Wave with 50 % duty cycle and 18V swing. | Normal and Standby Modes: Ramp $V_{SUP}$ while LIN signal is a 10 kHz Square Wave with 50 % duty cycle and 36V swing. See <a href="#">Fig 8</a> and <a href="#">Fig 9</a> | 4    |     | 48   | V    |
|                                    |                                                                                                                                                               | Sleep Mode                                                                                                                                                                | 4    |     | 48   | V    |
| $UV_{SUP}$                         | Under voltage $V_{SUP}$ threshold                                                                                                                             |                                                                                                                                                                           | 2.9  |     | 3.85 | V    |
| $UV_{HYS}$                         | Delta hysteresis voltage for $V_{SUP}$ under voltage threshold                                                                                                |                                                                                                                                                                           |      | 0.2 |      | V    |
| $I_{SUP}$                          | Supply Current                                                                                                                                                | Normal Mode: EN = High, bus dominant: total bus load where $R_{LIN} > 500 \Omega$ and $C_{LIN} < 10 \text{ nF}$ See <a href="#">Fig 14</a>                                |      | 1.2 | 7.5  | mA   |
| $I_{SUP}$                          | Supply Current                                                                                                                                                | Standby Mode: EN = Low, bus dominant: total bus load where $R_{LIN} > 500 \Omega$ and $C_{LIN} < 10 \text{ nF}$ See <a href="#">Fig 14</a>                                |      | 1.1 | 3.75 | mA   |
| $I_{SUP}$                          | Supply Current                                                                                                                                                | Normal Mode: EN = High, Bus Recessive: LIN = $V_{SUP}$ ,                                                                                                                  |      | 670 | 1300 | μA   |
| $I_{SUP}$                          | Supply Current                                                                                                                                                | Standby Mode: EN = Low, Bus Recessive: LIN = $V_{SUP}$ ,                                                                                                                  |      | 20  | 40   | μA   |
| $I_{SUP}$                          | Supply Current                                                                                                                                                | Sleep Mode: 4.0 V < $V_{SUP}$ < 14 V, LIN = $V_{SUP}$ , EN = 0 V, TXD and RXD Floating                                                                                    |      | 10  | 20   | μA   |
| $I_{SUP}$                          | Supply Current                                                                                                                                                | Sleep Mode: 14 V < $V_{SUP}$ < 36 V, LIN = $V_{SUP}$ , EN = 0 V, TXD and RXD Floating                                                                                     |      |     | 30   | μA   |
| <b>RXD OUTPUT PIN (OPEN DRAIN)</b> |                                                                                                                                                               |                                                                                                                                                                           |      |     |      |      |
| $V_{OL}$                           | Output Low voltage                                                                                                                                            | Based upon External pull up to $V_{CC}$                                                                                                                                   |      |     | 0.6  | V    |
| $I_{OL}$                           | Low level output current, open drain                                                                                                                          | LIN = 0 V, RXD = 0.4 V                                                                                                                                                    |      | 1.5 |      | mA   |
| $I_{ILG}$                          | Leakage current, high-level                                                                                                                                   | LIN = $V_{SUP}$ , RXD = 5 V                                                                                                                                               | -5   | 0   | 5    | μA   |
| <b>TXD INPUT PIN</b>               |                                                                                                                                                               |                                                                                                                                                                           |      |     |      |      |
| $V_{IL}$                           | Low level input voltage                                                                                                                                       |                                                                                                                                                                           | -0.3 |     | 0.8  | V    |
| $V_{IH}$                           | High level input voltage                                                                                                                                      |                                                                                                                                                                           | 2    |     | 5.5  | V    |
| $V_{HYS}$                          | Input threshold voltage, normal modes & selective wake modes                                                                                                  |                                                                                                                                                                           |      | 50  | 500  | mV   |

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                                                                           | TEST CONDITIONS                                                                                                          | MIN   | TYP | MAX   | UNIT      |
|----------------------|---------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|-------|-----|-------|-----------|
| $I_{ILG}$            | Low level input leakage current                                           | TXD = Low                                                                                                                | –5    | 0   | 5     | $\mu A$   |
| $R_{TXD}$            | Internal pulldown resistor value                                          |                                                                                                                          | 125   | 350 | 800   | $k\Omega$ |
| <b>EN INPUT PIN</b>  |                                                                           |                                                                                                                          |       |     |       |           |
| $V_{IL}$             | Low level input voltage                                                   |                                                                                                                          | –0.3  |     | 0.8   | V         |
| $V_{IH}$             | High level input voltage                                                  |                                                                                                                          | 2     |     | 5.5   | V         |
| $V_{HYS}$            | Hysteresis voltage                                                        | By design and characterization                                                                                           |       | 50  | 500   | mV        |
| $I_{ILG}$            | Low level input current                                                   | EN = Low                                                                                                                 | –5    | 0   | 5     | $\mu A$   |
| $R_{EN}$             | Internal Pulldown resistor                                                |                                                                                                                          | 125   | 350 | 800   | $k\Omega$ |
| <b>LIN PIN</b>       |                                                                           |                                                                                                                          |       |     |       |           |
| $V_{OH}$             | High level output voltage                                                 | LIN recessive, TXD = high, $I_O = 0$ mA, $V_{SUP} = 7$ V to 58 V                                                         | 0.85  |     |       | $V_{SUP}$ |
|                      |                                                                           | LIN recessive, TXD = high, $I_O = 0$ mA, $V_{SUP} = 4$ V $\leq V_{SUP} < 7$ V                                            | 3     |     |       | V         |
| $V_{OL}$             | Low level output voltage                                                  | LIN dominant, TXD = low, $V_{SUP} = 7$ V to 58 V                                                                         |       |     | 0.2   | $V_{SUP}$ |
|                      |                                                                           | LIN dominant, TXD = low, $V_{SUP} = 4$ V $\leq V_{SUP} < 7$ V                                                            |       |     | 1.2   | V         |
| $V_{SUP\_NON\_OP}$   | $V_{SUP}$ where Impact of recessive LIN Bus < 5% (ISO/DIS 17987 Param 56) | TXD & RXD open LIN = 4 V to 58 V                                                                                         | –0.3  |     | 58    | V         |
| $I_{BUS\_LIM}$       | Limiting current (ISO/DIS 17987 Param 57)                                 | TXD = 0 V, $V_{LIN} = 48$ V, $R_{MEAS} = 440 \Omega$ , $V_{SUP} = 48$ V, $V_{BUSdom} < 4.518$ V See <a href="#">图 13</a> | 75    | 120 | 300   | mA        |
| $I_{BUS\_PAS\_dom}$  | Receiver leakage current, dominant (ISO/DIS 17987 Param 58)               | LIN = 0 V, $V_{SUP} = 24$ V Driver off/recessive See <a href="#">图 14</a>                                                | –2    |     |       | mA        |
| $I_{BUS\_PAS\_rec1}$ | Receiver leakage current, recessive (ISO/DIS 17987 Param 59)              | LIN > $V_{SUP}$ , 8 V < $V_{SUP} < 48$ V Driver off; See <a href="#">图 15</a>                                            |       |     | 20    | $\mu A$   |
| $I_{BUS\_PAS\_rec2}$ | Receiver leakage current, recessive (ISO/DIS 17987 Param , 59)            | LIN = $V_{SUP}$ , Driver off; See <a href="#">图 15</a>                                                                   | –5    |     | 5     | $\mu A$   |
| $I_{BUS\_NO\_GND}$   | Leakage current, loss of ground (ISO/DIS 17987 Param 60)                  | GND = $V_{SUP}$ , 0 V $\leq V_{LIN} \leq 36$ V, $V_{SUP} = 24$ V; See <a href="#">图 16</a>                               | –2    |     | 2     | mA        |
| $I_{BUS\_NO\_BAT}$   | Leakage current, loss of supply (ISO/DIS 17987 Param 61)                  | 0 V $\leq V_{LIN} \leq 48$ V, $V_{SUP} = GND$ ; See <a href="#">图 17</a>                                                 |       |     | 5     | $\mu A$   |
| $V_{BUSdom}$         | Low level input voltage (ISO/DIS 17987 Param , 62)                        | LIN dominant (including LIN dominant for wake up) See <a href="#">图 10</a> and <a href="#">图 11</a>                      |       |     | 0.4   | $V_{SUP}$ |
| $V_{BUSrec}$         | High level input voltage (ISO/DIS 17987 Param , 63)                       | Lin recessive See <a href="#">图 10</a> and <a href="#">图 11</a>                                                          | 0.6   |     |       | $V_{SUP}$ |
| $V_{BUS\_CNT}$       | Receiver center threshold (ISO/DIS 17987 Param , 64)                      | $V_{BUS\_CNT} = (V_{I\_DOM} + V_{I\_REC})/2$ See <a href="#">图 10</a> and <a href="#">图 11</a>                           | 0.475 | 0.5 | 0.525 | $V_{SUP}$ |
| $V_{HYS}$            | Hysteresis voltage (ISO/DIS 17987 Param , 65)                             | $V_{HYS} = (V_{I\_REC} - V_{I\_DOM})$ See <a href="#">图 10</a> and <a href="#">图 11</a>                                  |       |     | 0.175 | $V_{SUP}$ |
| $V_{SERIAL\_DIODE}$  | Serial diode LIN term pullup path (ISO/DIS 17987 Param , 66)              | By design and characterization                                                                                           | 0.4   | 0.7 | 1     | V         |
| $R_{SLAVE}$          | Pullup resistor to $V_{SUP}$ (ISO/DIS 17987 Param , 71)                   | Normal and Standby modes                                                                                                 | 20    | 45  | 60    | $k\Omega$ |
| $I_{RSLEEP}$         | Pullup current source to $V_{SUP}$                                        | Sleep mode, $V_{SUP} = 27$ V, LIN = GND                                                                                  | –20   |     | –2    | $\mu A$   |
| $C_{LINPIN}$         | Capacitance of LIN pin                                                    | $V_{SUP} = 14$ V                                                                                                         |       |     | 25    | pF        |

## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER         |                                                      | TEST CONDITIONS                                                                                                                                                                                                                                                                       | MIN   | TYP | MAX   | UNIT |
|-------------------|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|-------|------|
| D1 <sub>12V</sub> | Duty Cycle 1 (ISO/DIS 17987 Param 27) <sup>(1)</sup> | $TH_{REC(MAX)} = 0.744 \times V_{SUP}$ , $TH_{DOM(MAX)} = 0.581 \times V_{SUP}$ , $V_{SUP} = 7\text{ V to }18\text{ V}$ , $t_{BIT} = 50\text{ }\mu\text{s}$ (20 kbps), $D1 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> )     | 0.396 |     |       |      |
| D1 <sub>12V</sub> | Duty Cycle 1                                         | $TH_{REC(MAX)} = 0.625 \times V_{SUP}$ , $TH_{DOM(MAX)} = 0.581 \times V_{SUP}$ , $V_{SUP} = 4\text{ V to }7\text{ V}$ , $t_{BIT} = 50\text{ }\mu\text{s}$ (20 kbps), $D1 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> )      | 0.396 |     |       |      |
| D2 <sub>12V</sub> | Duty Cycle 2 (ISO/DIS 17987 Param 28)                | $TH_{REC(MIN)} = 0.422 \times V_{SUP}$ , $TH_{DOM(MIN)} = 0.284 \times V_{SUP}$ , $V_{SUP} = 7.6\text{ V to }18\text{ V}$ , $t_{BIT} = 50\text{ }\mu\text{s}$ (20 kbps), $D2 = t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> )   |       |     | 0.581 |      |
| D3 <sub>12V</sub> | Duty Cycle 3 (ISO/DIS 17987 Param 29)                | $TH_{REC(MAX)} = 0.778 \times V_{SUP}$ , $TH_{DOM(MAX)} = 0.616 \times V_{SUP}$ , $V_{SUP} = 7\text{ V to }18\text{ V}$ , $t_{BIT} = 96\text{ }\mu\text{s}$ (10.4 kbps), $D3 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> )   | 0.417 |     |       |      |
| D3 <sub>12V</sub> | Duty Cycle                                           | $TH_{REC(MAX)} = 0.645 \times V_{SUP}$ , $TH_{DOM(MAX)} = 0.616 \times V_{SUP}$ , $V_{SUP} = 4\text{ V to }7\text{ V}$ , $t_{BIT} = 96\text{ }\mu\text{s}$ (10.4 kbps), $D3 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> )    | 0.417 |     |       |      |
| D4 <sub>12V</sub> | Duty Cycle 4 (ISO/DIS 17987 Param 30)                | $TH_{REC(MIN)} = 0.389 \times V_{SUP}$ , $TH_{DOM(MIN)} = 0.251 \times V_{SUP}$ , $V_{SUP} = 7.6\text{ V to }18\text{ V}$ , $t_{BIT} = 96\text{ }\mu\text{s}$ (10.4 kbps), $D4 = t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> ) |       |     | 0.59  |      |
| D1 <sub>24V</sub> | Duty Cycle 1 (ISO/DIS 17987 Param 27) <sup>(1)</sup> | $TH_{REC(MAX)} = 0.710 \times V_{SUP}$ , $TH_{DOM(MAX)} = 0.544 \times V_{SUP}$ , $V_{SUP} = 15\text{ V to }36\text{ V}$ , $t_{BIT} = 50\text{ }\mu\text{s}$ (20 kbps), $D1 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> )    | 0.33  |     |       |      |
| D2 <sub>24V</sub> | Duty Cycle 2 (ISO/DIS 17987 Param 28)                | $TH_{REC(MIN)} = 0.446 \times V_{SUP}$ , $TH_{DOM(MIN)} = 0.302 \times V_{SUP}$ , $V_{SUP} = 15.6\text{ V to }36\text{ V}$ , $t_{BIT} = 50\text{ }\mu\text{s}$ (20 kbps), $D2 = t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> )  |       |     | 0.642 |      |
| D3 <sub>24V</sub> | Duty Cycle 3 (ISO/DIS 17987 Param 29)                | $TH_{REC(MAX)} = 0.744 \times V_{SUP}$ , $TH_{DOM(MAX)} = 0.581 \times V_{SUP}$ , $V_{SUP} = 7\text{ V to }36\text{ V}$ , $t_{BIT} = 96\text{ }\mu\text{s}$ (10.4 kbps), $D3 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> )   | 0.386 |     |       |      |
| D3 <sub>24V</sub> | Duty Cycle                                           | $TH_{REC(MAX)} = 0.645 \times V_{SUP}$ , $TH_{DOM(MAX)} = 0.581 \times V_{SUP}$ , $V_{SUP} = 4\text{ V to }7\text{ V}$ , $t_{BIT} = 96\text{ }\mu\text{s}$ (10.4 kbps), $D3 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> )    | 0.386 |     |       |      |
| D4 <sub>24V</sub> | Duty Cycle 4 (ISO/DIS 17987 Param 30)                | $TH_{REC(MIN)} = 0.442 \times V_{SUP}$ , $TH_{DOM(MIN)} = 0.284 \times V_{SUP}$ , $V_{SUP} = 7.6\text{ V to }36\text{ V}$ , $t_{BIT} = 96\text{ }\mu\text{s}$ (10.4 kbps), $D4 = t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See <a href="#">Figure 18</a> and <a href="#">Figure 19</a> ) |       |     | 0.591 |      |

- (1) Duty cycles: LIN driver bus load conditions (CLINBUS, RLINBUS): Load1 = 1 nF, 1 k $\Omega$ ; Load2 = 10 nF, 500  $\Omega$ . Duty cycles 3 and 4 are defined for 10.4-kbps operation. The TLIN1029 also meets these lower data rate requirements, while it is capable of the higher speed 20-kbps operation as specified by duty cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details see the SAEJ2602 specification

## 6.8 Timing Requirements

| SYMBOL        | DESCRIPTION                                                                                                 | TEST CONDITIONS                                                                                                                                                                                                  | MIN | NOM | MAX | UNIT          |
|---------------|-------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| $t_{rx\_pdr}$ | Receiver rising propagation delay time (ISO/DIS 17987 Param 31)                                             | $R_{RXD} = 2.4\text{ k}\Omega$ , $C_{RXD} = 20\text{ pF}$ (See <a href="#">Figure 20</a> and <a href="#">Figure 21</a> )                                                                                         |     |     | 6   | $\mu\text{s}$ |
| $t_{rx\_pdf}$ | Receiver falling propagation delay time (ISO/DIS 17987 Param 31)                                            |                                                                                                                                                                                                                  |     |     | 6   | $\mu\text{s}$ |
| $t_{rs\_sym}$ | Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32) | Rising edge with respect to falling edge, $(tr_{x\_sym} = tr_{x\_pdf} - tr_{x\_pdr})$ , $R_{RXD} = 2.4\text{ k}\Omega$ , $C_{RXD} = 20\text{ pF}$ (See <a href="#">Figure 20</a> and <a href="#">Figure 21</a> ) | -2  |     | 2   | $\mu\text{s}$ |

**Timing Requirements (continued)**

| SYMBOL             | DESCRIPTION                                                                                                                                          | TEST CONDITIONS                                                                                                | MIN | NOM | MAX | UNIT    |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------|
| $t_{LINBUS}$       | LIN wakeup time (Minimum dominant time on LIN bus for wakeup)                                                                                        | See 图 24, 图 27 and 图 28                                                                                        | 25  | 100 | 150 | $\mu s$ |
| $t_{CLEAR}$        | Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bust stuck dominant fault) | See 图 28                                                                                                       | 8   | 17  | 50  | $\mu s$ |
| $t_{DST}$          | Dominant state time out                                                                                                                              |                                                                                                                | 20  | 34  | 80  | ms      |
| $t_{MODE\_CHANGE}$ | Mode change delay time                                                                                                                               | Time to change from standby mode to normal mode or normal mode to sleep mode through EN pin: See 图 22 and 图 29 | 2   |     | 15  | $\mu s$ |
| $t_{NOMINT}$       | Normal mode initialization time                                                                                                                      | Time for normal mode to initialize and data on RXD pin to be valid See 图 22                                    |     |     | 35  | $\mu s$ |
| $t_{PWR}$          | Power up time                                                                                                                                        | Upon power up time it takes for valid data on RXD                                                              |     |     | 1.5 | ms      |

## 6.9 Typical Characteristics

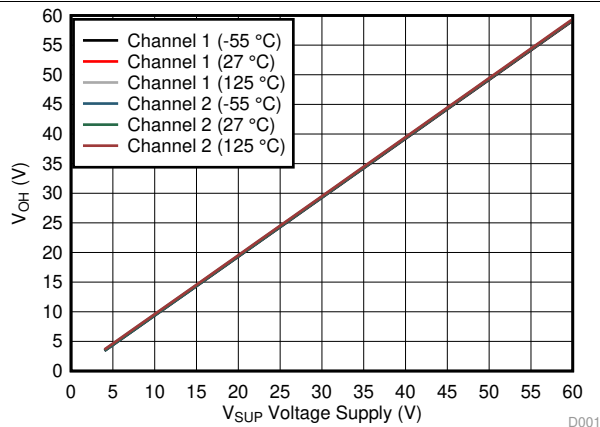


图 1.  $V_{OH}$  vs  $V_{SUP}$  and Temperature

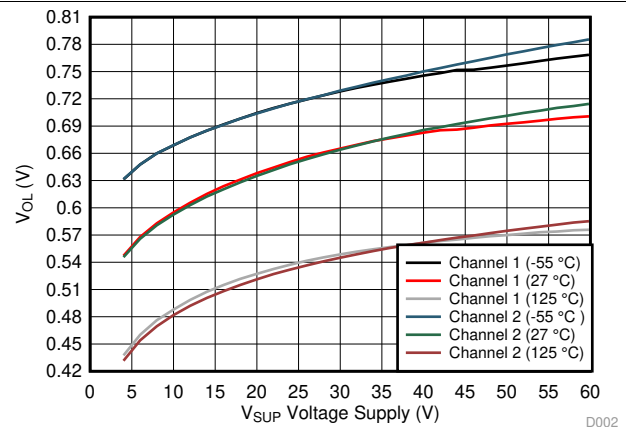
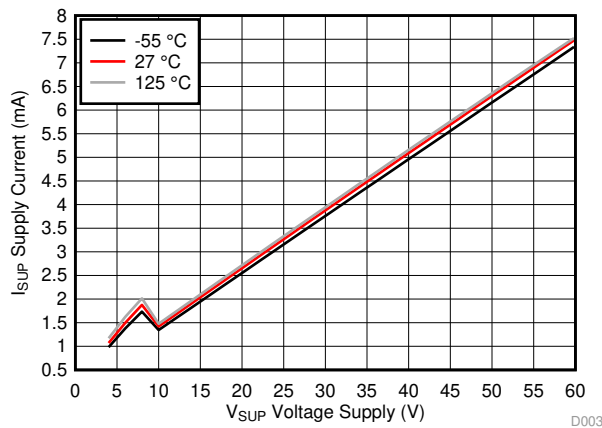
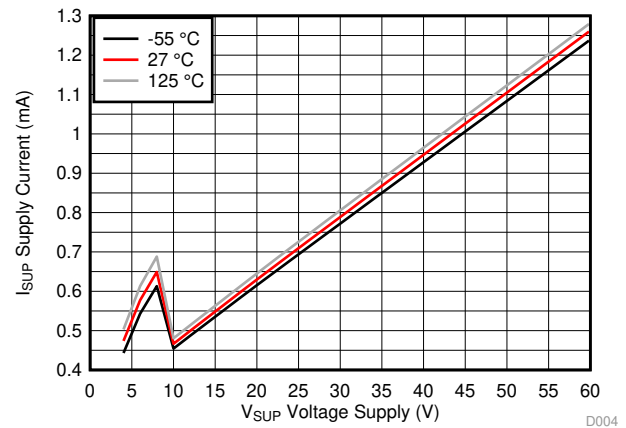


图 2.  $V_{OL}$  vs  $V_{SUP}$  and Temperature



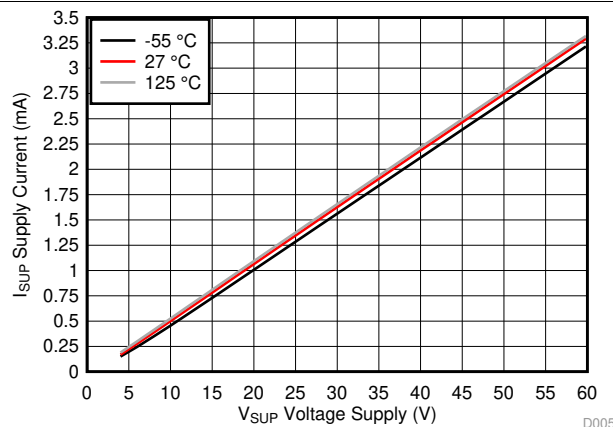
Normal Mode (Dominant)

图 3. Supply Current vs Voltage Supply Across Temperature



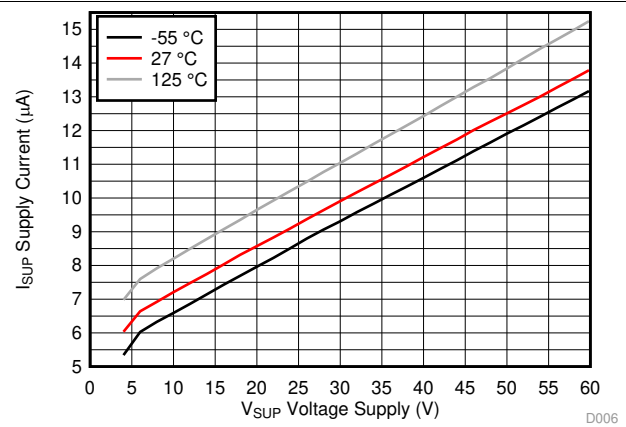
Normal Mode (Recessive)

图 4. Supply Current vs Voltage Supply Across Temperature



Standby Mode (Dominant)

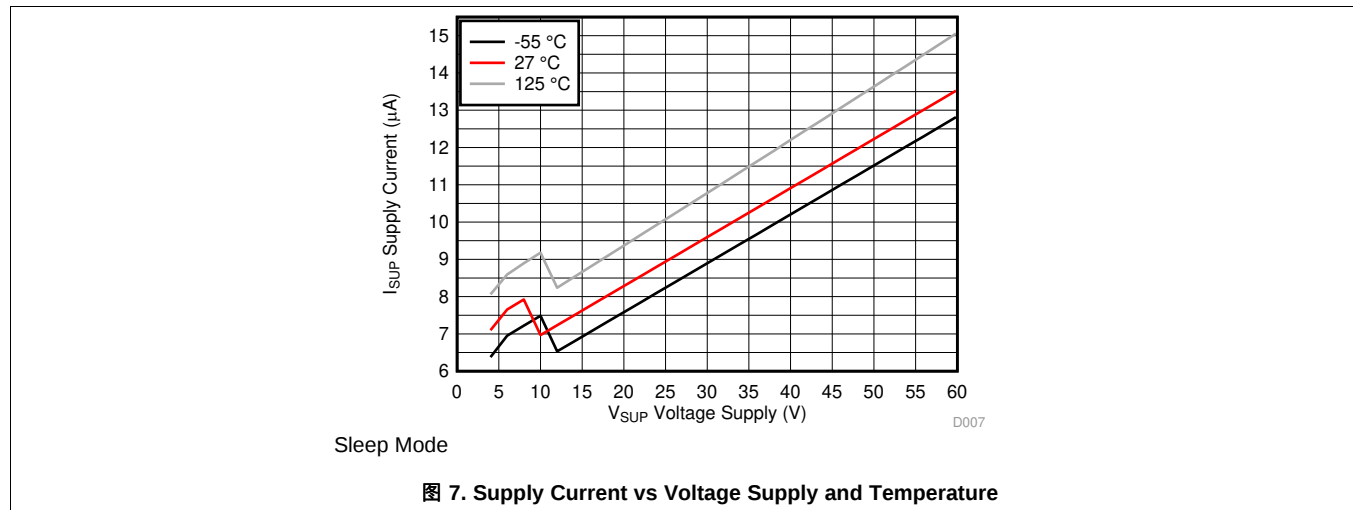
图 5. Supply Current vs Voltage Supply and Temperature



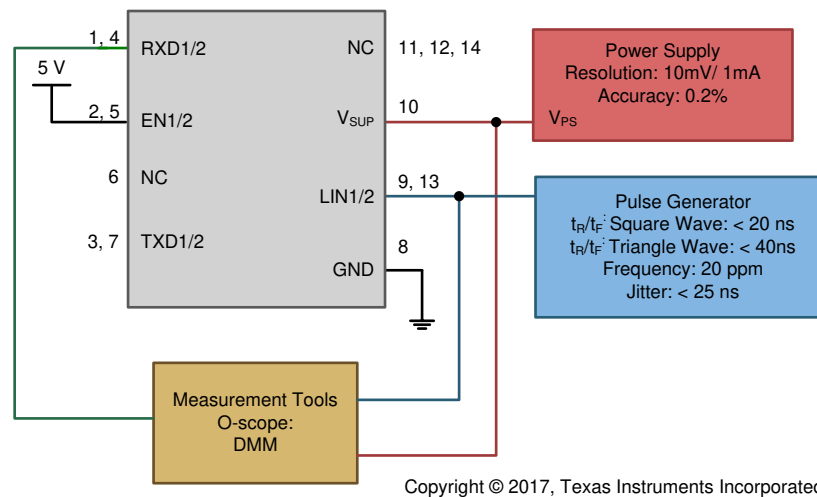
Standby Mode (Recessive)

图 6. Supply Current vs Voltage Supply and Temperature

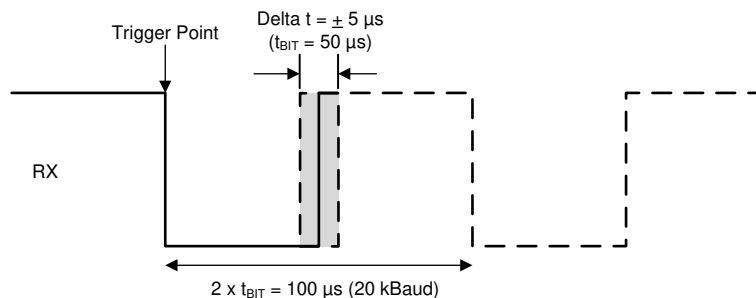
## Typical Characteristics (接下页)



## 7 Parameter Measurement Information



**图 8. Test System: Operating Voltage Range with RX and TX Access: Parameters 9, 10**



**图 9. RX Response: Operating Voltage Range**

## Parameter Measurement Information (接下页)

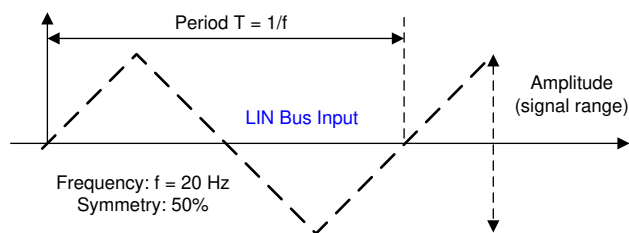
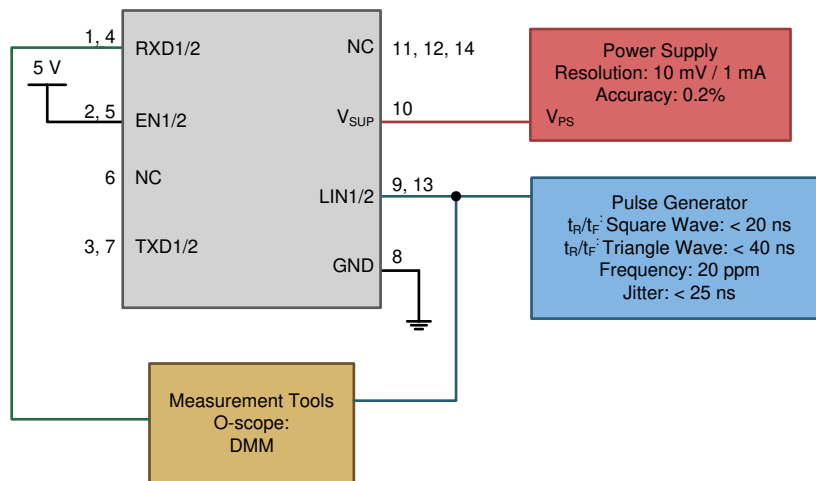
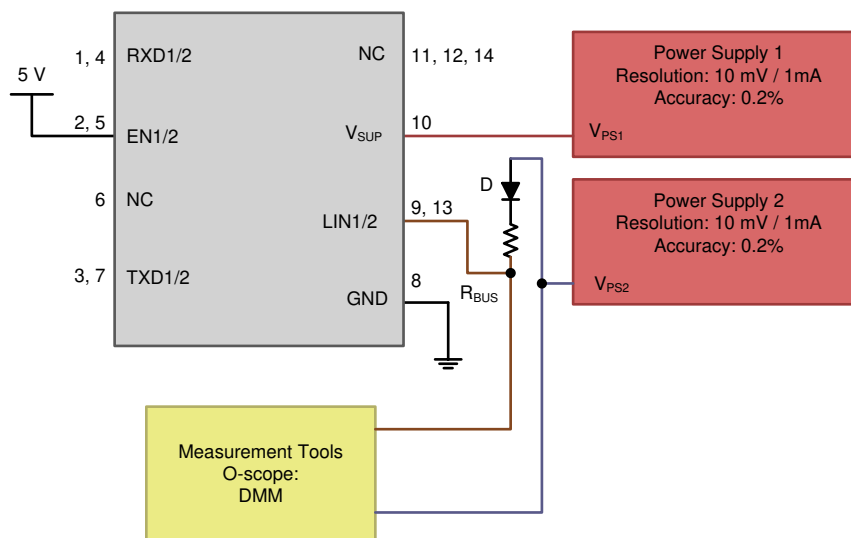


图 10. LIN Bus Input Signal



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图 11. LIN Receiver Test with RX access Parameters 17, 18, 19, 20



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图 12.  $V_{SUP\_NON\_OP}$  Parameters 11

## Parameter Measurement Information (接下页)

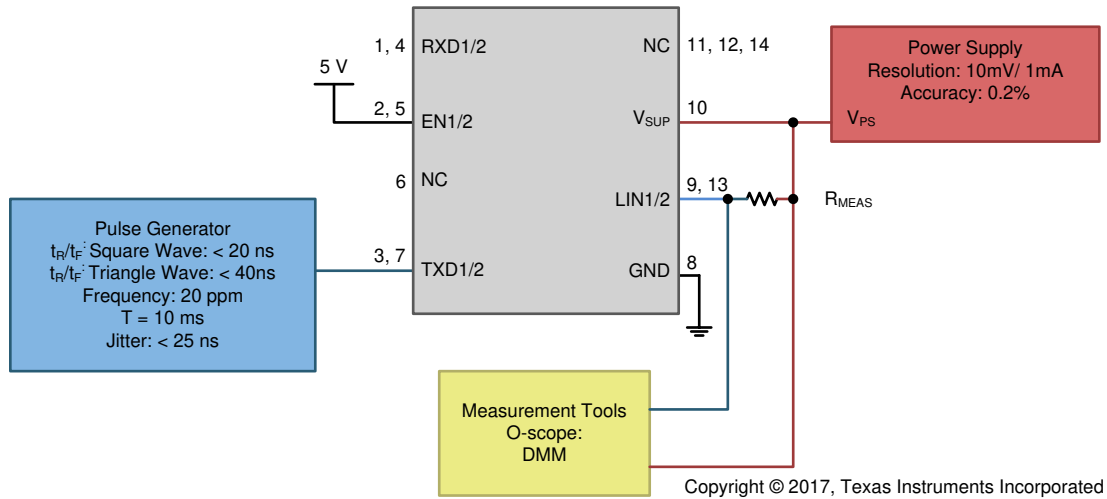


图 13. Test Circuit for  $I_{BUS\_LIM}$  at Dominant State (Driver on) Parameters 12

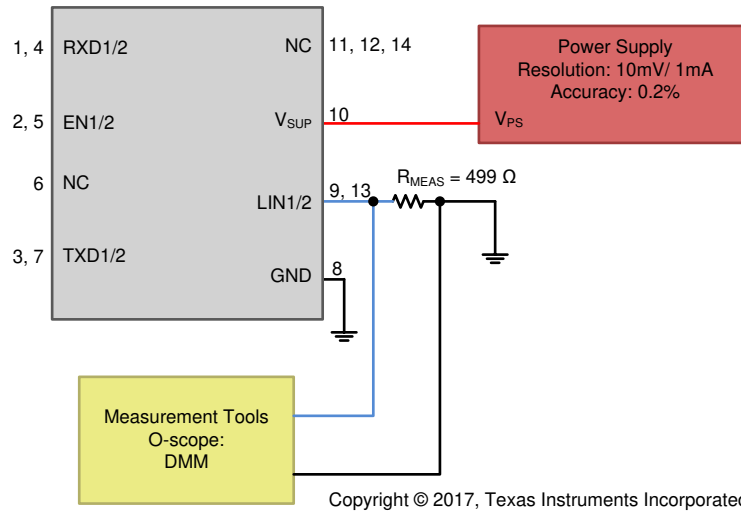


图 14. Test Circuit for  $I_{BUS\_PAS\_dom}$ ; TXD = Recessive State  $V_{BUS} = 0$  V, Parameters 13

## Parameter Measurement Information (接下页)

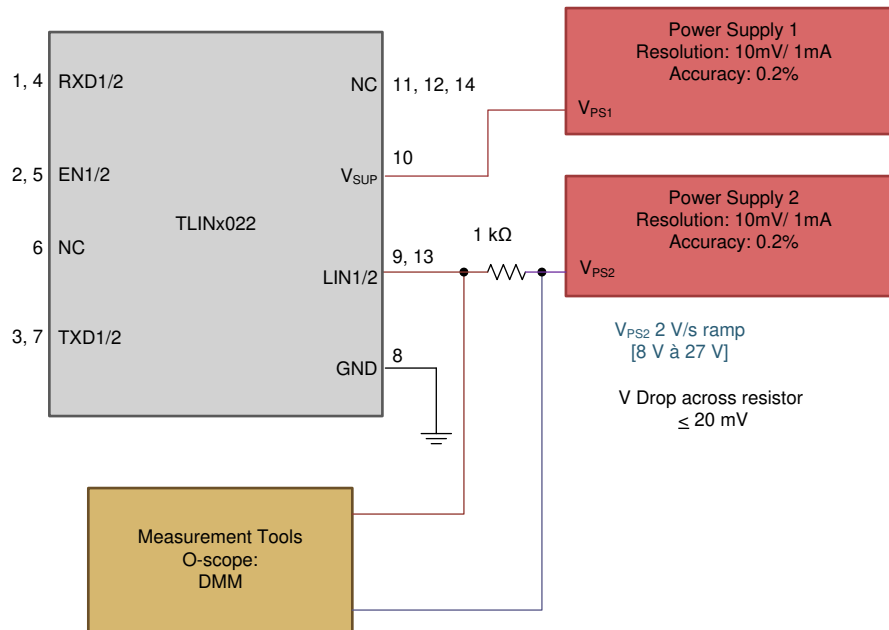
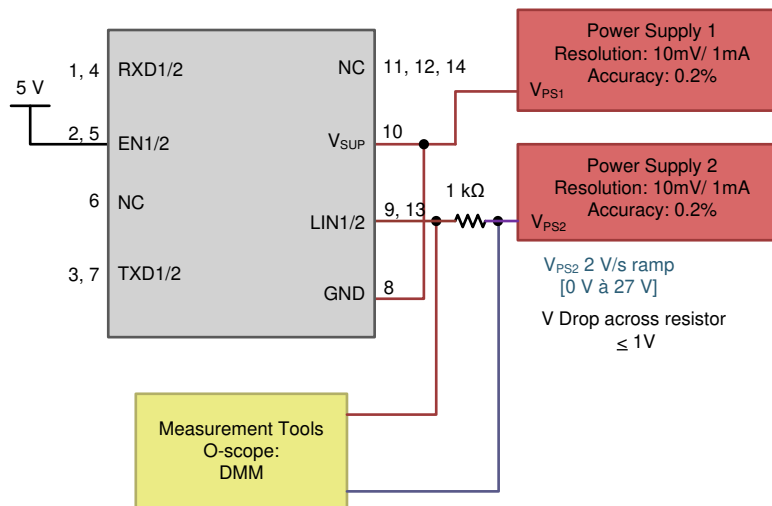


图 15. Test Circuit for  $I_{BUS\_PAS\_rec}$  Param 14



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图 16. Test Circuit for  $I_{BUS\_NO\_GND}$  Loss of GND

## Parameter Measurement Information (接下页)

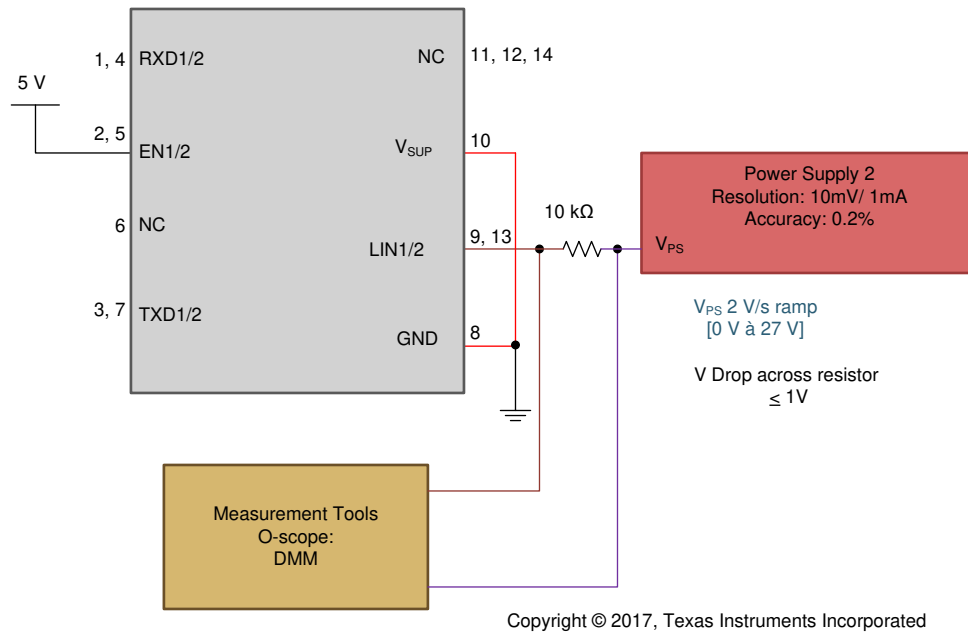


图 17. Test Circuit for  $I_{BUS\_NO\_BAT}$  Loss of Battery

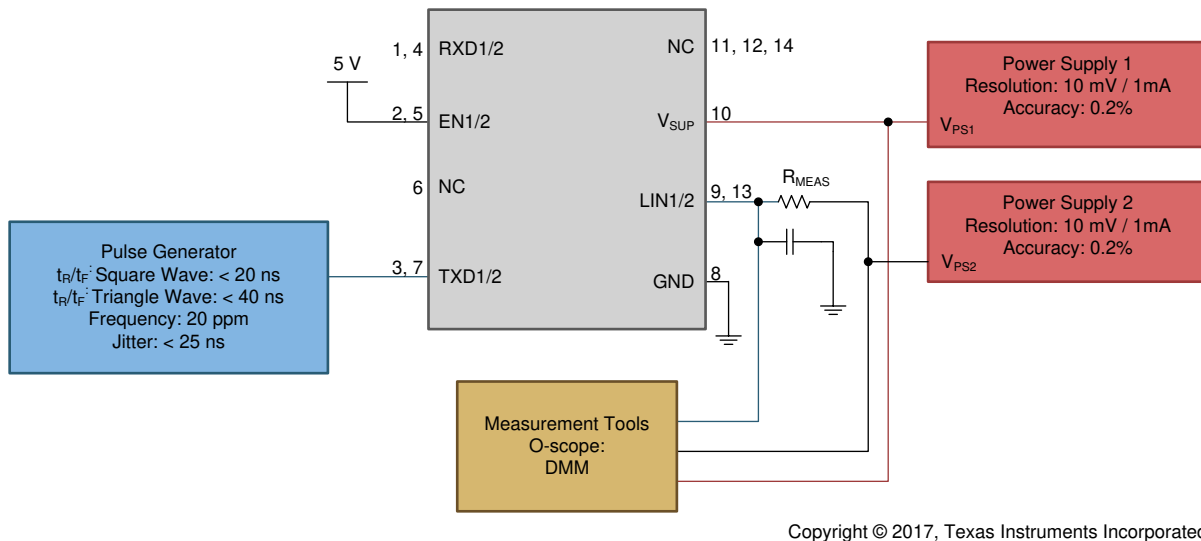


图 18. Test Circuit Slope Control and Duty Cycle Parameters 27, 28, 29, 30

## Parameter Measurement Information (接下页)

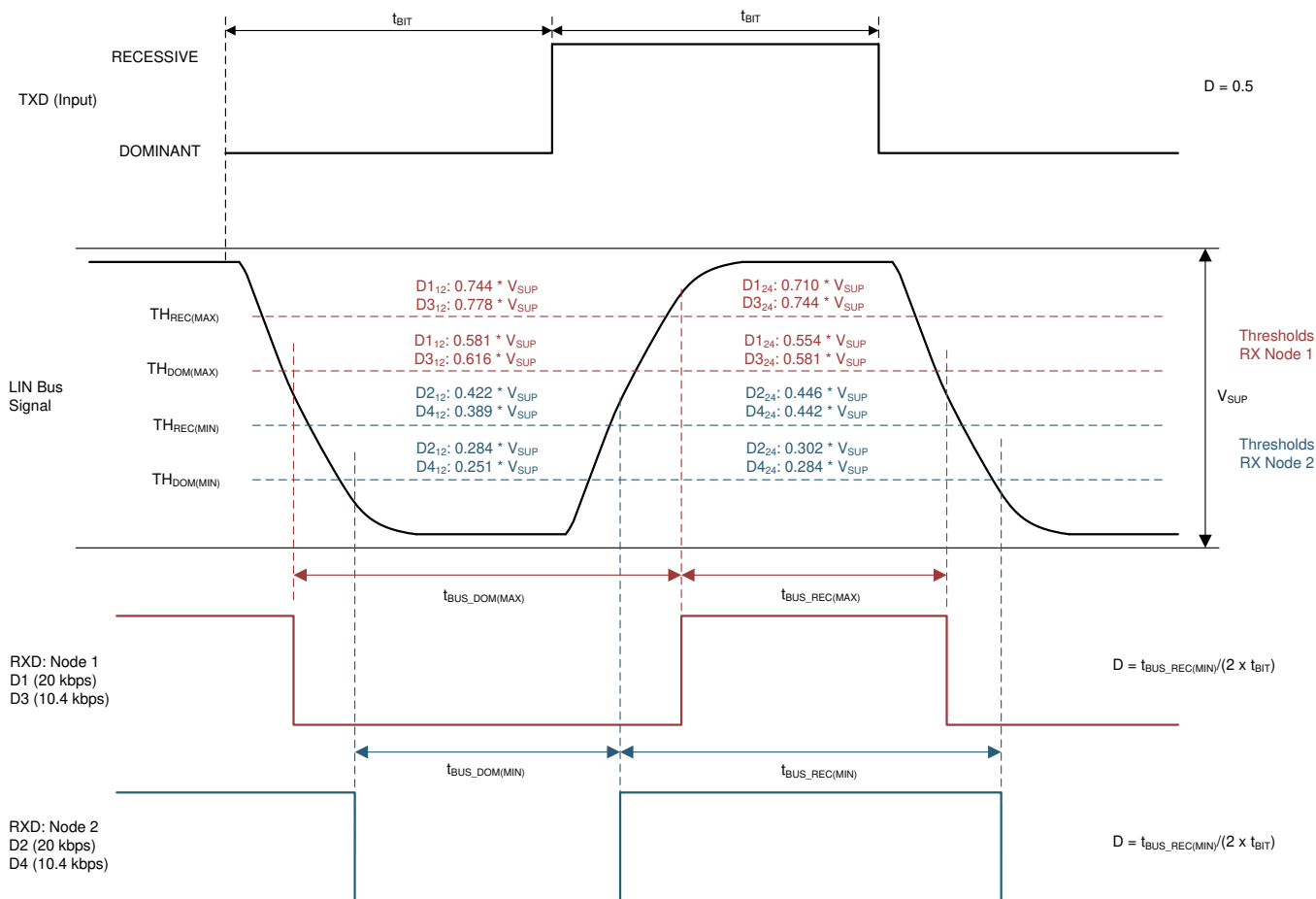
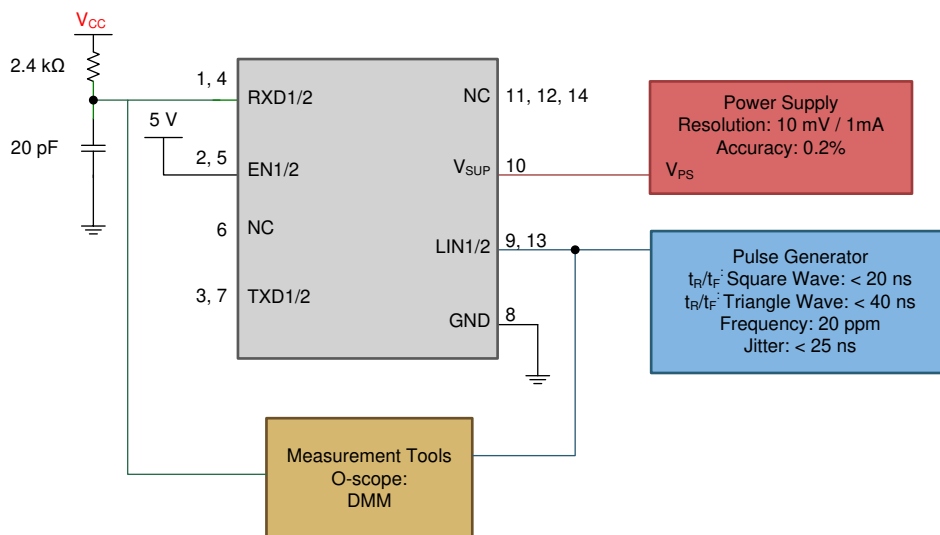


图 19. Definition of Bus Timing Parameters



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图 20. Propagation Delay Test Circuit; Parameters 31, 32

## Parameter Measurement Information (接下页)

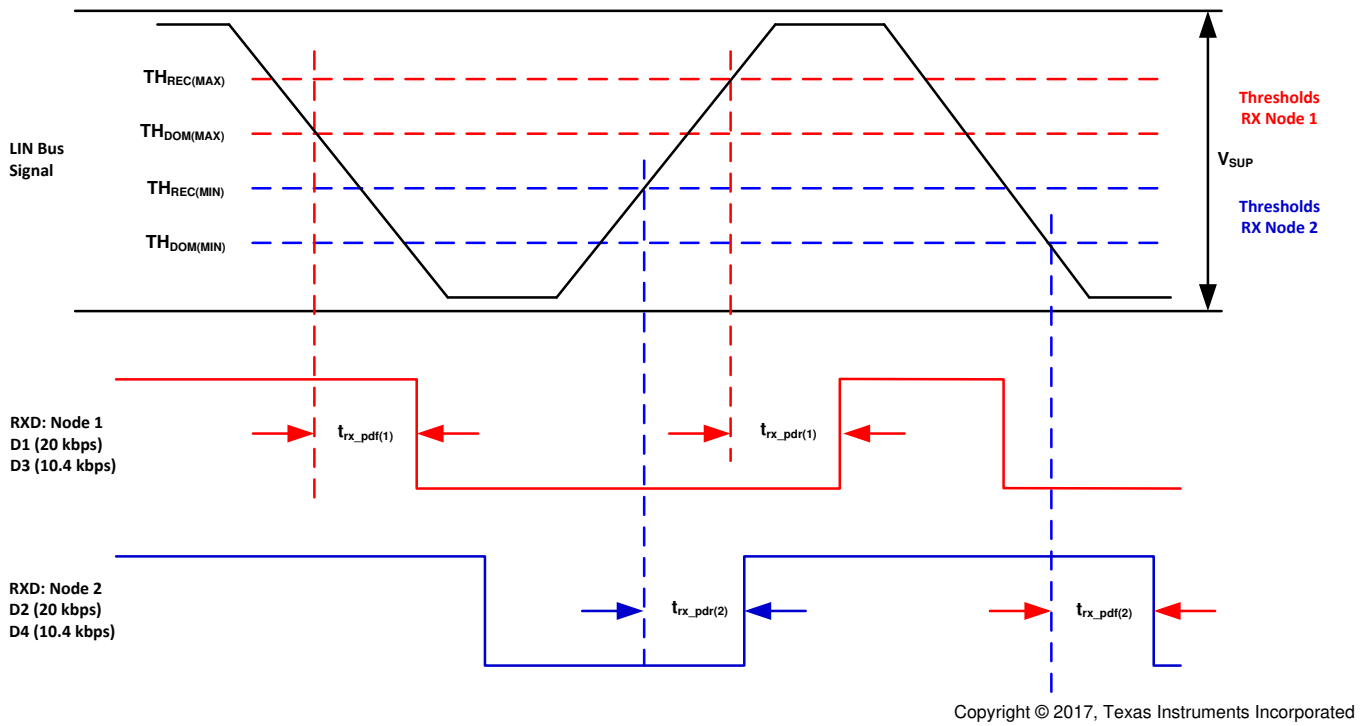
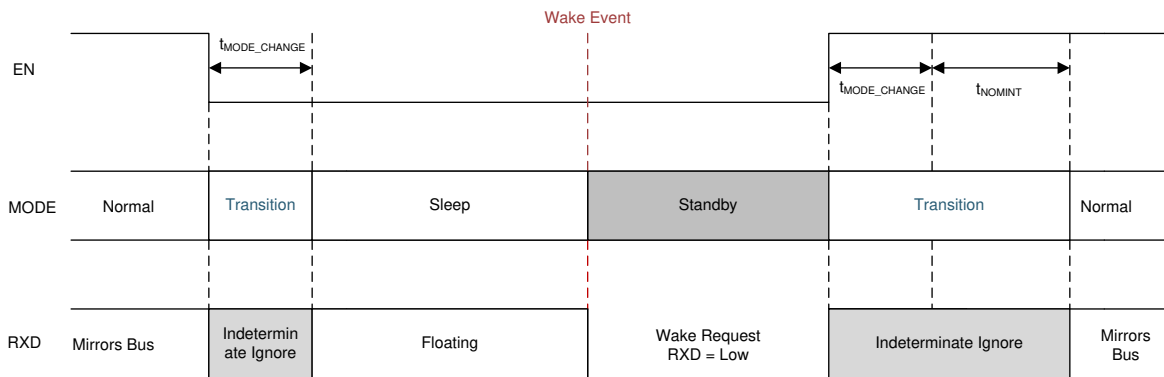


图 21. Propagation Delay



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图 22. Mode Transitions

## Parameter Measurement Information (接下页)

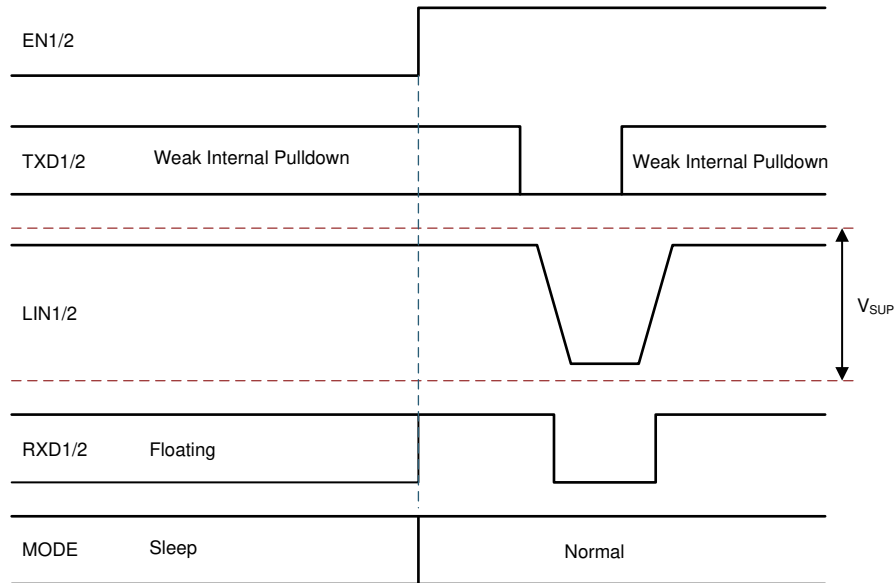


图 23. Wakeup Through EN

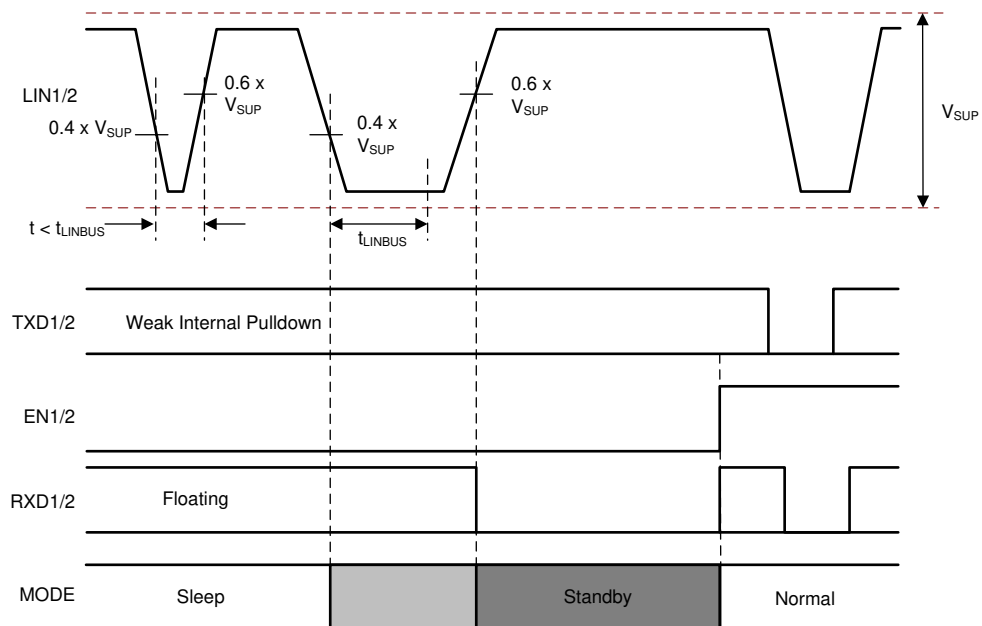


图 24. Wakeup through LIN

## Parameter Measurement Information (接下页)

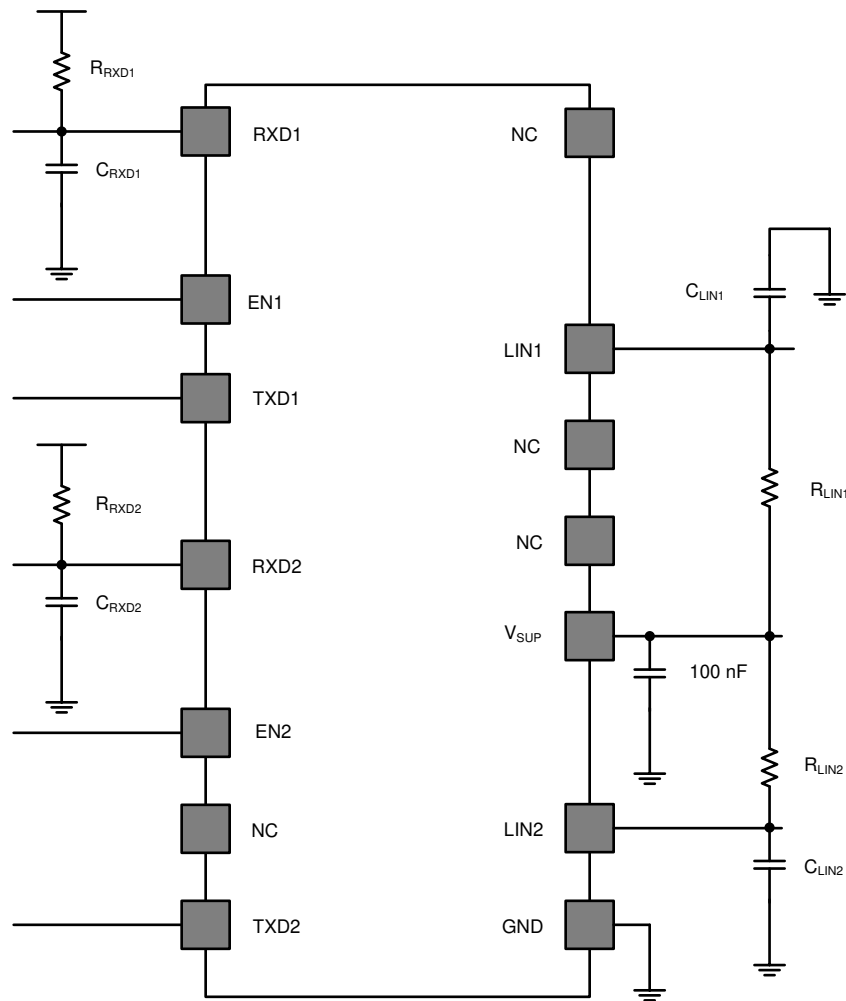


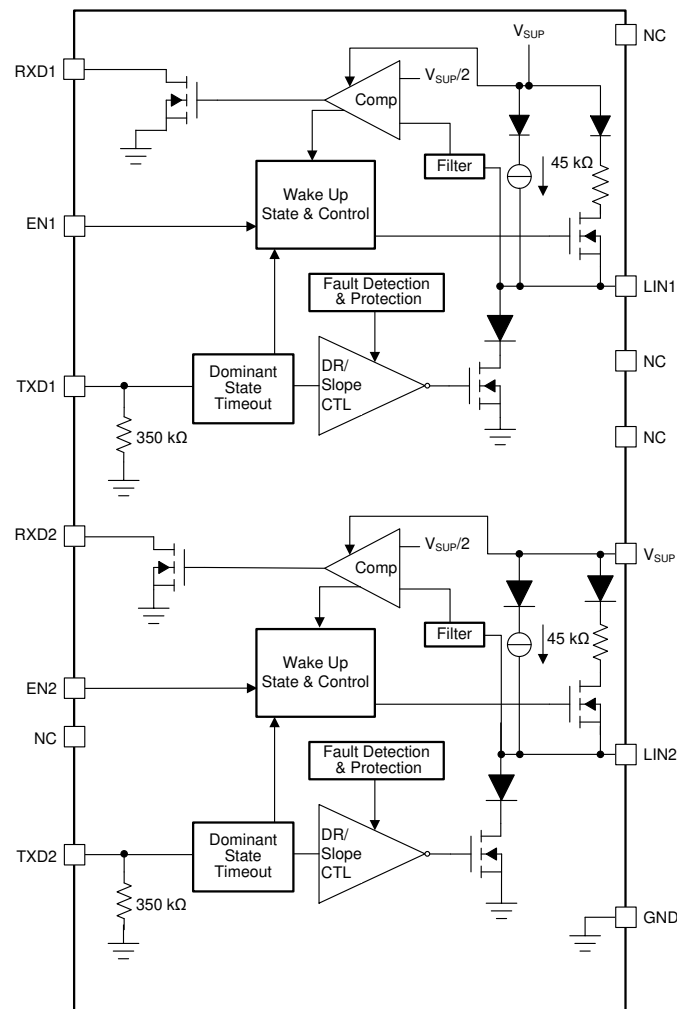
图 25. Test Circuit for AC Characteristics

## 8 Detailed Description

### 8.1 Overview

The TLIN2022-Q1 device is a Dual Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2, with integrated wake-up and protection features. The LIN bus is a single wire bidirectional bus typically used for low speed in-vehicle networks using data rates from 2.4 kbps to 20 kbps. The device TLIN2022-Q1 LIN receiver works up to 100 kbps supporting in-line programming. The LIN protocol data stream on the TXD input is converted by the TLIN2022-Q1 into a LIN bus signal using a current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for slave applications. Master applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification. The TLIN2022-Q1 provides many protection features such as ESD, EMC and high bus standoff voltage. The device also provides three methods to wake up, EN and from the LIN bus.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 LIN (Local Interconnect Network) Bus

This high voltage input/output pin is a single wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 58 V. Reverse currents from the LIN to supply ( $V_{SUP}$ ) are minimized with blocking diodes, even in the event of a ground shift or loss of supply ( $V_{SUP}$ ).

#### 8.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shut-down condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to  $V_{SUP}$ , so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor and series diode to  $V_{SUP}$  must be added when the device is used for a master node application.

#### 8.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are proportional to the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates ( $> 100$  kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN2022-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

##### 8.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to  $V_{SUP}$ , so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor ( $1\text{ k}\Omega$ ) and a series diode to  $V_{SUP}$  must be added when the device is used for master node applications as per the LIN specification.

图 26 shows a Master Node configuration and how the voltage levels are defined

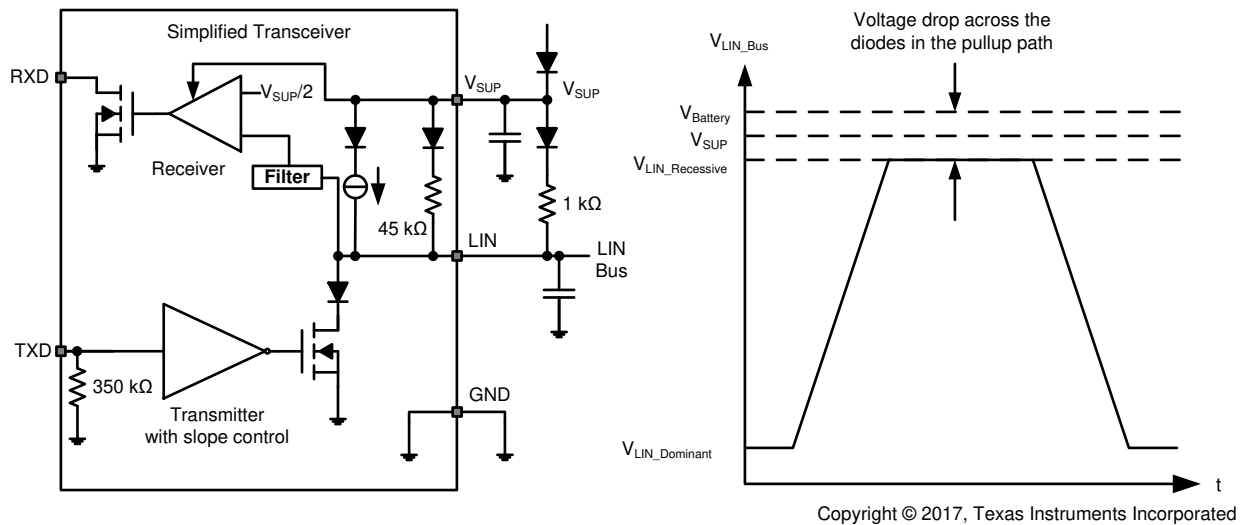


图 26. Master Node Configuration with Voltage Levels

### 8.3.2 TXD (Transmit Input and Output)

TXD is the interface to the processors LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground). When TXD is high the LIN output is recessive (near  $V_{Battery}$ ). See 图 26. The TXD input structure is compatible with processors using 3.3 V and 5 V I/O. TXD has an internal pull-down resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timer-out timer.

## Feature Description (接下页)

### 8.3.3 RXD (Receive Output)

RXD is the interface to the processors LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near  $V_{\text{Battery}}$ ) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 V I/O processors. If the processors RXD pin does not have an integrated pull-up, an external pull-up resistor to the processors I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake up request from the LIN bus.

### 8.3.4 $V_{\text{SUP}}$ (Supply Voltage)

$V_{\text{SUP}}$  is the power supply pin.  $V_{\text{SUP}}$  is connected to the battery through an external reverse battery blocking diode (See [图 26](#)). If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

### 8.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the  $V_{\text{SUP}}$  below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

### 8.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN floats.

### 8.3.7 Protection Features

The TLIN2022-Q1 has several protection features.

### 8.3.8 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than  $t_{\text{DST}}$ , the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the  $t_{\text{DST}}$  timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

### 8.3.9 Bus Stuck Dominant System Fault: False Wake Up Lockout

The TLIN2022-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. [图 27](#) and [图 28](#) show the behavior of this protection.

## Feature Description (接下页)

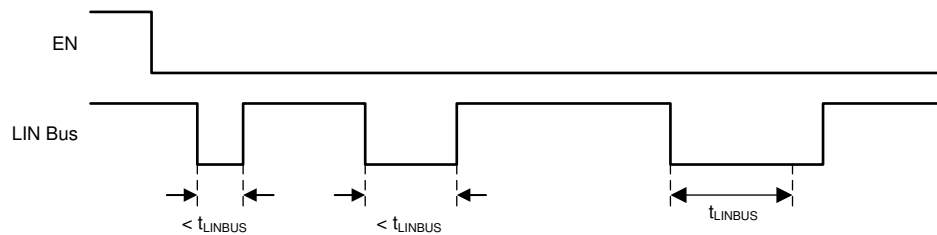


图 27. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

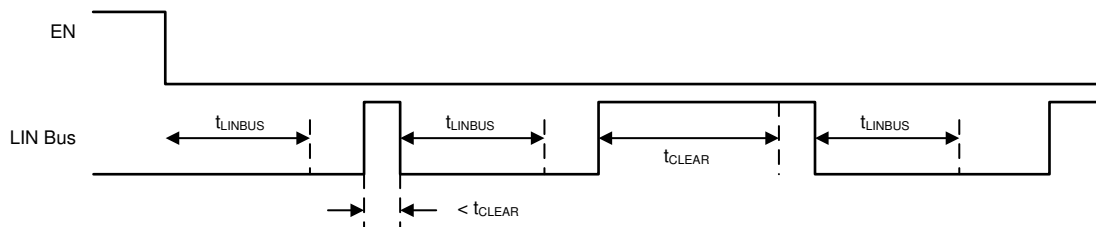


图 28. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

### 8.3.10 Thermal Shutdown

The LIN transmitter is protected by limiting the current; however if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pull-up termination remains on.

### 8.3.11 Under Voltage on $V_{SUP}$

The TLIN2022-Q1 contains a power on reset circuit to avoid false bus messages during under voltage conditions when  $V_{SUP}$  is less than  $UV_{SUP}$ .

### 8.3.12 Unpowered Device and LIN Bus

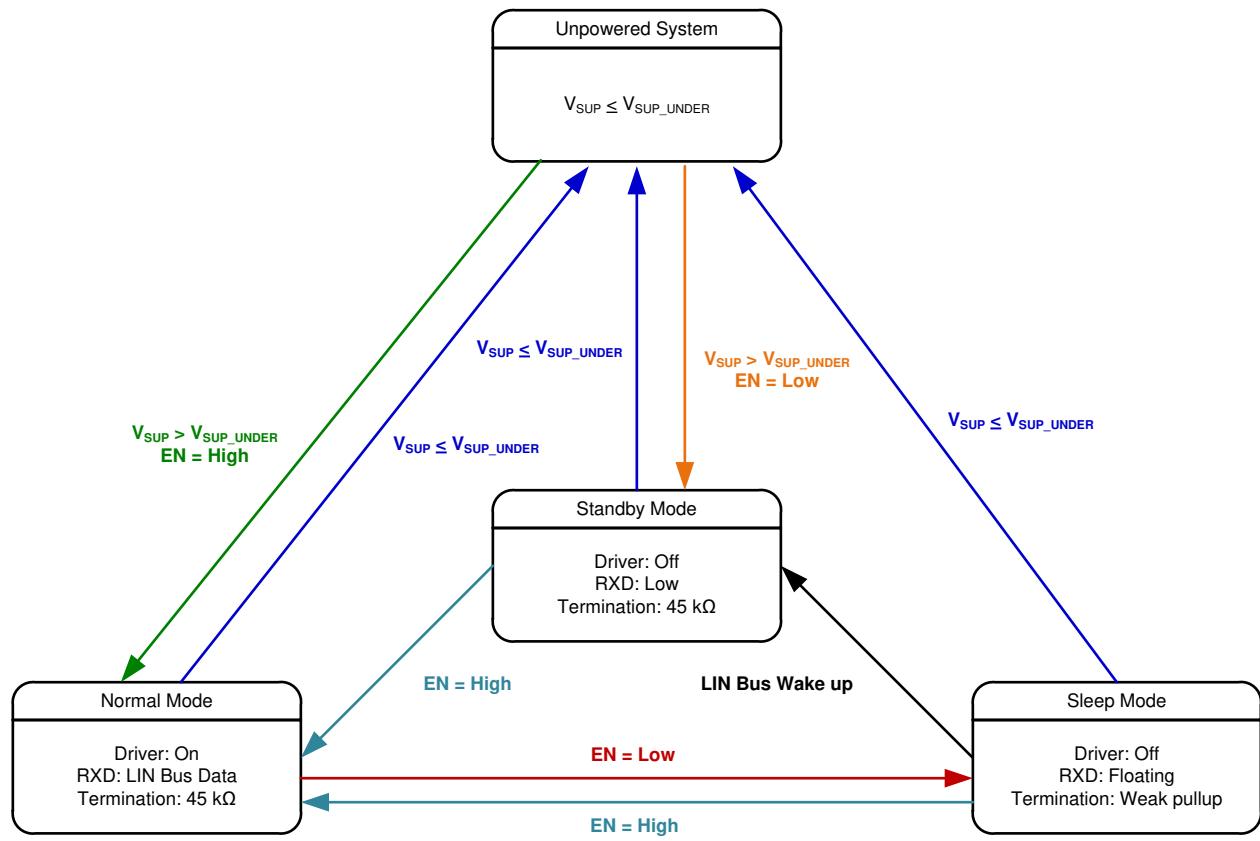
In automotive applications some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remains powered by the battery. The TLIN2022-Q1 has a low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

## 8.4 Device Functional Modes

The TLIN2022-Q1 has three functional modes of operation, normal, sleep, and standby. The next sections describe these modes as well as how the device moves between the different modes. 图 29 graphically shows the relationship while 表 1 shows the state of pins.

表 1. Operating Modes

| MODE    | EN   | RXD          | LIN BUS TERMINATION | TRANSMITTER | COMMENT                                          |
|---------|------|--------------|---------------------|-------------|--------------------------------------------------|
| Sleep   | Low  | Floating     | Weak Current Pullup | Off         |                                                  |
| Standby | Low  | Low          | 45 kΩ (typical)     | Off         | Wake up event detected, waiting on MCU to set EN |
| Normal  | High | LIN Bus Data | 45 kΩ (typical)     | Off         | LIN transmission up to 20 kbps                   |



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图 29. Operating State Diagram

#### 8.4.1 Normal Mode

If the EN pin is high at power up, the device powers up in normal mode, and if in low, it powers up in standby mode. The EN pin controls the mode of the device. In normal operational mode, the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a logic high and a dominate signal on the LIN bus is a logic low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the TLIN2022-Q1 is in sleep or standby mode for  $> t_{MODE\_CHANGE}$ .

#### 8.4.2 Sleep Mode

Sleep Mode is the power saving mode for the TLIN2022-Q1. Even with extremely low current consumption in this mode, the TLIN2022-Q1 can still wake up from LIN bus through a wake up signal or if EN is set high for  $> t_{MODE\_CHANGE}$ . The Lin bus is filtered to prevent false wake up events. The wake up events must be active for the respective time periods ( $t_{LINBUS}$ ).

Sleep mode is entered by setting EN low for longer than  $t_{MODE\_CHANGE}$ .

While the device is in sleep mode, the following conditions exist.

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake up receiver are active.

### 8.4.3 Standby Mode

This mode is entered whenever a wake up event occurs through LIN bus while the device is in sleep mode. The LIN bus slave termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See [Standby Mode Application Note](#) for more application information.

When EN is set high for longer than  $t_{\text{MODE\_CHANGE}}$  while the device is in standby mode, the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

### 8.4.4 Wake Up Events

There are two ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is held for  $t_{\text{LINBUS}}$  filter time. After this  $t_{\text{LINBUS}}$  filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event, eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake up through EN being set high for longer than  $t_{\text{MODE\_CHANGE}}$ .

#### 8.4.4.1 Wake Up Request (RXD)

When the TLIN2022-Q1 encounters a wake up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin is releasing the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

#### 8.4.4.2 Mode Transitions

When the TLIN2022-Q1 is transitioning between modes, the device needs the time,  $t_{\text{MODE\_CHANGE}}$ , to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby mode to normal mode, the transition time is the sum of  $t_{\text{MODE\_CHANGE}}$  and  $t_{\text{NOMINT}}$ .

## 9 Application and Implementation

### 注

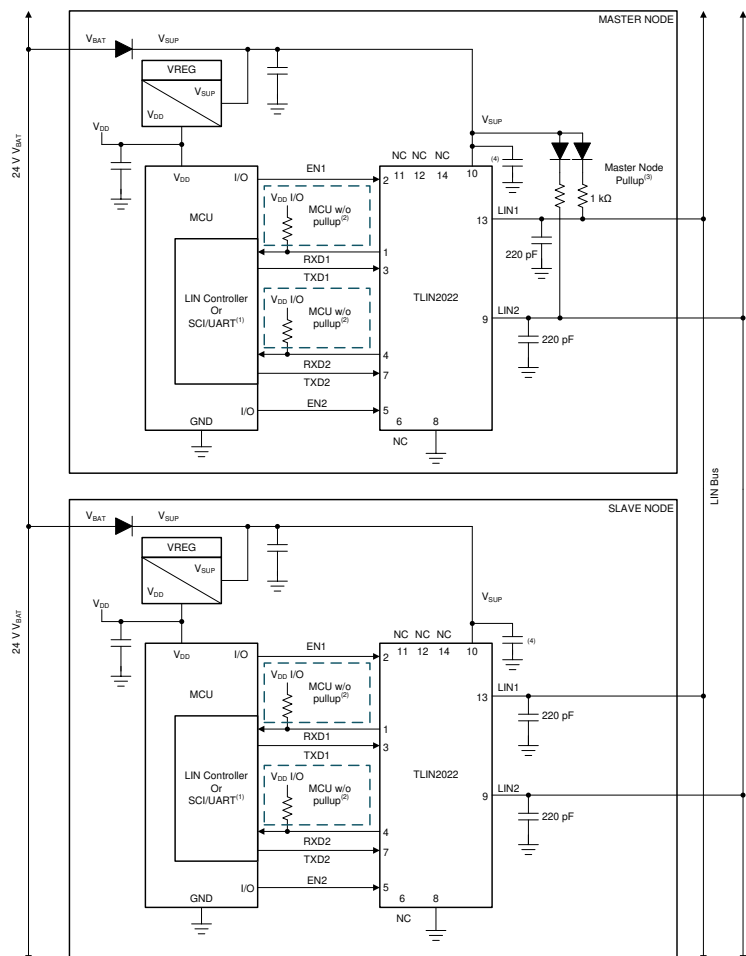
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TLIN2022-Q1 can be used as both a slave device and a master device in a LIN network. The device comes with the ability to support both remote wake up request and local wake up request.

### 9.2 Typical Application

The device comes with an integrated 45 kΩ pull-up resistor and series diode for slave applications. For master applications, an external 1 kΩ pull-up resistor with series blocking diode can be used. shows the device being used in both master and slave applications.



- (1) If RXD on MCU or LIN slave has internal pullup; no external pullup resistor is needed.
- (2) If RXD on MCU or LIN slave does not have an internal pullup requires external pullup resistor
- (3) Master node applications require an external 1 kΩ pullup resistor and serial diode.
- (4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 μF and ≥10 μF

图 30. Typical LIN Bus

## Typical Application (接下页)

### 9.2.1 Design Requirements

The RXD output structure is an open-drain output stage. This allows the TLIN2022-Q1 to be used with 3.3-V and 5-V I/O processor. If the RXD pin of the processor does not have an integrated pull-up, an external pull-up resistor to the processor I/O supply voltage is required. The select external pull-up resistor value should be between 1 kΩ to 10 kΩ. The  $V_{SUP}$  pin of the device should be decoupled with a 100 nF capacitor as close to the supply pin of the device as possible. The system should include 1 μF and ≥ 10 μF decoupling capacitors on  $V_{SUP}$  as per each application requirements.

### 9.2.2 Detailed Design Procedures

#### 9.2.2.1 Normal Mode Application Note

When using the TLIN2022-Q1 in systems which are monitoring the RXD pin for a wake up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake up request until  $t$  when going from normal to sleep mode or  $t_{MODE\_CHANGE}$  plus  $t_{NOMINT}$  when going from sleep or standby to normal mode. This is shown in 图 22

#### 9.2.2.2 Standby Mode Application Note

If the TLIN2022-Q1 detects an under voltage on  $V_{SUP}$  the RXD pin transitions low, and signals to the software that the TLIN2022-Q1 is in standby mode and should be returned to sleep mode for the lowest power state.

#### 9.2.2.3 TXD Dominant State Timeout Application Note

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for master and slave applications thus there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

### 9.2.3 Application Curves

图 31 and 图 32 show the propagation delay from the TXD pin to the LIN pin for both dominant to recessive and recessive to dominant stated under lightly loaded conditions.

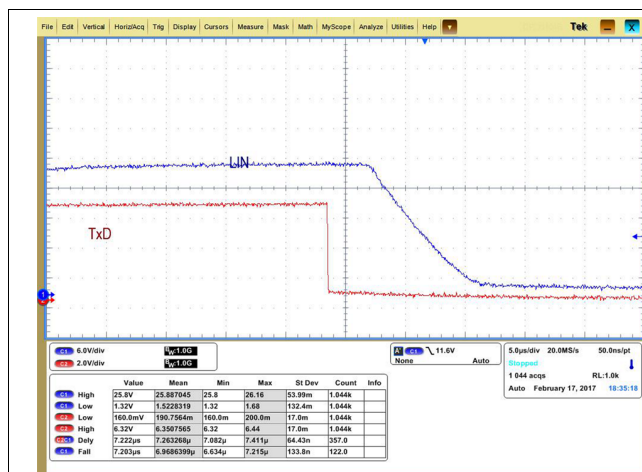


图 31. Dominant to Recessive Propagation

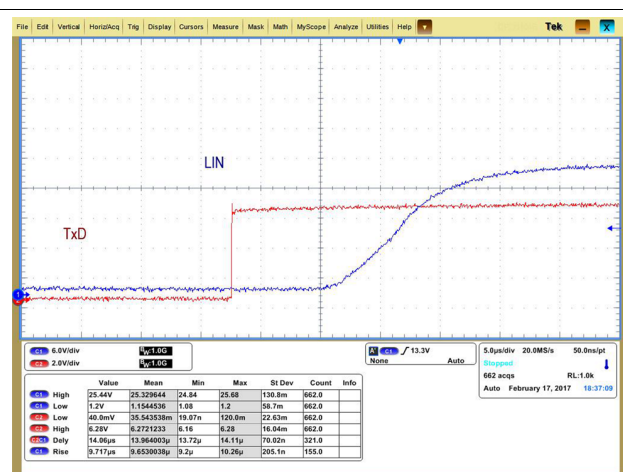


图 32. Recessive to Dominant Propagation

## 10 Power Supply Recommendations

The TLIN2022-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 4 V to 45 V. A 100 nF decoupling capacitor should be placed as close to the  $V_{SUP}$  pin of the device as possible.

## 11 Layout

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

### 11.1 Layout Guidelines

- **Pin 1, 4 (RXD1/2):** The pin is an open drain outputs and require an external pull-up resistor in the range of 1 k $\Omega$  and 10 k $\Omega$  to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pin 2, 5 (EN1/2):** EN is an input pin that is used to place the device in a low power sleep mode. If this feature is not used, the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor, values between 1 k $\Omega$  and 10 k $\Omega$ . Additionally, a series resistor may be placed on the pinto limit current on the digital lines in the event of an over voltage fault.
- **Pin 6 (NC):** Not Connected.
- **Pin 3, 7 (TXD1/2):** The TXD pins are the transmitter input signals to the device from the processor. A series resistor can be placed to limit the input current to the device in the case of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 8 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 9, 13 (LIN1/2):** This pin connects to the LIN bus. For slave applications, a 220 pF capacitor to ground is implemented. For maser applications and additional series resistor, a blocking diode should be placed between the LIN pin and the V<sub>SUP</sub> pin. See [图 30](#).
- **Pin 10 (V<sub>SUP</sub>):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 11, 12 and 14 (NC):** Not Connected.

---

#### 注

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

---

## 11.2 Layout Example

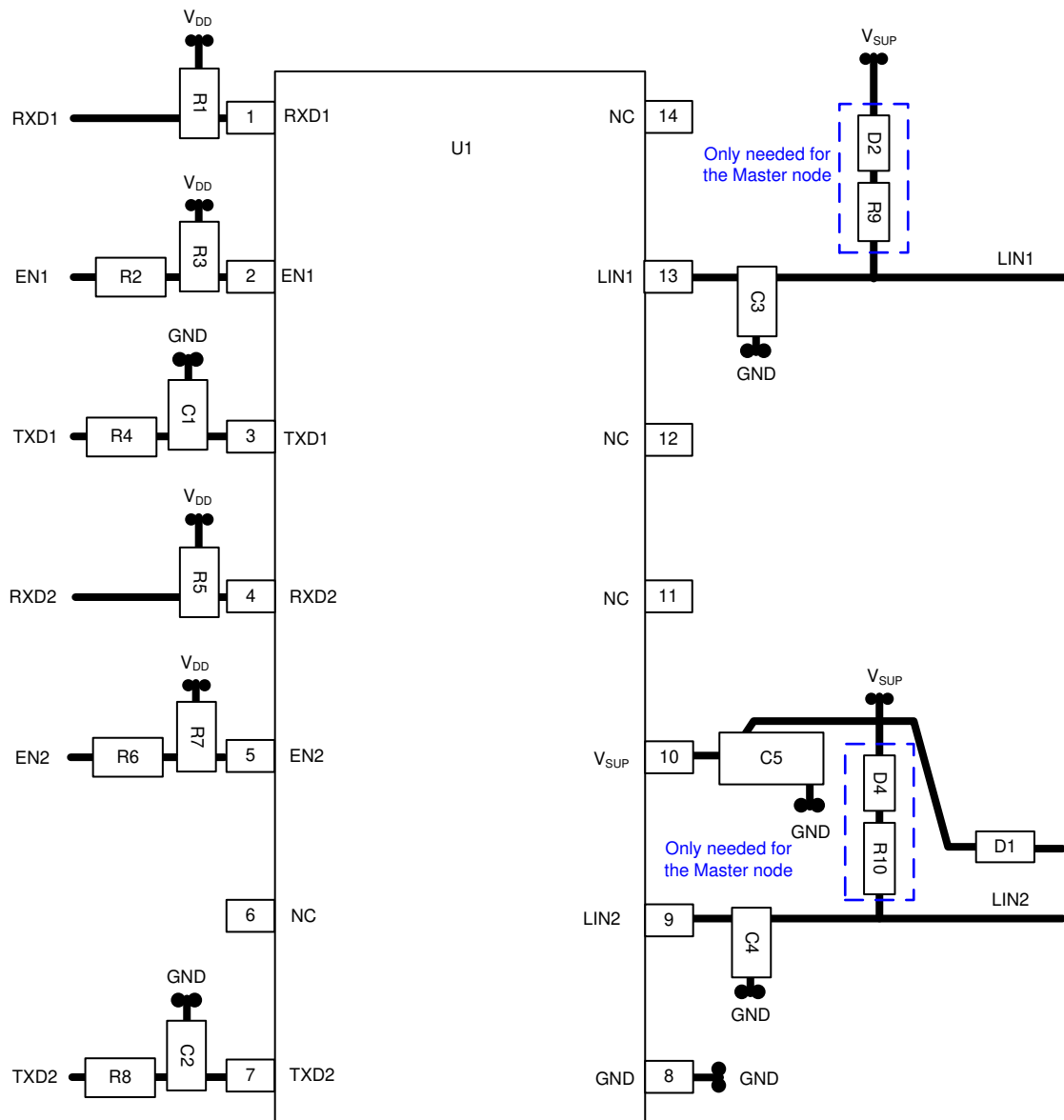


图 33. Layout Example

## 12 器件和文档支持

该器件将遵循以下 LIN 标准。本系统规格中涵盖了所有核心必要内容；但是，应为这些标准提供参考，并指出和探讨所有不符之处。本文档应提供所有基本必要内容。

### 12.1 文档支持

#### 12.1.1 相关文档

请参阅如下相关文档：

LIN 标准：

- ISO/DIS 17987-1.2: 道路车辆 - 局域互连网络 (LIN) - 第 1 部分：一般信息和用例定义
- ISO/DIS 17987-4.2: 道路车辆 - 局域互连网络 (LIN) - 第 4 部分：电气物理层规格 (EPL) 12V/24V
- SAEJ2602-1: 车用 LIN 网络 应用
- LIN2.0、LIN2.1、LIN2.2 和 LIN2.2A 规格

EMC 要求：

- SAEJ2962-2: TBD
- ISO 10605: 道路车辆 - 静电放电所产生电气干扰的测试方法
- ISO 11452-4:2011: 道路车辆 - 窄带辐射电磁能量的电子干扰组件试验方法 - 第 4 部分：线束激励方法
- ISO 7637-1:2015: 道路车辆 - 传导和耦合造成的电干扰 - 第 1 部分：定义和一般描述
- ISO 7637-3: 道路车辆 - 由传导和耦合引起的电干扰 - 第 3 部分：通过电容耦合和电感耦合经由非电源线线路的瞬间电传输
- IEC 62132-4:2006: 集成电路 - 150kHz - 1GHz 电磁抗扰度的测量 - 第 4 部分：直接射频功率注入法
- IEC 61000-4-2
- IEC 61967-4
- CISPR25

符合性测试要求：

- ISO/DIS 17987-7.2: 道路车辆 - 局域互连网络 (LIN) - 第 7 部分：电气物理层 (EPL) 符合性测试规格
- SAEJ2602-2: 车辆应用的 LIN 网络 符合性测试

### 12.2 接收文档更新通知

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### 12.3 支持资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## **13 机械、封装和可订购信息**

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航栏。

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## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLIN2022DMTRQ1   | ACTIVE        | VSON         | DMT                | 14   | 3000           | RoHS & Green    | Call TI                              | Level-2-260C-1 YEAR  | -40 to 125   | TL022                   | <a href="#">Samples</a> |
| TLIN2022DMTTQ1   | ACTIVE        | VSON         | DMT                | 14   | 250            | RoHS & Green    | Call TI                              | Level-2-260C-1 YEAR  | -40 to 125   | TL022                   | <a href="#">Samples</a> |
| TLIN2022DRQ1     | ACTIVE        | SOIC         | D                  | 14   | 2500           | RoHS & Green    | NIPDAUAG                             | Level-1-260C-UNLIM   | -40 to 125   | TL022                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## PACKAGE OPTION ADDENDUM

10-Dec-2020

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLIN2022DMTRQ1 | VSON         | DMT             | 14   | 3000 | 330.0              | 12.4               | 3.2     | 4.7     | 1.15    | 8.0     | 12.0   | Q1            |
| TLIN2022DMTTQ1 | VSON         | DMT             | 14   | 250  | 180.0              | 12.4               | 3.2     | 4.7     | 1.15    | 8.0     | 12.0   | Q1            |
| TLIN2022DRQ1   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.5     | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLIN2022DMTRQ1 | VSON         | DMT             | 14   | 3000 | 367.0       | 367.0      | 38.0        |
| TLIN2022DMTTQ1 | VSON         | DMT             | 14   | 250  | 213.0       | 191.0      | 35.0        |
| TLIN2022DRQ1   | SOIC         | D               | 14   | 2500 | 366.0       | 364.0      | 50.0        |

## GENERIC PACKAGE VIEW

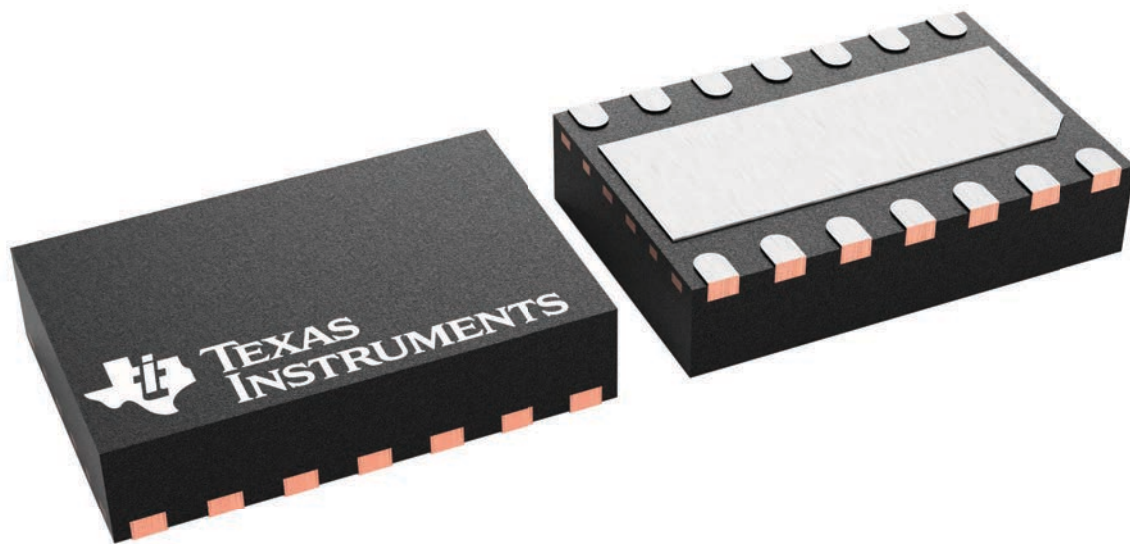
**DMT 14**

**VSON - 0.9 mm max height**

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



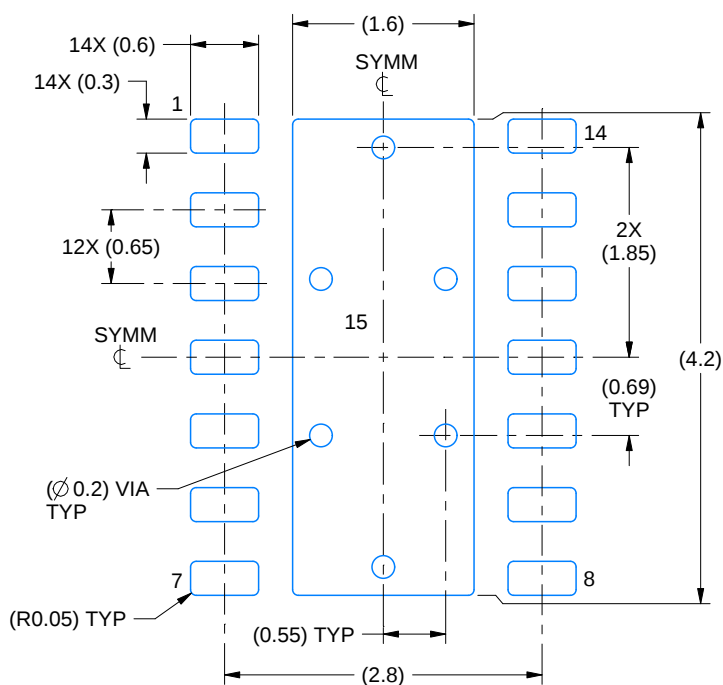
4225088/A



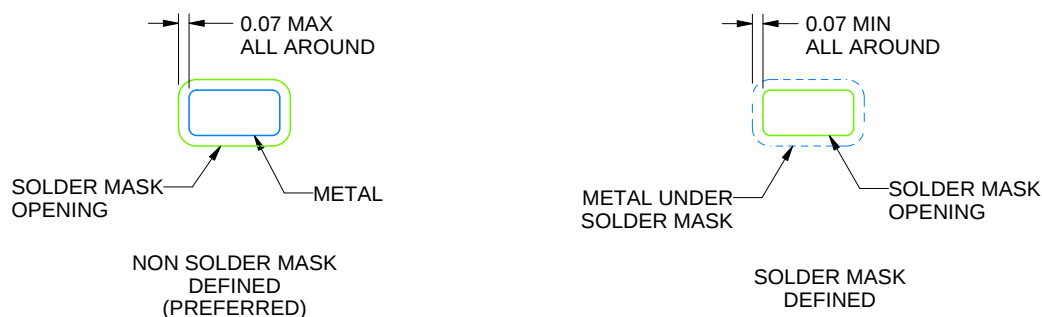
**DMT0014A**

**VSON - 0.9 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:15X



## SOLDER MASK DETAILS

4223033/B 10/2016

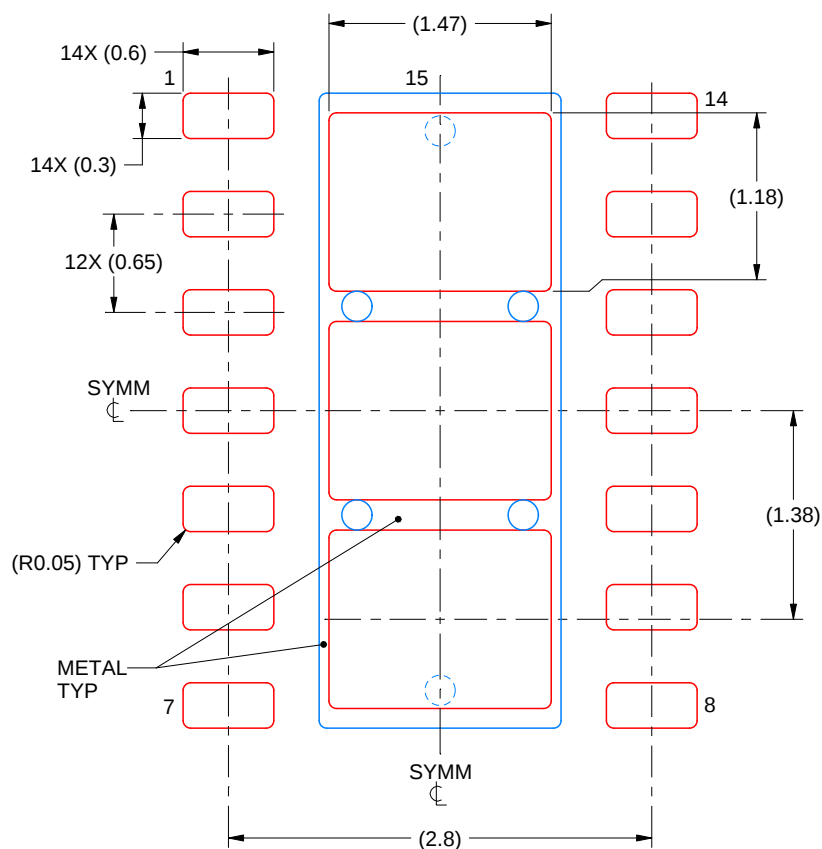
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DMT0014A**

**VSON - 0.9 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15  
77.4% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

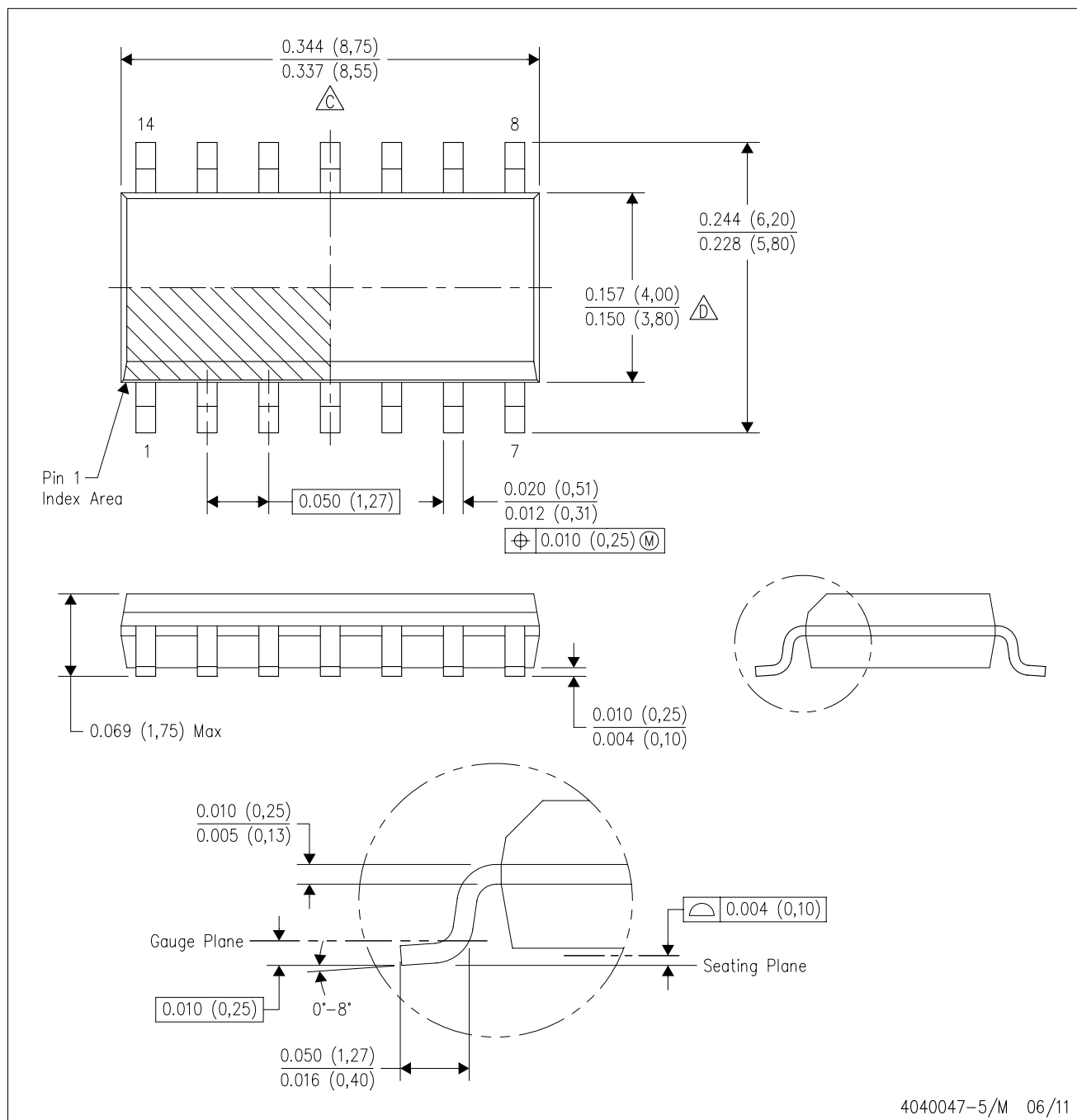
4223033/B 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

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