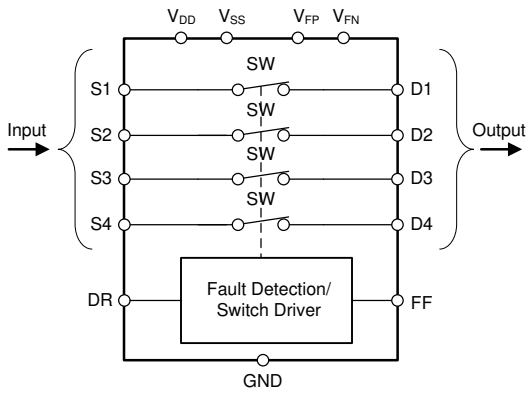
# TMUX7462F ±60 V Fault-Protected, Latch-Up Immune, Quad Channel Protector with Adjustable Fault Threshold and 1.8-V Logic

## 1 Features

- Wide Supply Range: ±5 V to ±22 V (Dual), 8 V to 44 V (Single)
- Channel Protector Without Need for Dedicated Select Pin Per Channel
  - Reduces Number of Control Logic Signals to Route Across PCB
- Integrated Fault Protection:
  - Overvoltage Protection, Source to Supplies or to Drain: ±85 V
  - Overvoltage Protection: ±60 V
  - Powered-Off Protection: ±60 V
  - Interrupt Flags to Indicate Fault Status
  - Adjustable Overvoltage Triggering Threshold from 3 V to Supplies
  - Adjustable Output Behavior (Clamped or Open) During Fault
- Latch-Up Immunity by Device Construction
- Low and Flat On-Resistance (8 Ω Typical)
- Industry-Standard TSSOP and Smaller WQFN Package

## 2 Applications

- Factory Automation and Control
- Programmable Logic Controllers (PLC)
- Analog Input Modules
- Semiconductor Test Equipment
- Battery Test Equipment
- Servo Drive Control Module
- Data Acquisition Systems (DAQ)




**Simplified Schematic**

## 3 Description

The TMUX7462F is a four-channel protector that can be placed on the front end of a signal path to protect sensitive components downstream from damages caused by overvoltage faults. Each of the 4 channels has an internal switch that is turned-off autonomously upon occurrence of an overvoltage fault without the need of external controls. This simplifies robust system level protection designs by removing the need for control signals for each channel of the device. The overvoltage protection is available in powered and powered-off conditions, making the TMUX7462F suitable for applications where power supply sequencing cannot be precisely controlled.

The switch channels remain in the high impedance state (regardless of switch input conditions) when the devices power supplies are floating, grounded, or at a level that is below the undervoltage (UV) threshold. If the signal level on any Sx pin exceeds the fault supply ($V_{FP}$ or $V_{FN}$) by a threshold voltage ($V_T$), then the Sx pin becomes high impedance and an output fault flag is asserted low to indicate a fault condition under normal operation. The drain pin (Dx) is either pulled to the fault supply voltage that was exceeded or left floating depending on the DR control logic.

The device works well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies. The low and flat on-resistance of the device makes the TMUX7462F an ideal solution for data acquisition applications where excellent linearity and low distortion is critical.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TMUX7462F | TSSOP (16) | 5.00 mm × 4.40 mm |
| | WQFN (16) | 4.00 mm × 4.00 mm |

(1) See the orderable addendum at the end of the data sheet for all available packages.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| March 2021 | * | Initial Release |

# 5 Pin Configuration and Functions

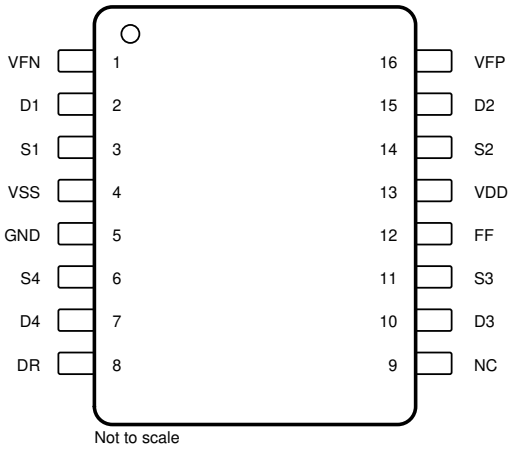


**Figure 5-1. PW Package 16-Pin TSSOP Top View**

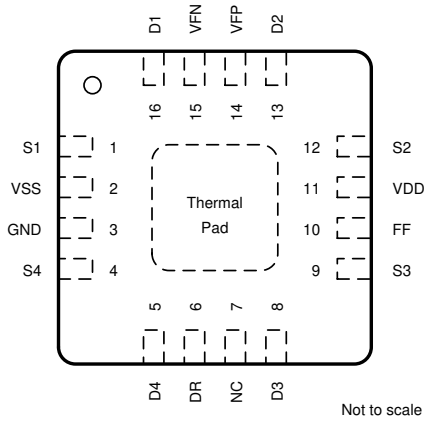


**Figure 5-2. RRP Package 16-Pin WQFN Top View**

**Table 5-1. Pin Functions**

| PIN | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | TSSOP | WQFN | | |
| D1 | 2 | 16 | I/O | Drain pin 1 can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range. |
| D2 | 15 | 13 | I/O | Drain pin 2 can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range. |
| D3 | 10 | 8 | I/O | Drain pin 3 can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range. |
| D4 | 7 | 5 | I/O | Drain pin 4 can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range. |
| DR | 8 | 6 | I | Drain Response (DR) input. Tying the DR pin to GND enables the drain to be pulled to $V_{FP}$ or $V_{FN}$ through a 40 kΩ resistor during an overvoltage fault event. |
| FF | 12 | 10 | O | General fault flag. This pin is an open drain output and is asserted low when overvoltage condition is detected on any of the source (Sx) pins. Connect this pin to an external supply (1.8 V to 5.5 V) through a 1 kΩ pull-up resistor. |
| GND | 5 | 3 | P | Ground (0 V) reference. |
| N.C. | 9 | 7 | — | No internal connection |
| S1 | 3 | 1 | I/O | Overvoltage protected source pin 1 can be an input or output. |
| S2 | 14 | 12 | I/O | Overvoltage protected source pin 2 can be an input or output. |
| S3 | 11 | 9 | I/O | Overvoltage protected source pin 3 can be an input or output. |
| S4 | 6 | 4 | I/O | Overvoltage protected source pin 4 can be an input or output. |
| $V_{DD}$ | 13 | 11 | P | Positive power supply. This pin is the most positive power-supply potential. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{DD}$ and GND for reliable operation. |
| $V_{FP}$ | 16 | 14 | P | Positive fault voltage supply that determines the overvoltage protection triggering threshold on the positive side. Connect to $V_{DD}$ if the triggering threshold is the same as the device's positive supply. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{FP}$ and GND for reliable operation. |
| $V_{FN}$ | 1 | 15 | P | Negative fault voltage supply that determines the overvoltage protection triggering threshold on the negative side. Connect to $V_{SS}$ if the triggering threshold is the same as the device's negative supply. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{FN}$ and GND for reliable operation. |
| $V_{SS}$ | 4 | 2 | P | Negative power supply. This pin is the most negative power-supply potential. This pin can be connected to ground in single-supply applications. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{SS}$ and GND for reliable operation. |
| Thermal Pad | | | — | The thermal pad is not connected internally. No requirement to solder this pad. For best performance it is recommended that the pad be tied to GND or VSS. |

(1) I = input, O = output, I/O = input and output, P = power.

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## 6 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ to $V_{SS}$ | Supply voltage | | 48 | V |
| $V_{DD}$ to GND | | –0.3 | 48 | V |
| $V_{SS}$ to GND | | –48 | 0.3 | V |
| $V_{FP}$ to GND | Fault clamping voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $V_{FN}$ to GND | | VSS – 0.3 | 0.3 | V |
| $V_S$ to GND | Source input pin (Sx) voltage to GND | –65 | 65 | V |
| $V_S$ to $V_{DD}$ | Source input pin (Sx) voltage to $V_{DD}$ | –90 | | V |
| $V_S$ to $V_{SS}$ | Source input pin (Sx) voltage to $V_{SS}$ | | 90 | V |
| $V_D$ | Drain pin (Dx) voltage | $V_{FN}$–0.7 | $V_{FP}$+0.7 | V |
| $V_{DIG\_IN}$ | Digital input pin (DR) voltage(2) | GND –0.7 | 48 | V |
| $V_{DIG\_OUT}$ | Digital output pin (FF) voltage(2) | GND –0.7 | 6 | V |
| $I_{DIG\_IN}$ | Digital input pin (DR) current(2) | –30 | 30 | mA |
| $I_{DIG\_OUT}$ | Digital output pin (FF) current(2) | –10 | 10 | mA |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx or Dx) | $I_{DC}$ ± 10 %(3) | $I_{DC}$ ± 10 %(3) | mA |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |
| $T_A$ | Ambient temperature | –55 | 150 | °C |
| $T_J$ | Junction temperature | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Stresses have to be kept at or below both voltage and current ratings at all time.

(3) Refer to Recommended Operating Conditions for $I_{DC}$ ratings.

## 7 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | | ±2000 | V |
| $V_{(ESD)}$ | Electrostatic discharge | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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## 8 Thermal Information

| THERMAL METRIC(1) | | TMUX7462F | | UNIT |
|---|---|---|---|---|
| | | PW (TSSOP) | RRP (WQFN) | |
| | | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | TBD | 42.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | TBD | 28.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | TBD | 17.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | TBD | 0.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | TBD | 17.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | TBD | 4.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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## 9 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ – $V_{SS}$ (1) | Power supply voltage differential | | 8 | | 22 | V |
| $V_{DD}$ | Positive power supply voltage | | 5 | | 44 | V |
| $V_{FP}$ | Positve fault clamping voltage | | 3 | | $V_{DD}$ | V |
| $V_{FN}$ | Negative fault clamping voltage | | $V_{SS}$ | | 0 | V |
| $V_S$ | Source pin (Sx) voltage (non-fault condition) | | $V_{FN}$ | | $V_{FP}$ | V |
| $V_S$ to GND | Source pin (Sx) voltage to GND (fault condition) | | –60 | | 60 | V |
| $V_S$ to $V_{DD}$ (2) | Source pin (Sx) voltage to $V_{DD}$ or $V_D$ (fault condition) | | –85 | | | V |
| $V_S$ to $V_{SS}$ (2) | Source pin (Sx) voltage to $V_{SS}$ or $V_D$ (fault condition) | | | | 85 | V |
| $V_D$ | Drain pin (Dx) voltage | | $V_{FN}$ | | $V_{FP}$ | V |
| $V_{DIG\_IN}$ | Digital input pin (DR) voltage | | GND | | 44 | V |
| $V_{DIG\_OUT}$ (3) | Digital output pin (FF) voltage | | GND | | 5.5 | V |
| $T_A$ | Ambient temperature | | –40 | | 125 | °C |
| IDC | Continuous current through switch, WQFN package | $T_A$ = 25°C | | | 150 | mA |
| IDC | Continuous current through switch, WQFN package | $T_A$ = 125°C | | | 60 | mA |

(1) $V_{DD}$ and $V_{SS}$ can be any value as long as 8 V ≤ ($V_{DD}$ – $V_{SS}$) ≤ 44 V.

(2) Source pin voltage (Sx) under a fault condition may not exceed 85 V from supply pins ($V_{DD}$ and $V_{SS}$.) or drain pins (D, Dx).

(3) Digital output pin (FF) is an open drain output and should be pulled up to a voltage within the max ratings

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## 10 Electrical Characteristics (Global)

at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $V_T$ | Threshold voltage for fault detector | | | | 0.7 | | V |
| **DIGITAL INPUT/ OUTPUT** | | | | | | | |
| $V_{IH}$ | High-level input voltage | DR pin | –40°C to +125°C | 1.3 | | 44 | V |
| $V_{IL}$ | Low-level input voltage | DR pin | –40°C to +125°C | 0 | | 0.8 | V |
| $V_{OL(FLAG)}$ | Low-level output voltage | FF pin, $I_O$ = 5 mA | –40°C to +125°C | | | 0.35 | V |
| **POWER SUPPLY** | | | | | | | |
| $V_{UVLO}$ | Undervoltage lockout (UVLO) threshold voltage ($V_{DD} – V_{SS}$) | Rising edge, single supply configuration only | –40°C to +125°C | 5 | 6 | 6.5 | V |
| | | Falling edge, single supply configuration only | –40°C to +125°C | 5 | 5.8 | 6.5 | V |

ADVANCE INFORMATION

## 11 ±15 V Dual Supply: Electrical Characteristics

$V_{DD}$ = +15 V ± 10%, $V_{SS}$ = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +15 V, $V_{SS}$ = –15 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = –10 V to +10 V<br>$I_D$ = –10 mA | 25°C | | 8.5 | | Ω |
| | | | –40°C to +85°C | | | 14 | |
| | | | –40°C to +125°C | | | 16.5 | |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = –10 V to +10 V<br>$I_D$ = –10 mA | 25°C | | 0.05 | | Ω |
| | | | –40°C to +85°C | | | 0.6 | |
| | | | –40°C to +125°C | | | 0.7 | |
| $R_{FLAT}$ | On-resistance flatness | $V_S$ = –10 V to +10 V<br>$I_D$ = –10 mA | 25°C | | 0.6 | 0.9 | Ω |
| | | | –40°C to +85°C | | | 1 | |
| | | | –40°C to +125°C | | | 1 | |
| $I_{S(ON)}$, $I_{,D(ON)}$ | Channel on leakage current (1) | $V_{DD}$ = 16.5 V, $V_{SS}$ = –16.5 V<br>Switch state is on<br>$V_S$ = $V_D$ = ±10 V | 25°C | | 0.3 | | nA |
| | | | –40°C to +85°C | –10 | | 10 | |
| | | | –40°C to +125°C | –25 | | 25 | |
| **FAULT CONDITION** | | | | | | | |
| $I_{S(FA)}$ | Input leakage current under overvoltage | $V_S$ = ± 60 V, GND = 0V, $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V | –40°C to +125°C | | ±100 | | µA |
| $I_{S(FA)}$ | Input leakage current under overvoltage | $V_S$ = ± 60 V, GND = 0V, $V_{DD}$ = $V_{SS}$ = $V_{FP}$ = $V_{FN}$= 0 V, $V_{DR}$ = 0 V or floating | –40°C to +125°C | | ±125 | | µA |
| $I_{S(FA)}$ | Input leakage current under overvoltage | $V_S$ = ± 60 V, GND = 0V, $V_{DD}$ = $V_{SS}$ = $V_{FP}$ = $V_{FN}$= floating, $V_{DR}$ = 0 V or floating | –40°C to +125°C | | ±125 | | µA |
| **DIGITAL INPUT/ OUTPUT** | | | | | | | |
| $I_{IH}$ | High-level input current | $V_{DR}$ = $V_{DD}$ | 25°C | –2 | ± 0.6 | 2 | µA |
| | | | –40°C to +125°C | –2 | | 2 | |
| $I_{IL}$ | Low-level input current | $V_{DR}$ = 0 V | 25°C | –2 | ± 0.6 | 2 | µA |
| | | | –40°C to +125°C | –2 | | 2 | |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $t_{RESPONSE}$ | Fault response time | $V_{FP}$ = 10 V, $V_{FN}$ = –10 V, $R_L$ = 1k Ω, $C_L$= 12 pF | 25°C | | 200 | | ns |
| | | | –40°C to +85°C | | | 600 | |
| | | | –40°C to +125°C | | | 600 | |
| $t_{RECOVERY}$ | Fault recovery time | $V_{FP}$ = 10 V, $V_{FN}$ = –10 V, $R_L$ = 1k Ω, $C_L$= 12 pF | 25°C | | 0.85 | | µs |
| | | | –40°C to +85°C | | | 1.8 | |
| | | | –40°C to +125°C | | | 1.8 | |
| $t_{RESPONSE(FLAG)}$ | Fault flag response time | $V_{FP}$ = 10 V, $V_{FN}$ = –10 V, $V_{PU}$ = 5 V, $R_{PU}$ = 1k Ω, $C_L$= 12 pF | 25°C | | 80 | | ns |
| $t_{RECOVERY(FLAG)}$ | Fault flag recovery time | $V_{FP}$ = 10 V, $V_{FN}$ = –10 V, $V_{PU}$ = 5 V, $R_{PU}$ = 1k Ω, $C_L$= 15 pF | 25°C | | 1 | | µs |
| $X_{TALK}$ | Intra-channel crosstalk | $R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF,<br>$V_S$ = 200m $V_{RMS}$, $V_{BIAS}$ = 0 V, f = 1 MHz | 25°C | | –60 | | dB |
| BW | –3 dB bandwidth | $R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF,<br>$V_S$ = 200m $V_{RMS}$, $V_{BIAS}$ = 0 V | 25°C | | 550 | | MHz |
| IL | Insertion loss | $R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF,<br>$V_S$ = 200m $V_{RMS}$, $V_{BIAS}$ = 0 V, f = 1 MHz | 25°C | | –0.7 | | dB |
| $C_{S(ON)}$, $C_{D(ON)}$ | Input/Output on-capacitance | f = 1 MHz, $V_S$ = 0 V | 25°C | | 16 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 0.35 | | mA |
| | | | –40°C to +85°C | | | 1 | |
| | | | –40°C to +125°C | | | 1 | |
| $I_{SS}$ | $V_{SS}$ supply current | $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 0.3 | | mA |
| | | | –40°C to +85°C | | | 0.6 | |
| | | | –40°C to +125°C | | | 0.7 | |

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$V_{DD}$ = +15 V ± 10%, $V_{SS}$ = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +15 V, $V_{SS}$ = –15 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GND}$ | GND current | $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 0.1 | | mA |
| $I_{FP}$ | $V_{FP}$ supply current | $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 100 | | µA |
| $I_{FN}$ | $V_{FN}$ supply current | $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 100 | | µA |
| $I_{DD(FA)}$ | $V_{DD}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 0.35 | | mA |
| | | | –40°C to +85°C | | | 1 | |
| | | | –40°C to +125°C | | | 1 | |
| $I_{SS(FA)}$ | $V_{SS}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 0.3 | | mA |
| | | | –40°C to +85°C | | | 0.6 | |
| | | | –40°C to +125°C | | | 0.7 | |
| $I_{GND(FA)}$ | GND current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 0.2 | | mA |
| $I_{FP(FA)}$ | $V_{FP}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 100 | | µA |
| $I_{FN(FA)}$ | $V_{FN}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 16.5 V, $V_{SS}$ = $V_{FN}$ = –16.5 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 100 | | µA |

(1) When $V_S$ is positive,$V_D$ is negative, and vice versa.

ADVANCE INFORMATION

## 12 ±20 V Dual Supply: Electrical Characteristics

$V_{DD}$ = +20 V ± 10%, $V_{SS}$ = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +20 V, $V_{SS}$ = –20 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = –15 V to +15 V<br>$I_D$ = –10 mA | 25°C | | 8.5 | | Ω |
| | | | –40°C to +85°C | | | 14 | |
| | | | –40°C to +125°C | | | 16.5 | |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = –15 V to +15 V<br>$I_D$ = –10 mA | 25°C | | 0.05 | | Ω |
| | | | –40°C to +85°C | | | 0.5 | |
| | | | –40°C to +125°C | | | 0.5 | |
| $R_{FLAT}$ | On-resistance flatness | $V_S$ = –15 V to +15 V<br>$I_D$ = –10 mA | 25°C | | 1 | | Ω |
| | | | –40°C to +85°C | | | 1.4 | |
| | | | –40°C to +125°C | | | 1.5 | |
| $I_{S(ON)}$, $I_{D(ON)}$ | Channel on leakage current | $V_{DD}$ = 22 V, $V_{SS}$ = –22 V<br>Switch state is on<br>$V_S$ = $V_D$ = ±15 V | 25°C | | 0.3 | | nA |
| | | | –40°C to +85°C | –10 | | 10 | |
| | | | –40°C to +125°C | –25 | | 25 | |
| **FAULT CONDITION** | | | | | | | |
| $I_{S(FA)}$ | Input leakage current under overvoltage | $V_S$ = ± 60 V, GND = 0V, $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V | –40°C to +125°C | | ±100 | | µA |
| $I_{S(FA)}$ | Input leakage current under overvoltage | $V_S$ = ± 60 V, GND = 0V, $V_{DD}$ = $V_{SS}$ = $V_{FP}$ = $V_{DR}$ = 0 V or floating | –40°C to +125°C | | ±125 | | µA |
| $I_{S(FA)}$ | Input leakage current under overvoltage | $V_S$ = ± 60 V, GND = 0V, $V_{DD}$ = $V_{SS}$ = $V_{FP}$ = $V_{FN}$= floating, $V_{DR}$ = 0 V or floating | –40°C to +125°C | | ±125 | | µA |
| **DIGITAL INPUT/ OUTPUT** | | | | | | | |
| $I_{IH}$ | High-level input current | $V_{DR}$ = $V_{DD}$ | 25°C | –2 | ± 0.6 | 2 | µA |
| | | | –40°C to +125°C | –2 | | 2 | |
| $I_{IL}$ | Low-level input current | $V_{DR}$ = 0 V | 25°C | –2 | ± 0.6 | 2 | µA |
| | | | –40°C to +125°C | –2 | | 2 | |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $t_{RESPONSE}$ | Fault response time | $V_{FP}$ = 10 V, $V_{FN}$ = –10 V, $R_L$ = 1k Ω, $C_L$= 12 pF | 25°C | | 200 | | ns |
| | | | –40°C to +85°C | | | 600 | |
| | | | –40°C to +125°C | | | 600 | |
| $t_{RECOVERY}$ | Fault recovery time | $V_{FP}$ = 10 V, $V_{FN}$ = –10 V, $R_L$ = 1k Ω, $C_L$= 12 pF | 25°C | | 0.85 | | µs |
| | | | –40°C to +85°C | | | 1.8 | |
| | | | –40°C to +125°C | | | 1.8 | |
| $t_{RESPONSE(FLAG)}$ | Fault flag response time | $V_{FP}$ = 10 V, $V_{FN}$ = –10 V, $V_{PU}$ = 5 V, $R_{PU}$ = 1k Ω, $C_L$= 12 pF | –40°C to +125°C | | 80 | | ns |
| $t_{RECOVERY(FLAG)}$ | Fault flag recovery time | $V_{FP}$ = 10 V, $V_{FN}$ = –10 V, $V_{PU}$ = 5 V, $R_{PU}$ = 1k Ω, $C_L$= 15 pF | –40°C to +125°C | | 1 | | µs |
| $X_{TALK}$ | Intra-channel crosstalk | $R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_S$ = 200m $V_{RMS}$, $V_{BIAS}$ = 0 V, f = 1 MHz | 25°C | | –60 | | dB |
| BW | –3 dB bandwidth | $R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_S$ = 200m $V_{RMS}$, $V_{BIAS}$ = 0 V | 25°C | | 550 | | MHz |
| IL | Insertion loss | $R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_S$ = 200m $V_{RMS}$, $V_{BIAS}$ = 0 V, f = 1 MHz | 25°C | | –0.7 | | dB |
| $C_{S(ON)}$, $C_{D(ON)}$ | Input/Output on-capacitance | f = 1 MHz, $V_S$ = 0 V | 25°C | | 16 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 0.35 | | mA |
| | | | –40°C to +85°C | | | 1 | |
| | | | –40°C to +125°C | | | 1 | |
| $I_{SS}$ | $V_{SS}$ supply current | $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 0.3 | | mA |
| | | | –40°C to +85°C | | | 0.6 | |
| | | | –40°C to +125°C | | | 0.7 | |

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$V_{DD}$ = +20 V ± 10%, $V_{SS}$ = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +20 V, $V_{SS}$ = –20 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GND}$ | GND current | $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 0.1 | | mA |
| $I_{FP}$ | $V_{FP}$ supply current | $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 100 | | µA |
| $I_{FN}$ | $V_{FN}$ supply current | $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 0 V | 25°C | | 100 | | µA |
| $I_{DD(FA)}$ | $V_{DD}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 0.35 | | mA |
| | | | –40°C to +85°C | | | 1 | |
| | | | –40°C to +125°C | | | 1 | |
| $I_{SS(FA)}$ | $V_{SS}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 0.3 | | mA |
| | | | –40°C to +85°C | | | 0.6 | |
| | | | –40°C to +125°C | | | 0.7 | |
| $I_{GND(FA)}$ | GND current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 0.2 | | mA |
| $I_{FP(FA)}$ | $V_{FP}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 100 | | µA |
| $I_{FN(FA)}$ | $V_{FN}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 22 V, $V_{SS}$ = $V_{FN}$ = –22 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 100 | | µA |

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## 13 12 V Single Supply: Electrical Characteristics

$V_{DD}$ = +12 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +12 V, $V_{SS}$ = 0 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to 7.8 V, $I_S$ = –10mA | 25°C | | 9 | | Ω |
| | | $V_S$ = 0 V to 7.8 V, $I_S$ = –10mA | –40°C to +85°C | | | 18 | Ω |
| | | $V_S$ = 0 V to 7.8 V, $I_S$ = –10mA | –40°C to +125°C | | | 20 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0 V to 7.8 V, $I_S$ = –10 mA | 25°C | | 0.05 | 0.5 | Ω |
| | | | –40°C to +85°C | | | 0.6 | |
| | | | –40°C to +125°C | | | 0.7 | |
| $R_{FLAT}$ | On-resistance flatness | $V_S$ = 0 V to 7.8 V, $I_S$ = –10 mA | 25°C | | 12 | 14 | Ω |
| | | | –40°C to +85°C | | | 19 | |
| | | | –40°C to +125°C | | | 23 | |
| $I_{S(ON)}$, $I_{D(ON)}$ | Output on leakage current(1) | Switch state is on, $V_S$ = floating, $V_D$ = 1 V/ 10 V, $V_{DD}$ = 13.2 | 25°C | | 0.3 | | nA |
| | | | –40°C to +85°C | –10 | | 10 | |
| | | | –40°C to +125°C | –25 | | 25 | |
| **FAULT CONDITION** | | | | | | | |
| $I_{S(FA)}$ | Input leakage current under overvoltage | $V_S$ = ± 60 V, GND = 0V, $V_{DD}$ = $V_{FP}$ = 13.2 V, $V_{SS}$ = $V_{FN}$ = 0 V | –40°C to +125°C | | ±100 | | µA |
| $I_{S(FA)}$ | Input leakage current under overvoltage | $V_S$ = ± 60 V, GND = 0V, $V_{DD}$ = $V_{SS}$ = $V_{FP}$ = $V_{FN}$= 0 V, $V_{DR}$ = 0 V or floating | –40°C to +125°C | | ±125 | | µA |
| $I_{S(FA)}$ | Input leakage current under overvoltage | $V_S$ = ± 60 V, GND = 0V, $V_{DD}$ = $V_{SS}$ = $V_{FP}$ = $V_{FN}$= floating, $V_{DR}$ = 0 V or floating | –40°C to +125°C | | ±125 | | µA |
| **DIGITAL INPUT/ OUTPUT** | | | | | | | |
| $I_{IH}$ | High-level input current | $V_{DR}$ =$V_{DD}$ | 25°C | –2 | ± 0.6 | 2 | µA |
| | | | –40°C to +125°C | –2 | | 2 | µA |
| $I_{IL}$ | Low-level input current | $V_{DR}$ = 0 V | 25°C | –2 | ± 0.6 | 2 | µA |
| | | | –40°C to +125°C | –2 | | 2 | |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $t_{RESPONSE}$ | Fault response time | $V_{FP}$ = 8 V, $V_{FN}$ = 0 V, $R_L$ = 1k Ω, $C_L$= 15 pF | 25°C | | 500 | 600 | ns |
| | | | –40°C to +85°C | | | 650 | |
| | | | –40°C to +125°C | | | 700 | |
| $t_{RECOVERY}$ | Fault recovery time | $V_{FP}$ = 8 V, $V_{FN}$ = 0 V, $R_L$ = 1k Ω, $C_L$= 15 pF | 25°C | | 1.5 | | µs |
| | | | –40°C to +85°C | | | 5 | |
| | | | –40°C to +125°C | | | 5 | |
| $t_{RESPONSE(FLAG)}$ | Fault flag response time | $V_{FP}$ = 8 V, $V_{FN}$ = 0 V, $V_{PU}$ = 5 V, $R_{PU}$ = 1k Ω, $C_L$= 15 pF | –40°C to +125°C | | 75 | | ns |
| $t_{RECOVERY(FLAG)}$ | Fault flag recovery time | $V_{FP}$ = 8 V, $V_{FN}$ = 0 V, $V_{PU}$ = 5 V, $R_{PU}$ = 1k Ω, $C_L$= 15 pF | –40°C to +125°C | | 60 | | µs |
| $X_{TALK}$ | Inter-channel crosstalk | $R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_S$ = 200m $V_{RMS}$, $V_{BIAS}$ = 2 V, f = 1 MHz | 25°C | | –60 | | dB |
| BW | –3 dB bandwidth | $R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_S$ = 200m $V_{RMS}$, $V_{BIAS}$ = 2 V | 25°C | | 550 | | MHz |
| IL | Insertion loss | $R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_S$ = 200m $V_{RMS}$, $V_{BIAS}$ = 2 V, f = 1 MHz | 25°C | | –0.7 | | dB |
| $C_{S(ON)}$, $C_{D(ON)}$ | Input/Output on-capacitance | f = 1 MHz, $V_S$ = 6 V | 25°C | | 16 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = $V_{FP}$ = 13.2 V, $V_{SS}$ = $V_{FN}$ = 0 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 6 V | 25°C | | 0.35 | | mA |
| | | | –40°C to +85°C | | | 1 | mA |
| | | | –40°C to +125°C | | | 1 | mA |
| $I_{GND}$ | GND current | $V_{DD}$ = $V_{FP}$ = 13.2 V, $V_{SS}$ = $V_{FN}$ = 0 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 6 V | 25°C | | 0.3 | | mA |
| $I_{FP}$ | $V_{FP}$ supply current | $V_{DD}$ = $V_{FP}$ = 13.2 V, $V_{SS}$ = $V_{FN}$ = 0 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 6 V | 25°C | | | 0.6 | µA |

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$V_{DD}$ = +12 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +12 V, $V_{SS}$ = 0 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{FN}$ | $V_{FN}$ supply current | $V_{DD}$ = $V_{FP}$ = 13.2 V, $V_{SS}$ = $V_{FN}$ = 0 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$, $V_S$ = 6 V | 25°C | | | 0.7 | µA |
| $I_{DD(FA)}$ | $V_{DD}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 13.2 V, $V_{SS}$ = $V_{FN}$ = 0 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 0.35 | | mA |
| | | | –40°C to +85°C | | | 1 | mA |
| | | | –40°C to +125°C | | | 1 | mA |
| $I_{GND(FA)}$ | GND current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 13.2 V, $V_{SS}$ = $V_{FN}$ = 0 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 0.7 | | mA |
| $I_{FP(FA)}$ | $V_{FP}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 13.2 V, $V_{SS}$ = $V_{FN}$ = 0 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 100 | | µA |
| $I_{FN(FA)}$ | $V_{FN}$ supply current under fault | $V_S$ = ± 60 V, $V_{DD}$ = $V_{FP}$ = 13.2 V, $V_{SS}$ = $V_{FN}$ = 0 V, $V_{DR}$ = 0V, 5V, or $V_{DD}$ | 25°C | | 100 | | µA |

(1) When $V_S$ is 10 V,$V_D$ is 1 V, and vice versa.

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# 14 Parameter Measurement Information

## 14.1 On-Resistance

The TMUX7462F's on-resistance is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol $R_{ON}$ is used to denote on-resistance. The measurement setup used to measure $R_{ON}$ is shown in Figure 14-1. $\Delta R_{ON}$ represents the difference between the $R_{ON}$ of any two channels, while $R_{ON\_FLAT}$ denotes the flatness that is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog signal range.

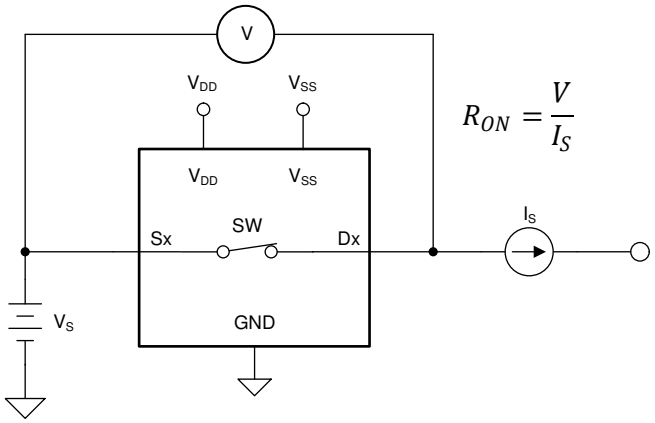


**Figure 14-1. On-Resistance Measurement Setup**

## 14.2 On-Leakage Current

Source on-leakage current ($I_{S(ON)}$) and drain on-leakage current ($I_{D(ON)}$) denotes the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. Figure 14-2 shows the circuit used for measuring the on-leakage currents.

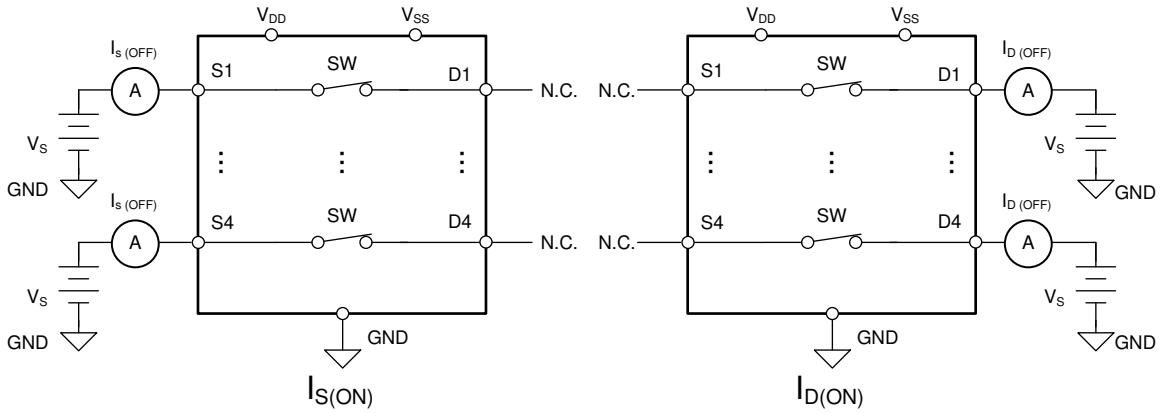


**Figure 14-2. On-Leakage Measurement Setup**

### 14.3 Input and Output Leakage Current under Overvoltage Fault

If any of the source pin voltage goes above the fault supplies ($V_{FP}$ or $V_{FN}$) by one threshold voltage ($V_T$), the TMUX7462F's overvoltage protection feature is triggered to turn off the switch under fault, keeping the fault channel in the high-impedance state. $I_{S(FA)}$ and $I_{D(FA)}$ denotes the input and output leakage current under overvoltage fault conditions, respectively. The supply (or supplies) can either be in normal operating condition (Figure 14-3) or abnormal operating condition (Figure 14-4) when the overvoltage fault occurs. The supply (or supplies) can either be unpowered ($V_{DD}$= $V_{SS}$ = $V_{FN}$ = $V_{FP}$ = 0 V), floating ($V_{DD}$= VSS = $V_{FN}$ = $V_{FP}$ = No Connection), or at any level that is below the undervoltage (UV) threshold during abnormal operating conditions.

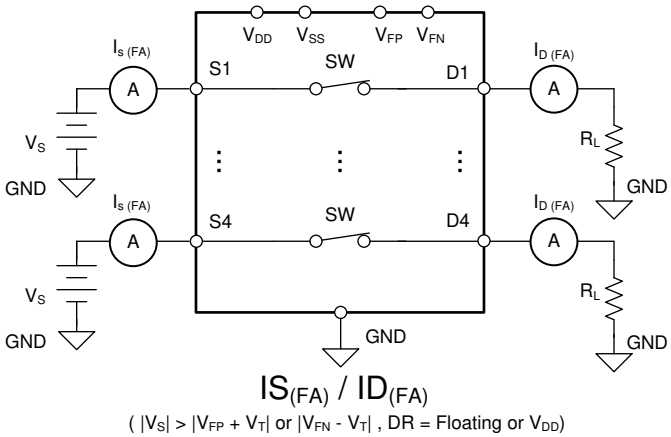


**Figure 14-3. Measurement Setup for Input and Output Leakage Current Under Overvoltage Fault with Normal Supplies**

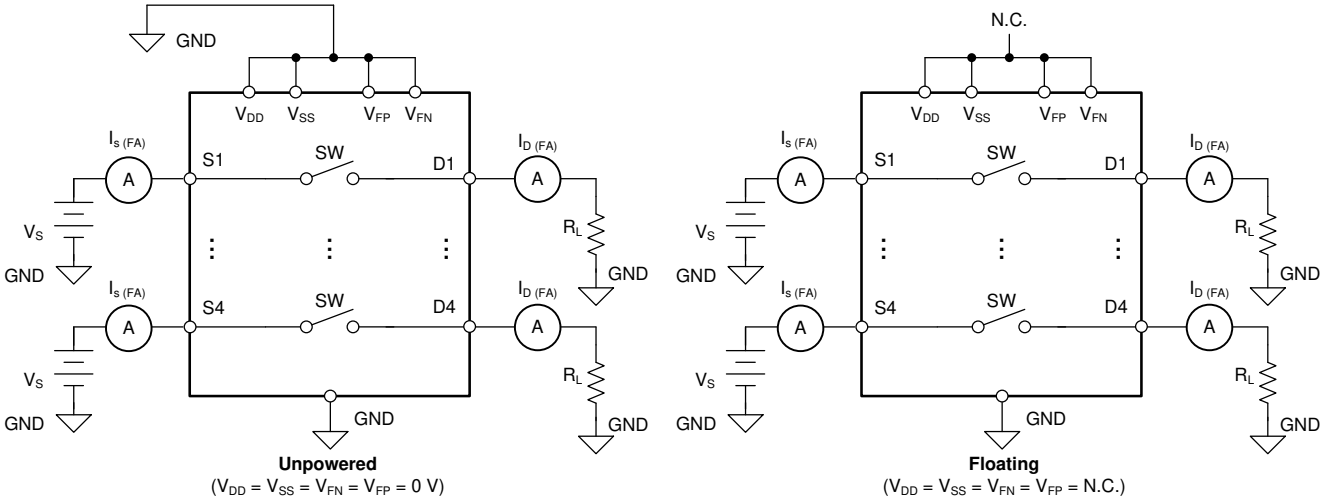


**Figure 14-4. Measurement Setup for Input and Output Leakage Current Under Overvoltage Fault with Unpowered or Floating Supplies**

## 14.4 Fault Flag Response Time

Fault flag response time ($t_{RESPONSE(FLAG)}$) measures the delay between the source voltage exceeding the fault supply voltage ($V_{FP}$ or $V_{FN}$) by 0.5 V and the general fault flag (FF) pin to go below 10% of its original value. Figure 14-5 shows the setup used to measure $t_{RESPONSE(FLAG)}$.

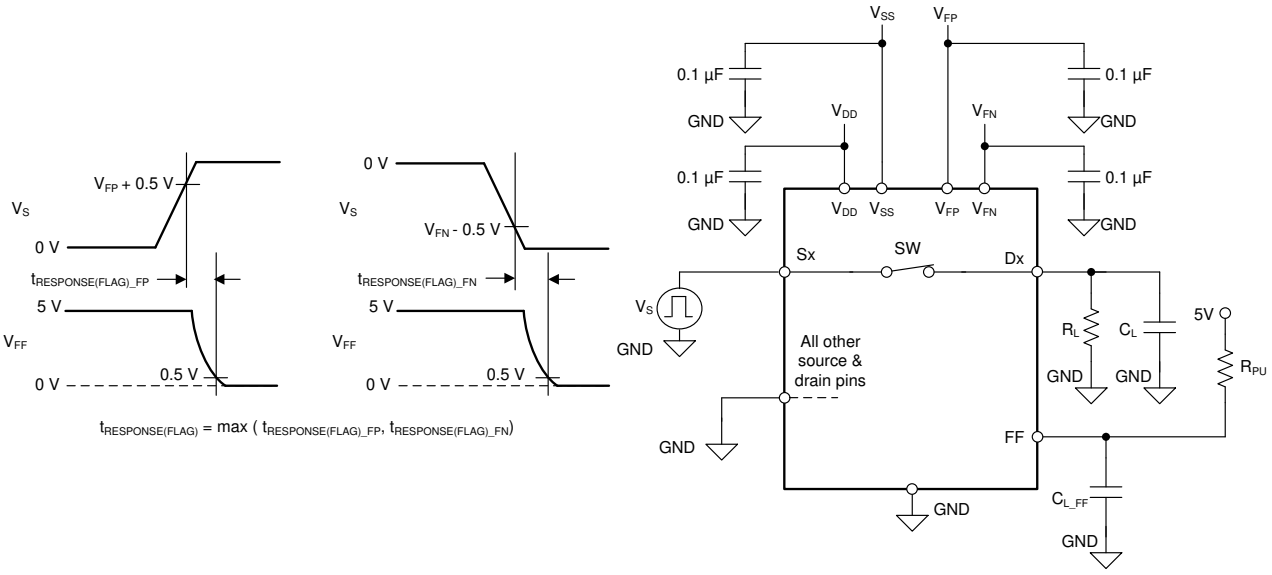


**Figure 14-5. Fault Flag Response Time Measurement Setup**

## 14.5 Fault Flag Recovery Time

Fault flag recovery time ($t_{RECOVERY(FLAG)}$) measures the delay between the source voltage falling from the overvoltage condition to below the fault supply voltage ($V_{FP}$ or $V_{FN}$) plus 0.5 V and the general fault flag (FF) pin to rise above 3 V with 5 V external pull-up. Figure 14-6 shows the setup used to measure $t_{RECOVERY(FLAG)}$.

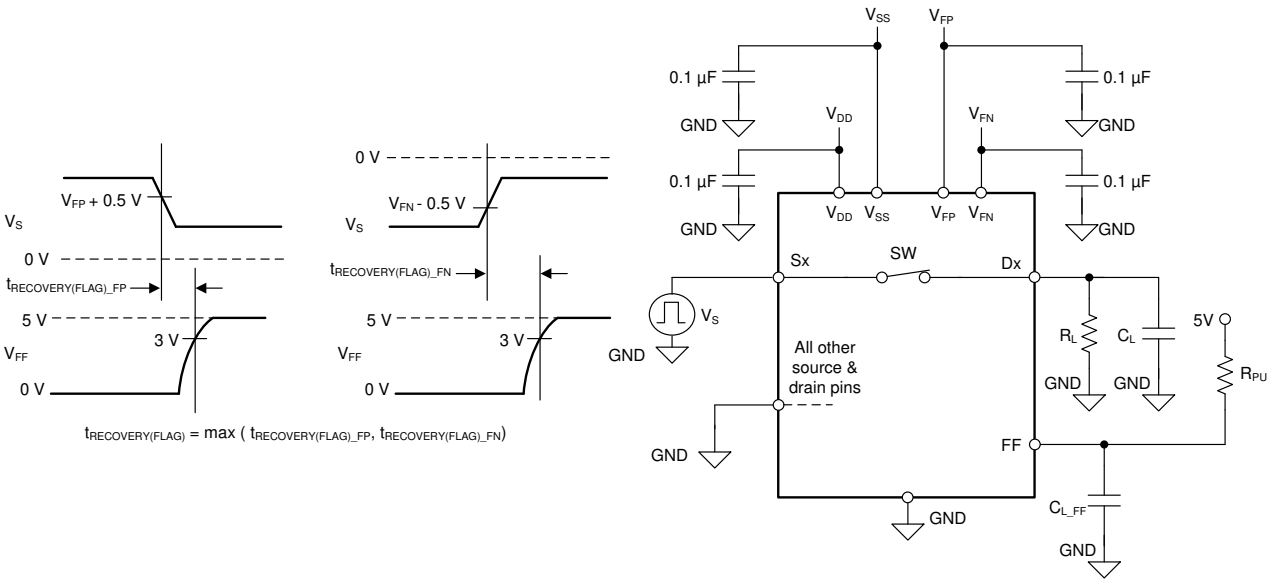


**Figure 14-6. Fault Flag Recovery Time Measurement Setup**

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## 14.6 Fault Drain Enable Time

$t_{RESPONSE(DR)}$ represents the delay between the voltage at the DR pin falling from a high to low signal and the output of the drain pin reaching 90% of the fault supplies ($V_{FP}$ or $V_{FN}$). $t_{RESPONSE(DR)}$ is a measure of how quickly the internal pull-up engages in response to the DR pin. Figure 14-7 shows the setup used to measure $t_{RESPONSE(DR)}$.

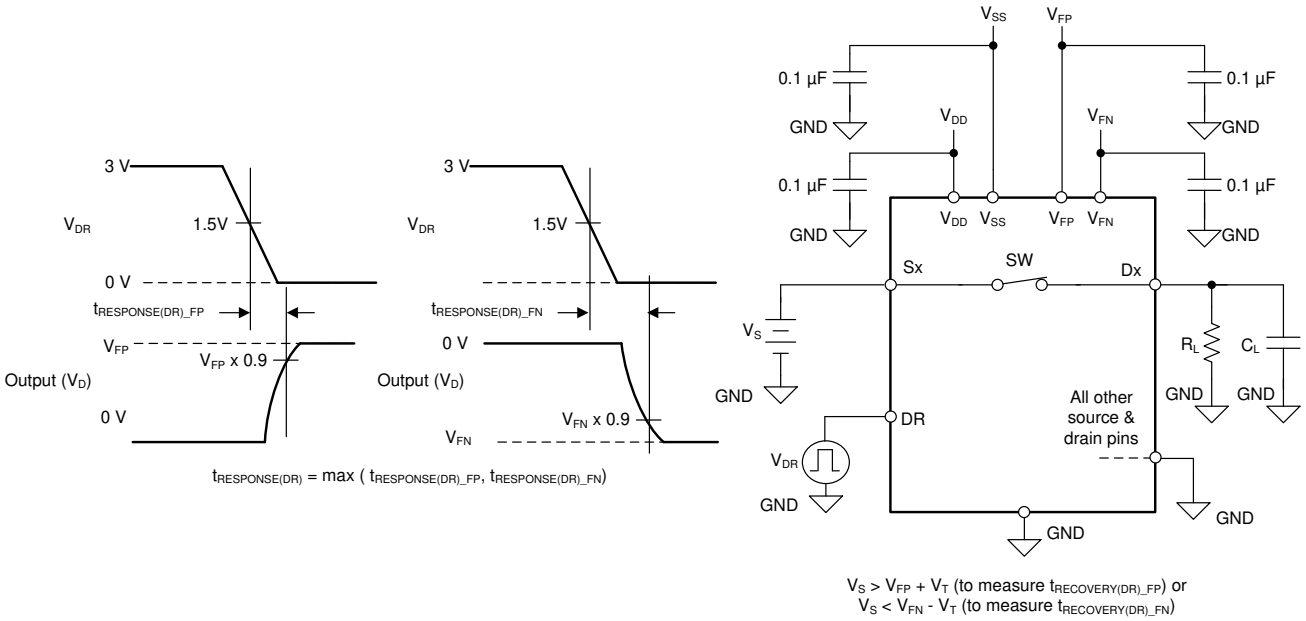
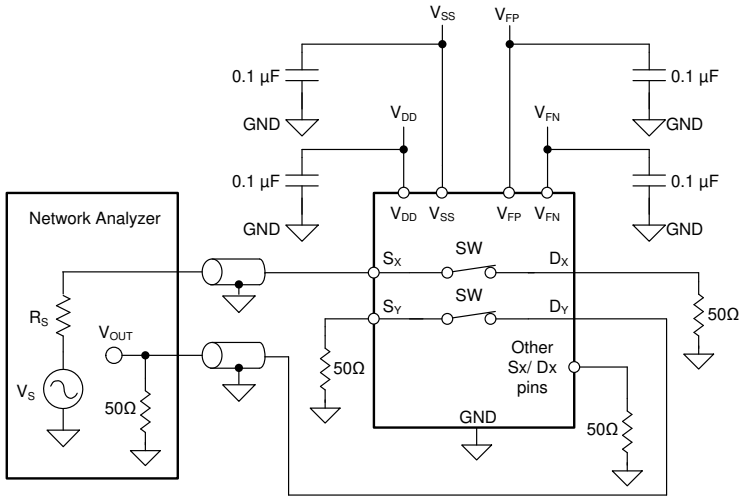



**Figure 14-7. Fault Drain Enable Time Measurement Setup**

## 14.7 Inter-Channel Crosstalk

Figure 14-8 shows how the inter-channel crosstalk ($X_{TALK(INTER)}$) is measured as the voltage at the source pin (Sx) of an on-switch input, when a 1-$V_{RMS}$ signal is applied at the source pin of an on-switch input in a different channel.

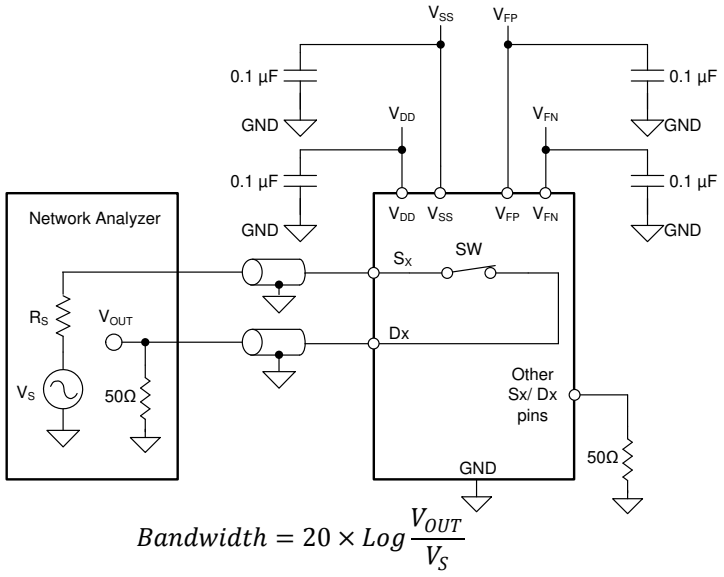



$$Inter-channel\ Crosstalk = 20 \times Log\frac{V_{OUT}}{V_S}$$

**Figure 14-8. Inter-Channel Crosstalk Measurement Setup**

## 14.8 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the TMUX7462F's drain pin (D or Dx). Figure 14-9 shows the setup used to measure bandwidth of the switch.




$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

**Figure 14-9. Bandwidth Measurement Setup**

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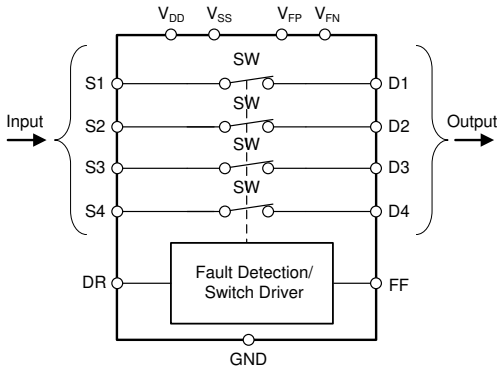
# 15 Detailed Description

## 15.1 Overview

The TMUX7462F is a four-channel protector that can be placed in series with the signal path to protect sensitive components downstream from overvoltage faults. The channel protector prevents overvoltages in both powered and powered-off conditions, making it suitable for applications where correct power supply sequencing cannot be precisely controlled. The powered-off condition includes floating power supplies, grounded power supplies, or power supplies at any level that are below the undervoltage (UV) threshold. The internal switch is turned-on and turned-off autonomously based on the fault situation without the need of external controls, making the device extremely easy to implement in the system. The primary supply voltages define the on-resistance profile, while the secondary supply voltages define the voltage level at which the overvoltage protection engages. The device works well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies (such as $V_{DD}$ = 12 V, $V_{SS}$ = –5 V).

### 15.1.1 Functional Block Diagram




### 15.1.2 Feature Description

#### *15.1.2.1 Flat ON-Resistance*

The TMUX7462F are designed with a special switch architecture to produce ultra-flat on-resistance ($R_{ON}$) across most of the switch input operation region. The flat $R_{ON}$ response allows the device to be used in precision sensor applications since the $R_{ON}$ is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

#### *15.1.2.2 Protection Features*

The TMUX7462F offer a number of protection features to enable robust system implementations.

##### 15.1.2.2.1 Input Voltage Tolerance

The maximum voltage that can be applied to any source input pin is +60 V or -60 V, allowing the device to handle typical voltage fault conditions in industrial applications. Take caution: the device has different maximum stress ratings across different pin combinations and are defined as the following:

1. **Between source pins and supply rails: 85 V**

   For example, if the device is powered by $V_{DD}$ supply of 25 V, then the maximum negative signal level on any source pin is –60 V. If the device is powered by $V_{DD}$ supply of 40 V, then the maximum negative signal level on any source pin is reduced to –45 V to maintain the 85 V maximum rating across the source pin and the supply.
2. **Between source pins and drain pin of the same channel: 85 V**

   For example, if the DR pin is left floating and an overvoltage voltage fault of –60 V occurs on the source pin S1, then the maximum positive voltage signal level driven on the drain pin channel D1 is 25 V to maintain the 85 V maximum rating across the source pin and the drain pin.

#### 15.1.2.2.2 Powered-Off Protection

The source (Sx) pins of the device remain in the high impedance (Hi-Z) state, and the device performance remains within the leakage performance specifications when the supplies of TMUX7462F are removed ($V_{DD}$/ $V_{SS}$ = 0 V or floating) or at a level that is below the undervoltage (UV) threshold. Powered-off protection minimizes system design complexity by removing the need to control the system's power supply sequencing. The feature prevents errant voltages on the input source pins from reaching the rest of the system and maintains isolation when the system is powering up. Without powered-off protection, signal on the input source pins can back-power the supply rails through internal ESD diodes and cause potential damage to the system.

A GND reference must always be present to ensure proper operation. Source and drain voltage levels of up to ±60 V are blocked in the powered-off condition.

#### 15.1.2.2.3 Fail-Safe Logic

Fail-Safe logic circuitry allows voltages on the control input pin (DR) to be applied before the supply pins. This eliminates the need for power sequencing of the logic signals and protects the device from potential damage. The control inputs are protected against positive faults of up to +44 V in the powered-off condition, but do not offer protection against a negative overvoltage condition.

#### 15.1.2.2.4 Overvoltage Protection and Detection

The TMUX7462F detects overvoltage inputs by comparing the voltage on a source pin (Sx) with the fault supplies ($V_{FP}$ and $V_{FN}$). A signal is considered overvoltage if it exceeds the fault supply voltages by the threshold voltage ($V_T$).

The switch automatically turns OFF and the source pin becomes high impedance to ensures only small leakage currents flow through the switch when an overvoltage is detected. The drain pin (Dx) behavior can be adjusted by controlling the drain response (DR) pin in the following ways:

1. **DR pin floating or driven above $V_{IH}$:**

   If the DR pin is driven about VIH level of the pin, then the drain pin becomes high impedance (Hi-Z) upon overvoltage fault.

2. **DR driven below $V_{IL}$:**

   If the DR pin is driven below VIL level of the pin, then the drain pin (Dx) is pulled to the supply that was exceeded. For example, if the source voltage exceeds $V_{FP}$, then the drain output is pulled to $V_{FP}$. If the source voltage exceeds $V_{FN}$, then the drain output is pulled to $V_{FN}$. The pull-up impedance is approximately 40 kΩ, and as a result, the drain current is limited to roughly 1 mA during a shorted load (to GND) condition.

$V_{FP}$ and $V_{FN}$ are required fault supplies that set the level at which the overvoltage protection is engaged. $V_{FP}$ can be supplied from 3 V to $V_{DD}$, while the $V_{FN}$ can be supplied from $V_{SS}$ to 0 V. If the fault supplies are not available in the system, then the $V_{FP}$ pin must be connected to $V_{DD}$, while the $V_{FN}$ pin must be connected to $V_{SS}$. In this case, the overvoltage protection then engages at the primary supply voltages $V_{DD}$ and $V_{SS}$.

#### 15.1.2.2.5 Latch-Up Immunity

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-up condition typically requires a power cycle to eliminate the low impedance path.

An insulating oxide layer is placed on top of the silicon substrate to prevent any parasitic junctions from forming in the TMUX7462F devices. As a result, the devices are latch-up immune under all circumstances by device construction.

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#### 15.1.2.2.6 EMC Protection

The TMUX7462F is not intended for standalone electromagnetic compatibility (EMC) protection in industrial applications. There are three common high voltage transient specifications that govern industrial high voltage transient specifications: IEC61000-4-2 (ESD), IEC61000-4-4 (EFT), and IEC61000-4-5 (surge immunity). A transient voltage suppressor (TVS), along with some low-value series current limiting resistor, are required to prevent source input voltages from going above the rated ±60 V limits.

It is critical to ensure that the maximum working voltage is greater than the normal operating range of the input source pins protected and any known system common-mode overvoltage that may be present due to incorrect wiring, loss of power, or short circuit when selecting a TVS protection device. Figure 15-1 shows an example of the proper design window when selecting a TVS device.

Region 1 denotes the normal operation region of TMUX7462F, where the input source voltages stay below the fault supplies $V_{FP}$ and $V_{FN}$. Region 2 represents the range of possible persistent DC (or long duration AC overvoltage fault) presented on the source input pins. Region 3 represents the margin between any known DC overvoltage level and the absolute maximum rating of the TMUX7462F. The TVS breakdown voltage must be selected to be less than the absolute maximum rating of the TMUX7462F, but greater than any known possible persistent DC or long duration AC overvoltage fault to avoid triggering the TVS inadvertently. Region 4 represents the margin the system designers must impose when selecting the TVS protection device to prevent accidental triggering of the TMUX7462F devices' ESD cells.

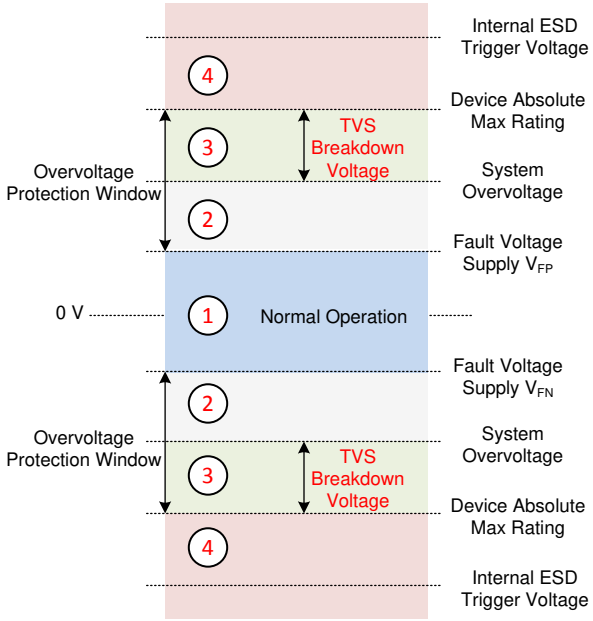


**Figure 15-1. System Operation Regions and Proper Region of Selecting a TVS Protection Device**

### *15.1.2.3 Overvoltage Fault Flags*

The voltages on TMUX7462F's source input pins are continuously monitored, and the status of whether an overvoltage condition occurs is indicated by an active low general fault flag (FF). The voltage on the FF pin indicates if any of the source input pins are experiencing an overvoltage condition. If any source pin voltage exceeds the fault supply voltages by a $V_T$, the FF output is pulled-down to below $V_{OL}$. The FF pin is an open-drain output, and external pull-up resistors of 1 kΩ are recommended. The pull-up voltage can be in the range of 1.8 V to 5.5 V, depending on the controller voltage the device interfaces with.

#### 15.1.2.4 Bidirectional and Rail-to-Rail Operation

The TMUX7462F conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has very similar characteristics in both directions; however, it is noted that the overvoltage protection is implemented only on the source (Sx) side. The voltage on the drain is only allowed to swing between $V_{FP}$ and $V_{FN}$ and no overvotlage protection is available on the drain side.

The primary supplies ($V_{DD}$ and $V_{SS}$) define the on-resistance profile of the switch channel, whereas the fault voltage supplies ($V_{FP}$ and $V_{FN}$) define the signal range that can be passed through from source to drain of the device. It is good practice to use voltages on $V_{FP}$ and $V_{FN}$ that are lower than $V_{DD}$ and $V_{SS}$ to take advantage of the flat on-resistance region of the device for better input-to-out linearity.

### 15.1.3 Device Functional Modes

The TMUX7462F offer two modes of operation (Normal mode and Fault mode) depending on whether any of the input pins experience an overvoltage condition.

#### 15.1.3.1 Normal Mode

In Normal mode operation, signals of up to $V_{FP}$ and $V_{FN}$ can be passed through the switch from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supples ($V_{DD}$ – $V_{SS}$) must be higher or equal to 8 V.
- $V_{FP}$ must be between 3 V and $V_{DD}$, and $V_{FN}$ must be between $V_{SS}$ and 0 V.
- The input signals on the source (Sx) or the drain (Dx) must be between $V_{FP}$+ $V_T$ and $V_{FN}$ – $V_T$.

#### 15.1.3.2 Fault Mode

The TMUX7462F enters into the Fault mode when any of the input signals on the source (Sx) pins exceed $V_{FP}$ or $V_{FN}$ by a threshold voltage $V_T$. The switch input experiencing the fault automatically turns off, and the source pin becomes high impedance with negligible amount of leakage current flowing through the switch under the overvoltage condition. Section 15.1.2.2.4 describes how the drain pin (Dx) behavior under the Fault mode can be programmed. The general fault flag (FF) is asserted low in the Fault mode.

The overvoltage protection is provided only for the source (Sx) input pins. The drain (Dx) pin, if used as signal input, must stay in between $V_{FP}$ and $V_{FN}$ at all time since no overvoltage protection is implemented on the drain pin.

#### 15.1.3.3 Truth Table

Table 15-1 shows the truth tables for the TMUX7462F. Each switch is independently controlled by its own select pin.

**Table 15-1. TMUX7462F Truth Table**

| DR PIN STATE | Dx State During Fault Condition |
|---|---|
| 0 | Pulled up to $V_{FP}$ or $V_{FN}$ |
| 1 | Open (HI-Z) |

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# 16 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 16.1 Application Information

The TMUX7462F is part of the fault protected switches and multiplexers family of devices. The abilty to protect downstream components from overvoltage events up to ±60 V and latch-up immunity features makes these switches and multiplexers suitable for harsh environments.

## 16.2 Typical Application

The need to monitor remote sensors is common among factory automation control systems. For example, an analog input module or mixed module (AI, AO, DI, and DO) of a programmable logic controller (PLC) will interface to a field transmitter to monitor various process sensors at remote locations around the factory. A switch or multiplexer is often used to connect multiple inputs from the system and reduce the number of downstream channels.

There are a number of fault cases that may occur that can be damaging to many of the integrated circuits. Such fault conditions may include, but are not limited to, human error due to miswiring, component failure, wire shorts, electromagnetic interference (EMI), transient distrubances, and more.

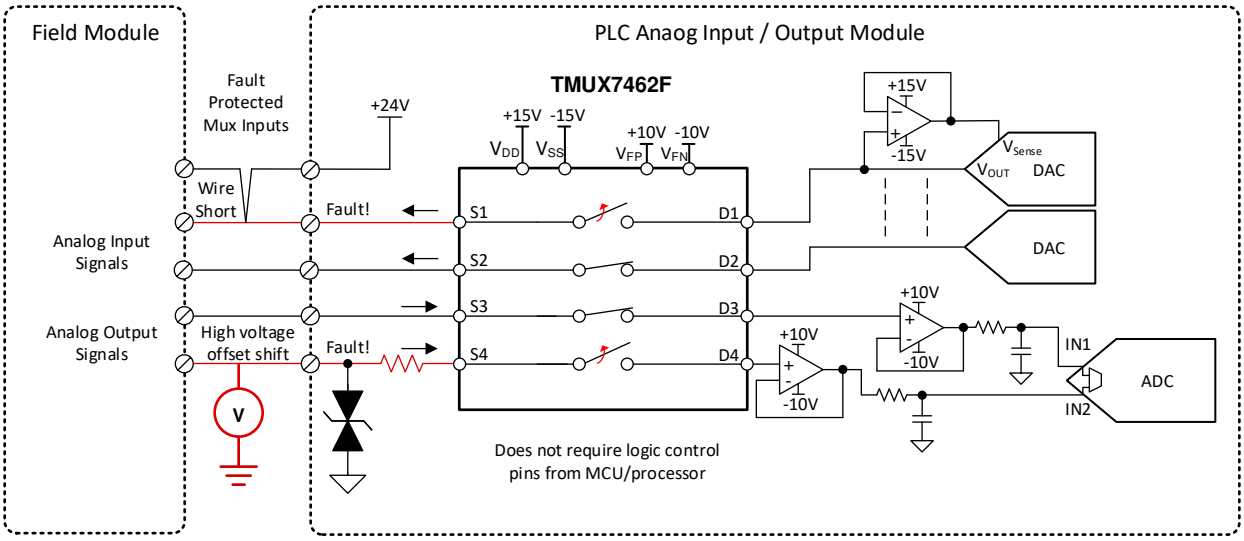


**Figure 16-1. Typical Application**

### 16.2.1 Design Requirements

**Table 16-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Positive supply ($V_{DD}$) mux | +15 V |
| Negative supply ($V_{SS}$) mux | -15 V |
| Power board supply voltage | 24 V |
| Input or output signal range non-faulted | -10 V to 10 V |
| Overvoltage protection levels | -60 V to 60 V |
| Control logic thresholds | 1.8 V compatible, up to 44 V |
| Temperature range | -40°C to +125°C |

### 16.2.2 Detailed Design Procedure

The TMUX7462F device's normal operation is to provide fault protection for the system while minimizing the control logic signals required to route across the PCB. The device works as a channel protector by allowing the signals to pass when in the valid voltage range, and opening the switch if there is a fault case. A fault protected switch can add extra robustness to the sytem against fault conditions while also reducing the number of components required to interface with the physical input channels.

The application shows two channels of the TMUX7462F connected as analog outputs and two channels connected as analog inputs to the PLC system. The analog input channels utilize the TMUX7462F to protect down stream operational amplifiers that are operating at a lower supply voltage than the multiplexer. The TMUX7462F only has overvoltage protection on the source pins, therefore these pins are connected to the external system connector on the analog output channels. If there is a miswiring or wire short issue on the connectors, the channel protector will open the switch channel to help prevent long term fault conditions from damaging the DAC.

If there is a fault condition, the drain pin of the channels can either be pulled up to the fault supply voltage ($V_{FP}$ and $V_{FN}$) through a 40 kΩ resistor or be left floating depending on the state of the DR pin. This can be configured to match the system requirements on how to handle a fault condition.

## 17 Power Supply Recommendations

The TMUX7462F operates across a wide supply range of ±5 V to ±22 V (8 V to 44 V in single-supply mode). The device also performs well with asymmetrical supplies such as $V_{DD}$ = 12 V and $V_{SS}$= –5 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 1 µF to 10 µF at the $V_{DD}$ and $V_{SS}$ pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped.

The fault supplies ($V_{FP}$ and $V_{FN}$) provide the current required to operate the fault protection, and thus, must be low impedance supplies. They can be derived from the primary supplies by using a resistor divider and buffer or be an independent supply rail. The fault supplies must not exceed the primary supplies as it might cause unexpected behavior of the switch. Use a supply decoupling capacitor ranging from 1 µF to 10 µF at the $V_{FP}$ and $V_{FN}$ pins to ground for improved supply noise immunity.

The positive supply, $V_{DD}$, must be ramped before the positive fault rail, $V_{FP}$, for proper power sequencing of the TMUX7462F. Similarly, the negative supply, $V_{SS}$, must be ramped before the negative fault voltage rail, $V_{FN}$.

# 18 Layout

## 18.1 Layout Guidelines

The image below illustrates an example of a PCB layout with the TMUX7462F. Some key considerations are:

- Decouple the $V_{DD}$ and $V_{SS}$ pins with a 1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supplies.
- Multiple decoupling capacitors can be used if their is a lot of noise in the system. For example, a 0.1-µF and 1-µF can be placed on the supply pins. If multiple capacitors are used, placing the lowest value capacitor closest to the supply pin is recommended.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

## 18.2 Layout Example

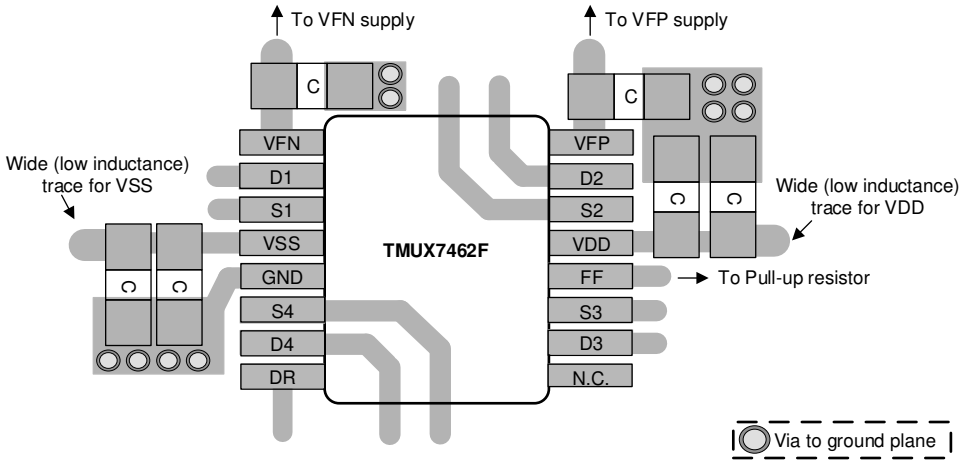


**Figure 18-1. TSSOP Layout Example**

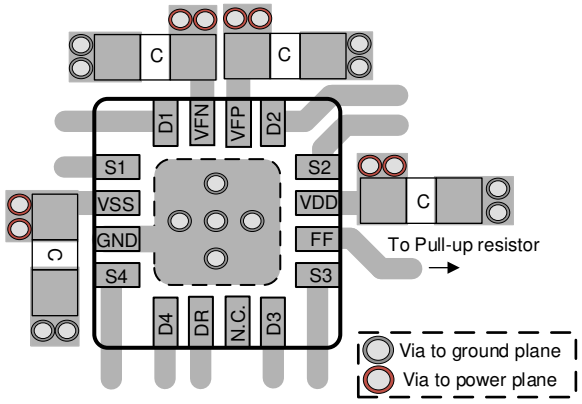


**Figure 18-2. WQFN Layout Example**

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# 19 Device and Documentation Support

## 19.1 Documentation Support

### 19.1.1 Related Documentation

- Texas Isntruments, *ADS8664 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges* data sheet
- Texas Instruments, *OPA140 High-Precision, Low-Noise, Rail-to-Rail Output, 11-MHz JFET Op Amp* data sheet
- Texas Instruments, *OPA192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-Trim™* data sheet

## 19.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 19.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 19.4 Trademarks

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## 19.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 19.6 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

# 20 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTMUX7462FRRPR | ACTIVE | WQFN | RRP | 16 | 3000 | Non-RoHS & Non-Green | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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