TMUX4157N 输入切换时无过冲的 2Ω 低 R_{ON}、-12V、2:1 (SPDT) 通用开关

1 特性

- 负电压支持：-4V 至 -12V
- 轨至轨运行
- 双向信号路径
- 兼容 1.8V 逻辑电平
- 失效防护逻辑
- 低导通电阻：2Ω
- -55°C 至 +125°C 工作温度
- 先断后合开关
- ESD 保护 HBM：2000V

2 应用

- 模拟和数字开关
- GaN 功率放大器栅极开关
- 远程射频单元 (RRU)
- 有源天线系统 mMIMO (AAS)
- 基带单元 (BBU)
- 无线通信测试

3 说明

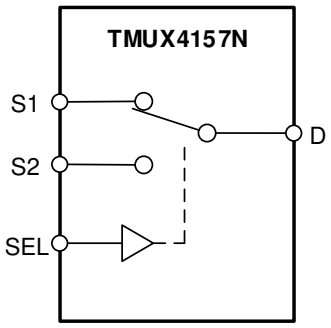
TMUX4157N 是一款仅支持负电源轨的通用 2:1 单极双投 (SPDT) 开关。电源电压范围为 -4V 至 -12V，而且该器件可在源极 (Sx) 和漏极 (D) 引脚上支持从 GND 到 V_{SS} 范围的双向模拟和数字信号。选择引脚 (SEL) 的状态决定连接到漏极引脚的源极引脚。

虽然 TMUX4157N 在电源引脚和信号路径上支持负电压，但逻辑输入引脚却通过正电压进行控制，以实现与典型控制逻辑电路（比如 GPIO 信号）的连接。逻辑输入引脚具有兼容 1.8V 逻辑电平的阈值，并可在高达 5.5V 的电压下运行以增加系统灵活性。失效防护逻辑电路允许先在控制引脚上施加电压，然后在电源引脚上施加电压，从而保护器件免受潜在的损害。

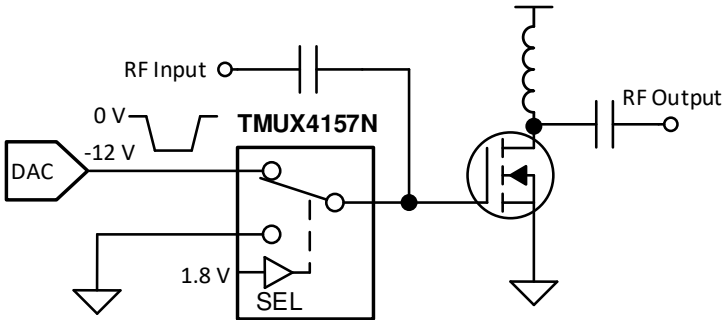
器件信息

器件型号(1)	封装	封装尺寸（标称值）
TMUX4157N	SC70 (6)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。



TMUX4157N 方框图



应用示例

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5 Pin Configuration and Functions

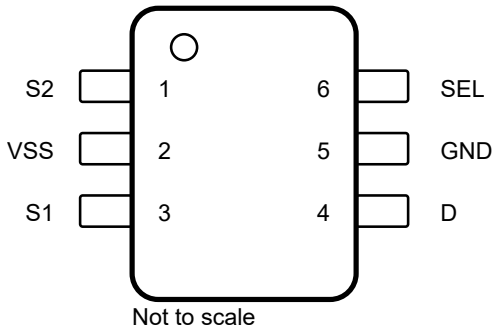

图 5-1. DCK Package 6-Pin SC70 Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
S2	1	I/O	Source pin 2. Can be an input or output.
V_{SS}	2	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
S1	3	I/O	Source pin 1. Can be an input or output.
D	4	I/O	Drain pin. Can be an input or output.
GND	5	P	Ground (0 V) reference
SEL	6	I	Select pin: controls state of the switch according to 表 7-1. (Logic Low = S1 to D, Logic High = S2 to D)

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to 节 7.4 for what to do with unused pins.

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2020	*	Initial Release

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
V_{SS}	Supply voltage	– 13	0.5	V
V_{SEL}	Logic control input pin voltage (SEL)	– 0.5	6	
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS} – 0.5	0.5	
I_{SEL}	Logic control input pin diode current (SEL)	– 50		mA
I_{IOK}	Switch source or drain pin diode current (Sx, D)	– 50	50	
I_S or $I_{D\ (CONT)}$	Continuous current through switch (Sx, D pins) – 40°C to +125°C	– 100	100	
I_S or $I_{D\ (CONT)}$	Continuous current through switch (Sx, D pins) – 40°C to +85°C	– 150	150	
I_S or $I_{D\ (PEAK)}$	Source and drain peak current: (1 ms period max, 10% duty cycle maximum) (Sx, D)	– 150	150	mA
T_{stg}	Storage temperature	– 65	150	°C
T_J	Junction temperature		150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage	– 12		– 4	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		GND	V
V_{SEL}	Logic control input pin voltage (SEL)	0		5.5	V
I_S or $I_{D\ (CONT)}$	Continuous current through switch (Sx, D pins) – 40°C to +125°C	– 100		100	mA
I_S or $I_{D\ (CONT)}$	Continuous current through switch (Sx, D pins) – 40°C to +85°C	– 150		150	mA
T_A	Ambient temperature	– 55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMUX4157N SC70 (DCK) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	181.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	132.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	56.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	72.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

At specified V_{SS} ±10%
Typical values measured at nominal V_{SS} and T_A = 25°C.

PARAMETER		TEST CONDITIONS	V_{SS}	– 55°C to 125°C MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-state switch resistance	V_S = V_{SS} to GND I_{SD} = 10 mA	– 12 V		1.8	6.5	Ω
			– 10 V		1.8	6.5	
			– 8 V		1.9	6.5	
			– 6 V		2	6.5	
			– 4 V		2.6	8	
$R_{ON\ FLAT}$	On-state switch resistance flatness	V_S = V_{SS} to GND I_{SD} = 10 mA	– 12 V		2.8		Ω
			– 10 V		2.8		
			– 8 V		2.8		
			– 6 V		2		
			– 4 V		2		
Δ_{RON}	On-state switch resistance matching between inputs	V_S = V_{SS} to GND I_{SD} = 10 mA	– 12 V		0.2		Ω
			– 10 V		0.2		
			– 8 V		0.25		
			– 6 V		0.25		
			– 4 V		0.3		
$I_{S(OFF)}$	Source off-state leakage current	Switch Off V_D = V_{SS} / GND V_S = GND / V_{SS}	– 10 V		±1	±15	µA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on-state leakage current	Switch On V_S = V_D = GND to V_{SS}	– 10 V		±1	±15	µA
C_{SOFF}	Source off capacitance	V_S = V_{SS} / 2 f = 1 MHz	– 10 V		13		pF
C_{SON} C_{DON}	On capacitance	V_S = V_{SS} / 2 f = 1 MHz	– 10 V		30		pF
POWER SUPPLY							
I_{SS}	V_{SS} supply current	Logic inputs = GND or 3.3 V V_S = V_{SS} or GND	– 12 V to – 4 V		20	70	

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6.5 Electrical Characteristics (continued)

At specified V_{SS} ±10%
Typical values measured at nominal V_{SS} and T_A = 25°C.

PARAMETER		TEST CONDITIONS	V_{SS}	– 55°C to 125°C			UNIT
				MIN	TYP	MAX	
LOGIC INPUT (SEL)							
V_{IH}	Input logic high		– 12 V	1.35		5	V
			– 10 V	1.35		5	
			– 8 V	1.35		5	
			– 6 V	1.35		5	
			– 4 V	1.35		5	
V_{IL}	Input logic low		– 12 V	0		0.8	V
			– 10 V	0		0.8	
			– 8 V	0		0.8	
			– 6 V	0		0.8	
			– 4 V	0		0.8	
I_{IH} I_{IL}	Logic input leakage current		– 12 V to – 4 V		±1	±30	µA
C_{IN}	Logic input capacitance		– 12 V to – 4 V		3		pF

6.6 Dynamic Characteristics

At specified V_{SS} ±10%
Typical values measured at nominal V_{SS} and T_A = 25°C.

PARAMETER		TEST CONDITIONS	V_{SS}	– 55°C to 125°C			UNIT
				MIN	TYP	MAX	
Q_{INJ}	Charge Injection	V_S = V_{SS} / 2 R_S = 0 Ω, C_L = 100 pF	– 12 V		– 80		pC
			– 10 V		– 60		
			– 8 V		– 55		
			– 6 V		– 40		
			– 4 V		– 30		
O_{ISO}	Off Isolation	V_{BIAS} = V_{SS} / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 1 MHz	– 12 V to – 4 V		– 65		dB
O_{ISO}	Off Isolation	V_{BIAS} = V_{SS} / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 10 MHz	– 12 V to – 4 V		– 40		dB
X_{TALK}	Crosstalk	V_{BIAS} = V_{SS} / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 1 MHz	– 12 V to – 4 V		– 65		dB
X_{TALK}	Crosstalk	V_{BIAS} = V_{SS} / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 10 MHz	– 12 V to – 4 V		– 42		dB
BW	Bandwidth	V_{BIAS} = V_{SS} / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF	– 12 V to – 4 V		340		MHz

6.7 Timing Characteristics

At specified V_{SS} ±10%
Typical values measured at nominal V_{SS} and T_A = 25°C.

PARAMETER		TEST CONDITIONS	V_{SS}	–55°C to 125°C			UNIT
				MIN	TYP	MAX	
t_{PD}	Propagation delay Sx to D, D to Sx	C_L = 100 pF	–12 V to –4 V		0.3	2	ns
$t_{TRAN\ HIGH}$	Transition-time between inputs turning on (high) SEL to D, SEL to Sx	R_L = 250 Ω, C_L = 100 pF V_S = V_{SS}	–12 V			210	ns
			–10 V			200	
			–8 V			205	
			–6 V			215	
			–4 V			280	
$t_{TRAN\ LOW}$	Transition-time between inputs turning off (low) SEL to D, SEL to Sx	R_L = 250 Ω, C_L = 100 pF V_S = V_{SS}	–12 V			210	ns
			–10 V			210	
			–8 V			215	
			–6 V			225	
			–4 V			260	
t_{BBM}	Break before make time	R_L = 50 Ω, C_L = 100 pF V_S = –2.5 V	–12 V	5			ns
			–10 V	5			
			–8 V	10			
			–6 V	10			
			–4 V	40			

7 Detailed Description

7.1 Overview

The TMUX4157N is an 2:1 (SPDT), 1-channel switch where the input is controlled with a single select (SEL) control pin.

7.2 Functional Block Diagram

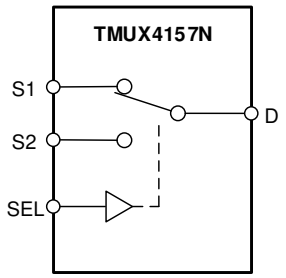

图 7-1. TMUX4157N Functional Block Diagram

7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX4157N conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX4157N ranges from GND to V_{SS}.

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7.3.3 1.8 V Logic Compatible Inputs

The TMUX4157N has 1.8-V logic compatible control for the logic control input (SEL). The logic input threshold scales with supply but still provides 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allow the TMUX4157N to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*

7.3.4 Fail-Safe Logic

The TMUX4157N supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the TMUX4157N to be ramped to 5.5 V while V_{SS} = 0 V. Additionally, the feature enables operation of the TMUX4157N with V_{SS} = 1.2 V while allowing the select pin to interface with a logic level of another device up to 5.5 V.

7.4 Device Functional Modes

The select (SEL) pin of the TMUX4157N controls which switch is connected to the drain of the device. When a given input is not selected, that source pin is in high impedance mode (HI-Z). The control pins can be as high as 5.5 V.

The TMUX4157N can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or logic high in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or D) should be connected to GND.

7.5 Truth Tables

表 7-1. TMUX4157N Truth Table

CONTROL LOGIC (SEL)	Selected Source (Sx) Connected To Drain (D) Pin
0	S1
1	S2

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMUX4157N system flexibilty in GaN power amlifier biasing by supporting neative voltages across a wide operating supply (-4 V to -12 V). This device include 1.8 V logic compatible control input pin that enables operation in systems with 1.8 V I/O rails. These features allow the switch to reduce system complexity, board size, and overall system cost.

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8.2 Typical Application

8.2.1 Negative Voltage Input Control for Power Amplifier

One application of the TMUX4157N is for input control of a power amplifier. Utilizing a switch allows a system to control when the DAC is connected to the power amplifier, and can stop biasing the power amplifier by switching the gate voltage. 图 8-1 shows the TMUX4157N configured for control of the power amplifier. The no overshoot when switching between inputs feature of the TMUX4157N is beneficial in applications such as this where the output is being switched across the full voltage range, and any overshoot on the output is undesired.

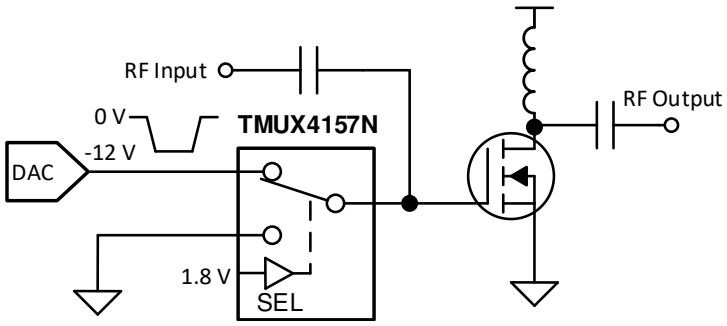

图 8-1. Input Control of Power Amplifier

8.2.1.1 Design Requirements

This design example uses the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{SS})	-12V V
Switch I/O signal range	0 V to V_{SS} (Rail to Rail)
Control logic thresholds (SEL)	1.8 V compatible (up to 5.5 V)

8.2.1.2 Detailed Design Procedure

The application shown in 图 8-1 demonstrates how to toggle between the DAC output and GND for control of a GaN power amplifier using a single control input. The DAC output is utilized to bias the gate of the power amplifier and can be disconnected from the circuit using the select pin of the switch. The TMUX4157N can support 1.8-V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX4157N can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a pull-down or pull-up resistor to ensure the input is in a known state if the control signal becomes disconnected. All inputs to the switch must fall within the recommend operating conditions of the TMUX4157N including signal range and continuous current.

9 Power Supply Recommendations

The TMUX4157N operates across a wide supply range of -4 V to -12 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{SS} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{SS} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

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10 Layout

10.1 Layout Guidelines

10.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection primarily occurs because the width of the trace changes. At the apex of the turn, the trace width increases to 1.414 times its width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self‑inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 10-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

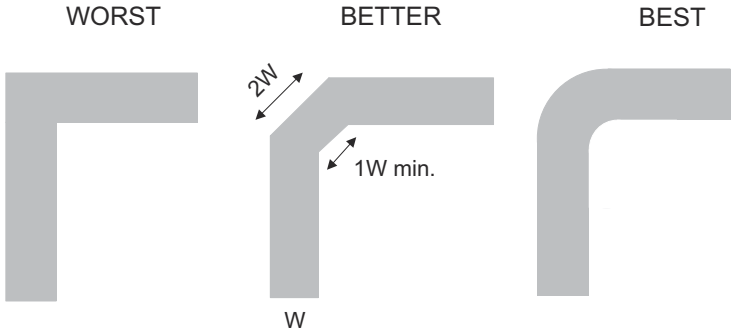


图 10-1. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 10-2 illustrates an example of a PCB layout with the TMUX4157N. Some key considerations are:

- Decouple the V_{SS} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{SS} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

10.2 Layout Example

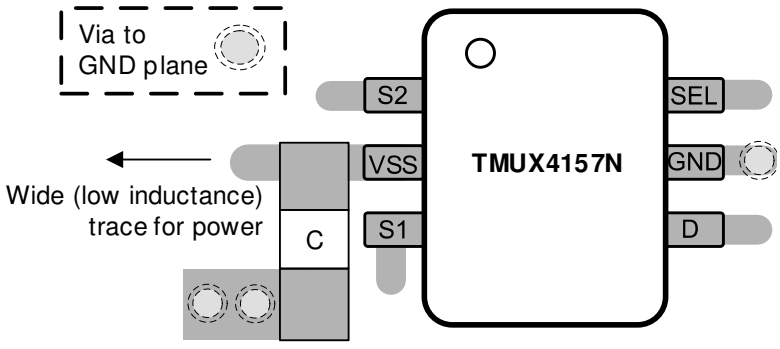


图 10-2. TMUX4157N Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.

Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.

Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX4157NDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1II	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

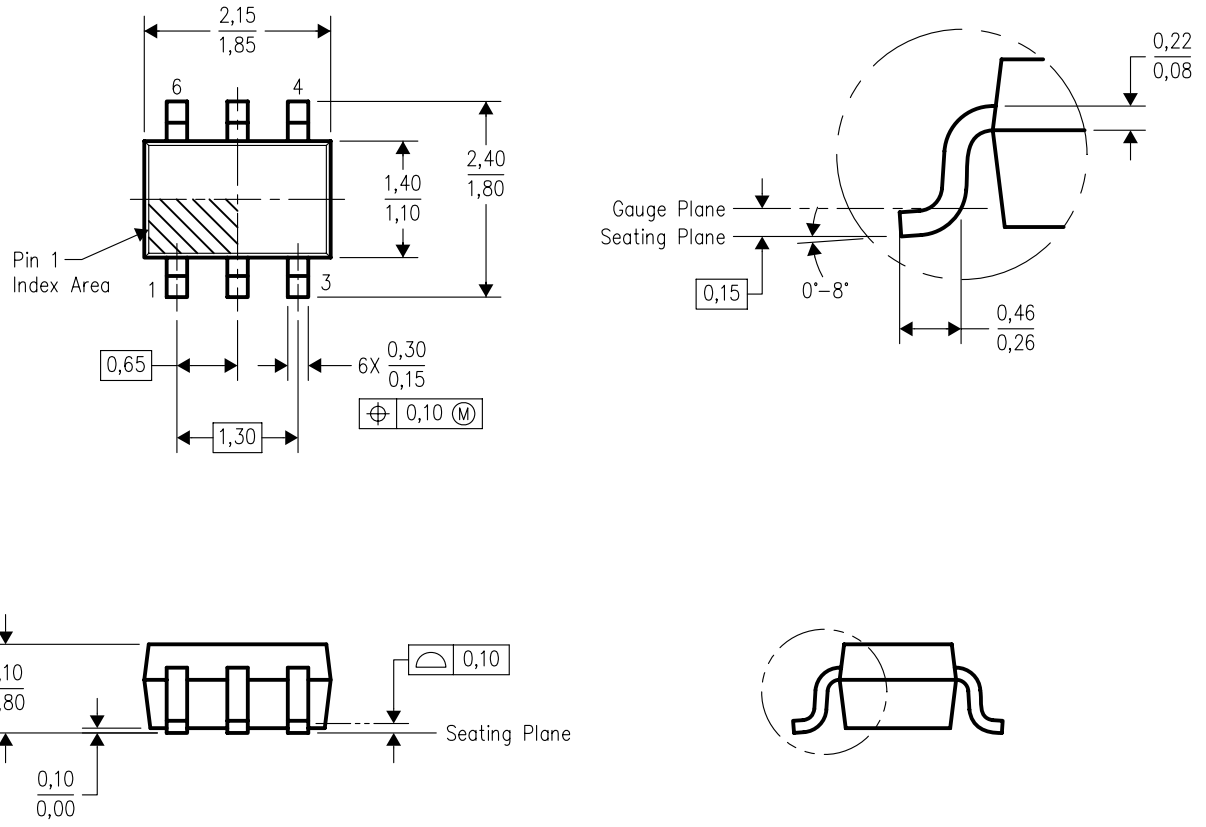
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

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