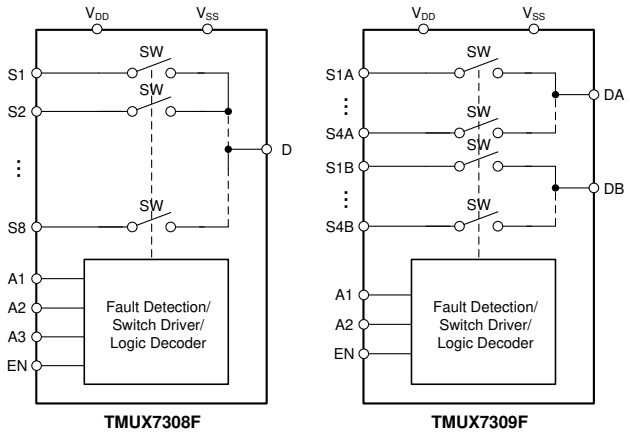
TMUX730xF ±60-V Fault-Protected, 8:1 and Dual 4:1 Multiplexers with 1.8-V Logic

1 Features

- Wide supply range:
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Integrated fault protection:
  - Overvoltage protection, source to supplies or to Ddrain: ±85 V
  - Overvoltage protection: ±60 V
  - Powered-off protection: ±60 V
  - Non-fault channels continue to operate with low leakage currents
  - Known state without digital inputs present
  - Output clamped to the supply in overvoltage condition
- Latch-up immunity by device construction
- Break-before-make switching action
- Logic levels: 1.8 V to V_{DD}
- Industry standard TSSOP and smaller WQFN packages

2 Applications

- Factory automation and control
- Programmable logic controllers (PLC)
- Analog input modules
- Semiconductor test equipment
- Battery test equipment
- Servo drive control module
- Data acquisition systems (DAQ)



Simplified Schematic

3 Description

The TMUX7308F and TMUX7309F are modern complementary metal-oxide semiconductor (CMOS) analog multiplexers in 8:1 (single ended) and 4:1 (differential) configurations. The devices work well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies. All control inputs support logic levels from 1.8 V to 44 V, enabling system level flexibility for controlling the multiplexer.

When no power supplies are present, the switch channels remain in the OFF state regardless of switch input conditions and logic control status. Under normal operation conditions, if the analog input signal level on any Sx pin exceeds the supply voltage (V_{DD} or V_{SS}) by a threshold voltage (V_T), the channel turns OFF and the Sx pin becomes high impedance. When the fault channel is selected, the drain pin (D or Dx) is pulled to the supply (V_{DD} or V_{SS}) that was exceeded. The device blocks fault voltage up to +60 V or –60 V relative to ground in both powered and powered-off conditions.

The low capacitance, low charge injection, and integrated fault protection enable the TMUX7308F and TMUX7309F devices to be used in front end data acquisition applications where high performance and high robustness are both critical. The devices are available in standard TSSOP package and smaller WQFN package (ideal if PCB space is limited).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX7308F TMUX7309F	TSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2021	*	Initial Release

Device Comparison Table

PRODUCT	DESCRIPTION
TMUX7308F	+60 V/ –60 V Tolerant, Fault-protected, Latch-up Immune, Single-Ended 8:1 Multiplexer
TMUX7309F	+60 V/ –60 V Tolerant, Fault-protected, Latch-up Immune, 4:1, 2-Channel Multiplexer

5 Pin Configuration and Functions

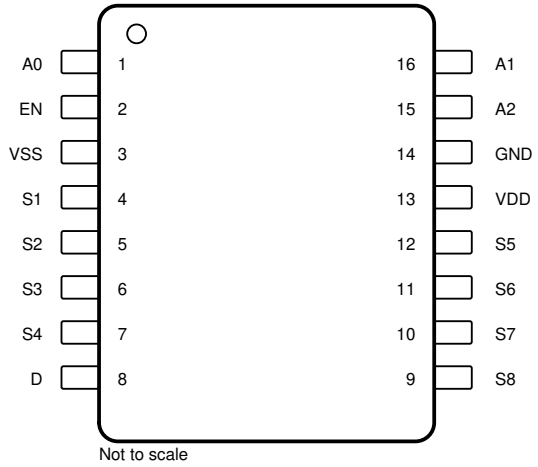

Figure 5-1. PW Package 16-Pin TSSOP Top View

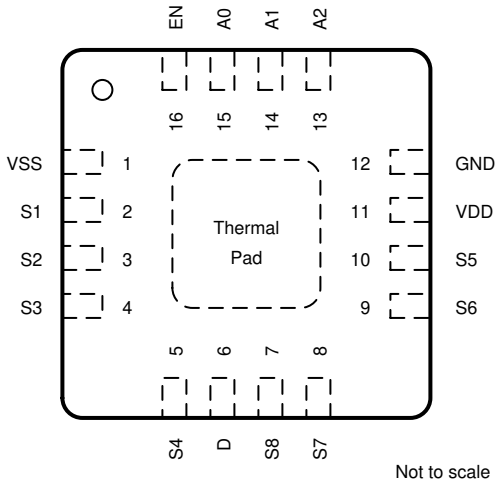

Figure 5-2. RRP Package 16-Pin WQFN Top View

Table 5-1. Pin Functions: TMUX7308F

PIN			TYPE(1)	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	I	Logic control input address 0 (A0).
EN	2	16	I	Active high digital enable (EN) pin. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states.
V_{SS}	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
S1	4	2	I/O	Source pin 1. Can be an input or output.
S2	5	3	I/O	Source pin 2. Can be an input or output.
S3	6	4	I/O	Source pin 3. Can be an input or output.
S4	7	5	I/O	Source pin 4. Can be an input or output.
D	8	6	I/O	Drain pin. Can be an input or output.
S8	9	7	I/O	Source pin 8. Can be an input or output.
S7	10	8	I/O	Source pin 7. Can be an input or output.
S6	11	9	I/O	Source pin 6. Can be an input or output.
S5	12	10	I/O	Source pin 5. Can be an input or output.
V_{DD}	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	14	12	P	Ground (0 V) reference
A2	15	13	I	Logic control input address 2 (A2).
A1	16	14	I	Logic control input address 1 (A1).
Thermal Pad	–	–	P	The thermal pad is not connected internally. No requirement to solder this pad. For best performance it is recommended that the pad be tied to GND or VSS

(1) I = input, O = output, I/O = input and output, P = power

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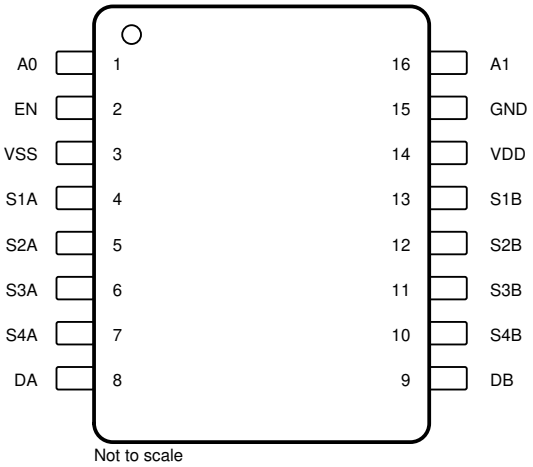

Figure 5-3. PW Package 16-Pin TSSOP Top View

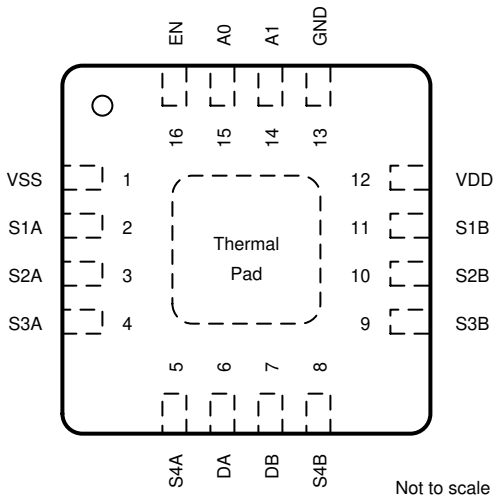

Figure 5-4. RRP Package 16-Pin WQFN Top View

Table 5-2. Pin Functions: TMUX7309F

PIN			TYPE[1]	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	I	Logic control input address 0 (A0).
EN	2	16	I	Active high digital enable (EN) pin. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states.
V_{SS}	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
S1A	4	2	I/O	Source pin 1A. Can be an input or output.
S2A	5	3	I/O	Source pin 2A. Can be an input or output.
S3A	6	4	I/O	Source pin 3A. Can be an input or output.
S4A	7	5	I/O	Source pin 4A. Can be an input or output.
DA	8	6	I/O	Drain terminal A. Can be an input or output.
DB	9	7	I/O	Drain terminal B. Can be an input or output.
S4B	10	8	I/O	Source pin 4B. Can be an input or output.
S3B	11	9	I/O	Source pin 3B. Can be an input or output.
S2B	12	10	I/O	Source pin 2B. Can be an input or output.
S1B	13	11	I/O	Source pin 1B. Can be an input or output.
V_{DD}	14	12	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	15	13	P	Ground (0 V) reference
A1	16	14	I	Logic control input address 1 (A1).
Thermal Pad	–	–	P	The thermal pad is not connected internally. No requirement to solder this pad. For best performance it is recommended that the pad be tied to GND or VSS

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		48	V
V_{DD} to GND		–0.3	48	V
V_{SS} to GND		–48	0.3	V
V_S to GND	Source input pin (Sx) voltage to GND	–60	60	V
V_S to V_{DD}	Source input pin (Sx) voltage to V_{DD}	–85		V
V_S to V_{SS}	Source input pin (Sx) voltage to V_{SS}		85	V
V_D	Drain pin (D or Dx) voltage	V_{SS}–0.7	V_{DD}+0.7	V
V_{SEL} or V_{EN}	Logic control input pin voltage (EN, A0, A1, A2)(2)	GND –0.7	48	V
I_{SEL} or I_{EN}	Logic control input pin current (EN, A0, A1, A2)(2)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx or D)	I_{DC} ± 10 %(3)	I_{DC} ± 10 %(3)	mA
T_{stg}	Storage temperature	–65	150	°C
T_A	Ambient temperature	–55	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Stresses have to be kept at or below both voltage and current ratings at all time.
(3) Refer to Recommended Operating Conditions for I_{DC} ratings.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TMUX7308F/ TMUX7309F		UNIT
		PW (TSSOP)	RRP (QFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	43.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	28.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	17.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential	8		22	V
V_{DD}	Positive power supply voltage	5		44	V
V_S	Source pin (Sx) voltage (non-fault condition)	V_{SS}		V_{DD}	V
V_{S_FAULT} (2)	Source pin (Sx) voltage (fault condition)	–60		60	V
V_D	Drain pin (D, Dx) voltage	V_{SS}		V_{DD}	V
V_{SEL} of V_{EN}	Logic control input pin voltage (EN, A0, A1, A2)	0		44	V
T_A	Ambient temperature	–40		125	°C
IDC TMUX7308F	Continuous current through switch, WQFN package, 25°C			13	mA
	Continuous current through switch, WQFN package, 125°C			8	mA

(1) V_{DD} and V_{SS} can be any value as long as 8 V ≤ (V_{DD} – V_{SS}) ≤ 44 V, and the minimum V_{DD} is met.
(2) Source pin voltage (Sx) under a fault condition may not exceed 85 V from supply pins (V_{DD} and V_{SS}.) or drain pins (D, Dx).

6.5 Electrical Characteristics (Global)

at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_T	Threshold voltage for fault detector		25°C		0.7		V
DIGITAL INPUT/ OUTPUT							
V_{IH}	High-level input voltage	EN, Ax pins	–40°C to +125°C	1.3		44	V
V_{IL}	Low-level input voltage	EN, Ax pins	–40°C to +125°C	0		0.8	V
POWER SUPPLY							
V_{UVLO}	Undervoltage lockout (UVLO) threshold voltage ($V_{DD} – V_{SS}$)	Rising edge, single supply configuration only	–40°C to +125°C	5	6	6.5	V
V_{UVLO}	Undervoltage lockout (UVLO) threshold voltage ($V_{DD} – V_{SS}$)	Falling edge, single supply configuration only	–40°C to +125°C	5	5.8	6.5	V

6.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V, I_S = –1 mA	25°C		250	300	Ω
			–40°C to +85°C			330	
			–40°C to +125°C			390	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V, I_S = –1 mA	25°C		2.5	6	Ω
			–40°C to +85°C			12	
			–40°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = –10 V to +10 V, I_S = –1 mA	25°C		1.5	3.5	Ω
			–40°C to +85°C			4	
			–40°C to +125°C			4	
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–8		8	
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V	25°C	–2	0.1	2	nA
			–40°C to +85°C	–5		5	
			–40°C to +125°C	–15		15	
$I_{S(ON)}$, $I_{,D(ON)}$	Channel on leakage current	Switch state is on, V_S = floating, V_D = –10 V/ +10 V, or V_S = –10 V/ +10 V, V_D = floating, V_{DD} = 16.5 V, V_{SS} = –16.5 V	25°C	–2	0.3	2	nA
			–40°C to +85°C	–20		20	
			–40°C to +125°C	–25		25	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current under overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = 16.5 V, V_{SS} = –16.5 V	25°C		±90		µA
			–40°C to +85°C		±95		
			–40°C to +125°C		±100		
		V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = 0 V, V_{EN} = V_{Ax} = 0 V or floating	25°C		±120		µA
			–40°C to +85°C		±125		
			–40°C to +125°C		±130		
		V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = floating, V_{EN} = V_{Ax} = 0 V or floating	25°C		±120		µA
			–40°C to +85°C		±125		
			–40°C to +125°C		±130		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–2	± 0.6	2	µA
			–40°C to +125°C	–2		2	
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–2	± 0.6	2	µA
			–40°C to +125°C	–2		2	
t_{TRAN}		V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		160		ns
			–40°C to +85°C			380	
			–40°C to +125°C			400	

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V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		150		ns
			–40°C to +85°C			300	
			–40°C to +125°C			400	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		120		ns
			–40°C to +85°C			300	
			–40°C to +125°C			400	
$t_{RESPONSE}$	Fault response time	R_L = 4 kΩ, C_L= 12 pF	25°C		90		ns
			–40°C to +85°C			200	
			–40°C to +125°C			300	
$t_{RECOVERY}$	Fault recovery time	R_L = 4 kΩ, C_L= 12 pF	25°C		0.7		µs
			–40°C to +85°C			2	
			–40°C to +125°C			2.5	
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–40°C to +125°C	50	120		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF, R_S = 0 Ω	25°C		–13		pC
OFF_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–65		dB
X_{TALK}	Intra-channel crosstalk (TMUX7308F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–60		dB
	Inter-channel crosstalk (TMUX7309F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–75		dB
BW	–3 dB bandwidth (TMUX7308F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V	25°C		100		MHz
	–3 dB bandwidth (TMUX7309F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V	25°C		150		MHz
IL	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–10		dB
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V	25°C		5		pF
$C_{D(OFF)}$	Output off-capacitance (TMUX7308F)	f = 1 MHz, V_S = 0 V	25°C		40		pF
	Output off-capacitance (TMUX7309F)	f = 1 MHz, V_S = 0 V	25°C		20		pF
$C_{S(ON)}$, $C_{D(ON)}$	Input/Output on-capacitance (TMUX7308F)	f = 1 MHz, V_S = 0 V	25°C		40		pF
	Input/Output on-capacitance (TMUX7309F)	f = 1 MHz, V_S = 0 V	25°C		20		pF

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V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}, V_S = 0 V	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}, V_S = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
I_{GND}	GND current	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}, V_S = 0 V	25°C		0.1		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.2		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.13	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	

(1) When V_S is positive,V_D is negative, and vice versa.

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6.7 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V, I_S = –1 mA	25°C		180	270	Ω
			–40°C to +85°C			340	
			–40°C to +125°C			400	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V, I_S = –1 mA	25°C		2.5	6	Ω
			–40°C to +85°C			12	
			–40°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = –15 V to +15 V, I_S = –1 mA	25°C		1.5	3.5	Ω
			–40°C to +85°C			4	
			–40°C to +125°C			4	
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V, I_S = –1 mA	–40°C to +125°C		0.05		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +15 V/ –15 V, V_D = –15 V/ + 15 V, V_{DD} = 22 V, V_{SS} = –22 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–8		8	
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = +15 V/ –15 V, V_D = –15 V/ + 15 V, V_{DD} = 22 V, V_{SS} = –22 V	25°C	–2	0.1	2	nA
			–40°C to +85°C	–5		5	
			–40°C to +125°C	–15		15	
$I_{S(ON)}$, $I_{,D(ON)}$	Channel on leakage current	Switch state is on, V_S = floating, V_D = –15 V/ +15 V, or V_S = –15 V/ +15 V, V_D = floating, V_{DD} = 22 V, V_{SS} = –22 V	25°C	–2	0.3	2	nA
			–40°C to +85°C	–20		20	
			–40°C to +125°C	–25		25	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current under overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = 22 V, V_{SS} = –22 V	25°C		±90		μA
			–40°C to +85°C		±95		
			–40°C to +125°C		±100		
		V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = 0 V, V_{EN} = V_{Ax} = 0 V or floating	25°C		±120		μA
			–40°C to +85°C		±125		
			–40°C to +125°C		±130		
		V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = floating, V_{EN} = V_{Ax} = 0 V or floating	25°C		±120		μA
			–40°C to +85°C		±125		
			–40°C to +125°C		±130		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–2	± 0.6	2	μA
			–40°C to +125°C	–2		2	
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–2	± 0.6	2	μA
			–40°C to +125°C	–2		2	
t_{TRAN}	Transition time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		160		ns
			–40°C to +85°C			380	
			–40°C to +125°C			400	

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		150		ns
			–40°C to +85°C			300	
			–40°C to +125°C			400	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		120		ns
			–40°C to +85°C			300	
			–40°C to +125°C			400	
$t_{RESPONSE}$	Fault response time	R_L = 4 kΩ, C_L= 12 pF	25°C		90		ns
			–40°C to +85°C			200	
			–40°C to +125°C			300	
$t_{RECOVERY}$	Fault recovery time	R_L = 4 kΩ, C_L= 12 pF	25°C		0.7		µs
			–40°C to +85°C			2	
			–40°C to +125°C			2.5	
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–40°C to +125°C	50	120		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF, R_S = 0 Ω	25°C		–13		pC
OFF_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–65		dB
X_{TALK}	Intra-channel crosstalk (TMUX7308F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–60		dB
	Inter-channel crosstalk (TMUX7309F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–75		
BW	–3 dB bandwidth (TMUX7308F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V	25°C		100		MHz
	–3 dB bandwidth (TMUX7309F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V	25°C		150		
IL	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–10		dB
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V	25°C		5		pF
$C_{D(OFF)}$	Output off-capacitance (TMUX7308F)	f = 1 MHz, V_S = 0 V	25°C		40		pF
	Output off-capacitance (TMUX7309F)	f = 1 MHz, V_S = 0 V	25°C		20		
$C_{S(ON)}$, $C_{D(ON)}$	Input/Output on-capacitance (TMUX7308F)	f = 1 MHz, V_S = 0 V	25°C		40		pF
	Input/Output on-capacitance (TMUX7309F)	f = 1 MHz, V_S = 0 V	25°C		20		

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V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}, V_S = 0 V	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}, V_S = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
I_{GND}	GND current	V_{DD} = 22 V, V_{SS} = –22 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}, V_S = 0 V	25°C		0.1		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = 22 V, V_{SS} = –22 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = 22 V, V_{SS} = –22 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = 22 V, V_{SS} = –22 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}	25°C		0.2		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.13	1	mA
			–40°C to +85°C			1	mA
			–40°C to +125°C			1	mA
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.5	mA
			–40°C to +125°C			0.6	mA

(1) When V_S is positive,V_D is negative, and vice versa.

ADVANCE INFORMATION

6.8 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 7.8 V, I_S = –1 mA	25°C		190	320	Ω
R_{ON}	On-resistance	V_S = 0 V to 7.8 V, I_S = –1 mA	–40°C to +85°C			330	Ω
R_{ON}	On-resistance	V_S = 0 V to 7.8 V, I_S = –1 mA	–40°C to +125°C			400	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 7.8 V, I_S = –1 mA	25°C		2.5	6	Ω
			–40°C to +85°C			12	
			–40°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 7.8 V, I_S = –1 mA	25°C		20	25	Ω
			–40°C to +85°C			27	
			–40°C to +125°C			27	
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = 1 V/ 10 V, V_D = 10 V/ 1 V, V_{DD} = 13.2 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–8		8	
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = 1 V/ 10 V, V_D = 10 V/ 1 V, V_{DD} = 13.2 V	25°C	–2	0.1	2	nA
			–40°C to +85°C	–5		5	
			–40°C to +125°C	–15		15	
$I_{S(ON)}$, $I_{,D(ON)}$	Output on leakage current(1)	Switch state is on, V_S = floating, V_D = 1 V/ 10 V, V_{DD} = 13.2	25°C	–2	0.3	2	nA
			–40°C to +85°C	–20		20	
			–40°C to +125°C	–25		25	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current under overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = 13.2 V, V_{SS} = 0 V	25°C		±90		µA
			–40°C to +85°C		±95		
			–40°C to +125°C		±100		
		V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = 0 V, V_{EN} = V_{Ax} = 0 V or floating	25°C		±120		µA
			–40°C to +85°C		±125		
			–40°C to +125°C		±130		
		V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = floating, V_{EN} = V_{Ax} = 0 V or floating	25°C		±120		µA
			–40°C to +85°C		±125		
			–40°C to +125°C		±130		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–2	± 0.6	2	µA
			–40°C to +125°C	–2		2	µA
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–2	± 0.6	2	µA
			–40°C to +125°C	–2		2	
t_{TRAN}	Transition time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	25°C		160		ns
			–40°C to +85°C			380	
			–40°C to +125°C			400	

ADVANCE INFORMATION

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	25°C		150		ns
			–40°C to +85°C			300	
			–40°C to +125°C			400	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	25°C		120		ns
			–40°C to +85°C			300	
			–40°C to +125°C			400	
$t_{RESPONSE}$	Fault response time	R_L = 4 kΩ, C_L= 12 pF	25°C		90		ns
			–40°C to +85°C			200	
			–40°C to +125°C			300	
$t_{RECOVERY}$	Fault recovery time	R_L = 4 kΩ, C_L= 12 pF	25°C		0.7		µs
			–40°C to +85°C			2	
			–40°C to +125°C			2.5	
Q_J	Charge injection	V_S = 6 V, C_L = 1 nF, R_S = 0 Ω	25°C		–13		pC
OFF_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–65		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–60		dB
X_{TALK}	Inter-channel crosstalk (TMUX7309F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–75		dB
BW	–3 dB bandwidth (TMUX7308F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 6 V	25°C		100		MHz
	–3 dB bandwidth (TMUX7309F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 6 V	25°C		150		
IL	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–10		dB
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 6 V	25°C		5		pF
$C_{D(OFF)}$	Output off-capacitance (TMUX7308F)	f = 1 MHz, V_S = 6 V	25°C		40		pF
	Output off-capacitance (TMUX7309F)	f = 1 MHz, V_S = 6 V	25°C		20		
$C_{S(ON)}$, $C_{D(ON)}$	Input/Output on-capacitance (TMUX7308F)	f = 1 MHz, V_S = 6 V	25°C		40		pF
	Input/Output on-capacitance (TMUX7309F)	f = 1 MHz, V_S = 6 V	25°C		20		

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V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}, V_S = 6 V	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
I_{SS}	V_{SS} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}, V_S = 6 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
I_{GND}	GND current	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}, V_S = 6 V	25°C		0.1		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = 13.2 V, V_{SS} = 0 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = 13.2 V, V_{SS} = 0 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = 13.2 V, V_{SS} = 0 V, V_{EN}/ V_{Ax} = 0V, 5V, or V_{DD}	25°C		0.2		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.13	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	

(1) When V_S is 10 V,V_D is 1 V, and vice versa.

ADVANCE INFORMATION

7 Parameter Measurement Information

7.1 Truth Tables

Table 7-1 shows the truth tables for the TMUX7308F.

Table 7-1. TMUX7308F Truth Table

EN	A2	A1	A0	Selected Source Connected to Drain Pin (D)
0	X(1)	X(1)	X(1)	All sources are off (HI-Z)
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1) "X" means "do not care".

Table 7-2 shows the truth tables for the TMUX7309F.

Table 7-2. TMUX7309F Truth Table

EN	A1	A0	Selected Source Connected to Drain Pins (DA, DB)
0	X(1)	X(1)	All sources are off (HI-Z)
1	0	0	S1A and S1B
1	0	1	S2A and S2B
1	1	0	S3A and S3B
1	1	1	S4A and S4B

(1) "X" means "do not care".

7.2 On-Resistance

The on-resistance of the TMUX7308F and TMUX7309F is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 7-1. ΔR_{ON} represents the difference between the R_{ON} of any two channels, while R_{ON_FLAT} denotes the flatness that is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog signal range.

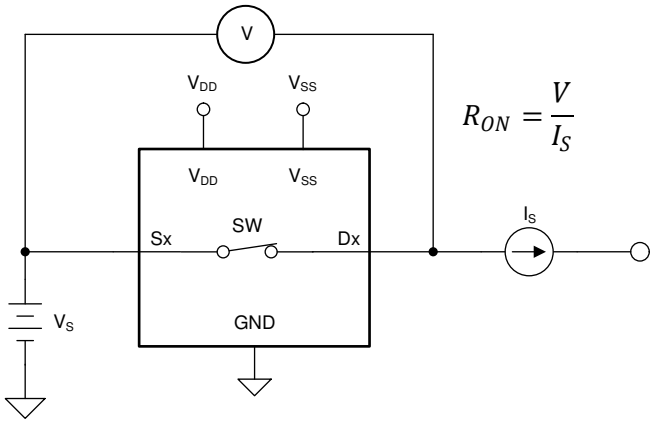

Figure 7-1. On-Resistance Measurement Setup

7.3 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

The setup used to measure both off-leakage currents is shown in Figure 7-2.

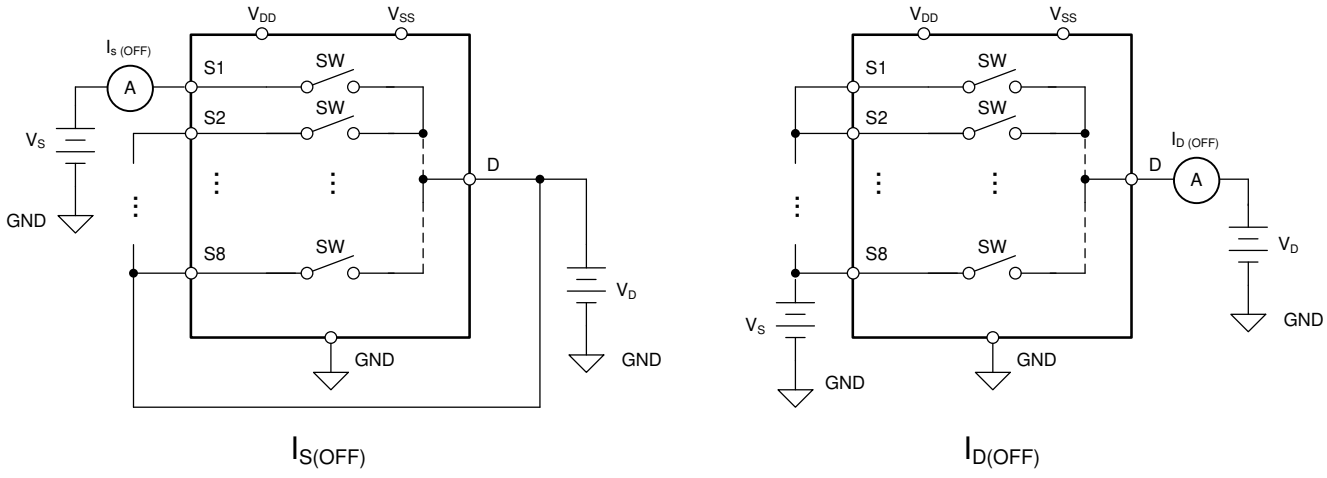

Figure 7-2. Off-Leakage Measurement Setup

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7.4 On-Leakage Current

Source on-leakage current ($I_{S(ON)}$) and drain on-leakage current ($I_{D(ON)}$) denote the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. Figure 7-3 shows the circuit used for measuring the on-leakage currents.

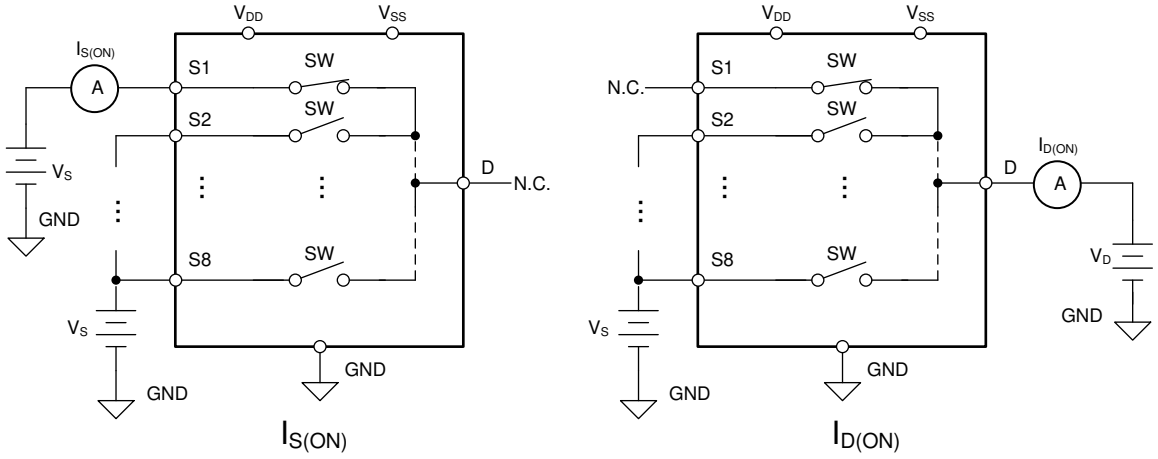


Figure 7-3. On-Leakage Measurement Setup

7.5 Break-Before-Make Delay

The break-before-make delay is a safety feature of the TMUX7308F and TMUX7309F. The ON switches first break the connection before the OFF switches make connection. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-4 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

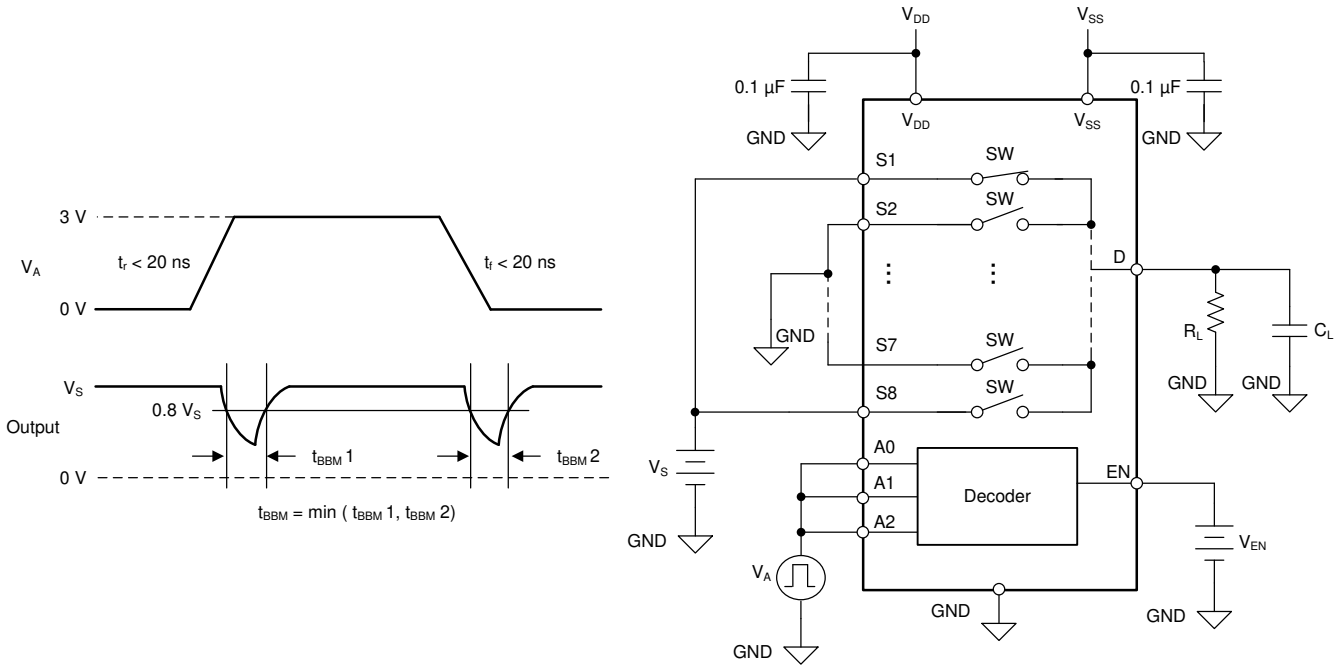


Figure 7-4. Break-Before-Make Delay Measurement Setup

7.6 Enable Delay Time

$t_{ON(EN)}$ time is defined as the time taken by the output of the TMUX7308F and TMUX7309F to rise to a 90% final value after the EN signal has risen to a 50% final value. $t_{OFF(EN)}$ is defined as the time taken by the output of the TMUX7308F and TMUX7309F to fall to a 10% initial value after the EN signal has fallen to a 50% initial value. Figure 7-5 shows the setup used to measure the enable delay time.

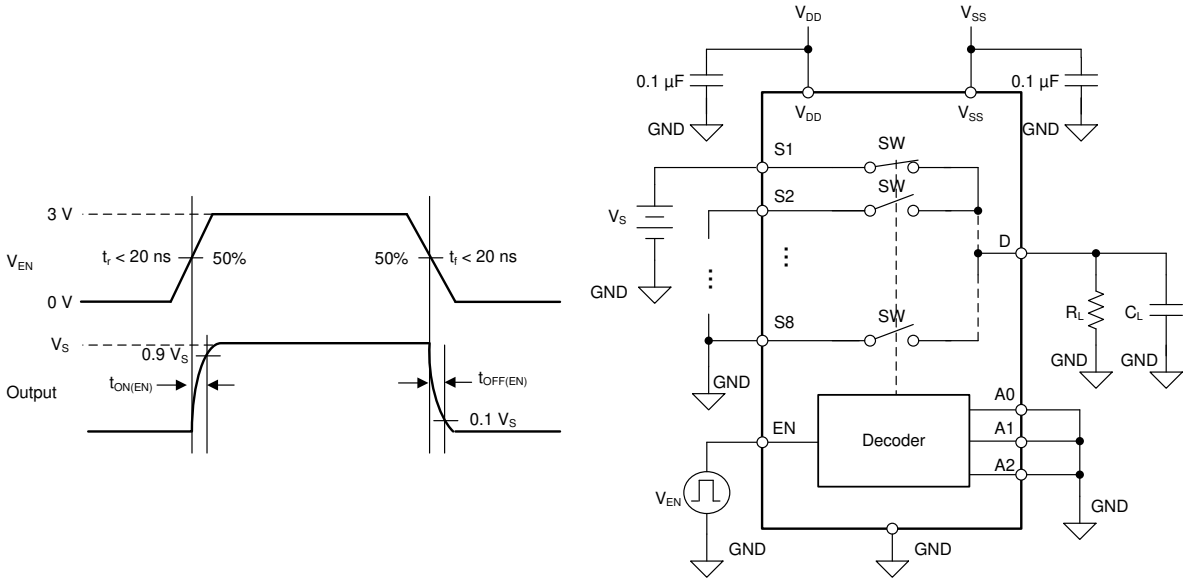


Figure 7-5. Enable Delay Measurement Setup

7.7 Transition Time

Transition time is defined as the time taken by the output of the device to rise (to 90% of the transition) or fall (to 10% of the transition) after the address signal (Ax) has fallen or risen to 50% of the transition. Figure 7-6 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.

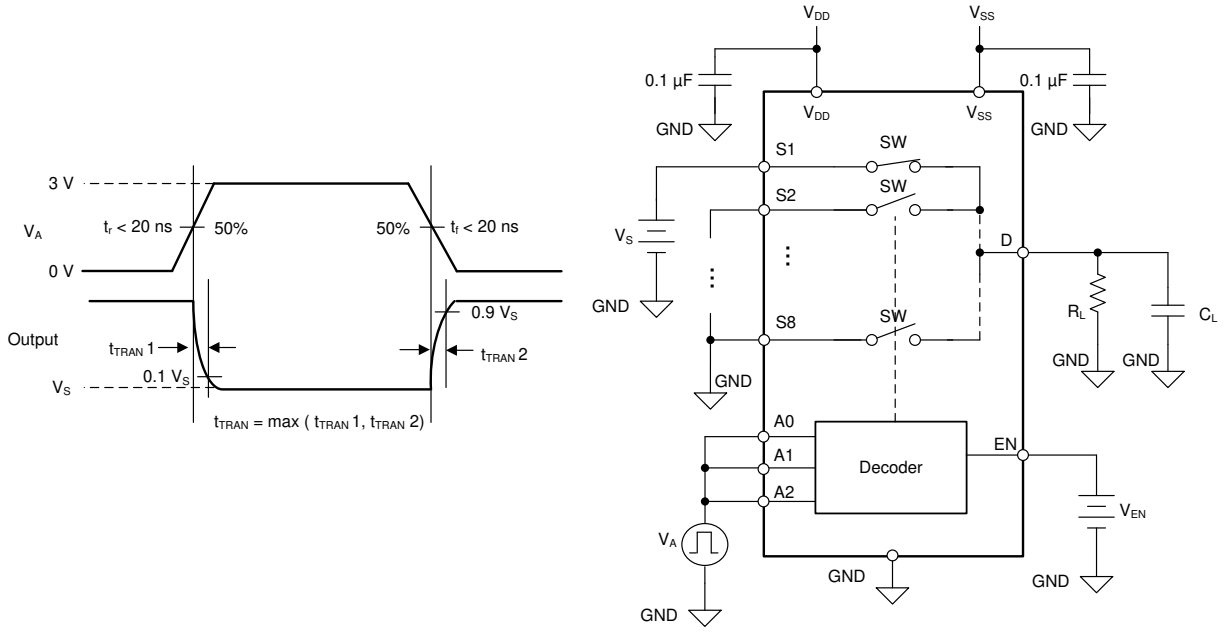


Figure 7-6. Transition Time Measurement Setup

ADVANCE INFORMATION

7.8 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching, and is denoted by the symbol Q_{INJ}. Figure 7-7 shows the setup used to measure charge injection from the source to drain.

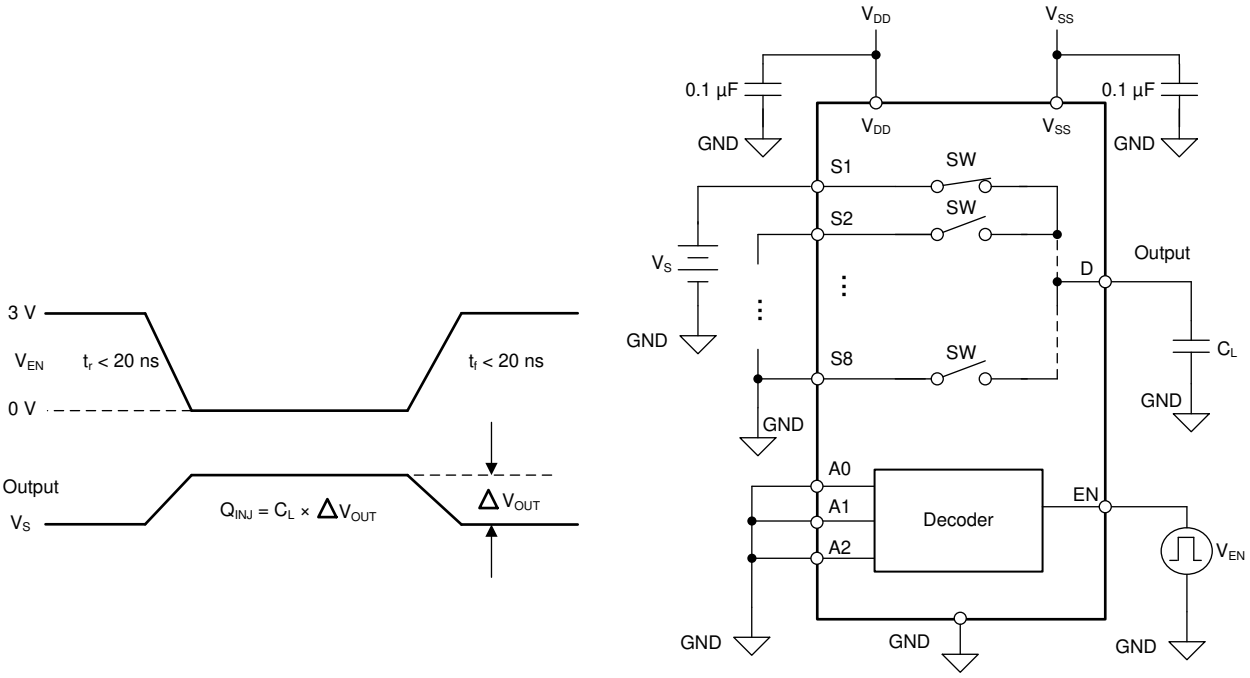
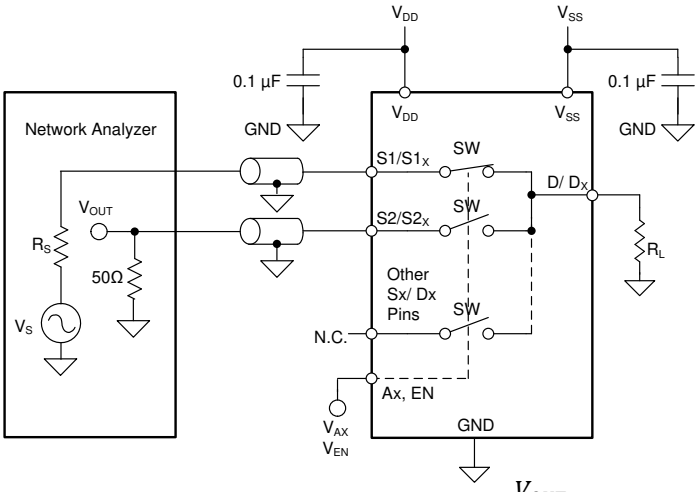


Figure 7-7. Charge-Injection Measurement Setup

7.9 Crosstalk

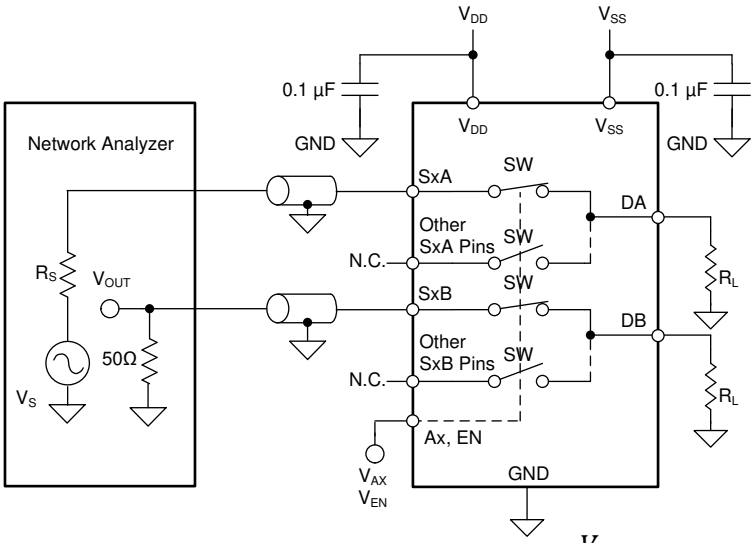
There are two types of crosstalk that can be defined for the devices:

1. Intra-channel crosstalk ($X_{TALK(INTRA)}$): the voltage at the source pin (Sx) of an off-switch input, when a 1-V_{RMS} signal is applied at the source pin of an on-switch input in the same channel, as shown in Figure 7-8 .
2. Inter-channel crosstalk ($X_{TALK(INTER)}$): the voltage at the source pin (Sx) of an on-switch input, when a 1-V_{RMS} signal is applied at the source pin of an on-switch input in a different channel, as shown in Figure 7-9. Inter-channel crosstalk applies only to the TMUX7309F device.



$$Intra-channel\ Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 7-8. Intra-channel Crosstalk Measurement Setup



$$Inter-channel\ Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 7-9. Inter-channel Crosstalk Measurement Setup

ADVANCE INFORMATION

7.10 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D or Dx) of the TMUX730xF. Figure 7-10 shows the setup used to measure bandwidth of the switch.

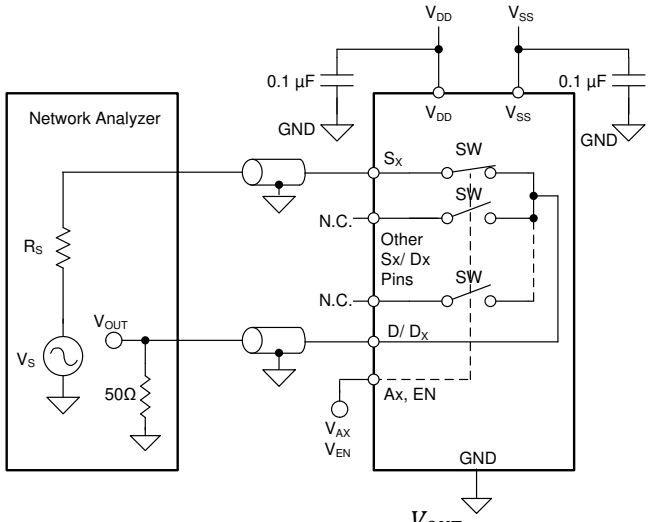


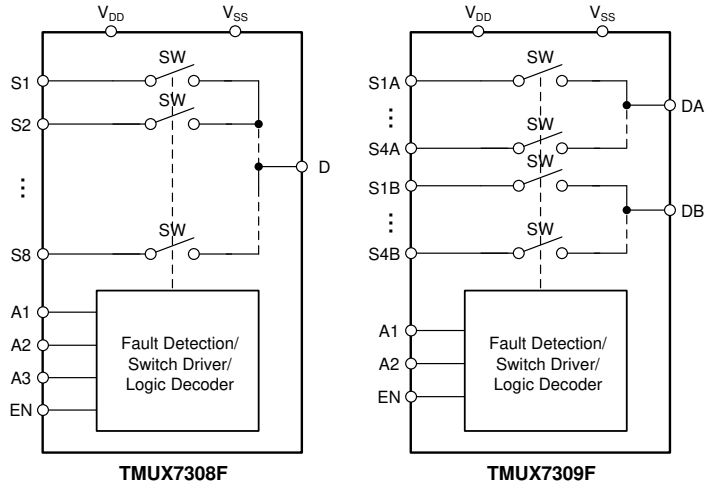
Figure 7-10. Bandwidth Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX7308F and TMUX7309F are a modern complementary metal-oxide semiconductor (CMOS) analog multiplexeres in 8:1 (single ended) and 4:1 (differential) configurations. The devices work well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies (such as V_{DD} = 15 V, V_{SS} = –5 V). The devices feature overvoltage protection feature on the source pins under powered and powered-off condition, allowing them to be used in harsh industrial environments.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Flat On - Resistance

The TMUX7308F and TMUX7309F are designed with a special switch architecture to produce ultra-flat on-resistance (R_{ON}) across most of the switch input operation region. The flat R_{ON} response allows the device to be used in precision sensor applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

8.3.2 Protection Features

The TMUX7308F and TMUX7309F offer a number of protection features to enable robust system implementations.

8.3.2.1 Input Voltage Tolerance

The maximum voltage that can be applied to any source input pin is +60 V or -60 V, allowing the device to handle typical voltage fault condition in industrial applications. It shall be cautioned that the device is rated to handle maximum stress of 85 V across different pins:

1. **Between the source pins and supply rails :**

   For example, if the device is powered by V_{DD} supply of 20 V, the maximum negative signal level on any source pin is –60 V to maintain the 60 V maximum rating on any source pin. If the device is powered by V_{DD} supply of 40 V, the maximum negative signal level on any source pin is reduced to –45 V to maintain the 85 V maximum rating across the source pin and the supply.
2. **Between the source pins and one or more drain pins:**

   For example, if channel S1 is ON and the voltage on S1(A) pin is 40 V. In this case, the drain voltage is also 40 V. The maximum negative voltage on any of the other source pins is –45 V to maintain the 85 V maximum rating across the source pin and the drain pin.

ADVANCE INFORMATION

8.3.2.2 Powered-off Protection

When the supplies of TMUX7308F and TMUX7309F are removed (V_{DD}/ V_{SS} = 0 V or floating), the source (Sx) pins of the device remain in high impedance (Hi-Z) state, and the device performance remains within the leakage performance mentioned in the Electrical Specifications. Powered-off protection minimizes system complexity by removing the need to control power supply sequencing of the system. The feature prevents errant voltages on the input source pins from reaching the rest of the system and maintains isolation when the system is powering up. Without powered-off protection, signal on the input source pins can back-power the supply rails through internal ESD diodes and cause potential damage to the system.

The switch remains OFF regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Source and drain voltage levels of up to ±60 V are blocked in the powered-off condition.

8.3.2.3 Fail-Safe Logic

Fail-Safe logic circuitry allows voltages on the digital control pins to be applied before the supply pins, protecting the device from potential damage. The switch is specified to be in the OFF state, regardless of the state of the digital logic signals. The digital inputs are protected against positive faults of up to +44 V in powered-off condition, but do not offer protection against negative overvoltage condition.

8.3.2.4 Overvoltage Protection and Detection

The TMUX7308F and TMUX7309F detect overvoltage inputs by comparing the voltage on a source pin (Sx) with the supplies (V_{DD} and V_{SS}). A signal is considered overvoltage if it exceeds the supply voltages by the threshold voltage (V_T).

When an overvoltage is detected, the switch automatically turns OFF regardless of the digital logic controls. The source pin becomes high impedance and ensures only small leakage current flows through the switch. When the fault channel is selected by the digital logic control, the drain pin (D or Dx) is pulled to the supply that was exceeded. For example, if the source voltage exceeds V_{DD}, the drain output is pulled to V_{DD}. If the source voltage exceeds V_{SS}, the drain output is pulled to V_{SS}. The pull-up impedance is approximately 40 kΩ, and as a result, the drain current is limited to roughly 1 mA during a shorted load (to GND) condition. Figure depicts the protection structure of the device.

8.3.2.5 Latch-up Immunity

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

In the TMUX7308F and TMUX7309F devices, an insulating oxide layer is placed on top of the silicon substrate to prevent any parasitic junctions from forming. As a result, the devices are latch-up immune under all circumstances by device construction.

8.3.2.6 EMC Protection

The TMUX7308F and TMUX7309F are not intended for standalone electromagnetic compatibility (EMC) protection in industrial applications. There are three common high voltage transient specifications that govern industrial high voltage transient specification: IEC61000-4-2 (ESD), IEC61000-4-4 (EFT), and IEC61000-4-5 (surge immunity). A transient voltage suppressor (TVS), along with some low-value series current limiting resistor, are required to prevent source input voltages from going above the rated ±60 V limits.

When selecting a TVS protection device, it is critical to ensure that the maximum working voltage is greater than both the normal operating range of the input source pins to be protected and any known system common-mode overvoltage that may be present due to miswiring, loss of power, or short circuit. Figure 8-1 shows ane example of the proper design window when selecting a TVS device.

Region 1 denotes normal operation region of TMUX7308F and TMUX7309F, where the input source voltages stay below the fault supplies V_{FP} and V_{FN}. Region 2 represents the range of possible persistent DC (or long

duration AC overvoltage fault) presented on the source input pins. Region 3 represents the margin between any known DC overvoltage level and the absolute maximum rating of the TMUX7308F and TMUX7309F. The TVS breakdown voltage must be selected to be less than the absolute maximum rating of the TMUX730xF, but greater than any known possible persistent DC or long duration AC overvoltage fault to avoid triggering the TVS inadvertently. Region 4 represents the margin system designers must impose when selecting the TVS protection device to prevent accidental triggering of ESD cells of the TMUX7308F and TMUX7309F devices.

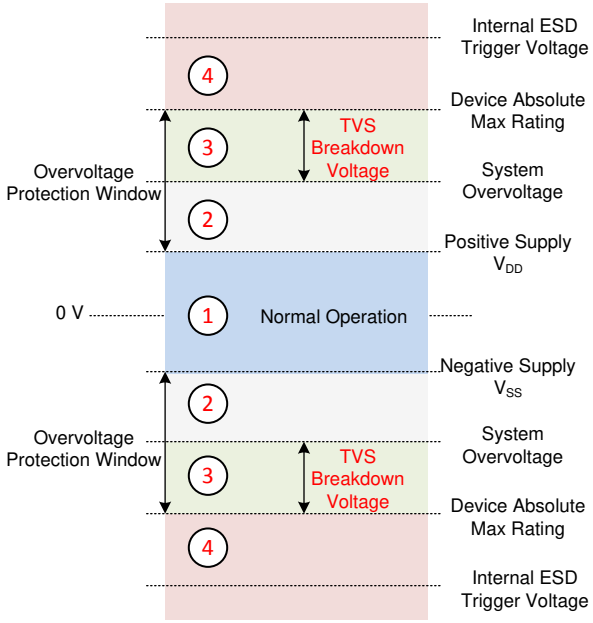


Figure 8-1. System Operation Regions and Proper Region of Selecting a TVS Protection Device

8.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX7308F and TMUX7309F conduct equally well from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). Each signal path has very similar characteristics in both directions. However, it is to be noted that the overvoltage protection is implemented only on the source (Sx) side. The voltage on the drain is only allowed to swing between V_{DD} and V_{SS} and no overvotlage protection is available on the drain side.

8.4 Device Functional Modes

The TMUX7308F and TMUX7309F offer two modes, Normal Mode and Fault Mode, of operation depending on whether any of the input pins experience overvoltage condition.

8.4.1 Normal Mode

In Normal Mode operation, signals of up to V_{DD} and V_{SS} can be passed through the switch from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). The address (Ax) pins and the enable (EN) pin determines which switch path to turn on, according to Table 7-1 and Table 7-2. The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supples (V_{DD} – V_{SS}) must be higher or equal to 8 V. With a minimum V_{DD} of 5 V.
- The input signals on the source (Sx) or the drain (D or Dx) must be be between V_{FP}+ V_T and V_{FN} – V_T.
- The digital logic control (Ax and EN) must have selected the switch.

8.4.2 Fault Mode

The TMUX7308F and TMUX7309F enter into Fault Mode when any of the input signals on the source (Sx) pins exceed V_{DD} or V_{SS} by a threshold voltage V_T. Under the overvoltage condition, the switch input experiencing the fault automatically turns OFF regardless of the digital logic status, and the source pin becomes high impedance with negligible amount of leakage current flowing through the switch. When the fault channel is selected by the

ADVANCE INFORMATION

digital logic control, the drain pin (D or Dx) is pulled to the supply that was exceeded through a 40 kΩ internal resistor.

The overvoltage protection is provided only for the source (Sx) input pins. The drain (D or Dx) pin, if used as signal input, must stay in between V_{DD} and V_{SS} at all time since no overvotlage protection is implemented on the drain pin.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMUX7308F and TMUX7309F are part of the fault protected switches and multiplexers family of devices. The abilty to protect downstream components from overvoltage events up to ±60 V makes these switches and multiplexers suitable for harsh environments.

9.2 Typical Application

In analog input programable logic controllers (PLC) a multiplexer is often used to switch multiple sensors to a single ADC. By using a multiplexer the number of compnents in the system can be reduced to save system cost and size. In a PLC module a ±10 V input signal range is common for interacing with external field transmitters and sensors, however there are a number of fault cases that may occure that can be damaging to many of the integrated circuits. Such fault conditions may include, but are not limited to, human error from mis-wiring connections, component failure / wire shorts, EMI / transient distrubances and so forth.

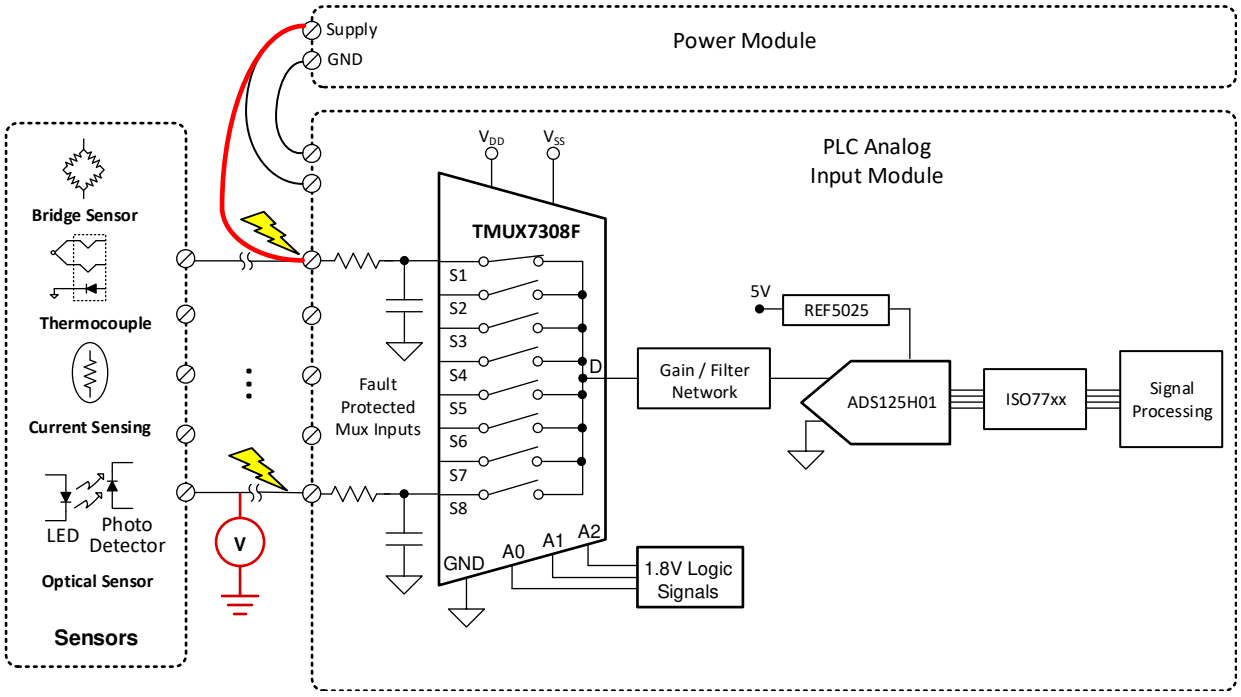


Figure 9-1. Typical Application

9.2.1 Design Requirements

Table 9-1. Design Parameters

PARAMETER	VALUE
Positive supply (V_{DD}) mux and ADC	+15 V
Negative supply (V_{SS}) mux and ADC	-15 V
Power board supply voltage	24 V
Input / output signal range non-faulted	-15 V to 15 V
Overvoltage protection levels	-60 V to 60 V
Control logic thresholds	1.8 V compatible, up to 44 V
Temperature range	-40°C to +125°C

9.2.2 Detailed Design Procedure

The image shows the case where a human mis-wiring condition occured and one of the input connectors has been short to the power board supply voltage. If the board supply voltage is higher than the power supply of the multiplexer, the TMUX7308F or TMUX7309F will disconnect the source input from passing the signal to protect the downstream ADC. The drain pin of the mux will be pulled up to the supply voltage VDD through a 40 kΩ resistor to allow the ADC to determine a fault condition has occured.

10 Power Supply Recommendations

The TMUX7308F and TMUX7309F operate across a wide supply range of ±5 V to ±22 V (8 V to 44 V in single-supply mode). They also perform well with asymmetrical supplies such as V_{DD} = 15 V and V_{SS}= –5 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped. As a best practice, it is recommended to ramp V_{SS} first before V_{DD} in dual or asymmetrical supply applications.

ADVANCE INFORMATION

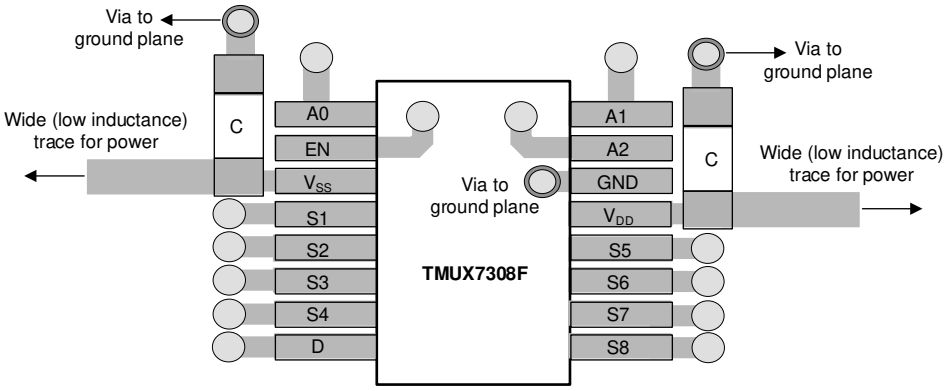
11 Layout

11.1 Layout Guidelines

The image below illustrates an example of a PCB layout with the TMUX7308F and TMUX7309F. Some key considerations are:

- Decouple the V_{DD} and V_{SS} pins with a 1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example



ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- Texas Instruments, *ADS8664 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges* data sheet
- Texas Instruments, *OPA140 High-Precision, Low-Noise, Rail-to-Rail Output, 11-MHz JFET Op Amp* data sheet
- Texas Instruments, *OPA192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-Trim™* data sheet

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

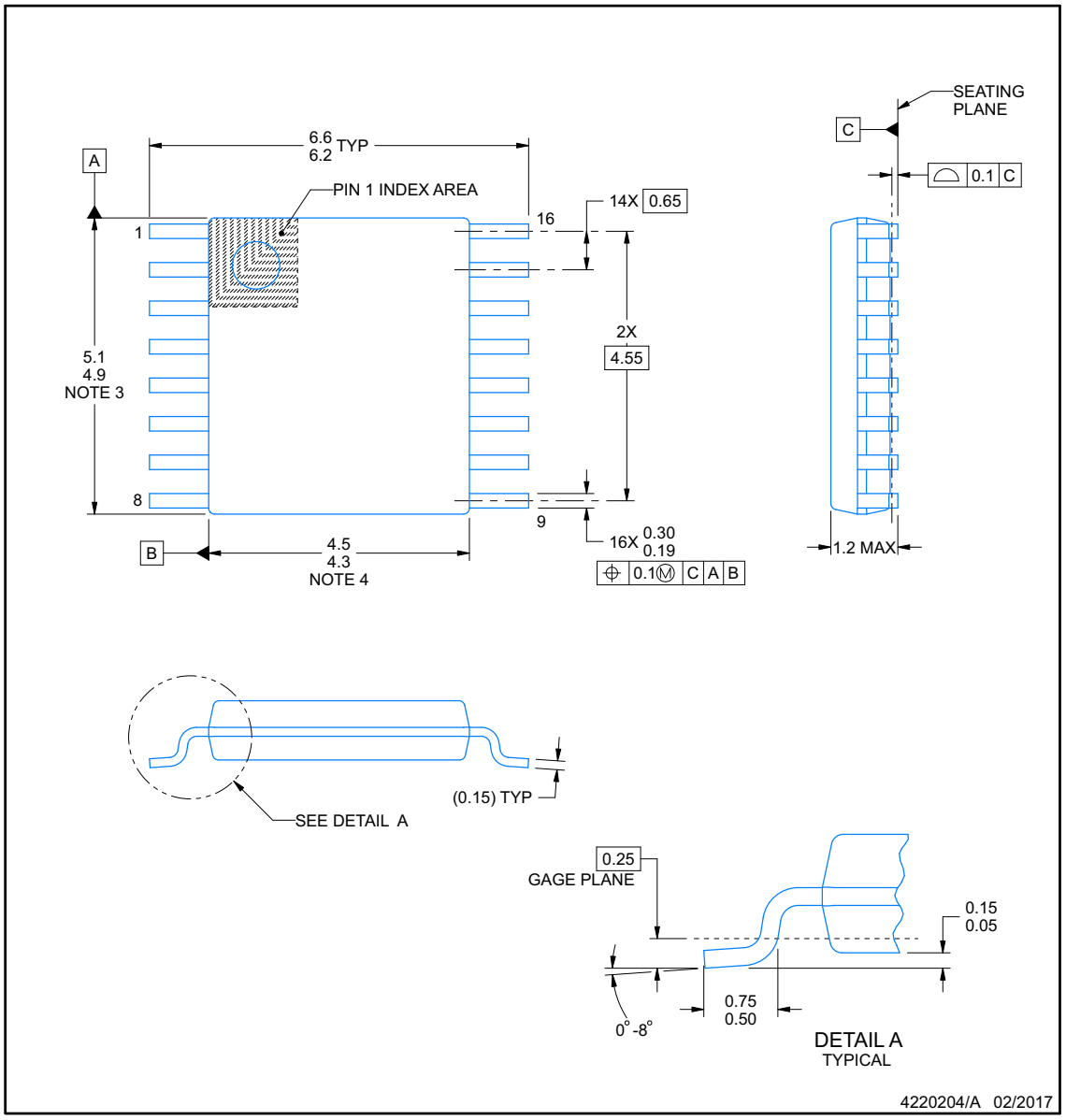
ADVANCE INFORMATION

PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

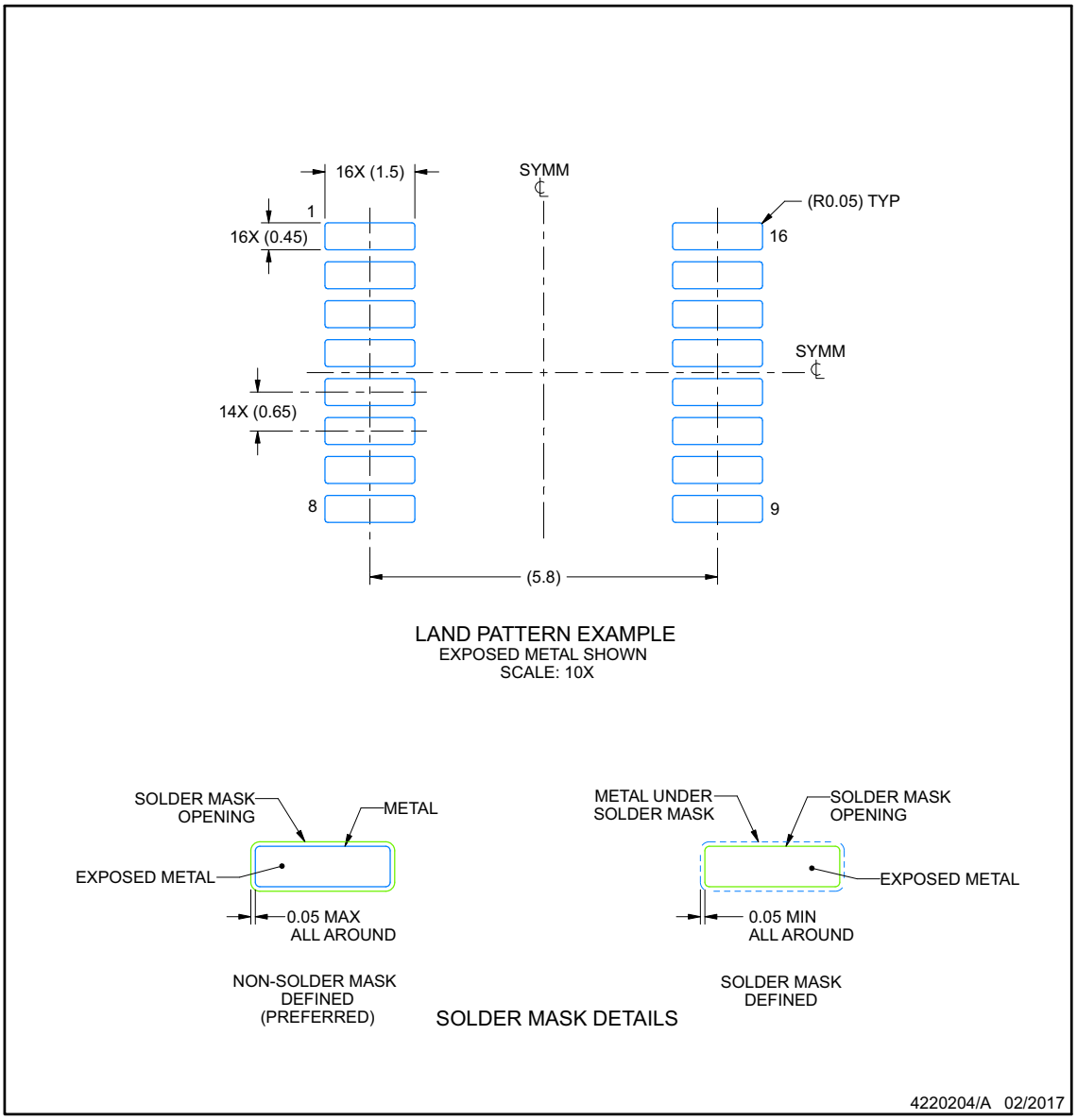
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

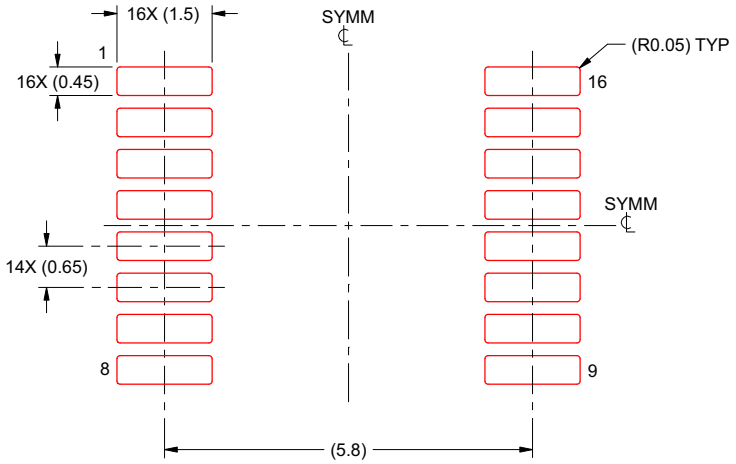
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PW0016A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

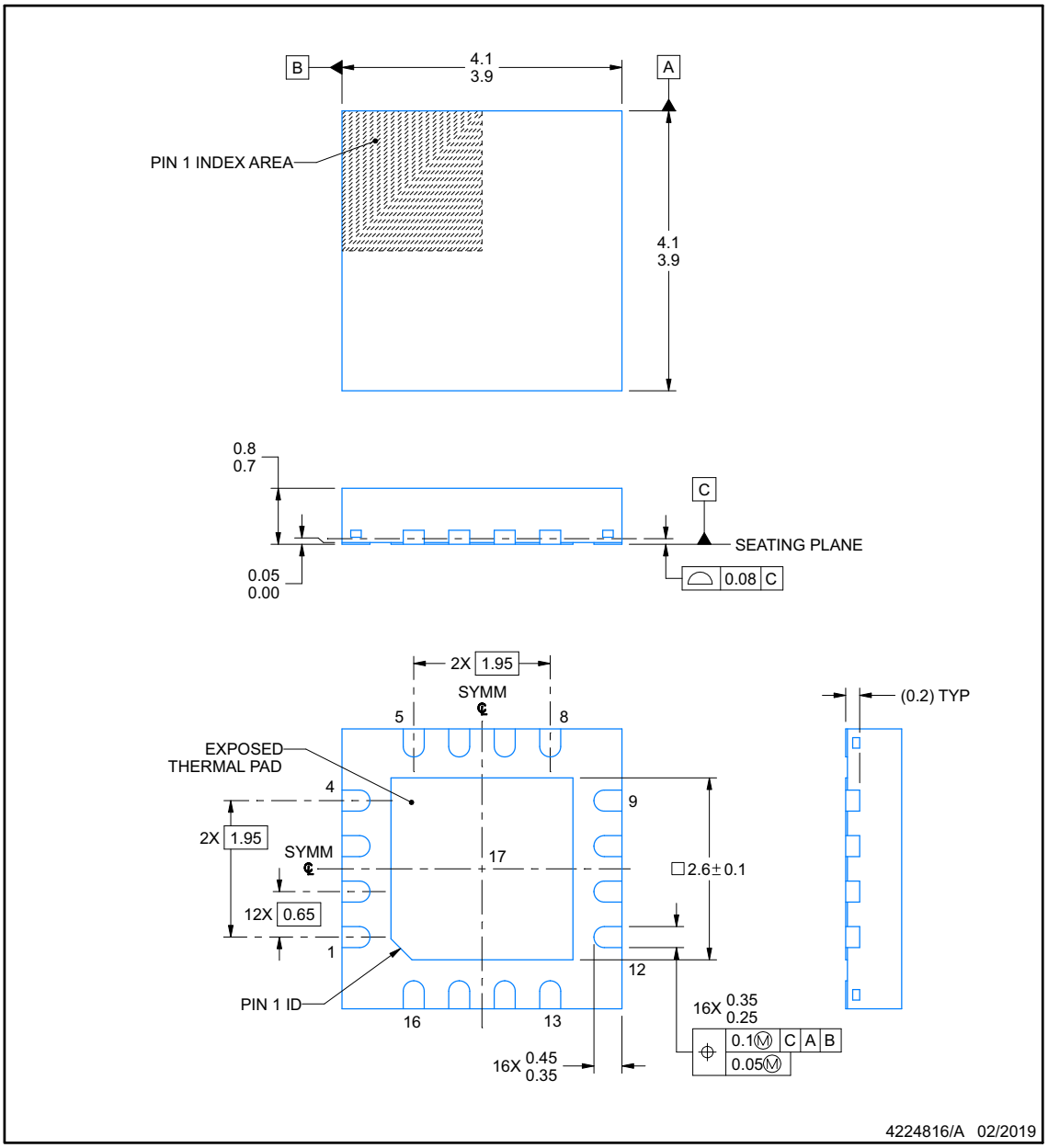
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RRP0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

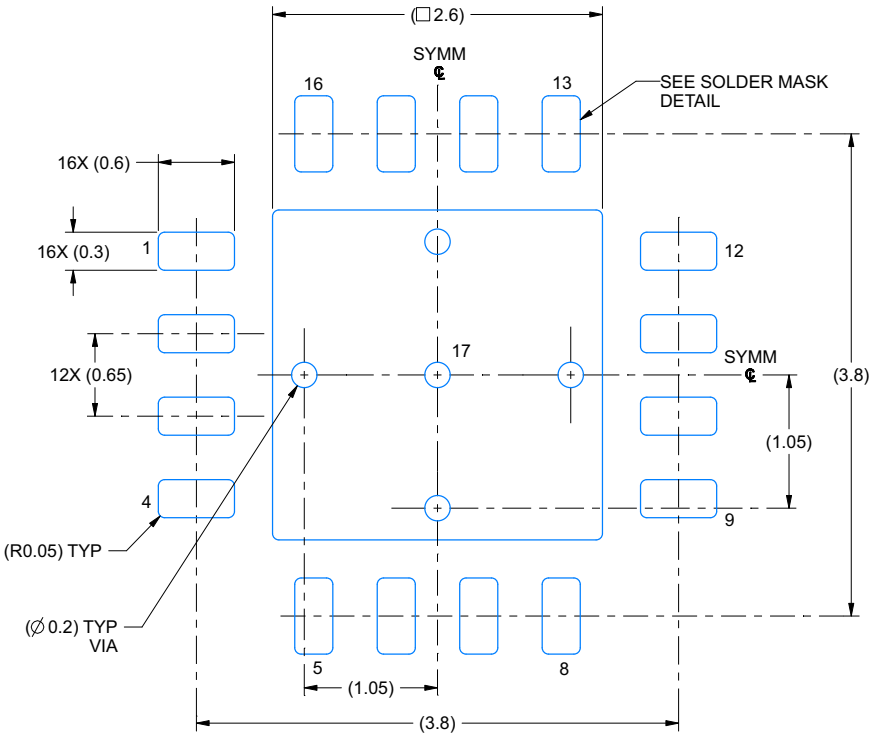
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

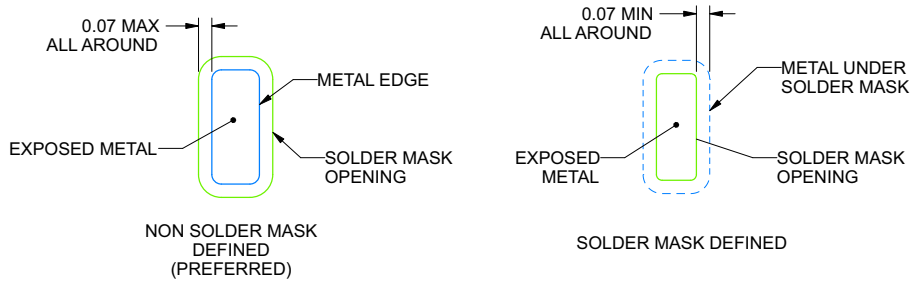
RRP0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224816/A 02/2019

NOTES: (continued)

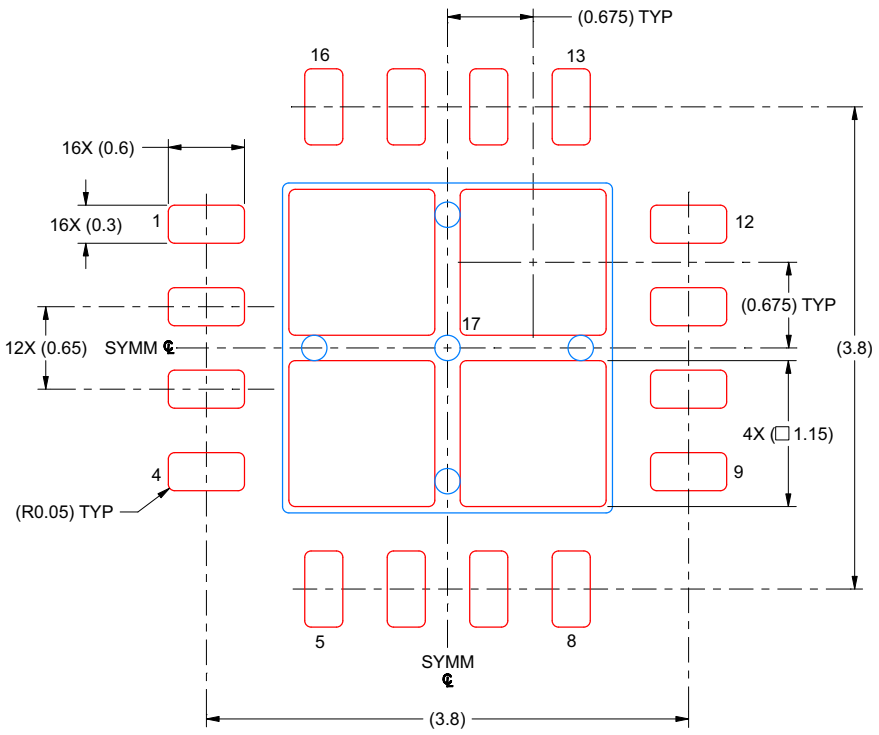
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RRP0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224816/A 02/2019

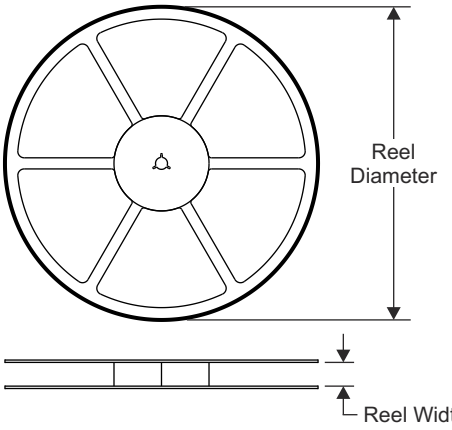
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

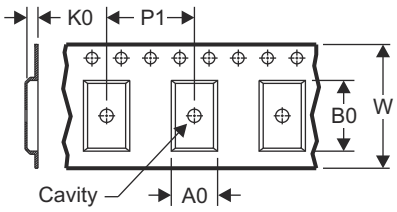
ADVANCE INFORMATION

13.1 Tape and Reel Information

REEL DIMENSIONS

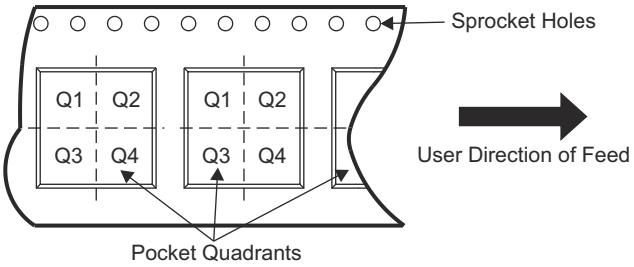


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

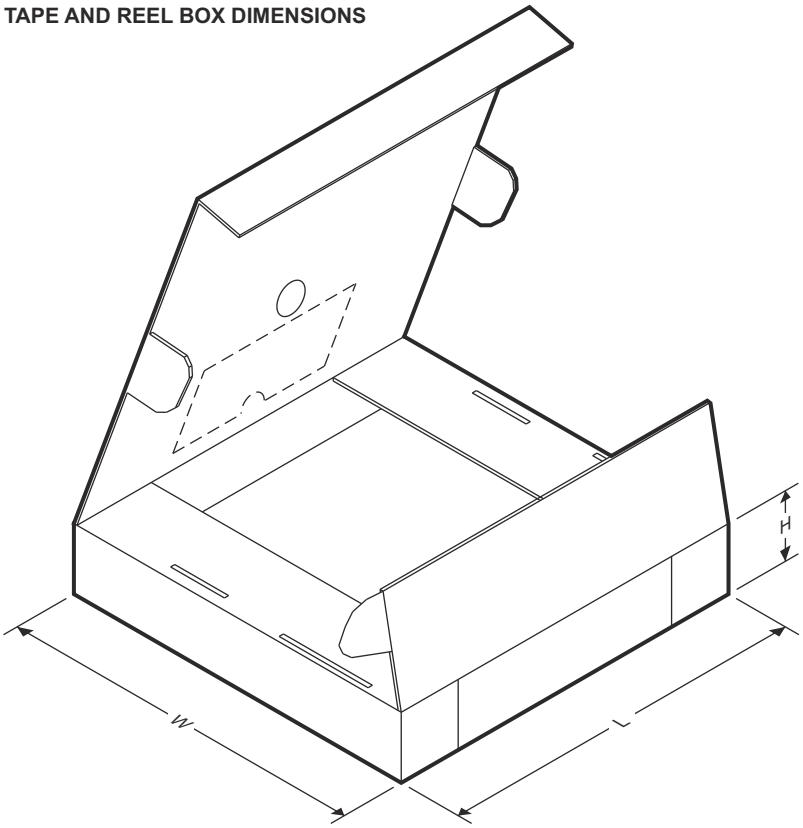
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7308FRRPR	WQFN	RRP	16	3000	330	12.4	4.25	4.25	1.15	8	12	Q2
TMUX7308FPWR	TSSOP	PW	16	2000	330	12.4	6.9	5.6	1.6	8	12	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7308FRRPR	WQFN	RRP	16	3000	367	367	35
TMUX7308FPWR	TSSOP	PW	16	2000	367	367	35

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX7308FRRPR	ACTIVE	WQFN	RRP	16	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265