带 1.8V 逻辑的 TMUX6208 36V、低导通电阻、8:1 精密多路复用器

1 特性

- 单电源电压范围：4.5V 至 36V
- 双电源电压范围：±4.5V 至 ±18V
- 低导通电阻：4 Ω
- 抗闩锁效应
- -40°C 至 +125°C 工作温度
- 1.8V 逻辑兼容输入
- 失效防护逻辑
- 轨到轨运行
- 双向信号路径
- 先断后合开关

2 应用

- 工厂自动化和控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- 半导体测试设备
- {9}电池测试设备{10}https://www.ti.com.cn/solution/cn/battery-test
- 超声波扫描仪
- 患者监护和诊断
- 光纤网络
- 光学测试设备
- 有线网络
- 数据采集系统 (DAQ)

3 说明

TMUX6208 是一款 8:1 精密单通道多路复用器，具有低导通电阻和电荷注入。TMUX6208 获取八个输入之一并将它连接到根据使能引脚和地址引脚的状态确定的共模输出。该器件支持单电源（±4.5V 至 ±36V）、双电源（±4.5V 至 18V）或非对称电源（例如，VDD =12V，VSS = –5V）。TMUX6208 可在源极 (Sx) 和漏极 (D) 引脚上支持从 V_{SS} 到 V_{DD} 范围的双向模拟和数字信号。

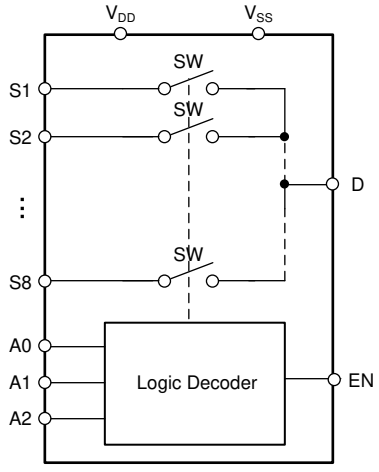
所有逻辑控制输入均支持 1.8V 到 V_{DD} 的逻辑高电平，因此，当器件在有效电源电压范围内运行时，可确保 TTL 和 CMOS 逻辑兼容性。Fail-Safe Logic 电路允许在电源引脚之前的控制引脚上施加电压，从而保护器件免受潜在的损害。

TMUX6208 是精密开关和多路复用器系列器件的一部分。这些器件具有非常低的导通和关断泄漏电流以及较低的电荷注入，因此可用于高精度测量应用。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
TMUX6208	TSSOP	5.00mm × 4.40mm
	WQFN	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



TMUX6208

简化框图

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
November 2020	*	Initial Release

5 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX6208	8:1, 1-Ch. multiplexer

6 Pin Configuration and Functions

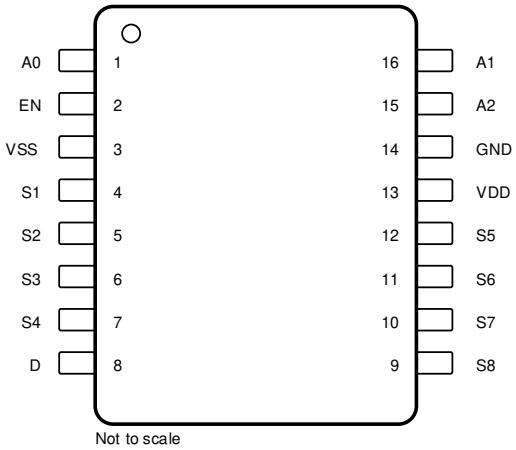


图 6-1. TMUX6208: PW Package 16-Pin TSSOP Top View

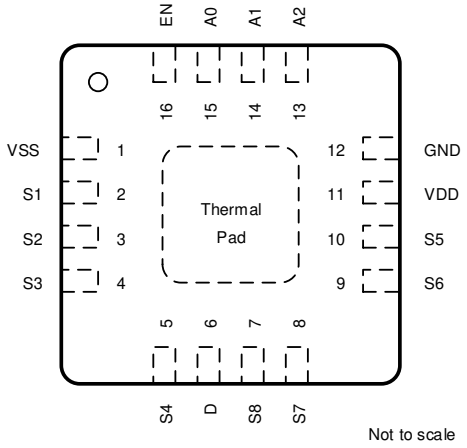


图 6-2. TMUX6208: RUM Package 16-Pin WQFN Top View

表 6-1. TMUX6208 Pin Functions

NAME	PW NO.	RUM NO.	TYPE	DESCRIPTION
A0	1	15	I	Logic control input.
EN	2	16	I	Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the Ax logic input determines which switch is turned on.
VSS	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μF to 10 μF between V_{SS} and GND.
S1	4	2	I/O	Source pin 1. Can be an input or output.
S2	5	3	I/O	Source pin 2. Can be an input or output.
S3	6	4	I/O	Source pin 3. Can be an input or output.
S4	7	5	I/O	Source pin 4. Can be an input or output.
D	8	6	I/O	Drain pin. Can be an input or output.
S8	9	7	I/O	Source pin 8. Can be an input or output.
S7	10	8	I/O	Source pin 7. Can be an input or output.
S6	11	9	I/O	Source pin 6. Can be an input or output.
S5	12	10	I/O	Source pin 5. Can be an input or output.
VDD	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μF to 10 μF between V_{DD} and GND.
GND	14	12	P	Ground (0 V) reference.
A2	15	13	I	Logic control input.
A1	16	14	I	Logic control input
Thermal Pad			—	The thermal pad is not connected internally. No requirement to solder this pad, if connected it is recommended that the pad be left floating or tied to GND.

ADVANCE INFORMATION

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
V_{DD} – V_{SS}	Power supply voltage differential		38	V
V_{DD}	Supply voltage	– 0.5	38	V
V_{SS}	Supply voltage	– 38	0.5	V
V_{SEL} or V_{EN}	Logic control input voltage (EN, Ax)	– 0.5	38	V
I_{SEL} or I_{EN}	Logic control input current (EN, Ax)	– 30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS} – 0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(4)	– 30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)	I_{DC} ± 10 %(5)		mA
T_A	Ambient temperature	– 55	135	°C
T_{stg}	Storage temperature	– 65	150	°C
T_J	Junction temperature		140	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(5) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC (1)		TMUX6208		UNIT
		PW (TSSOP)	RUM (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.5	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.9	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.0	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.4	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD} - V_{SS} (1)	Power supply voltage differential		4.5		36	V
V_{DD} (2)	Positive power supply voltage	Single supply	4.5		36	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)		V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage		0		36	V
T_A	Ambient temperature		–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 36 V, and the minimum V_{DD} is met.
(2) When V_{SS} = 0 V, V_{DD} can range from 4.5 V to 36 V.

7.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC})		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
PW (TSSOP)	±15 V Dual Supply	300	190	110	mA
	+12 V Single Supply	220	150	90	mA
	±5 V Dual Supply	210	140	90	mA
	+5 V Single Supply	170	110	70	mA

ADVANCE INFORMATION

ADVANCE INFORMATION

7.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = – 15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = – 15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		– 40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = – 10 V to +10 V I_D = – 10 mA	25°C		4	5.9	Ω
			– 40°C to +85°C			7.5	Ω
			– 40°C to +125°C			8.9	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = – 10 V to +10 V I_D = – 10 mA	25°C		0.1	0.5	Ω
			– 40°C to +85°C			0.75	Ω
			– 40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = – 10 V to +10 V I_S = – 10 mA	25°C		0.5	0.9	Ω
			– 40°C to +85°C			1.3	Ω
			– 40°C to +125°C			1.7	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = – 10 mA	– 40°C to +125°C		0.035		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = – 16.5 V Switch state is off V_S = +10 V / – 10 V V_D = – 10 V / + 10 V	25°C		0.02		nA
			– 40°C to +85°C		0.3		nA
			– 40°C to +125°C	– 5		5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = – 16.5 V Switch state is off V_S = +10 V / – 10 V V_D = – 10 V / + 10 V	25°C		0.04		nA
			– 40°C to +85°C		1		nA
			– 40°C to +125°C	– 25		25	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = – 16.5 V Switch state is on V_S = V_D = ±10 V	25°C		0.05		nA
			– 40°C to +85°C		1		nA
			– 40°C to +125°C	– 25		25	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		– 40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		– 40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		– 40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		– 40°C to +125°C	– 0.1	– 0.005		µA
C_{IN}	Logic input capacitance		– 40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = – 16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		35	57	µA
			– 40°C to +85°C			65	µA
			– 40°C to +125°C			80	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = – 16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		5	9	µA
			– 40°C to +85°C			10	µA
			– 40°C to +125°C			30	µA

(1) When V_S is positive, V_D is negative, and vice versa.
(2) When V_S is at a voltage potential, V_D is floating, and vice versa.

7.7 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = – 15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = – 15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		130	200	ns
			– 40°C to +85°C			220	ns
			– 40°C to +125°C			240	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		130	200	ns
			– 40°C to +85°C			220	ns
			– 40°C to +125°C			240	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		190	250	ns
			– 40°C to +85°C			260	ns
			– 40°C to +125°C			270	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		50		ns
			– 40°C to +85°C	1			ns
			– 40°C to +125°C	1			ns
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF	25°C		550		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF	25°C		– 5		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		– 85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		– 85		dB
BW	– 3dB Bandwidth	R_L = 50 Ω, C_L = 5 pF V_S = 0 V	25°C		33		MHz
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		15		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		125		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		180		pF

ADVANCE INFORMATION

ADVANCE INFORMATION

7.8 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		–40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA	25°C		6.8	11.5	Ω
			–40°C to +85°C			14.5	Ω
			–40°C to +125°C			17	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA	25°C		0.15	0.75	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.95	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA	25°C		1.9	3.5	Ω
			–40°C to +85°C			3.7	Ω
			–40°C to +125°C			4.4	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA	–40°C to +125°C		0.035		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C		0.02		nA
			–40°C to +85°C		0.3		nA
			–40°C to +125°C	–5		5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C		0.04		nA
			–40°C to +85°C		1		nA
			–40°C to +125°C	–25		25	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V	25°C		0.04		nA
			–40°C to +85°C		1		nA
			–40°C to +125°C	–25		25	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	μA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		μA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		33	50	μA
			–40°C to +85°C			55	μA
			–40°C to +125°C			65	μA

(1) When V_S is positive, V_D is negative, and vice versa.
(2) When V_S is at a voltage potential, V_D is floating, and vice versa.

7.9 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		130	210	ns
			–40°C to +85°C			250	ns
			–40°C to +125°C			285	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		130	210	ns
			–40°C to +85°C			250	ns
			–40°C to +125°C			285	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		200	300	ns
			–40°C to +85°C			330	ns
			–40°C to +125°C			350	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF	25°C		75		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF	25°C		900		ps
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 1 nF	25°C		–5		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–85		dB
BW	–3dB Bandwidth	R_L = 50 Ω, C_L = 5 pF V_S = 6 V	25°C		30		MHz
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		18		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		145		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		195		pF

ADVANCE INFORMATION

ADVANCE INFORMATION

7.10 ±5 V Dual Supply: Electrical Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = – 5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = – 5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		– 40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_{DD} = +4.5 V, V_{SS} = – 4.5 V V_S = – 4.5 V to +4.5 V I_D = – 10 mA	25°C		7.5	13.5	Ω
			– 40°C to +85°C			17	Ω
			– 40°C to +125°C			19	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = – 4.5 V to +4.5 V I_D = – 10 mA	25°C		0.25	0.7	Ω
			– 40°C to +85°C			0.85	Ω
			– 40°C to +125°C			0.95	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = – 4.5 V to +4.5 V I_D = – 10 mA	25°C		2.5	3.8	Ω
			– 40°C to +85°C			4.5	Ω
			– 40°C to +125°C			4.5	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = – 10 mA	– 40°C to +125°C		0.035		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Switch state is off V_S = +4.5 V / – 4.5 V V_D = – 4.5 V / + 4.5 V	25°C		0.02		nA
			– 40°C to +85°C		0.3		nA
			– 40°C to +125°C	– 5		5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Switch state is off V_S = +4.5 V / – 4.5 V V_D = – 4.5 V / + 4.5 V	25°C		0.04		nA
			– 40°C to +85°C		1		nA
			– 40°C to +125°C	– 20		20	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Switch state is on V_S = V_D = ±4.5 V	25°C		0.04		nA
			– 40°C to +85°C		1		nA
			– 40°C to +125°C	– 20		20	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		– 40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		– 40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		– 40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		– 40°C to +125°C	– 0.1	– 0.005		µA
C_{IN}	Logic input capacitance		– 40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		25	35	µA
			– 40°C to +85°C			45	µA
			– 40°C to +125°C			60	µA
I_{SS}	V_{SS} supply current	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		3	9	µA
			– 40°C to +85°C			10	µA
			– 40°C to +125°C			20	µA

(1) When V_S is positive, V_D is negative, and vice versa.
(2) When V_S is at a voltage potential, V_D is floating, and vice versa.

7.11 ±5 V Dual Supply: Switching Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = – 5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = – 5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 3 V R_L = 300 Ω, C_L = 35 pF	25°C		150	280	ns
			– 40°C to +85°C			310	ns
			– 40°C to +125°C			340	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF	25°C		150	280	ns
			– 40°C to +85°C			310	ns
			– 40°C to +125°C			340	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF	25°C		250	380	ns
			– 40°C to +85°C			400	ns
			– 40°C to +125°C			420	ns
t_{BBM}	Break-before-make time delay	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF	25°C		75		ns
			– 40°C to +85°C	1			ns
			– 40°C to +125°C	1			ns
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF	25°C		900		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF	25°C		– 5		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		– 85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		– 85		dB
BW	– 3dB Bandwidth	R_L = 50 Ω, C_L = 5 pF V_S = 0 V	25°C		30		MHz
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		19		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		150		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		200		pF

ADVANCE INFORMATION

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TMUX6208 is an 8:1, 1-channel multiplexer. Each input is turned on or turned off based on the state of the enable and address pins.

8.2 Functional Block Diagram

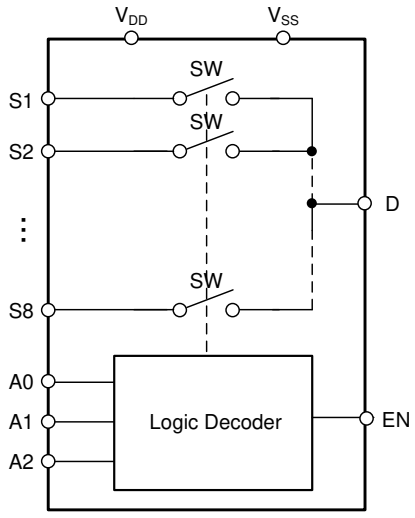


图 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Bidirectional Operation

TMUX6208 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input or output voltage for TMUX6208 ranges from V_{SS} to V_{DD}.

8.3.3 1.8 V Logic Compatible Inputs

TMUX6208 has 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

8.3.4 Fail-Safe Logic

TMUX6208 supports Fail-Safe Logic on the control input pins (EN and Ax) allowing it to operate up to 36 V, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the TMUX6208 logic input pins to ramp up to +36 V while V_{DD} and V_{SS} = 0 V. The logic control inputs are protected against positive faults of up to +36 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

8.4 Device Functional Modes

When the EN pin of the TMUX6208 is pulled high, one of the switches is closed based on the state of the Ax pin. When the EN pin is pulled low, all of the switches are in an open state regardless of the state of the Ax pin. The control pins can be as high as 36 V.

8.5 Truth Tables

表 8-1 shows the truth tables for the TMUX6208.

表 8-1. TMUX6208 Truth Table

EN	A2	A1	A0	Selected Source Connected To Drain (D) Pin
0	X(1)	X	X	All sources are off (HI-Z)
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1) X denotes *don't care*.

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX6208 is part of the precision switches and multiplexers family of devices. These devices operate with dual supplies (±4.5 V to ±18 V), a single supply (4.5 V to 36 V), or asymmetric supplies (such as VDD = 12 V, VSS = – 5 V), and offer true rail-to-rail input and output. The TMUX6208 offers low RON, low on and off leakage currents and ultra-low charge injection performance. These features makes the TMUX62xx a family of precision, robust, high-performance analog multiplexers for high-voltage, industrial applications.

9.2 Typical Application

One example to take advantage of TMUX6208 performance is the implementation of multiplexed data aquisition front end for multiple input sensors. Applications such as analog input modules for programmable logic controllers (PLCs), data aquisition (DAQ), and seminconducter test systems commonly need to monitor multiple signals into a single ADC channel. The multiple inputs can come from different system voltages being montitored, or environemental sensors such as temperature or humidity. Figure 9-1 shows a simplified example of monitoring multiple inputs into a single ADC using a multiplexer.

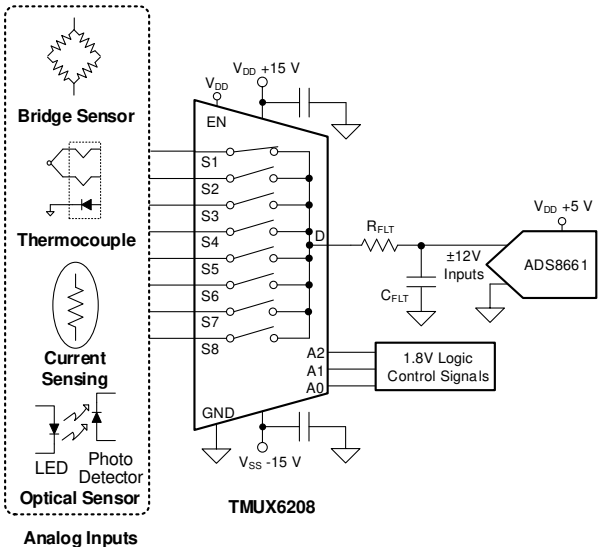


图 9-1. Multiplexed Data Aqcuisition Front End

9.3 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
Positive supply (VDD)	+15 V
Negative supply (V_{SS})	-15 V
Input / output signal range	-12 V to 12 V (limit of ADC)
Control logic thresholds	1.8 V compatible
Temperature range	-40°C to +125°C

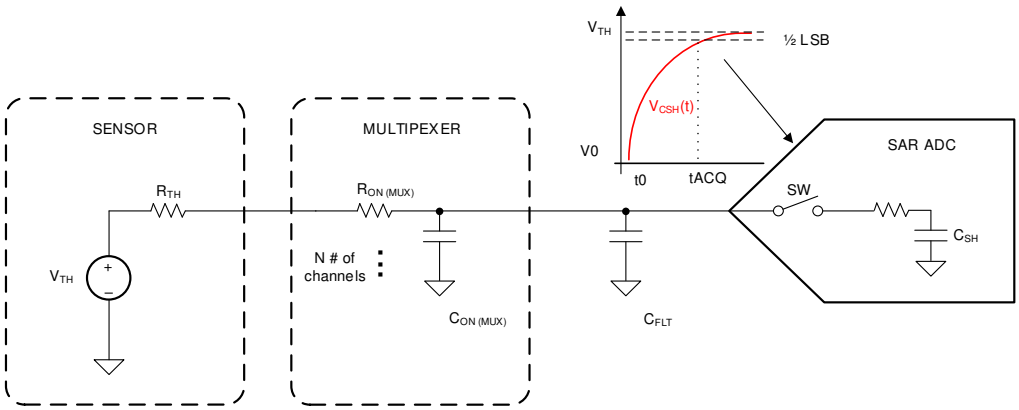
9.3.1 Detailed Design Procedure

The application shown in Figure 9-1 demonstrates how a multiplexer can be used to simplfy the signal chain and monitor multiple input signals to a signle ADC channel. In this example the ADC (ADS8661) has software programmable input ranges up to ±12.288 V. The ADC also has overvotlage protection up to ±20 V which allows for the multiplexer to be powered with wider supply voltages than the input signal range to maximize on-resistance performance of the multiplxer, while still maintaining system level overvotlage protection beyond the usuable signal range. Both the multiplexer and the ADC are capable of operation in extended industrial temperature range of -40°C to +125°C allowing for use in a wider array of industrial systems.

Many SAR ADCs have an analog input structure that consists of a sampling switch and a sampling capacitor. Many signal chains will have a driver amplifier to help charge the input of the ADC to meet a fast system aquisition time. However a driver amplifier is not always needed to drive SAR ADCs. Figure 9-2 shows a typical diagram of a sensor driving the SAR ADC input directly after being passed through the multiplxer. A filter capacitor (C_{FLT}) is connected to the input of the ADC to reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitor of the ADC.

The sensor block simplifies the device into a Thevenin equivalant voltage source (V_{TH}) and resistance (R_{TH}) which can be extracted from the device datasheets. Similarly the multixplexer can be thought of as a series resistance ($R_{ON(MUX)}$) and capacitance ($C_{ON(MUX)}$). To ensure maximum precison of the signal chain the system should be able to settle within 1/2 of an LSB within the acquisition time of the ADC. The time constant can be calculated as shown in the figure Figure 9-2. This equation highlights the importance of selecting a multiplexer with low on-resistance to further reduce the system time constant. Additionaly low charge injection performance of the multiplexer is helpful to reduce conversion errors and improve accuracy of the measurements.

ADVANCE INFORMATION



$t_{ACQ} > k \times \tau_{FLT}$

- $\tau_{FLT} = (R_{TH} + R_{ON\ (MUX)})\ X\ (C_{FLT} + C_{ON\ (MUX)})$
- k is single pole time constant for N bit ADC

图 9-2. Driving SAR ADC

10 Power Supply Recommendations

The TMUX6208 operates across a wide supply range of of ±4.5 V to ±18 V (4.5 V to 36 V in single-supply mode). The device also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = – 5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Always ensure the ground (GND) connection is established before supplies are ramped.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self – inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

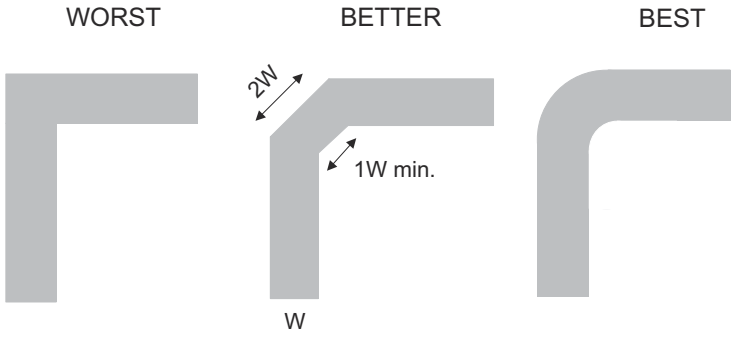


图 11-1. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

11.2 Layout Example

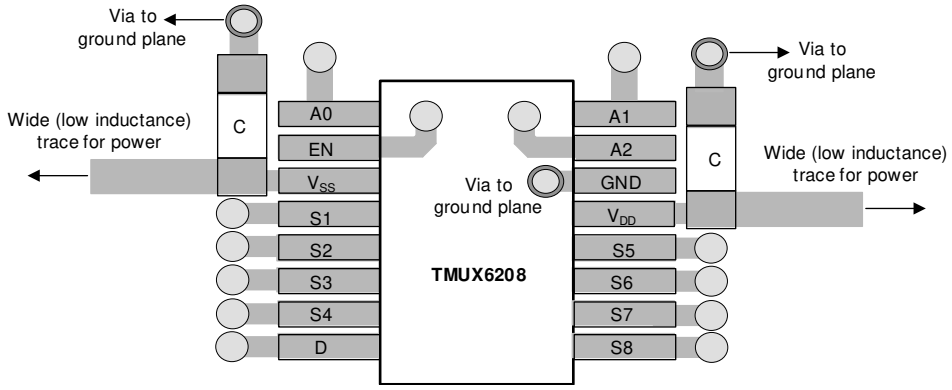


图 11-2. TMUX6208 Layout Example

图 11-2 illustrates an example of a PCB layout with the TMUX6208.

Some key considerations are:

- Decouple the supply pins with a 0.1-µF and 1-µF capacitor, placed lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible; only make perpendicular crossings when necessary.

ADVANCE INFORMATION

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.

Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit*.

Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.

Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.

Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

Texas Instruments, *QFN/SON PCB Attachment*.

Texas Instruments, *Quad Flatpack No-Lead Logic Packages*.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX6208PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X208	Samples
TMUX6209PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X209	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

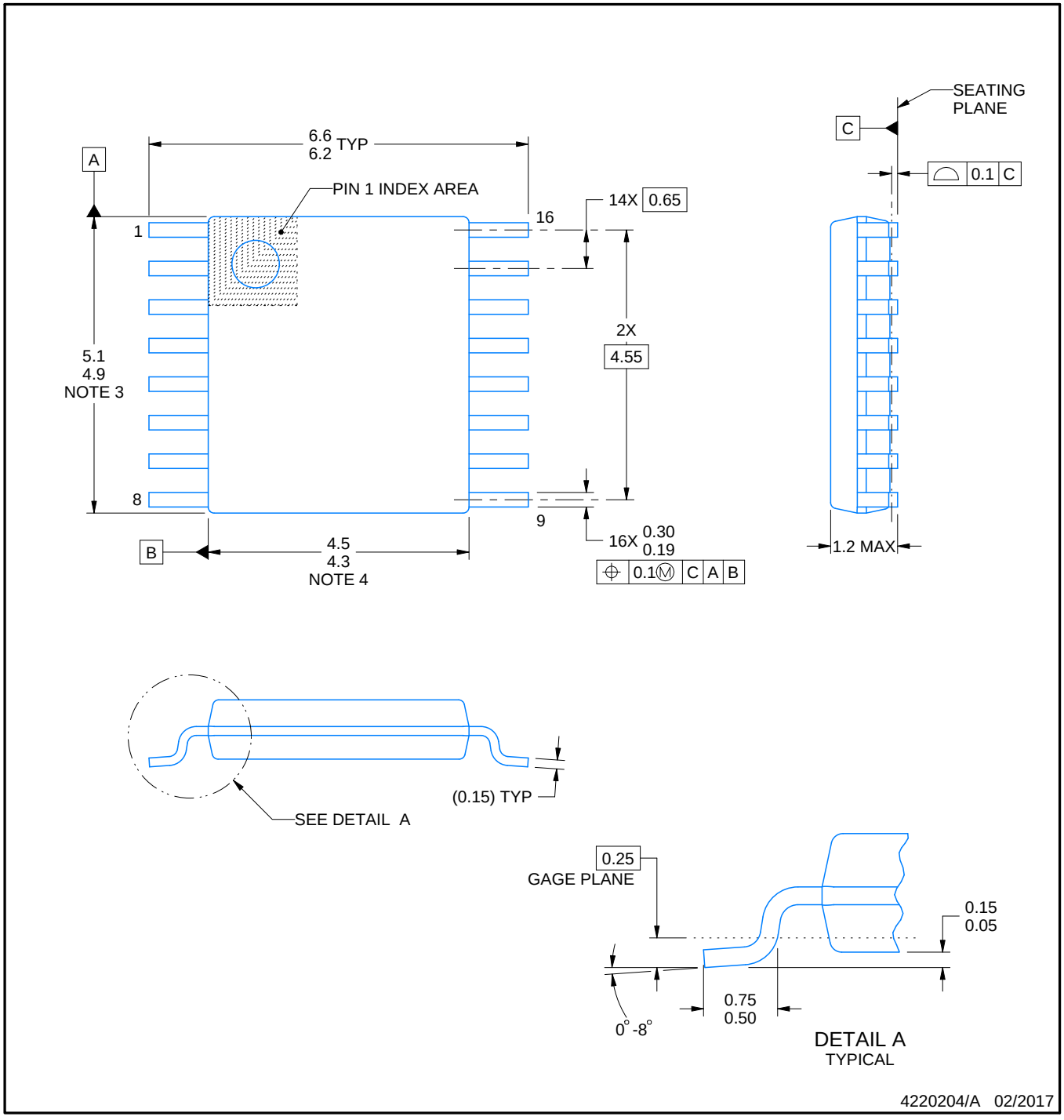
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PW0016A

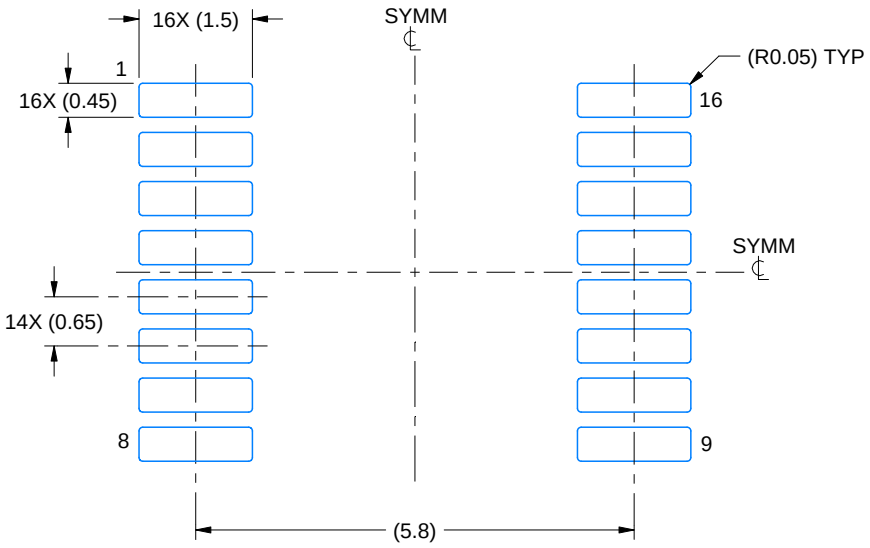
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

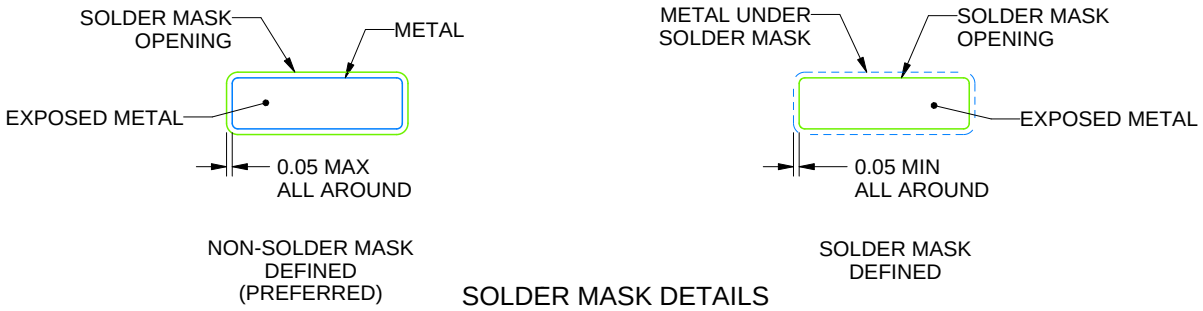


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

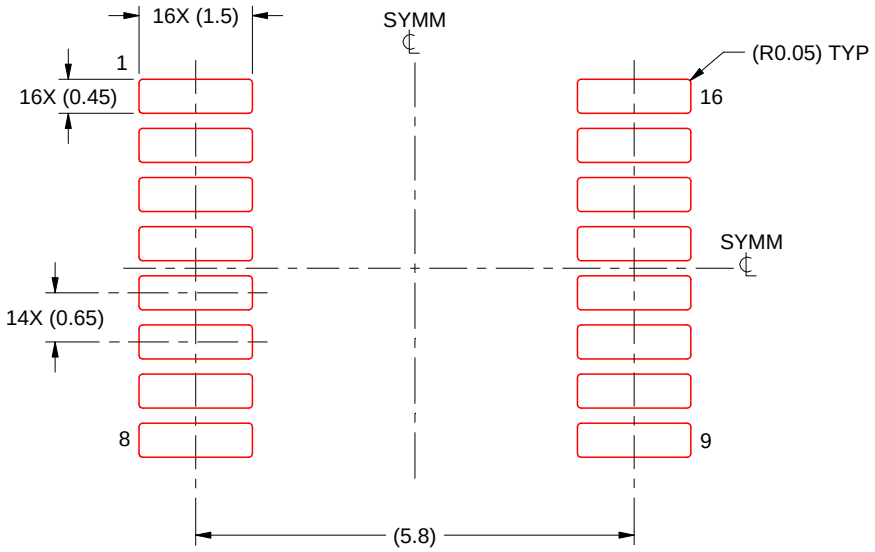


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122