TS3A24159 0.3Ω 双通道 SPDT 双向模拟开关
双通道 2:1 多路复用器和多路信号分离器

1 特性

- 指定的先断后合开关
- 低导通电阻（最大值为 0.3Ω）
- 低电荷注入
- 出色的导通状态电阻匹配
- 低总谐波失真 (THD)
- 1.65V 至 3.6V 单电源运行
- 控制输入兼容 1.8V 逻辑
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范
- 静电放电 (ESD) 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 手机
- 个人数字助理 (PDA)
- 便携式仪表
- 音频和视频信号路由
- 低压数据采集系统
- 通信电路
- 调制解调器
- 硬盘
- 计算机外设
- 无线终端和外设

3 说明

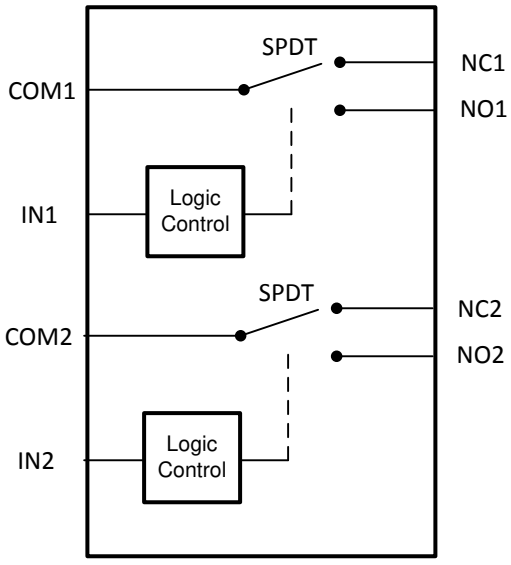
TS3A24159 器件是 2 通道单极双投 (SPDT) 双向模拟开关，设计的工作电压为 1.65V 至 3.6V。该器件提供低通态电阻和出色的通态电阻匹配以及先断后合功能，能够防止信号从一个通道传输至另一通道时失真。该器件具有出色的总谐波失真 (THD) 性能、低通态电阻和极低的功耗。由于具有这些 特性， 该器件适用于各种市场和不同 应用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS3A24159	VSSOP (10)	3.00mm × 3.00mm
	VSON (10)	3.00mm × 3.00mm
	DSBGA (10)	1.86mm × 1.35mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

功能方框图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (March 2019) to Revision F **Page**

- Changed the YZP package image view From: Top-Through View To: Bottom View 4

Changes from Revision D (July 2015) to Revision E **Page**

- Changed the YZP Package image and deleted the *YZP Package Terminal Assignments* table 4
- Changed Turnon time V_{CC} (Full) value From: 2.3 V to 2.7 V To: 2.7 V to 3.6 V in *Switching Characteristics for a 3-V Supply* 10
- Changed Turnon time V_{CC} (Full) value From: 2.3 V to 2.7 V To: 2.7 V to 3.6 V in *Switching Characteristics for a 2.5-V Supply* 10

Changes from Revision C (February 2008) to Revision D **Page**

- 已添加 添加了*引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分和*机械、封装和可订购信息* 部分 1
- 通篇将 V+ 更改为 V_{CC} 以符合 JEDEC 标准 1

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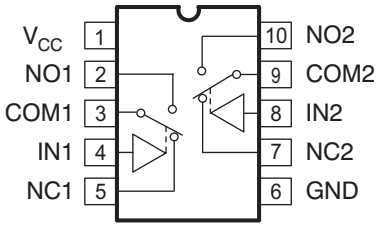
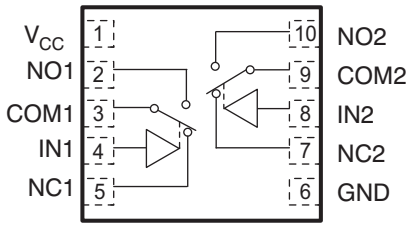
5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



DRC Package
10-Pin VSON
Top View



Pin Functions - VSSOP and VSON

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{CC}	—	Power Supply
2	NO1	I/O	Normally Open Signal Path
3	COM1	I/O	Common Signal Path
4	IN1	I	Digital Control to Connect COM to NO or NC
5	NC1	I/O	Normally Closed Signal Path
6	GND	—	Ground
7	NC2	I/O	Normally Closed Signal Path
8	IN2	I	Digital Control to Connect COM to NO or NC
9	COM2	I/O	Common Signal Path
10	NO2	I/O	Normally Open Signal Path

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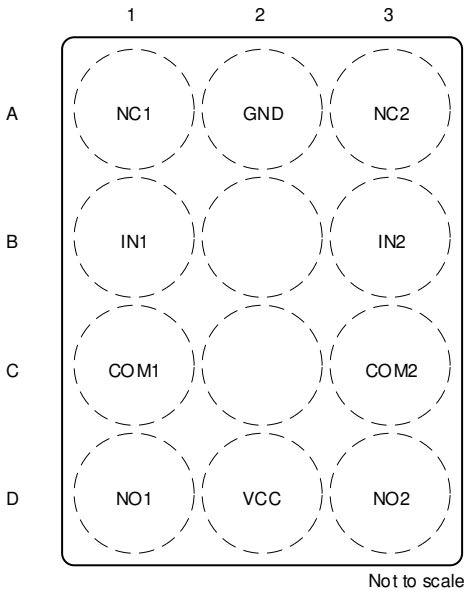
YZP Package
10-Pin DSBGA
Bottom View



Not to scale

Pin Functions - DSBGA

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	NC1	I/O	Normally Closed Signal Path
A2	GND	—	Ground
A3	NC2	I/O	Normally Closed Signal Path
B1	IN1	I	Digital Control to Connect COM to NO or NC
B3	IN2	I	Digital Control to Connect COM to NO or NC
C1	COM1	I/O	Common Signal Path
C3	COM2	I/O	Common Signal Path
D1	NO1	I/O	Normally Open Signal Path
D2	V_{CC}	—	Power Supply
D3	NO2	I/O	Normally Open Signal Path

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.5	3.6	V
V_{NC} V_{NO} V_{COM}	Signal voltage(3)(4)		–0.5	V_{CC} + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50	50	mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	–300	300	mA
	ON-state peak switch current(5)		–500	500	
V_{IN}	Digital input voltage		–0.5	3.6	V
I_{IK}	Digital input clamp current(3)	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) This value is limited to 5.5 V maximum.
(5) Pulse at 1-ms duration <10% duty cycle

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.6	V
V_{NC} V_{NO} V_{COM}	Signal Voltage	0	V_{CC}	V
V_{IN}	Digital Input Voltage	0	V_{CC}	V

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6.4 Thermal Information

THERMAL METRIC[1]		TS3A24159			UNIT
		DGS (VSSOP)	DRC (VSON)	YZP (DSBGA)	
		10 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154	49.4	90.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.9	71.2	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.6	23.8	8.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	2.2	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.2	23.8	8.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 3-V Supply

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.2	0.3	Ω
				Full				0.35	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.26	0.3	Ω
				Full				0.34	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.01	0.05	Ω
				Full				0.05	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.13		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C			0.01	0.04	Ω
				Full				0.05	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 11	25°C	3.6 V	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	3.6 V	–10		10	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch ON, See Figure 12	25°C	3.6 V	–10		10	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2)[2]									
Input logic high	V_{IH}			Full		1.4			V
Input logic low	V_{IL}			Full				0.5	V
Input leakage current	I_{IH}, I_{IL}	V_I = 3.6 V or 0		25°C	3.6 V	–40	5	40	nA
				Full		–50		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics for 3-V Supply (continued)

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 19	25°C	3 V		9		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 13	25°C	3 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	3 V		224		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	3 V		250		pF
Digital input capacitance	C_I	V_{IN} = V_{CC} or GND,	See Figure 13	25°C	3 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	3 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	3 V		–72		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	3 V		–96		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	3 V		0.003%		
SUPPLY									
Positive supply current	I_{CC}	V_{IN} = V_{CC} or GND		25°C	3.6 V		15	100	nA
				Full			1		µA

6.6 Electrical Characteristics for 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V			0.35	Ω
				Full				0.45	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V				Ω
				Full				0.4	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V		0.01	0.05	Ω
				Full			0.05	0.05	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V		0.05		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C			0.03	0.08	
				Full				0.1	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 11	25°C	2.7 V	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	2.7 V	–10		10	nA
				Full		–100		100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

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Electrical Characteristics for 2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH (continued)									
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.2 V,	Switch ON, See Figure 12	25°C	2.7 V	–10		10	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.25			V
Input logic low	V_{IL}			Full				0.5	V
Input leakage current	I_{IH}, I_{IL}	V_I = 2.7 V or 0		25°C	2.7 V	–40	5	40	nA
				Full		–50		50	
DYNAMIC									
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 19	25°C	2.5 V		8		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 13	25°C	2.5 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	2.5 V		250		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	2.5 V		250		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 13	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	2.5 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	2.5 V		–72		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	2.5 V		–96		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	2.5 V		0.003%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND		25°C	2.7 V		10	100	nA
				Full			700		

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.7 Electrical Characteristics for 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤V_{CC}, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.4	0.7	Ω
				Full				0.8	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.3	0.45	Ω
				Full				0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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Electrical Characteristics for 1.8-V Supply (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH (continued)									
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.02	0.04	Ω
				Full				0.05	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.13		Ω
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C			0.08	0.15	
				Full				0.2	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 11	25°C	1.95	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	1.95 V	–10		10	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V,	Switch ON, See Figure 12	25°C	1.95 V	–10		10	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2) (2)									
Input logic high	V_{IH}			Full		1			V
Input logic low	V_{IL}			Full				0.4	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or 0		25°C	1.95 V	–40	5	40	nA
				Full		–50		50	
DYNAMIC									
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 19	25°C	1.8 V		5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 13	25°C	1.8 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	1.8 V		250		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	1.8 V		250		pF
Digital input capacitance	C_{IN}	V_I = V_{CC} or GND,	See Figure 13	25°C	1.8 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	1.8 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	1.8 V		–73		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	1.8 V		–97		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	1.8 V		0.005%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND		25°C	1.95 V		100	50	nA
				Full				700	

(2) All unused digital inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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6.8 Switching Characteristics for a 3-V Supply

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See Figure 14	25°C	3.0 V		20	35	ns
				Full	2.7 V to 3.6 V			40	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See Figure 14	25°C	3.0 V		12	25	ns
				Full	2.7 V to 3.6 V			30	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See Figure 15	25°C	3.0 V	1	10	25	ns
				Full	2.7 V to 3.6 V	0.5		30	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

6.9 Switching Characteristics for a 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See Figure 14	25°C	2.5 V		23	45	ns
				Full	2.3 V to 2.7 V			50	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See Figure 14	25°C	2.5 V		17	27	ns
				Full	2.3 V to 2.7 V			30	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See Figure 15	25°C	2.5 V	2	14	30	ns
				Full	2.3 V to 2.7 V	1		35	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

6.10 Switching Characteristics for a 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See Figure 14	25°C	1.8 V		53	75	ns
				Full	1.65 V to 1.96 V			80	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See Figure 14	25°C	1.8 V		24	35	ns
				Full	1.65 V to 1.96 V			40	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See Figure 15	25°C	1.8 V	2	30	40	ns
				Full	1.65 V to 1.96 V	1		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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6.11 Typical Characteristics

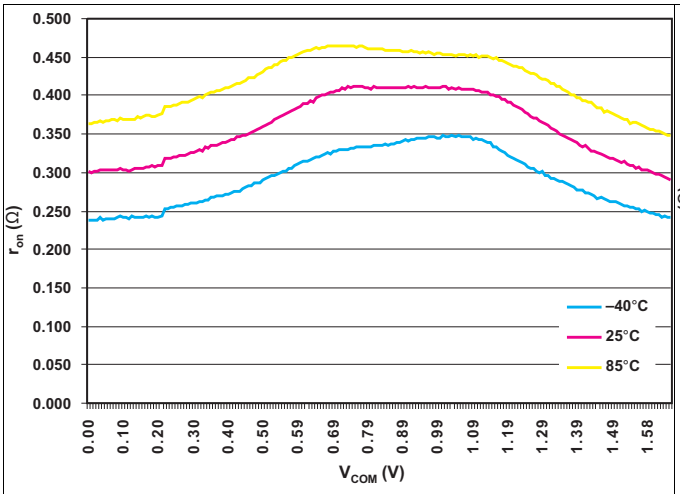

Figure 1. r_{on} vs V_{COM} (V_{CC} = 1.65 V)

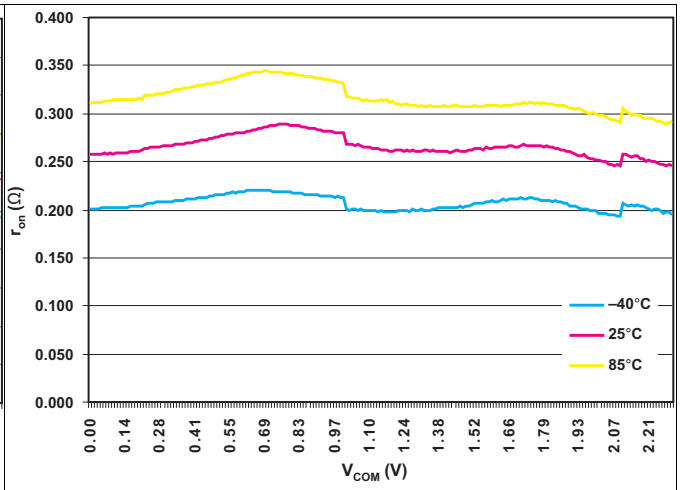

Figure 2. r_{on} vs V_{COM} (V_{CC} = 2.3 V)

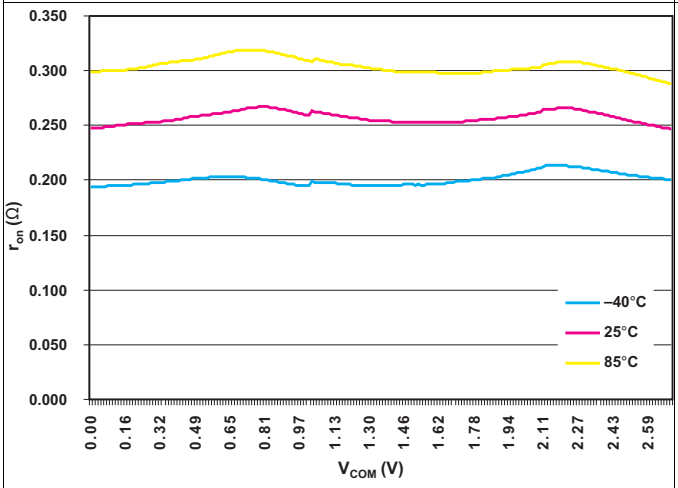

Figure 3. r_{on} vs V_{COM} (V_{CC} = 2.7 V)

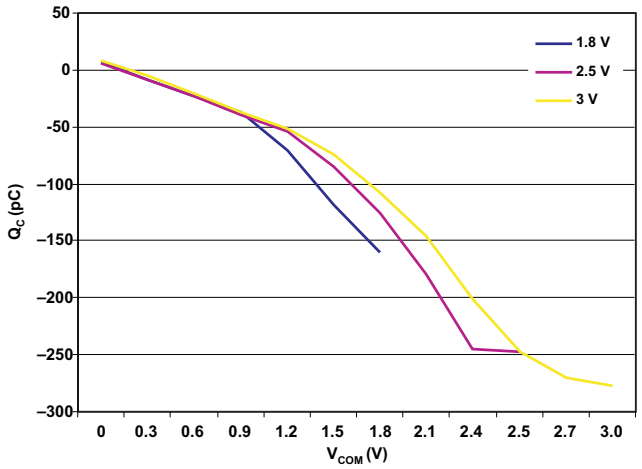

Figure 4. Charge Injection (Q_C) vs V_{COM} (T_A = 25°C)

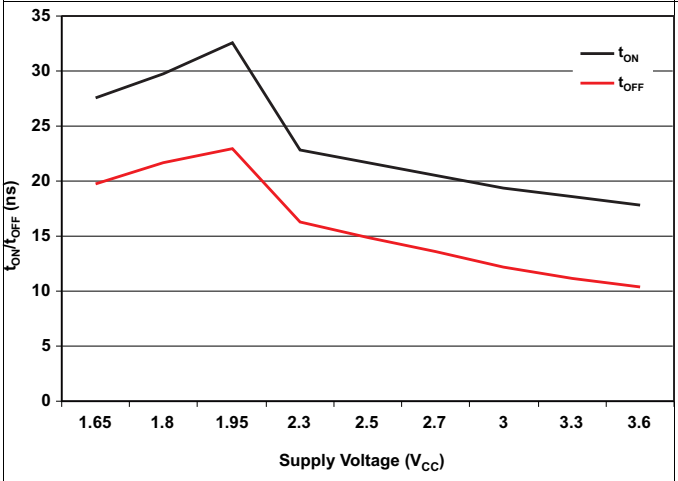

Figure 5. t_{ON} and t_{OFF} vs Supply Voltage (T_A = 25°C)

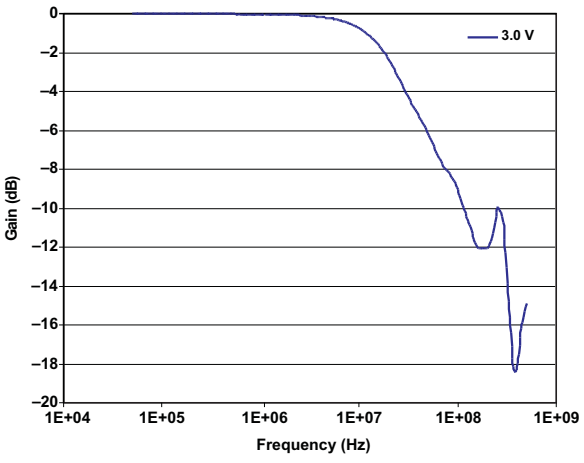

Figure 6. Bandwidth

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Typical Characteristics (continued)

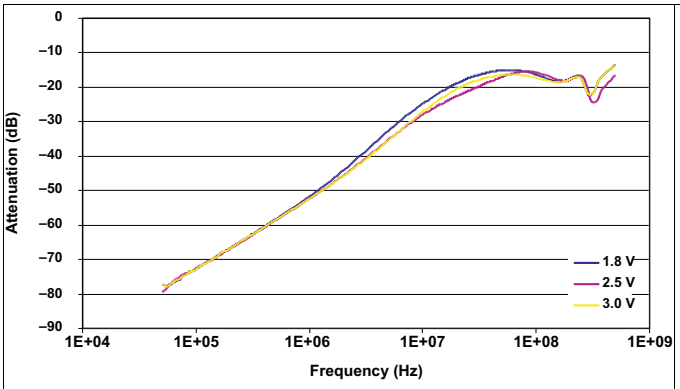

Figure 7. OFF Isolation

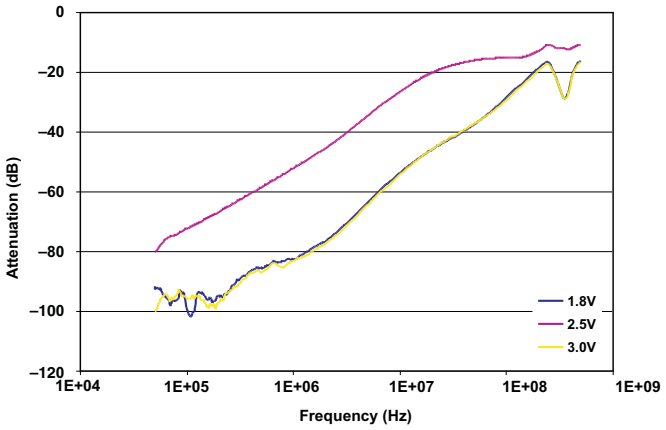

Figure 8. Crosstalk

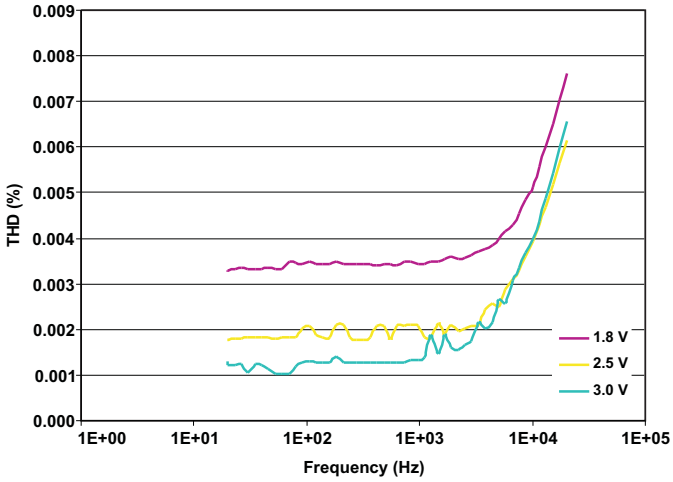

Figure 9. Total Harmonic Distortion vs Frequency

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7 Parameter Measurement Information

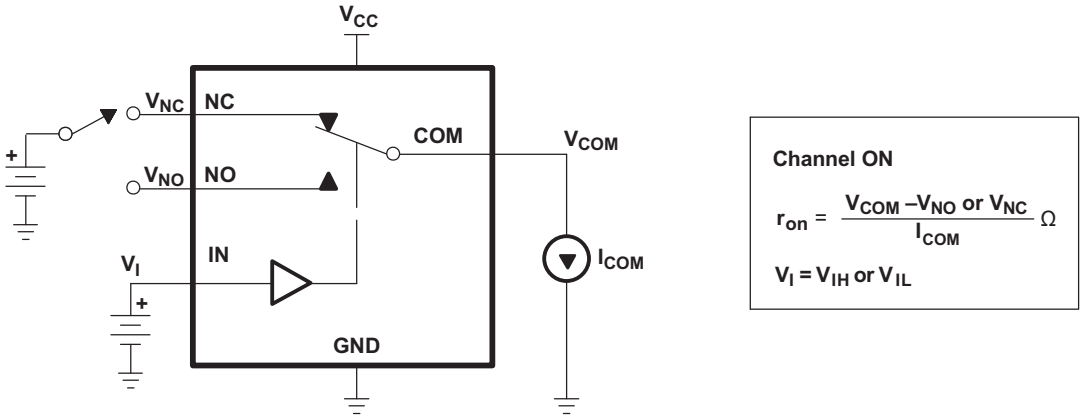

Figure 10. ON-State Resistance

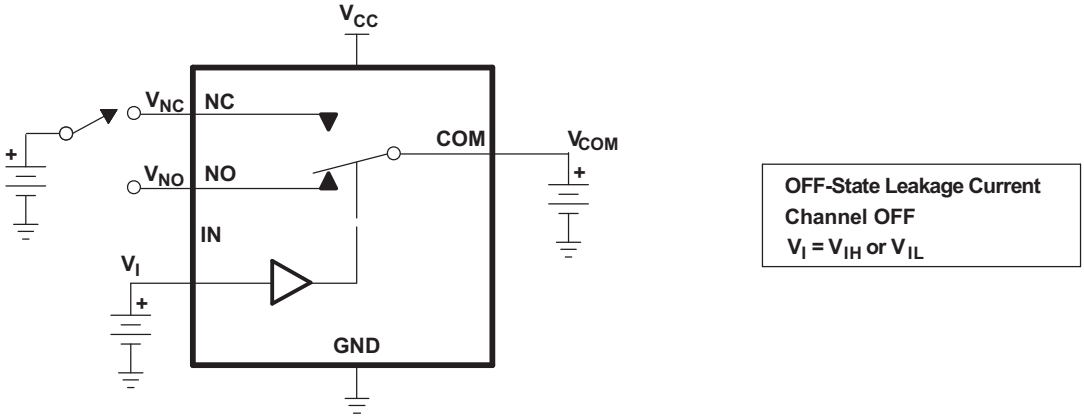

Figure 11. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

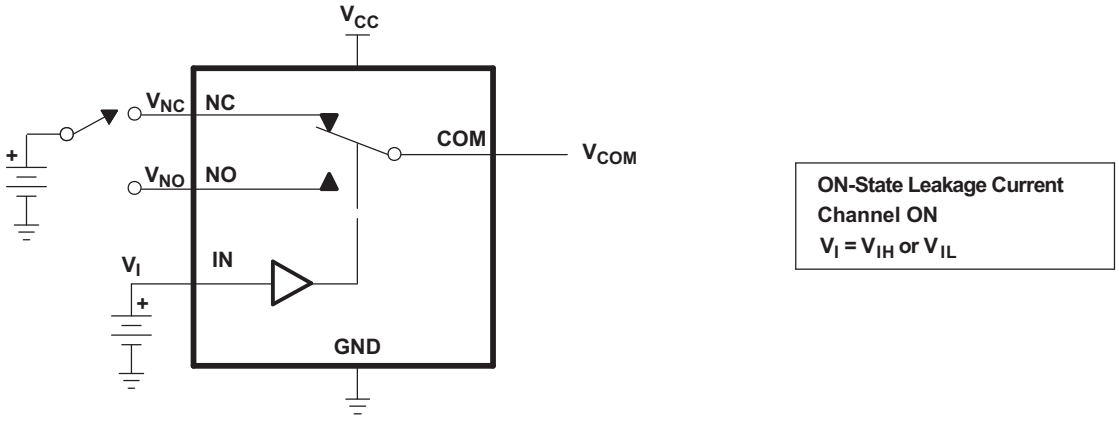

Figure 12. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

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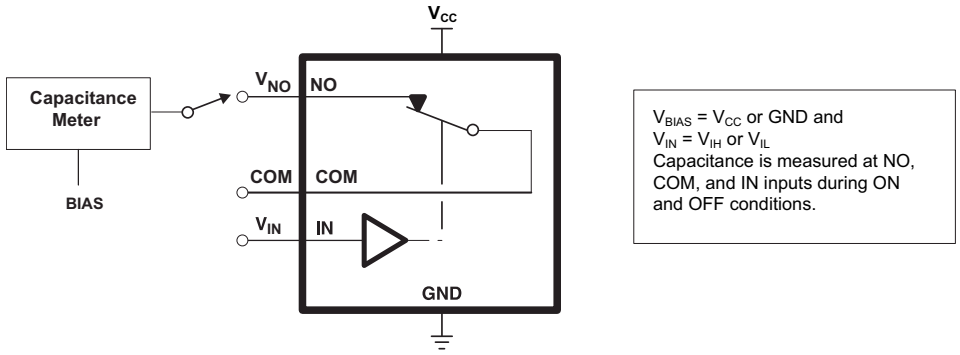
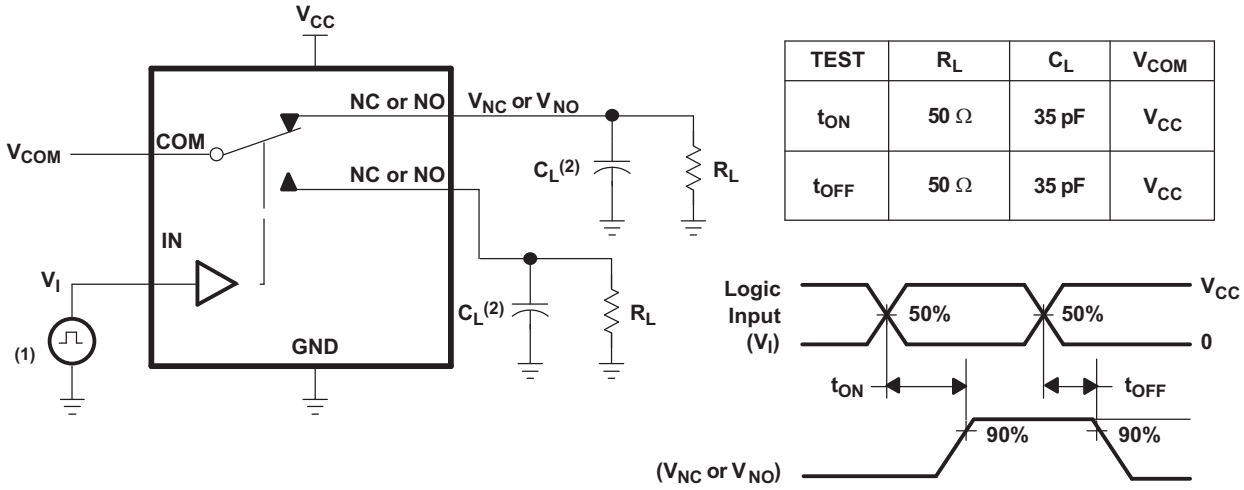


Figure 13. Capacitance C_I, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

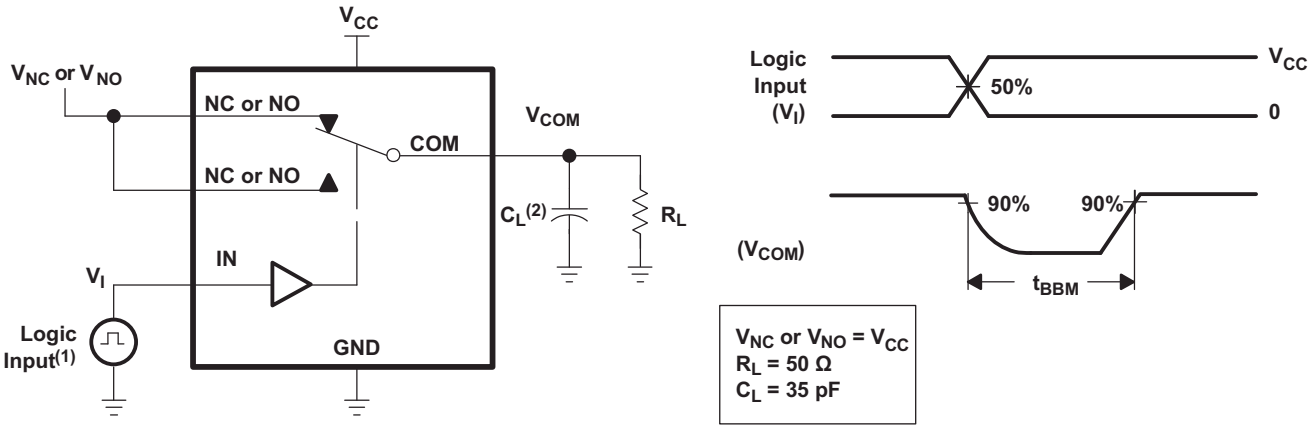


TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{CC}
t_{OFF}	50 Ω	35 pF	V_{CC}

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 14. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 15. Break-Before-Make Time (t_{BBM})

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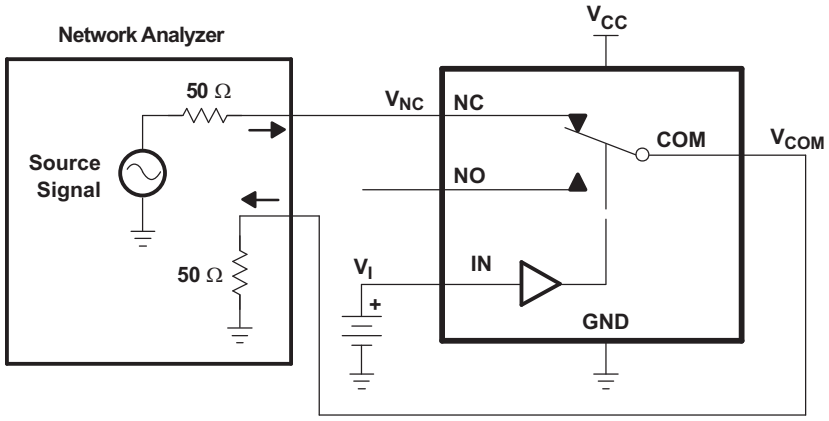


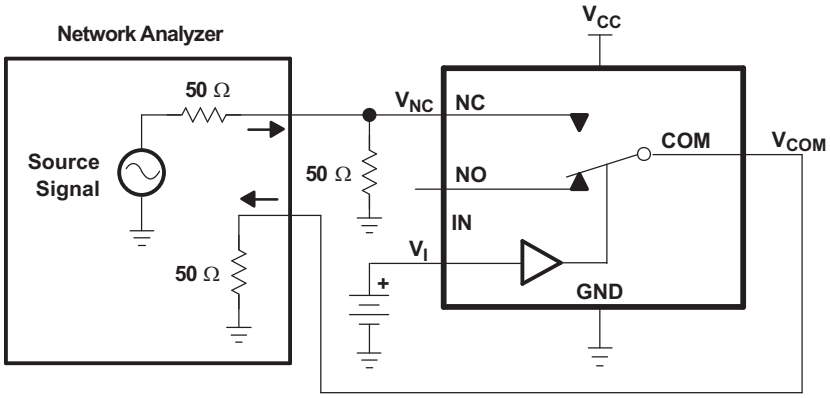
Channel ON: NC to COM
$V_I = V_{CC}$ or GND

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 16. Bandwidth (BW)



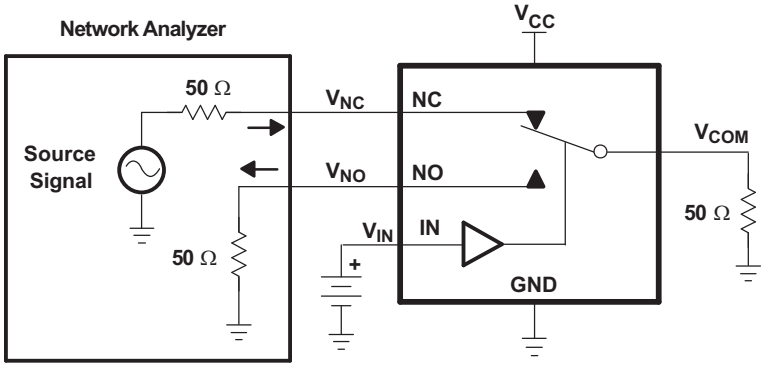
Channel OFF: NC to COM
$V_I = V_{CC}$ or GND

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 17. OFF Isolation (O_{ISO})



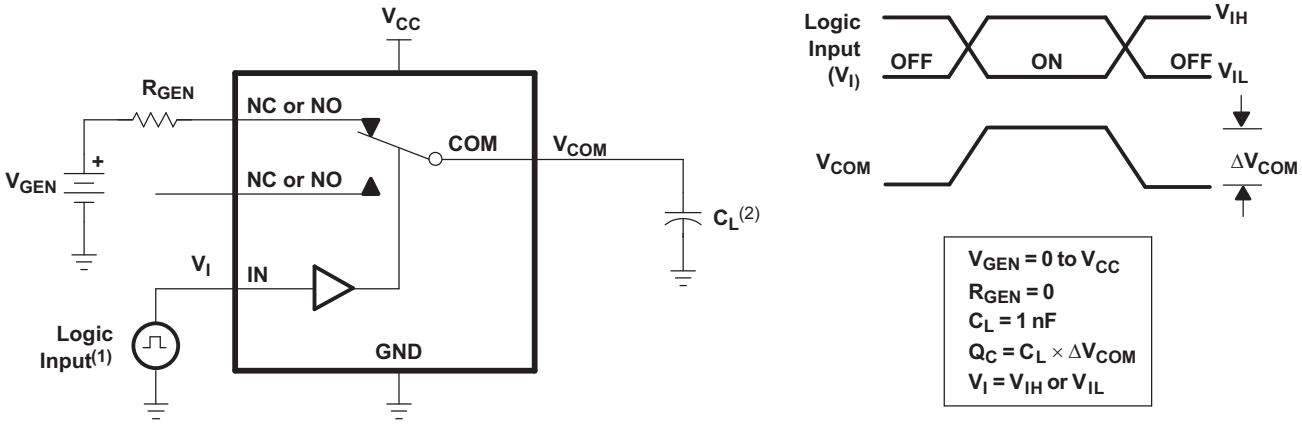
Channel ON: NC to COM
Channel OFF: NO to COM
$V_{IN} = V_{CC}$ or GND

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

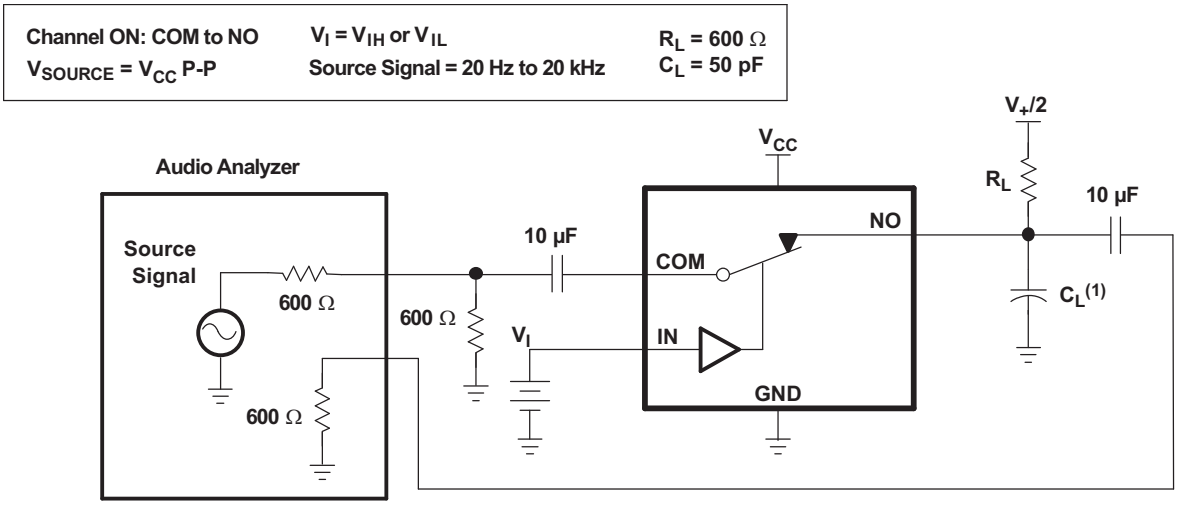
Figure 18. Crosstalk (X_{TALK})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 19. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

Figure 20. Total Harmonic Distortion (THD)

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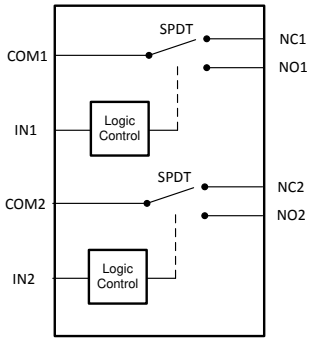
8 Detailed Description

8.1 Overview

The TS3A24159 is a 2-channel single-pole double-throw (SPDT) bidirectional analog switch that is designed to operate from 1.65 V to 3.6 V. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance, low ON-state resistence, and consumes very low power. These are some of the features make this device suitable for a variety of markets and many different applications.

8.2 Functional Block Diagram



8.3 Feature Description

The TS3A24159 device is bidirectional with two single-pole, double-throw switches. Each of the two switches are controlled independently by two digital signals.

8.4 Device Functional Modes

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

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9 Application and Implementation

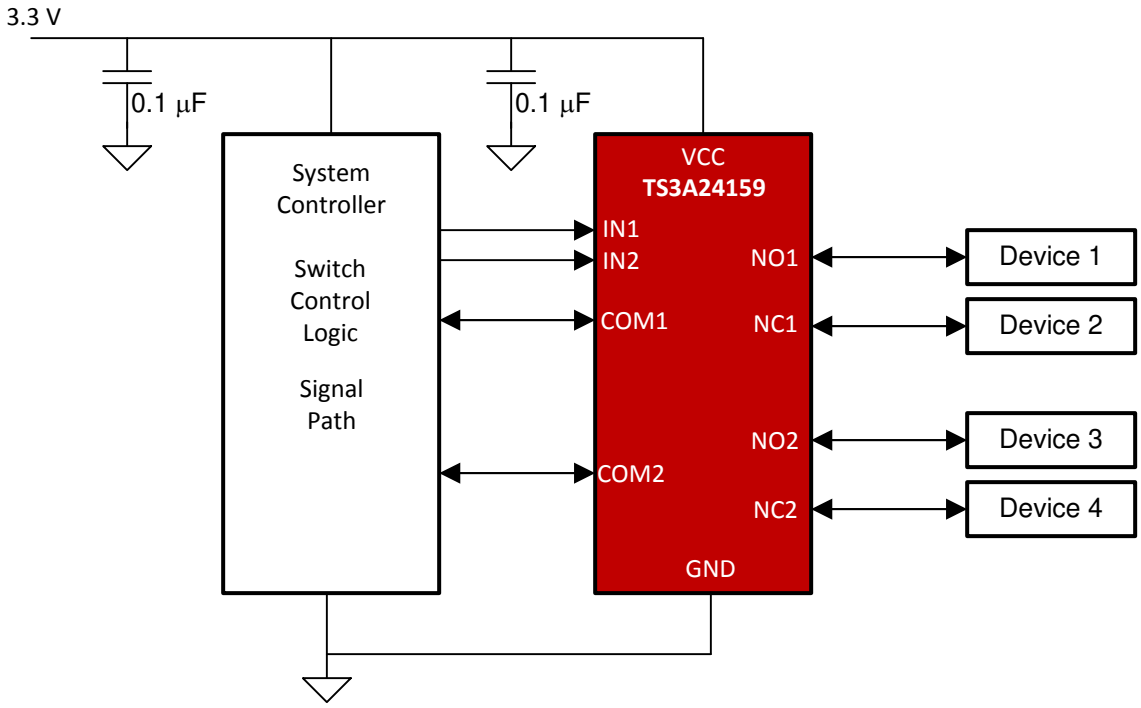
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The switch of the TS3A23159 device is bidirectional. Hence, NO, NC and COM pins can be used as both inputs or outputs.

9.2 Typical Application



9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are with in the specified ranges to ensure proper performance.

Table 2. Design Parameters

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.6	V
V_{NC} V_{NO} V_{COM}	Signal Voltage	0	V_{CC}	V
V_{IN}	Digital Input Voltage	0	V_{CC}	V

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9.2.2 Detailed Design Procedure

The TS3A23159 device can be properly operated without any external components. However, it is recommended that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. It is also recommended that the digital control pins (IN1 and IN2) be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin.

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS3A23159 input/output signal swing through NO and COM are dependant of the supply voltage VCC.

9.2.3 Application Curve

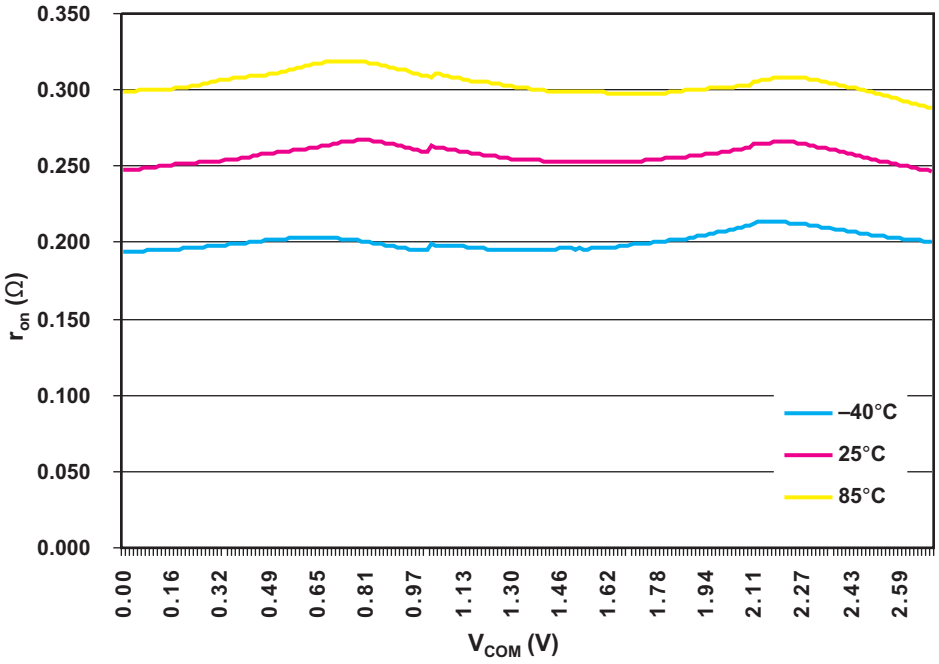

Figure 21. r_{ON} vs V_{COM}

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10 Power Supply Recommendations

- Proper power-supply sequencing is recommended for all CMOS devices.
- Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device.
- Always sequence VCC on first, followed by NO or COM.
- Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components.
- A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended. Bypass capacitors must be used on power supplies. Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example

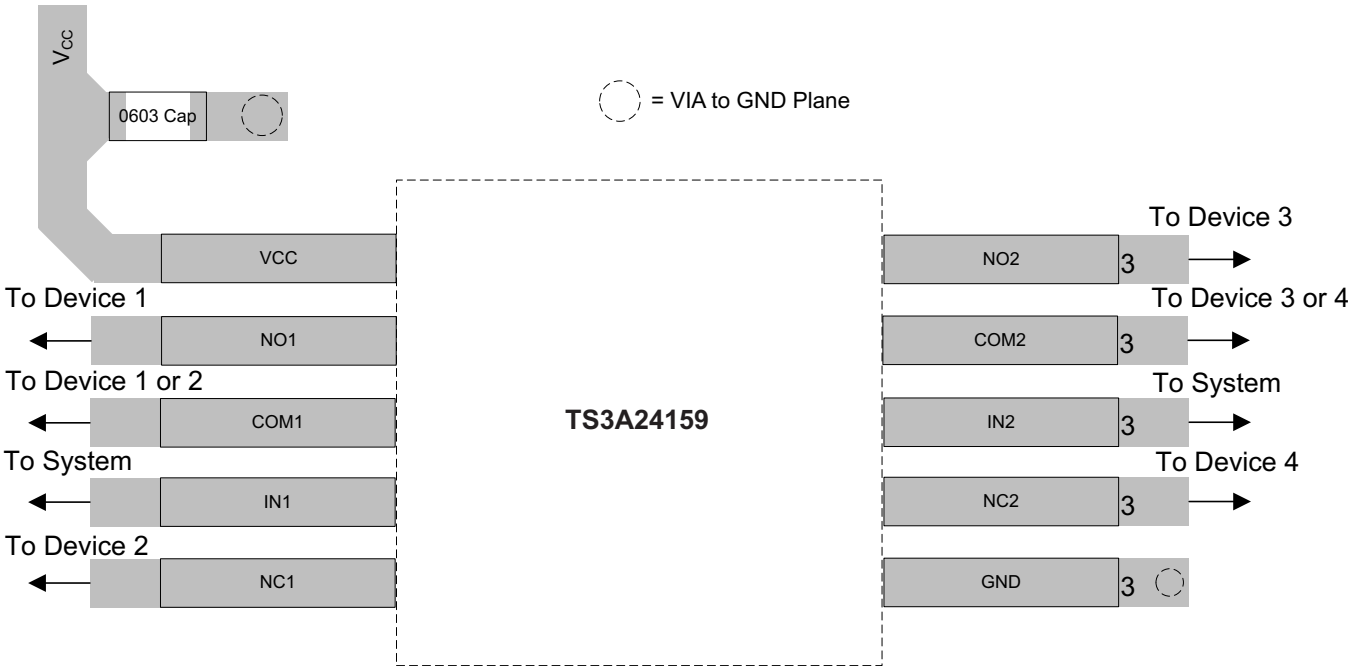

Figure 22. Layout Example

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

如需相关文档，请参阅以下资源：*《慢速或浮点 CMOS 输入的影响》*(SCBA004)。

12.2 社区资源

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A24159DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L8Q, L8R)	Samples
TS3A24159DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L8Q, L8R)	Samples
TS3A24159DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWS	Samples
TS3A24159DRCRG4	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWS	Samples
TS3A24159YZPR	ACTIVE	DSBGA	YZP	10	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	L87	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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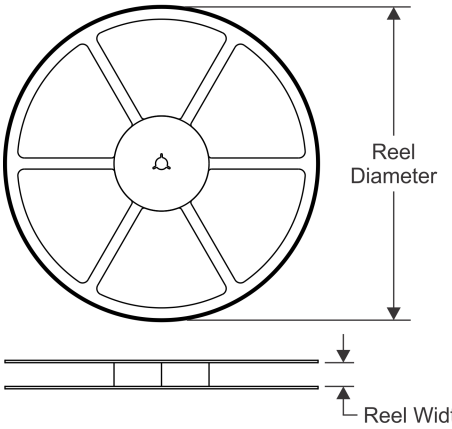
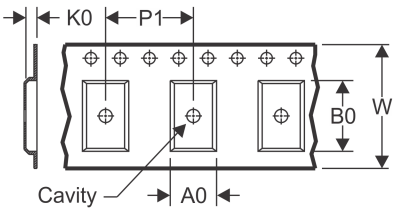
TAPE AND REEL INFORMATION

REEL DIMENSIONS

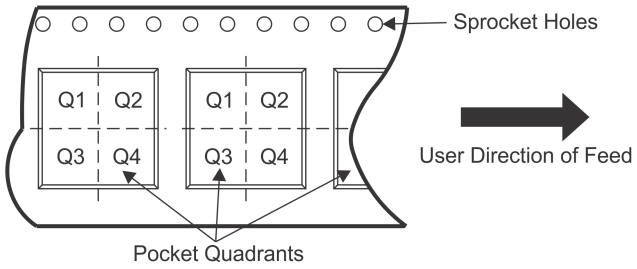


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

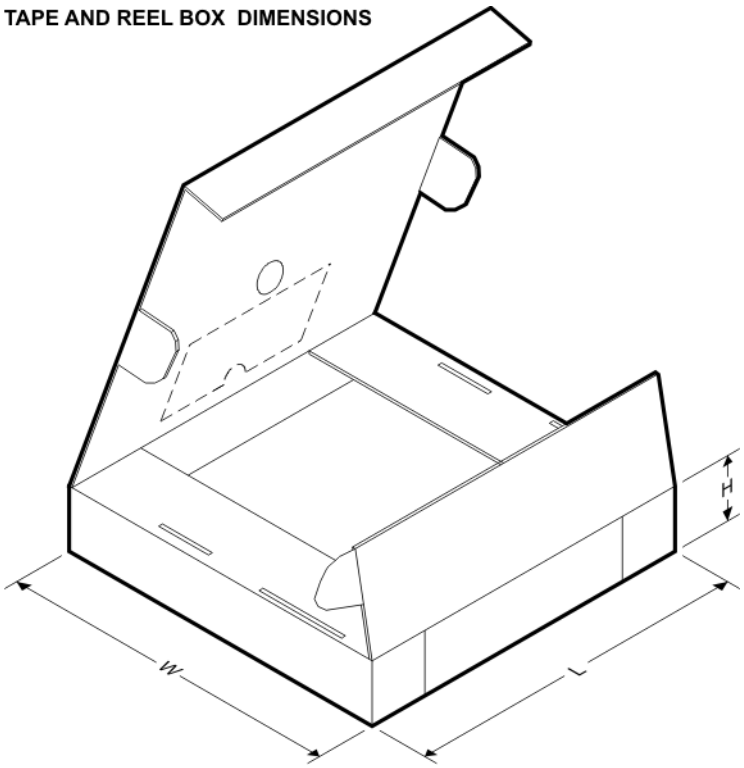
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

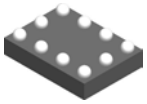
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A24159DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS3A24159DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3A24159YZPR	DSBGA	YZP	10	3000	178.0	9.2	1.49	1.99	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A24159DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS3A24159DRCR	VSON	DRC	10	3000	853.0	449.0	35.0
TS3A24159YZPR	DSBGA	YZP	10	3000	220.0	220.0	35.0

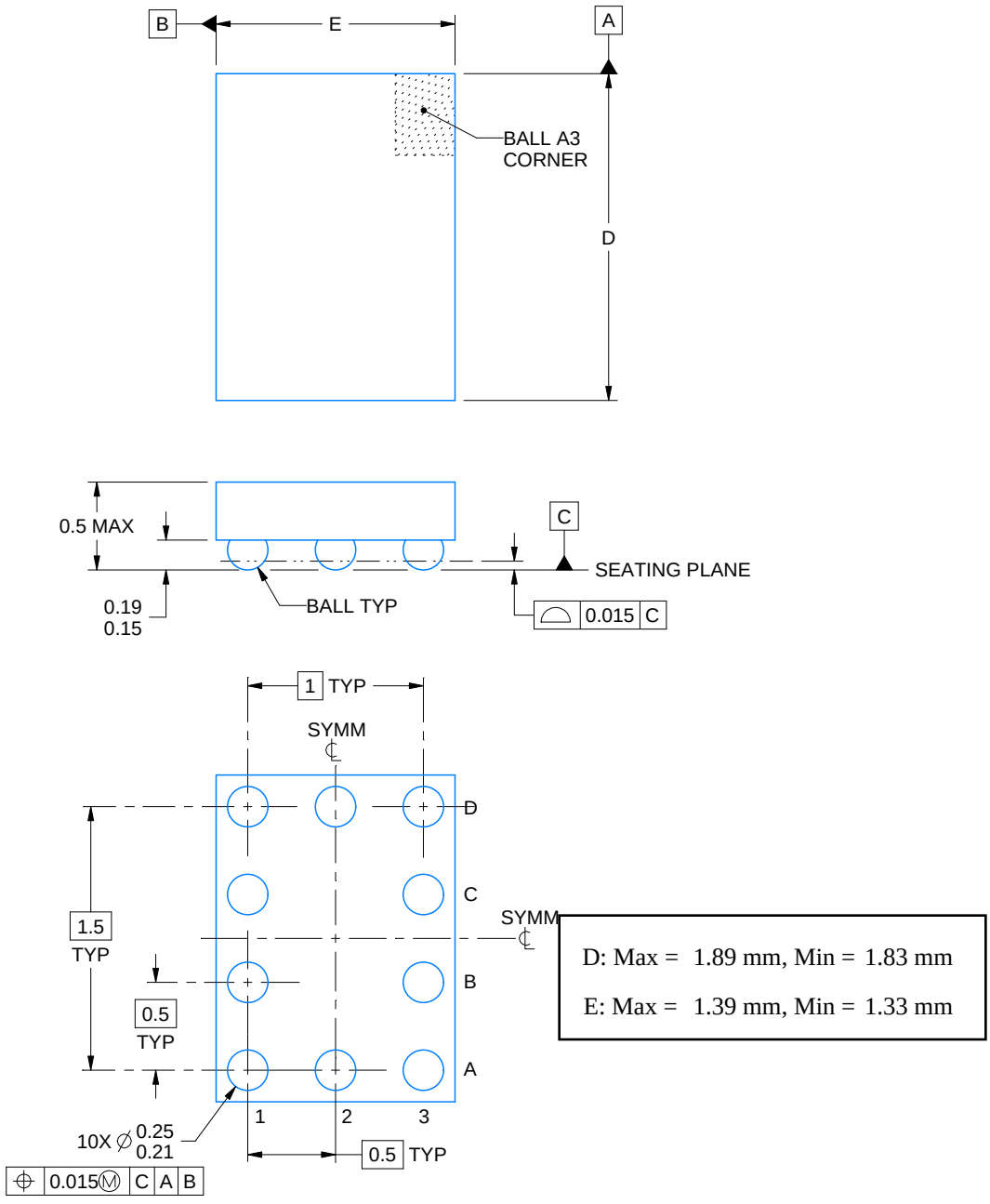


PACKAGE OUTLINE

YZP0010

DSBGA - 0.5 mm max height

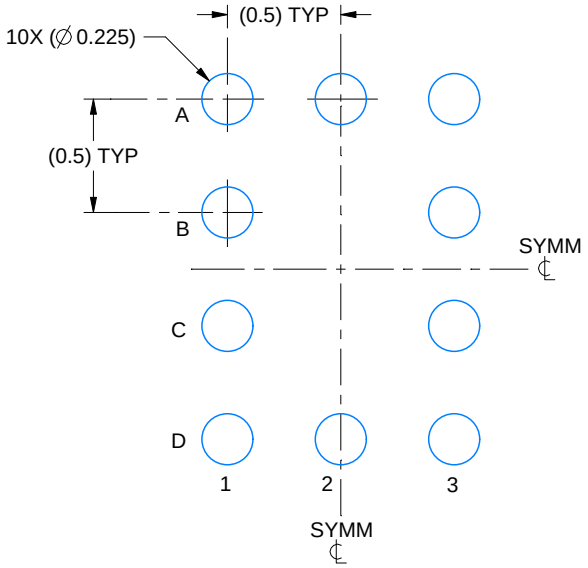
DIE SIZE BALL GRID ARRAY



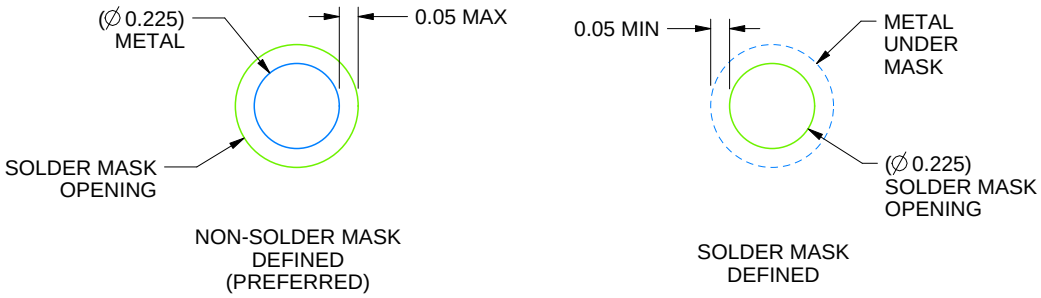
4219350/B 11/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4219350/B 11/2017

NOTES: (continued)

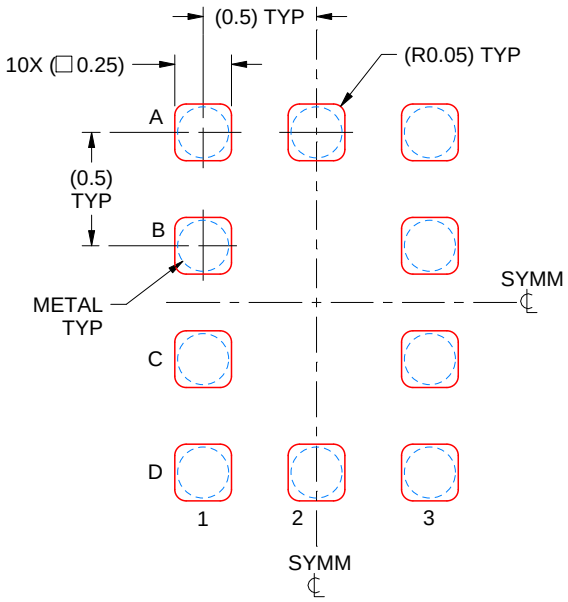
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219350/B 11/2017

NOTES: (continued)

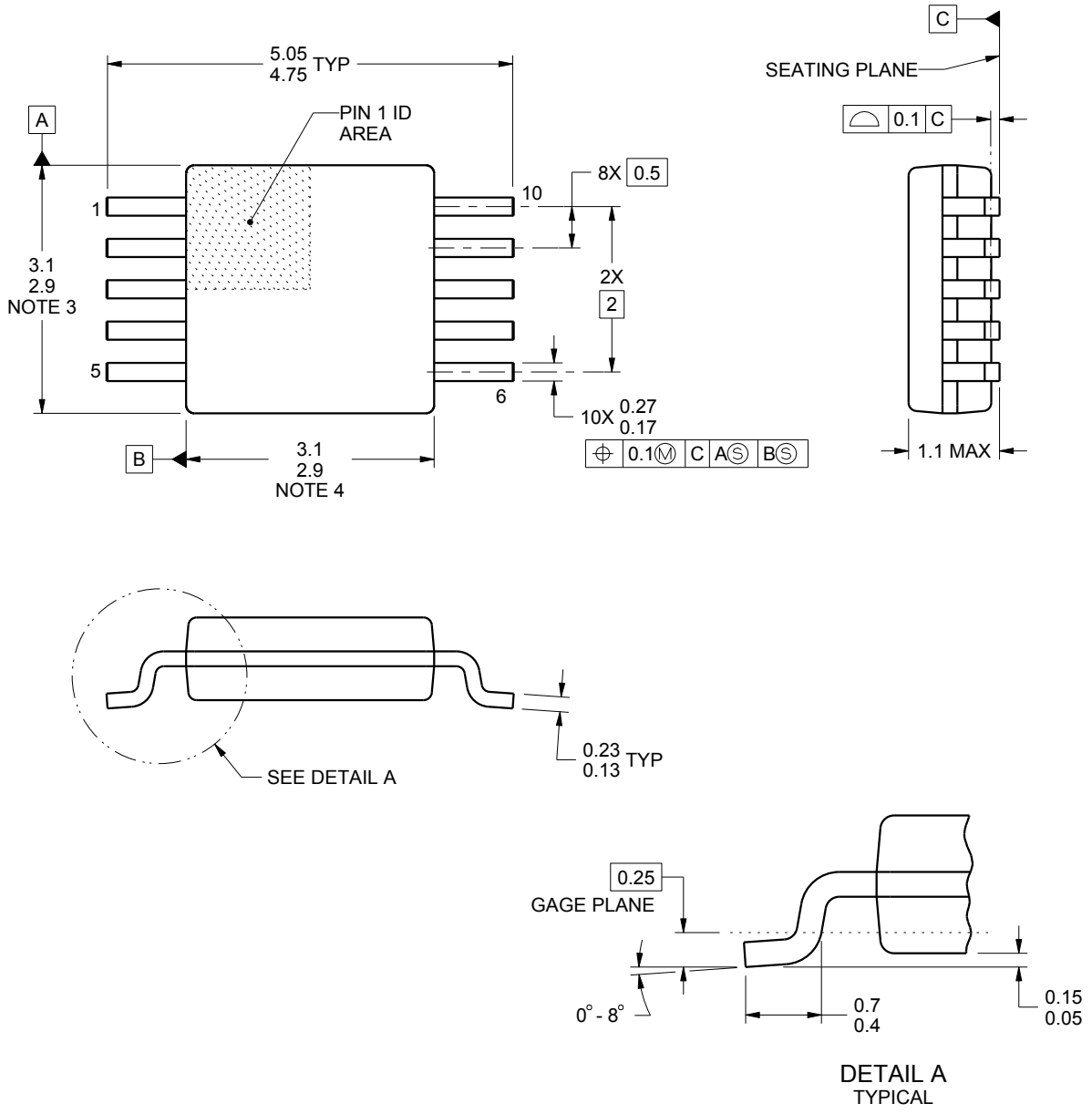
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DGS0010A

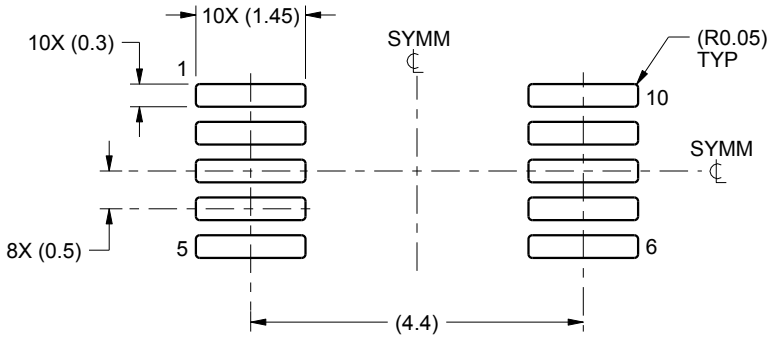
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

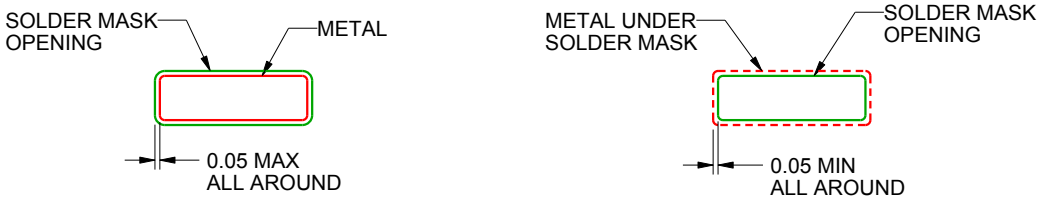


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

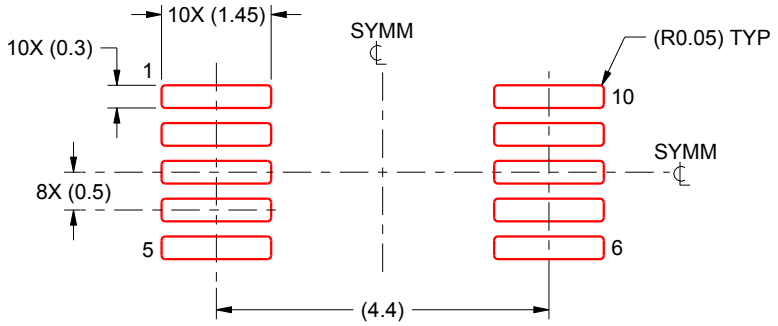


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

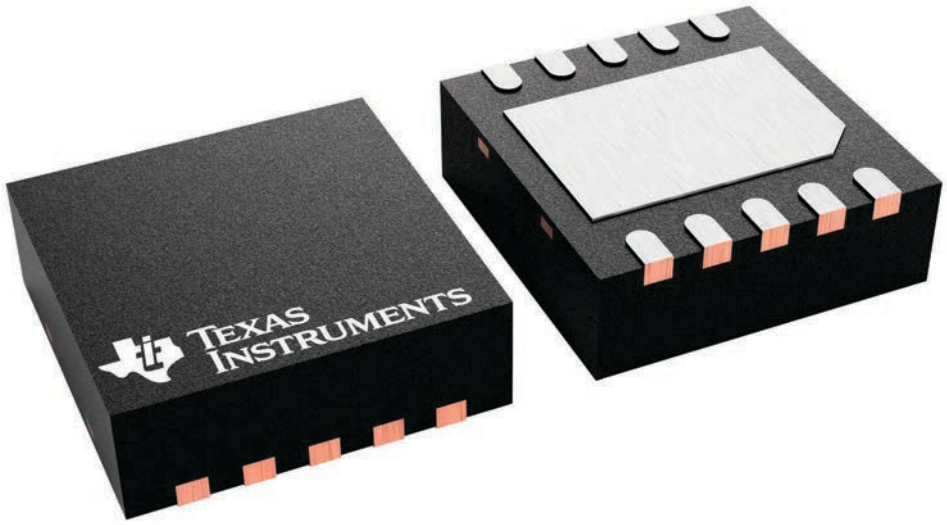
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



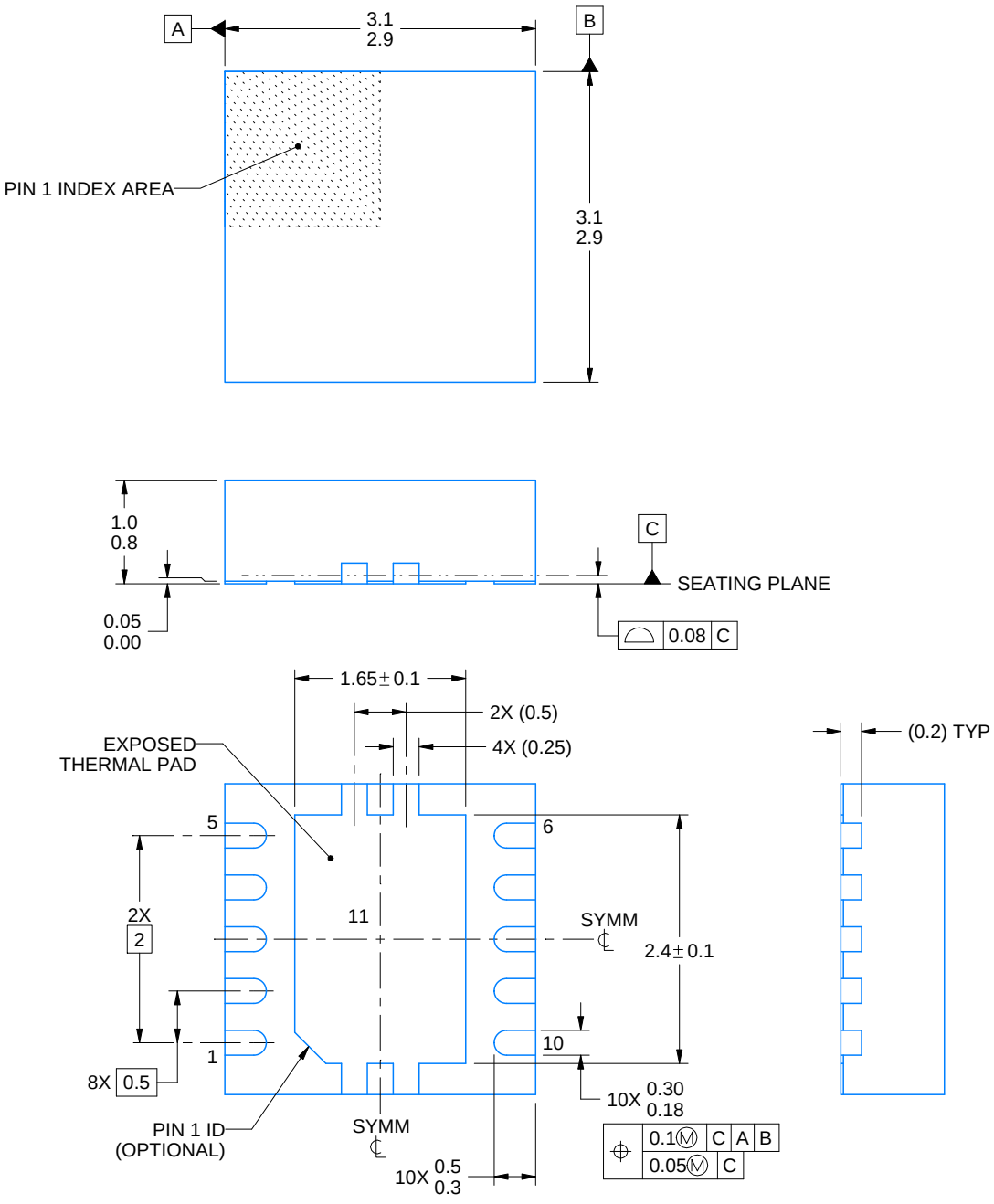
4226193/A

DRC0010J

PACKAGE OUTLINE

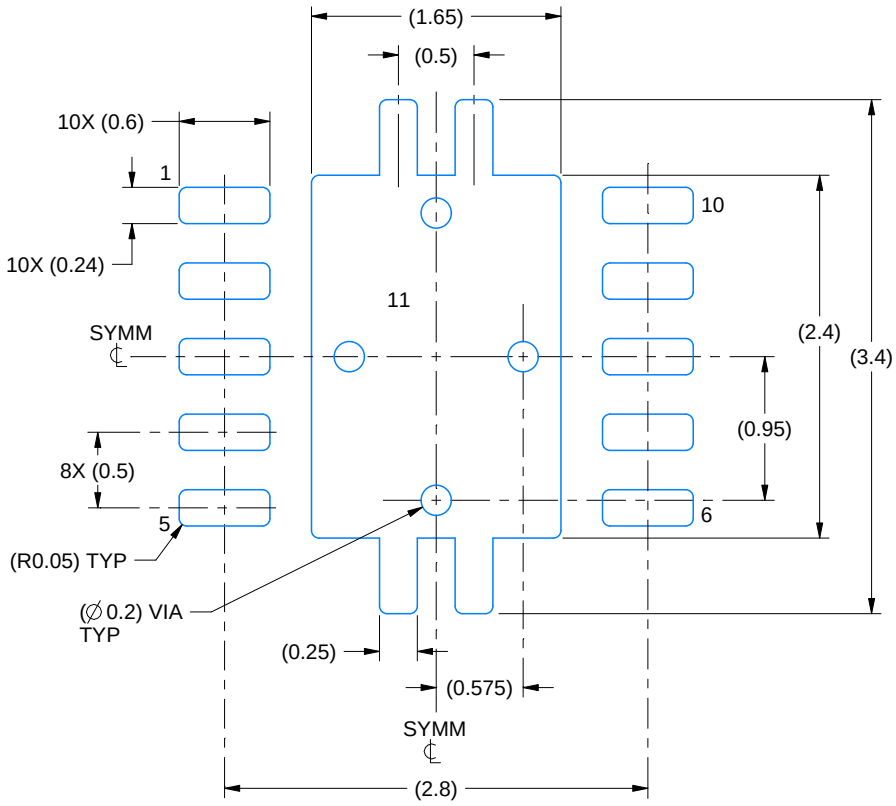
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

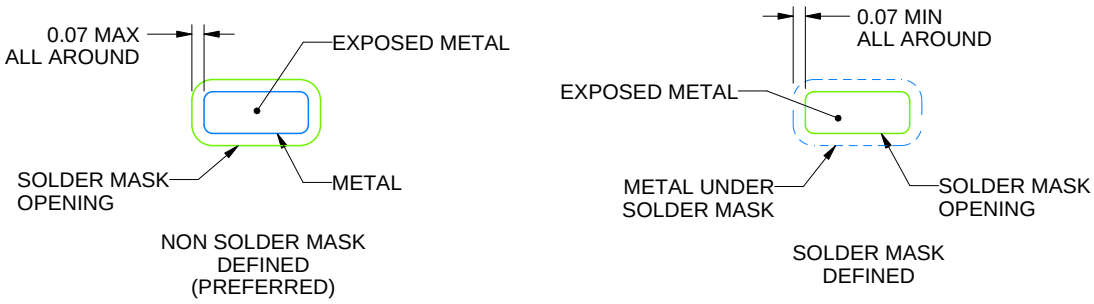


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

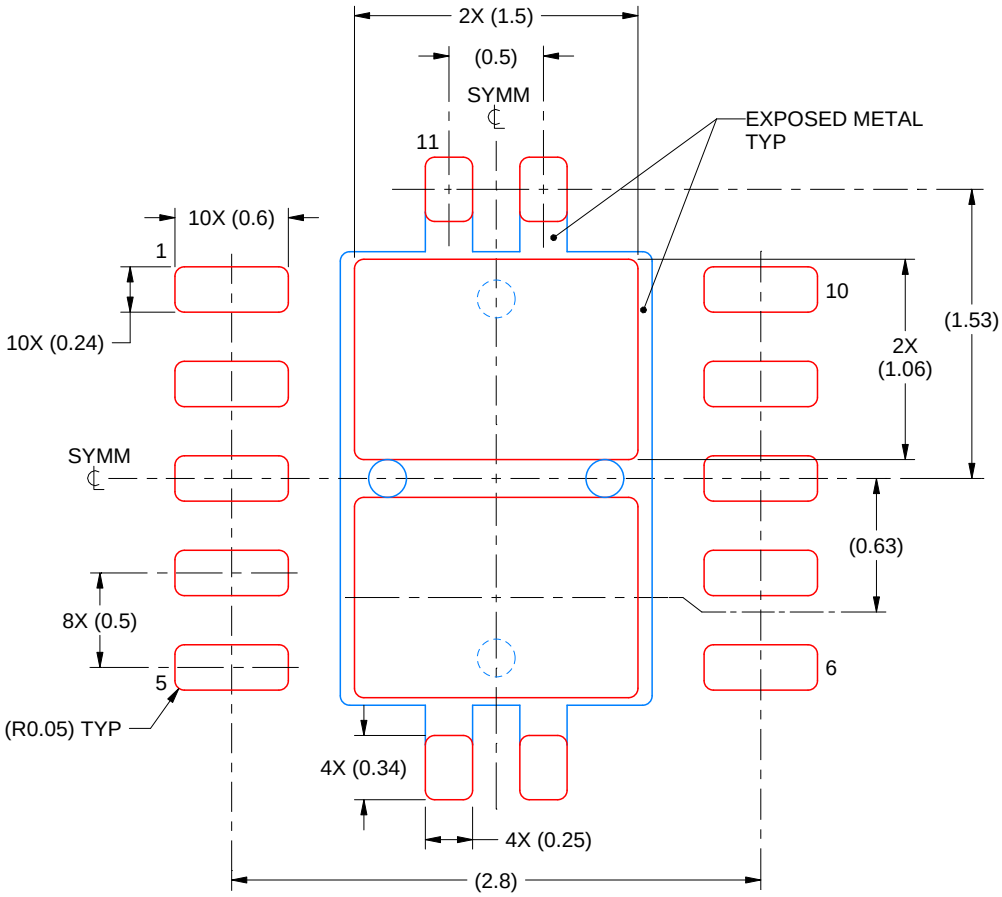
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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