TS3DS10224 高速差动交叉点、1:4 差分多路复用器和多路信号分离器、双通道差分 1:2 多路复用器和多路信号分离器或扇出开关

1 特性

- 可用于配置
  - 差动交叉点开关
  - 差分单通道 1:4 多路复用器和多路信号分离器
  - 差分双通道 1:2 多路复用器和多路信号分离器
  - 信号对至两个端口的同步差动扇出
- 双向运转
- 失效防护保护：I_{OFF} 保护可防止在掉电状态 (V_{CC} = 0V) 下泄漏电流
- 高带宽（典型值 1.2GHz）
- 低 R_{ON} 和 C_{ON}：
  - 典型值 13Ω R_{ON}
  - 典型值 9pF C_{ON}
- 静电放电性能（I/O 引脚）
  - ±8kV 接触放电 (IEC 61000-4-2)
  - JESD22-A114E（至 GND）对应的 2 kV 人体模型
- ESD 性能（所有引脚）
  - JESD22 A114E 对应的 2 kV 人体模型
- 小型 WQFN 封装（3.00 mm × 3.00 mm，0.4mm 间距）

2 应用

- 差动交叉点开关
- 台式机和笔记本电脑
- Displayport 辅助通道复用
- USB 2.0 复用
- 上网笔记本、电子书和平板电脑

3 说明

TS3DS10224 器件是一款双向差动交叉点、1:4 或 1:2 多路复用器和多路信号分离器；或高达 720Mbps 的高速差分信号 应用 扇出开关。TS3DS10224 逻辑表可对任何输入到输出进行布线，创建各种可能的开关或多路复用配置。常见配置包括：差动交叉点开关、差分 1:4 多路复用器，或差分双通道 1:2 多路复用器和多路信号分离器。TS3DS10224 提供 1.2GHz 高带宽，具有 13 Ω 的通道 R_{ON}（典型值）。

TS3DS10224 也可用于将差分信号对同步扇出至两个端口（扇出配置）。在这个配置中，带宽性能有所降低。

TS3DS10224 需由 3V 至 3.6V 的电源供电。该器件的 I/O 引脚上具有最高可达 ±8kV 的接触放电 ESD 保护和 2kV 人体模型。

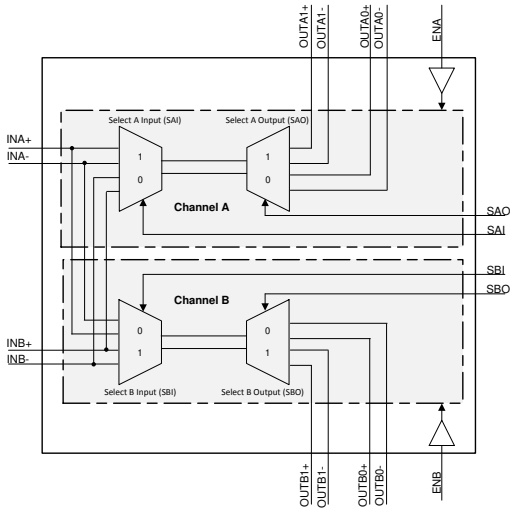
在电源 (V_{CC}) 不存在时，TS3DS10224 使用高阻抗隔离 I/O 引脚以提供失效防护保护。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS3DS10224	WQFN (20)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能方框图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (May 2019) to Revision E — **Page**

- Changed mapping for OUTB0, and OUTB1 in Table 6 ... 18

Changes from Revision C (November 2017) to Revision D — **Page**

- Changed Figure 2 ... 7

Changes from Revision B (December 2016) to Revision C — **Page**

- Changed columns OUTA1, OUTB0, and OUTB1 in Table 6 ... 18

Changes from Revision A (May 2013) to Revision B — **Page**

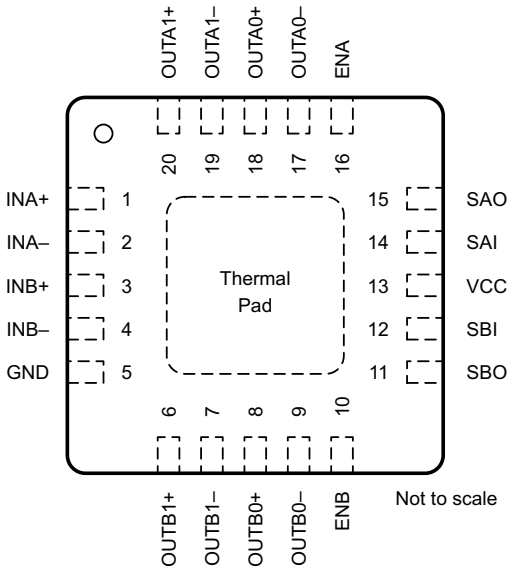
- 已添加 *器件信息表*、*引脚配置和功能*部分、*规格*部分、*ESD 额定值*表、*详细 说明*部分，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Added *Thermal Information* table ... 4
- Changed $R_{\theta JA}$ value From: 82.7 To: 45.2 ... 4

Changes from Original (June 2011) to Revision A — **Page**

- 使用整篇文档替换了 1 页 ... 1

5 Pin Configuration and Functions

RUK Package
20-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	INA+	I/O	A channel signal path
2	INA–	I/O	A channel signal path
3	INB+	I/O	B channel signal path
4	INB–	I/O	B channel signal path
5	GND	—	Ground
6	OUTB1+	I/O	B channel signal path
7	OUTB1–	I/O	B channel signal path
8	OUTB0+	I/O	B channel signal path
9	OUTB0–	I/O	B channel signal path
10	ENB	I	Enable B channel: LOW = disables channel B and places the signal path in high impedance state, HIGH = enables channel B.
11	SBO	I	Select B channel output, controls output selection: LOW = selects OUTB0 signals, HIGH = selects OUTB1 signals.
12	SBI	I	Select B channel input, controls input selection: LOW = selects INA signals to pass through the B channel, HIGH = selects INB signals to pass through the B channel.
13	VCC	—	Power supply
14	SAI	I	Select A channel input, controls input selection: LOW = selects INB signals to pass through the A channel, HIGH = selects INA signals to pass through the A channel.
15	SAO	I	Select A channel output, controls output selection: LOW = selects OUTA0 signals, HIGH = selects OUTA1 signals.
16	ENA	I	Enable A channel: LOW = disables channel A and places the signal path in high impedance state, HIGH = enables channel A.
17	OUTA0–	I/O	A channel signal path
18	OUTA0+	I/O	A channel signal path
19	OUTA1–	I/O	A channel signal path
20	OUTA1+	I/O	A channel signal path

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

	MIN	MAX	UNIT
Supply voltage	–0.3	4	V
Analog I/O voltage(2)(3)(4)	–0.3	V_{CC} + 0.3	V
Control input voltage(2)(4), V_{IN}	–0.3	V_{CC} + 0.3	V
ON-state switch current(5), I_{IO}		±100	mA
Continuous current through VCC or GND		±100	mA
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) V_I and V_O are used to denote specific conditions for V_{IO}.
(4) The input and output voltage rating may be exceeded if the input and output clamp-current ratings are observed.
(5) I_I and I_O are used to denote specific conditions for I_{IO}.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).(1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage	0.75 × V_{CC}	V_{CC}	V
V_{IL}	Low-level control input voltage	0	0.6	V
V_{IO}	Input and output voltage	0	V_{CC}	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(2) TI recommends pulling down to ground unused I/O pins through a 1-kΩ resistor.

6.4 Thermal Information

THERMAL METRIC(1)		TS3DS10224 RUK (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: Differential 1:4 or 2-Channel 1:2 Configurations

Minimum and maximum values are at T_A = –40°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Digital input clamp voltage	V_{CC} = 3.6 V, I_I = –18 mA	–1.2	–0.9		V
I_{IN}	Digital input leakage current	V_{CC} = 3.6 V, V_{IN} = 0 to 3.6 V			±2	µA
I_{OZ}	OFF-state leakage current(2)	V_{CC} = 3.6 V, V_O = 0 V to 3.6 V, V_I = 0 V, Switch OFF			±2	µA
I_{OFF}	Power off leakage current	V_{CC} = 0 V, V_{IN} = V_{CC} or GND,V_{IO} = 0 V to 3.6 V			±5	µA
I_{CC}	Supply current	V_{CC} = 3.6 V, I_{IO} = 0, Switch ON or OFF		50	100	µA
C_{IN}	Digital input capacitance	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND		3	5	pF
$C_{IO(OFF)}$	OFF capacitance	V_{CC} = 3.3 V, V_{IO} = 3.3 V or 0, f = 10 MHz, Switch OFF		6	7	pF
$C_{IO(ON)}$	ON capacitance	V_{CC} = 3.3 V, V_{IO} = 3.3 V or 0, f = 10 MHz, Switch ON		9	10	pF
r_{ON}	ON-state resistance	V_{CC} = 3.6 V, V_I = V_{CC}, I_O = –30 mA		13	19	Ω
		V_{CC} = 3.3 V, V_I = 0.5 V, I_O = –30 mA		10		Ω
Δr_{ON}	ON-state resistance match between channels	V_{CC} = 3 V, V_I = 0 to V_{CC}, I_O = –30 mA		2	2.5	Ω
$r_{ON(flat)}$	ON-state resistance flatness	V_{CC} = 3 V, V_I = 1.5 V and V_{CC}, I_O = –30 mA		4	6	Ω

(1) V_{IN} and I_{IN} refer to the digital control input pins.
(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

6.6 Electrical Characteristics: Fan-Out 1:2 Configurations

T_A = –40°C to 85°C; typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Digital input clamp voltage	V_{CC} = 3.6 V, I_I = –18 mA	–1.2	–0.9		V
I_{IN}	Digital input leakage current	V_{CC} = 3.6 V, V_{IN} = 0 to 3.6 V			±2	µA
I_{OZ}	OFF-state leakage current(2)	V_{CC} = 3.6 V, V_O = 0 V to 3.6 V, V_I= 0 V, Switch OFF			±2	µA
I_{OFF}	Power off leakage current	V_{CC} = 0 V, V_{IN} = V_{CC} or GND, V_{IO} = 0 V to 3.6 V			±5	µA
I_{CC}	Supply current	V_{CC} = 3.6 V, I_{IO} = 0, Switch ON or OFF		50	100	µA
C_{IN}	Digital input capacitance	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND		3	5	pF
$C_{IO(OFF)}$	OFF capacitance	V_{CC} = 3.3 V, V_{IO} = 3.3 V or 0, f = 10 MHz, Switch OFF		6	7	pF
$C_{IO(ON)}$	ON capacitance	V_{CC} = 3.3 V, V_{IO} = 3.3 V or 0, f = 10 MHz, Switch ON		12	13	pF
r_{ON}	ON-state resistance	V_{CC} = 3.6 V, V_I = V_{CC}, I_O = –30 mA		13	19	Ω
Δr_{ON}	ON-state resistance match between channels	V_{CC} = 3 V, V_I = 0 to V_{CC}, I_O = –30 mA		2	2.5	Ω
$r_{ON(flat)}$	ON-state resistance flatness	V_{CC} = 3 V, V_I = 1.5 V and V_{CC}, I_O = –30 mA		4	6	Ω

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

6.7 Switching Characteristics: Differential 1:4 or 2-Channel 1:2 Configurations

T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay(1)	R_L = 50 Ω, C_L = 2 pF		50		ps
t_{ON}	SAI, SAO, SBI, or SBO to OUTAx or OUTBx	R_L = 50 Ω, C_L = 2 pF		40	100	ns
t_{OFF}	SAI, SAO, SBI, or SBO to OUTAx or OUTBx	R_L = 50 Ω, C_L = 2 pF		20	30	ns
$t_{sk(o)}$	Timing difference between output channels(2)	R_L = 50 Ω, C_L = 2 pF		40		ps
$t_{sk(p)}$	Timing difference between propagation delays(3)	R_L = 50 Ω, C_L = 2 pF		40		ps

(1) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source(zero output impedance).
(2) Output skew between center channel and any other channel.
(3) Skew between opposite transitions of the same output ($|t_{PHL} – t_{PLH}|$).

6.8 Switching Characteristics: Fan-Out 1:2 Configurations

T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay(1)	R_L = 50 Ω, C_L = 2 pF		140		ps
t_{ON}	SAI, SAO, SBI, or SBO to OUTAx or OUTBx	R = 50 Ω, C_L = 2 pF		40	100	ns
t_{OFF}	SAI, SAO, SBI, or SBO to OUTAx or OUTBx	R_{LL} = 50 Ω, C_L = 2 pF		20	30	ns
$t_{sk(o)}$	Timing difference between output channels(2)	R_L = 50 Ω, C_L = 2 pF		60		ps
$t_{sk(p)}$	Timing difference between propagation delays(3)	R_L = 50 Ω, C_L = 2 pF		60		ps

(1) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) Output skew between center channel and any other channel.
(3) Skew between opposite transitions of the same output ($|t_{PHL} – t_{PLH}|$).

6.9 Dynamic Characteristics: Differential 1:4 or 2-Channel 1:2 Configurations

T_A = –40°C to 85°C; typical values are at V_{CC} = 3.3 V ± 10% and T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TYP	UNIT
BW	Bandwidth	R_L = 50 Ω, Switch ON	1.2	GHz
O_{ISO}	OFF Isolation	R_L = 50 Ω , f = 250 MHz	–30	dB
X_{TALK}	Crosstalk	R_L = 50 Ω , f = 250 MHz	–30	dB

6.10 Dynamic Characteristics: Fan-Out 1:2 Configurations

T_A = –40°C to 85°C; typical values are at V_{CC} = 3.3 V ± 10% and T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TYP	UNIT
BW	Bandwidth	R_L = 50 Ω, Switch ON	500	MHz
O_{ISO}	OFF Isolation	R_L = 50 Ω , f = 250 MHz	–30	dB
X_{TALK}	Crosstalk	R_L = 50 Ω , f = 250 MHz	–30	dB

6.11 Typical Characteristics

6.11.1 Single-Channel 1:4 or Dual-Channel 1:2 Configurations

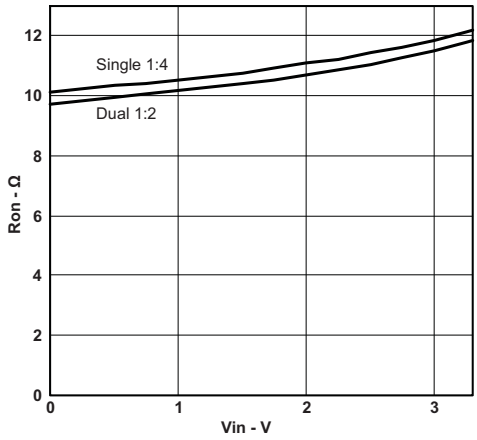


Figure 1. ON-Resistance vs V_{IN}

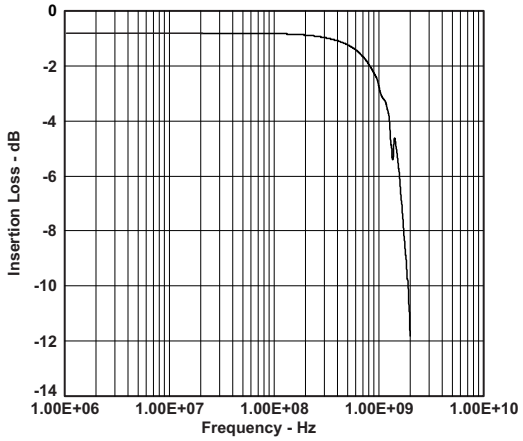


Figure 2. Insertion Loss vs Frequency

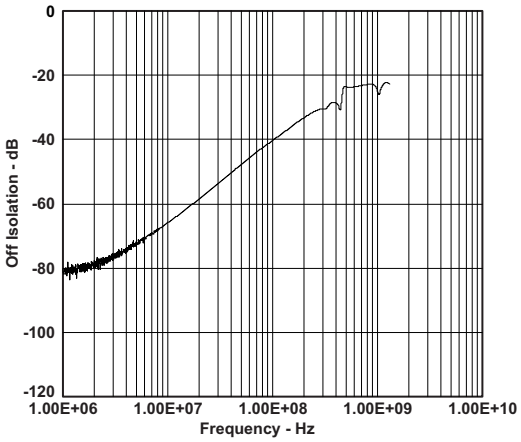


Figure 3. Off Isolation vs Frequency

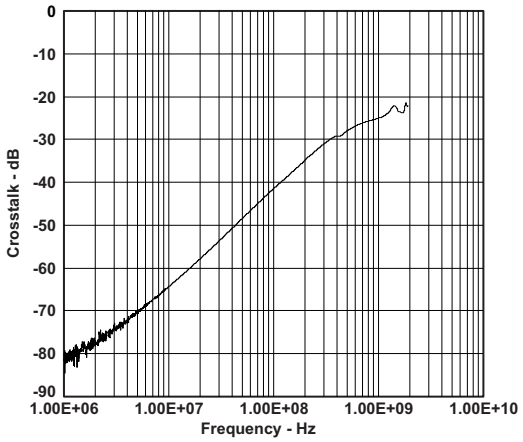


Figure 4. Crosstalk vs Frequency

6.11.2 Fan-Out 1:2 Configurations

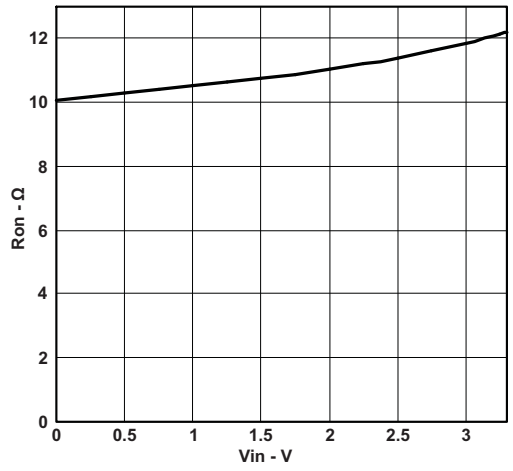


Figure 5. ON-Resistance vs V_{IN}

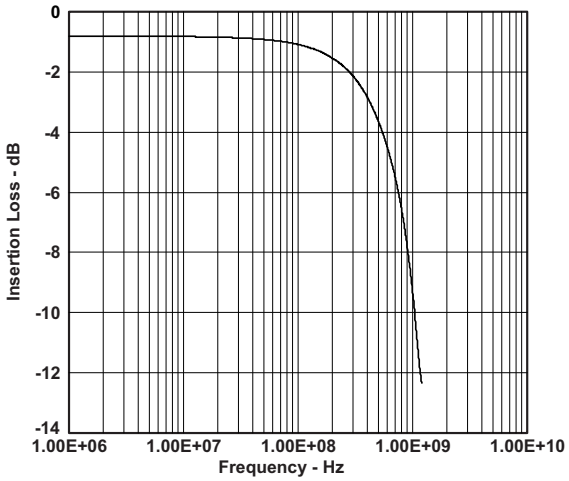


Figure 6. Insertion Loss vs Frequency

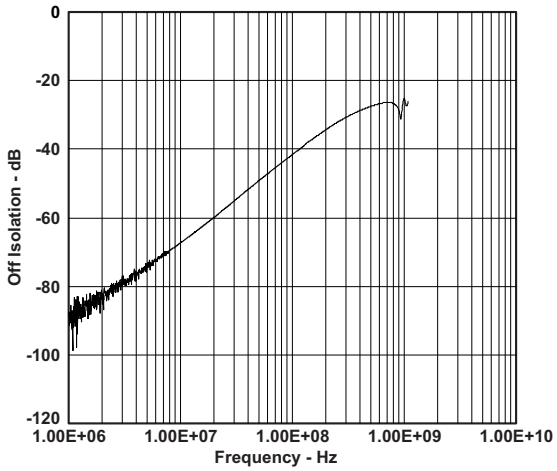


Figure 7. Off Isolation vs Frequency

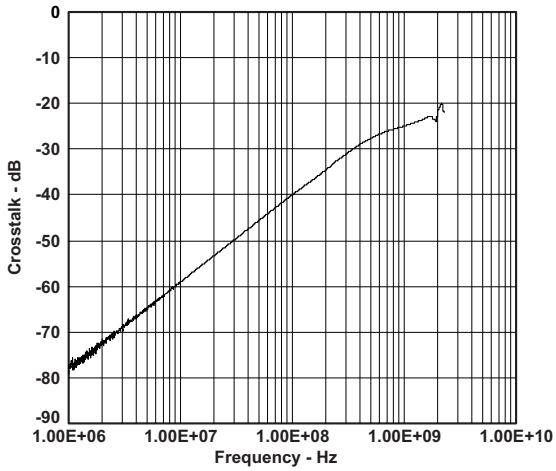
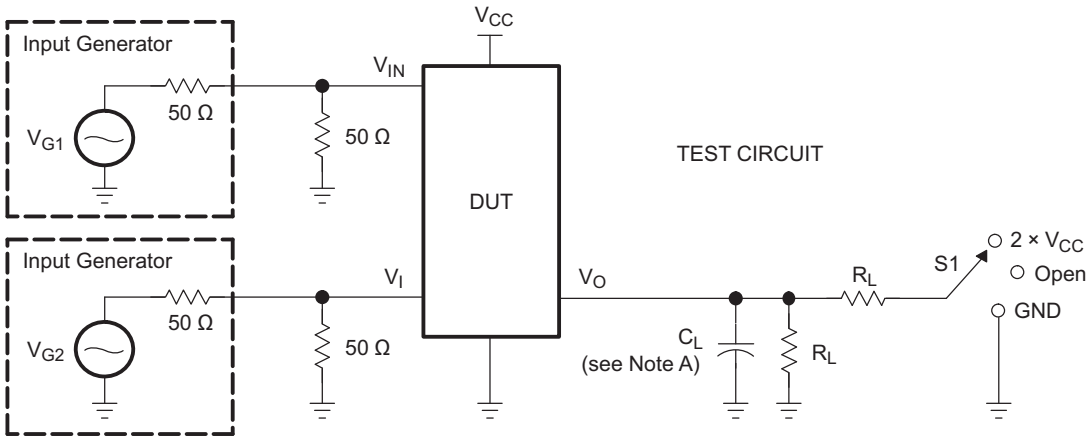
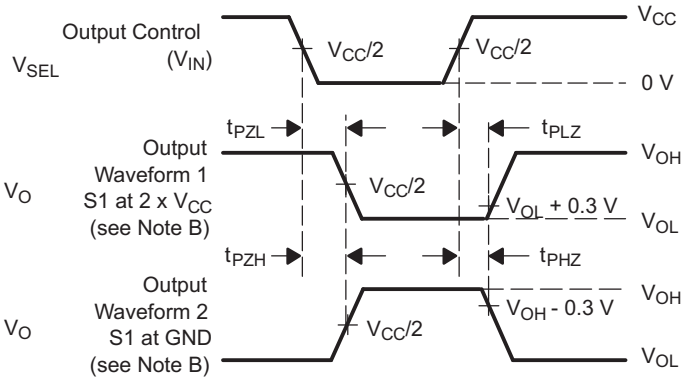


Figure 8. Crosstalk vs Frequency

7 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 × V_{CC}	50 Ω	GND	2 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	50 Ω	V_{CC}	2 pF	0.3 V

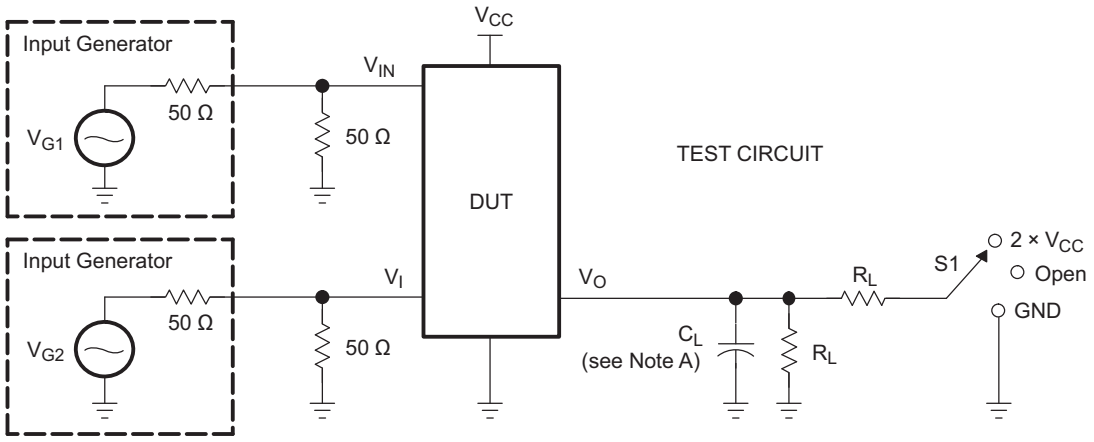


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

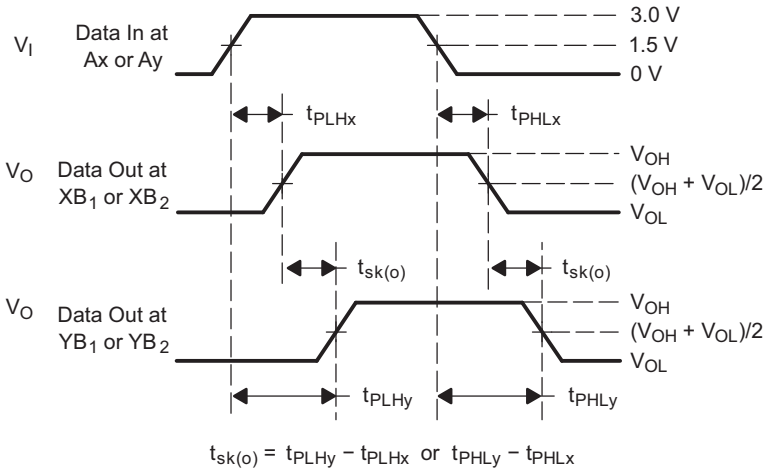
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics:PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{OFF}.
F. t_{PZL} and t_{PZH} are the same as t_{ON}.

Figure 9. Test Circuit and Voltage Waveforms

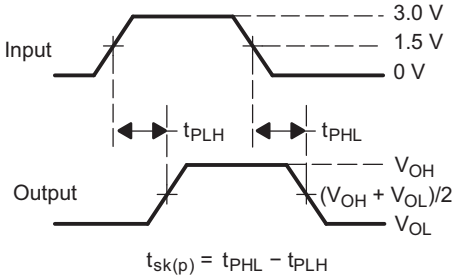
Parameter Measurement Information (continued)



TEST	V_{CC}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	50 Ω	V_{CC} or GND	2 pF
$t_{sk(p)}$	3.3 V ± 0.3 V	Open	50 Ω	V_{CC} or GND	2 pF



VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 10. Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

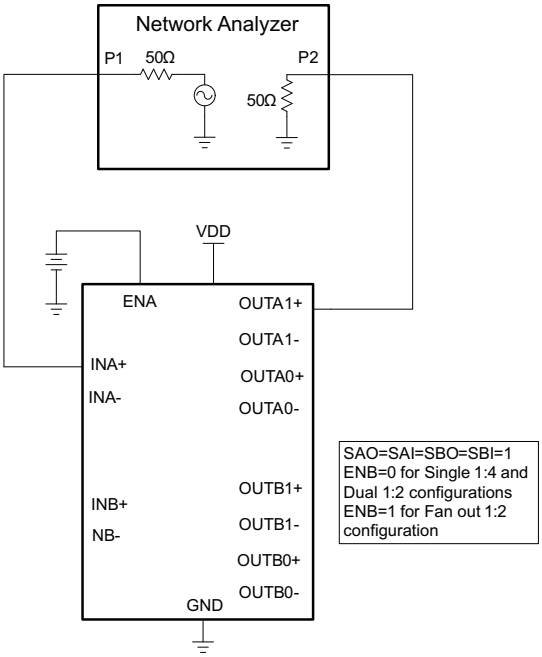


Figure 11. Frequency Response (BW)

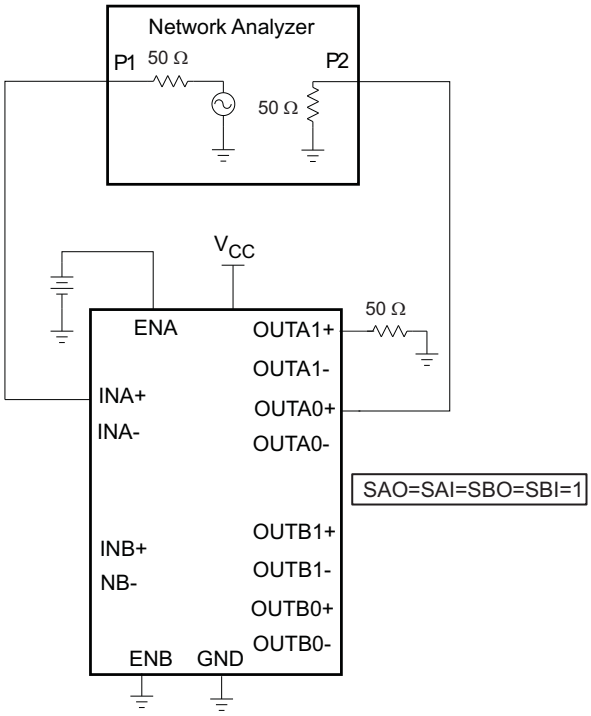


Figure 12. Off Isolation (O_{ISO})

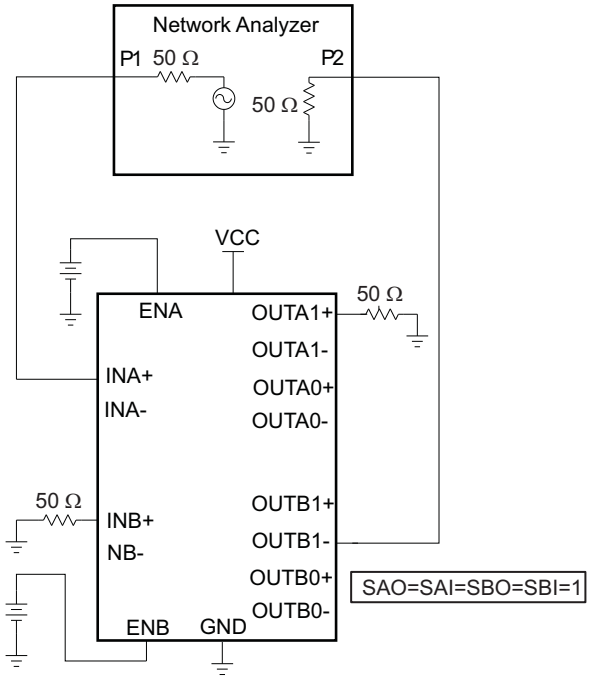


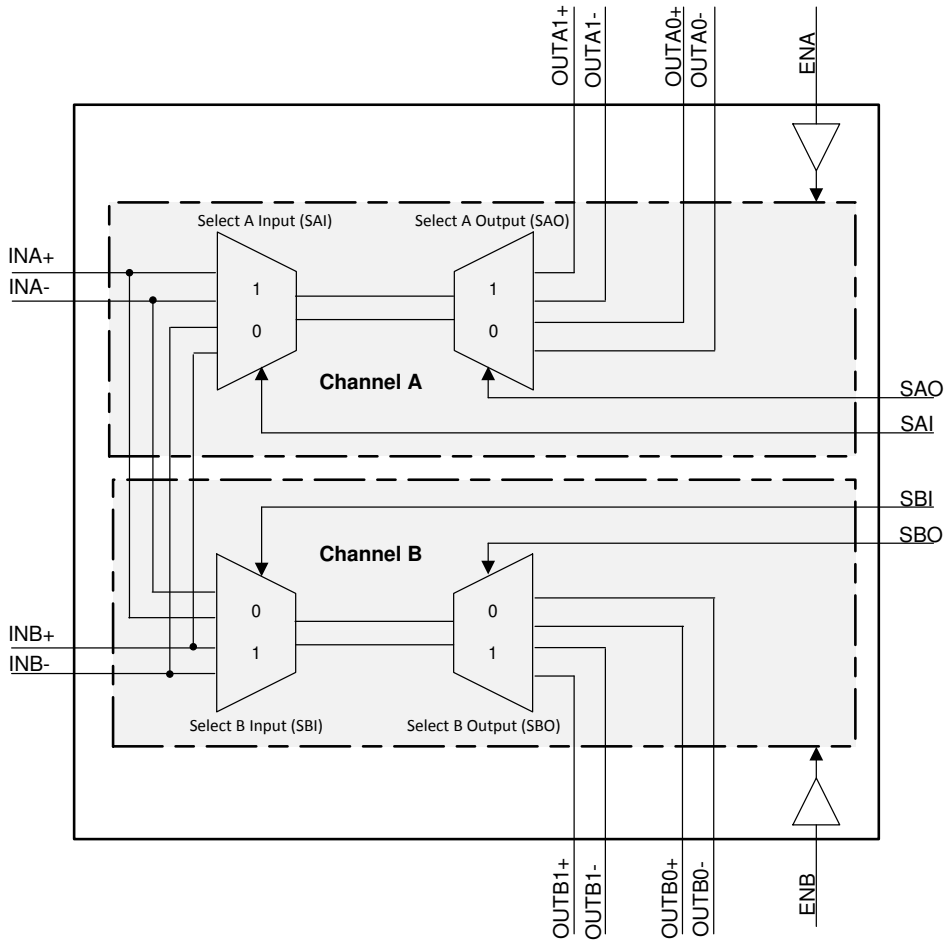
Figure 13. Crosstalk (X_{TALK})

8 Detailed Description

8.1 Overview

The TS3DS10224 is a 3-V, bidirectional, differential crosspoint, differential 1:4, 2-channel differential 1:2 multiplexer and demultiplexer, or fan-out switch for high-speed differential signal applications. The TS3DS10224 can route any input to any output creating a wide range of possible switching or multiplexing configurations. Differential crosspoint switching, differential 1:4 mux, or 2-channel differential 1:2 multiplexer and demultiplexer are commonly used configurations of the device. Additionally the TS3DS10224 can also be used to fan out a differential signal pair to two ports simultaneously (fan-out configuration). However, the BW performance is lower in this configuration.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fail-Safe Protection

I_{OFF} protection prevents current leakage in powered down state (V_{CC} = 0 V).

The TS3DS10224 device places the signal paths in a high-impedance state when the device is not powered. This isolates the data bus if the IC loses power on the supply pin.

8.4 Device Functional Modes

8.4.1 Enable and Disable

The TS3DS10224 has two enable pins (ENA and ENB). Setting these pins LOW disables the signal path and place them in a high-impedance (Hi-Z) state.

Table 1. Enable and Disable Function Table

ENA	ENB	INA	INB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	Enabled	Hi-Z	Hi-Z	Enabled	Enabled
1	0	Enabled	Hi-Z	Enabled	Enabled	Hi-Z	Hi-Z
1	1	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

8.4.2 Differential Crosspoint Switch

The TS3DS10224 can be configured as a differential crosspoint switch. Crosspoint switches are particularly helpful when traces have to cross in simplifying layouts, and when switching the top and bottom signals of the reversible connector in USB Type-C applications.

Table 2 shows that the inputs INA and INB can be routed to OUTA or OUTB. This is accomplished by setting the Select A Output (SAO) and Select B Output (SBO) LOW and selecting which input goes to the output by toggling the Select A Input (SAI) and Select B Input (SBI) pins.

Table 2. Differential Crosspoint Switch Function Table

LOGIC CONTROL SETTING				SIGNAL ROUTING	
SAI	SBI	SAO	SBO	INA	INB
0	0	0	0	OUTB0	OUTA0
1	1	0	0	OUTA0	OUTB0

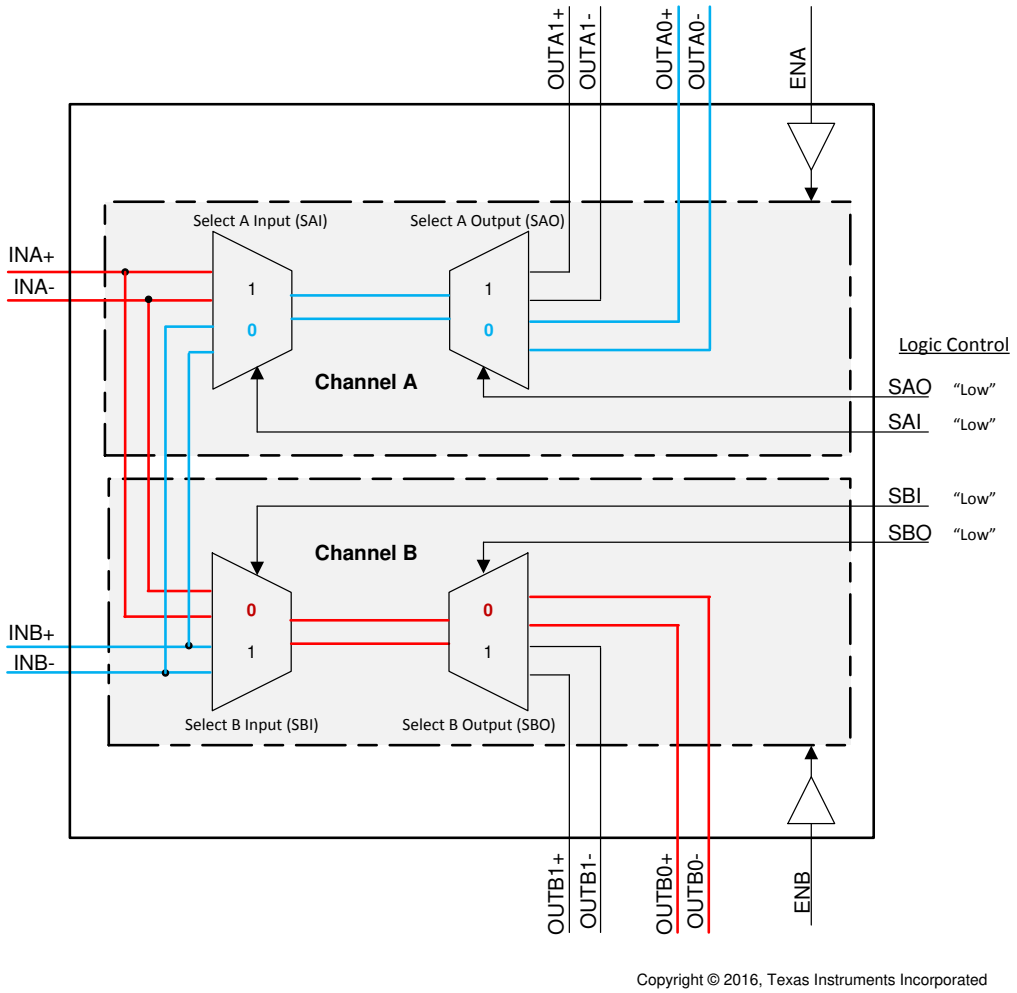


Figure 14. Differential Crosspoint Switch Block Diagram

8.4.3 2-Channel 1:2 Mux

The TS3DS10224 can be configured to be differential 2-channel 1:2 mux.

Table 3 shows that the inputs INA and INB can be routed to 2 different places. This is accomplished by setting the Select A Input (SAI) and Select B Input (SBI) HIGH and selecting an output by toggling the Select A Output (SAO) and Select B Output (SBO) pins.

Table 3. 2-Channel 1:2 Mux Function Table

LOGIC CONTROL SETTING				SIGNAL ROUTING	
SAI	SBI	SAO	SBO	INA	INB
1	1	0	0	OUTA0	OUTB0
1	1	0	1	OUTA0	OUTB1
1	1	1	0	OUTA1	OUTB0
1	1	1	1	OUTA1	OUTB1

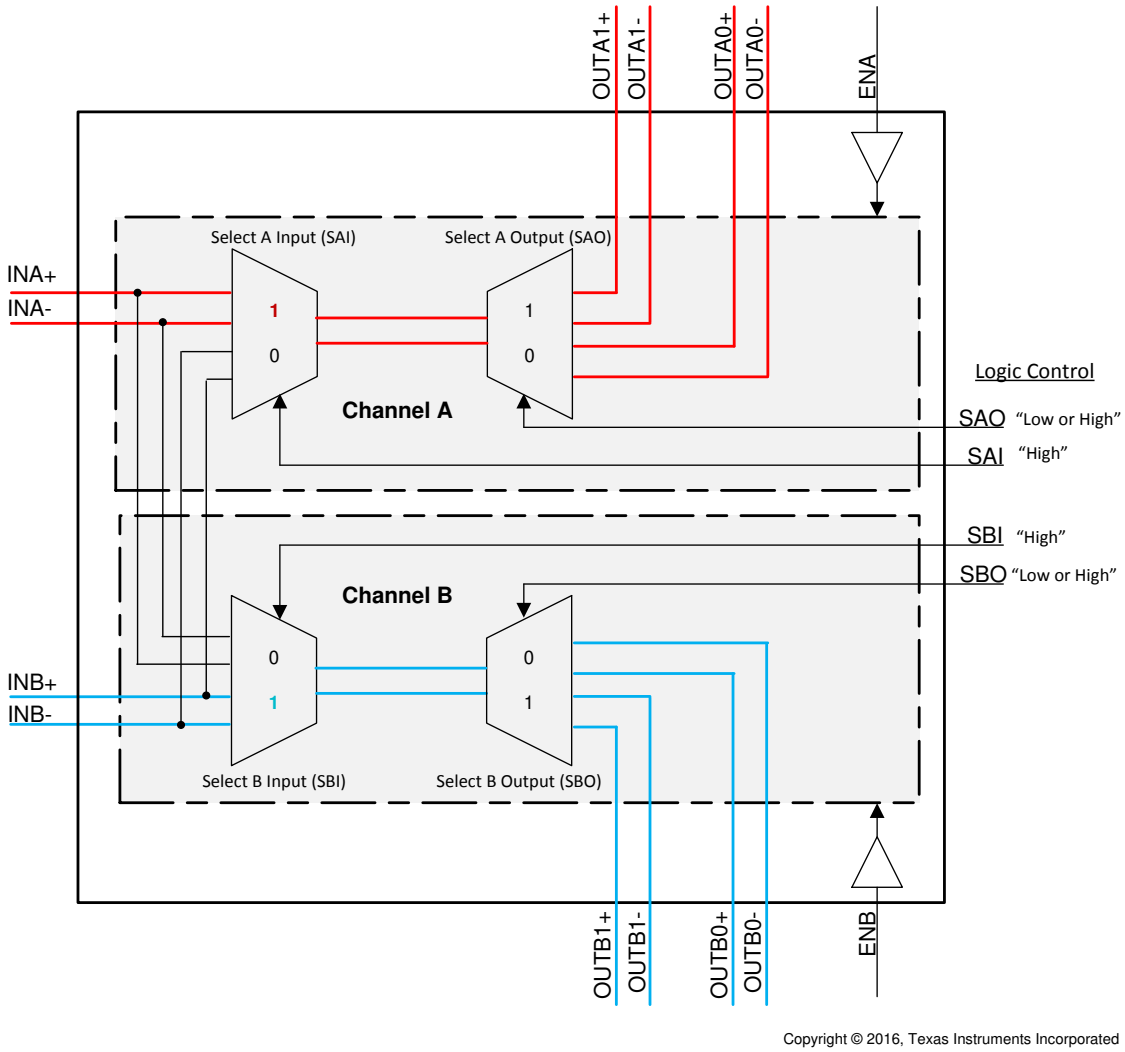


Figure 15. 2-Channel 1:2 Block Diagram

8.4.4 1-Channel 1:4 Mux

The TS3DS10224 can be configured as differential 1-channel 1:4 mux.

The truth table below shows that the inputs INA can be routed to 4 different places. This is accomplished by setting the Select A Input (SAI) and Select B Input (SBI) HIGH and selecting an output by toggling the Select A Output (SAO) and Select B Output (SBO) pins.

Unused pins INB+ and INB– must be left floating in this configuration.

Table 4. 1-Channel 1:4 Mux Function Table

LOGIC CONTROL SETTINGS				SIGNAL ROUTING	
SAI	SBI	SAO	SBO	INA	INB
1	1	0	—	OUTA0	—
1	1	1	—	OUTA1	—
0	0	—	0	OUTB0	—
0	0	—	1	OUTB1	—

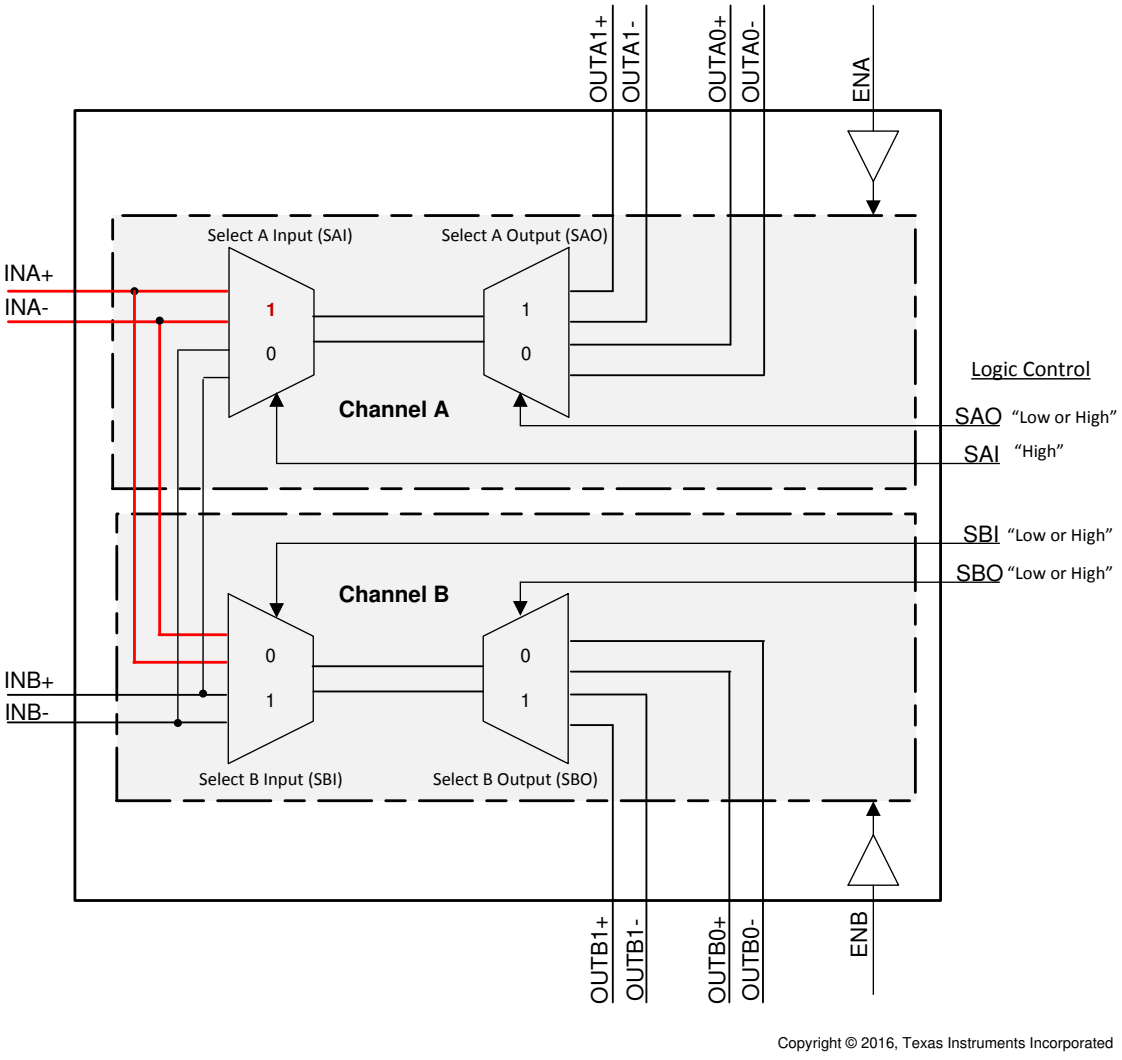


Figure 16. 1-Channel 1:4 Mux Functional Block Diagram

8.4.5 Fan-Out 1:2 Configuration

The TS3DS10224 can be configured in a differential fan-out 1:2 mux.

The truth table below shows that the inputs INA or INB can be routed to output A or output B simultaneously. This is accomplished by setting the Select A Input (SAI) and Select B Input (SBI) HIGH and selecting an output by toggling the Select A Output (SAO) and Select B Output (SBO) pins.

Unused pins INB+ and INB– must be left floating in this configuration.

Table 5. Fan-Out 1:2 Function Table

LOGIC CONTROL SETTINGS				SIGNAL ROUTING	
SAI	SBI	SAO	SBO	INA	INB
1	0	0	0	OUTA0 and OUTB0	—
1	0	0	1	OUTA0 and OUTB1	—
1	0	1	0	OUTA1 and OUTB0	—
1	0	1	1	OUTA1 and OUTB1	—

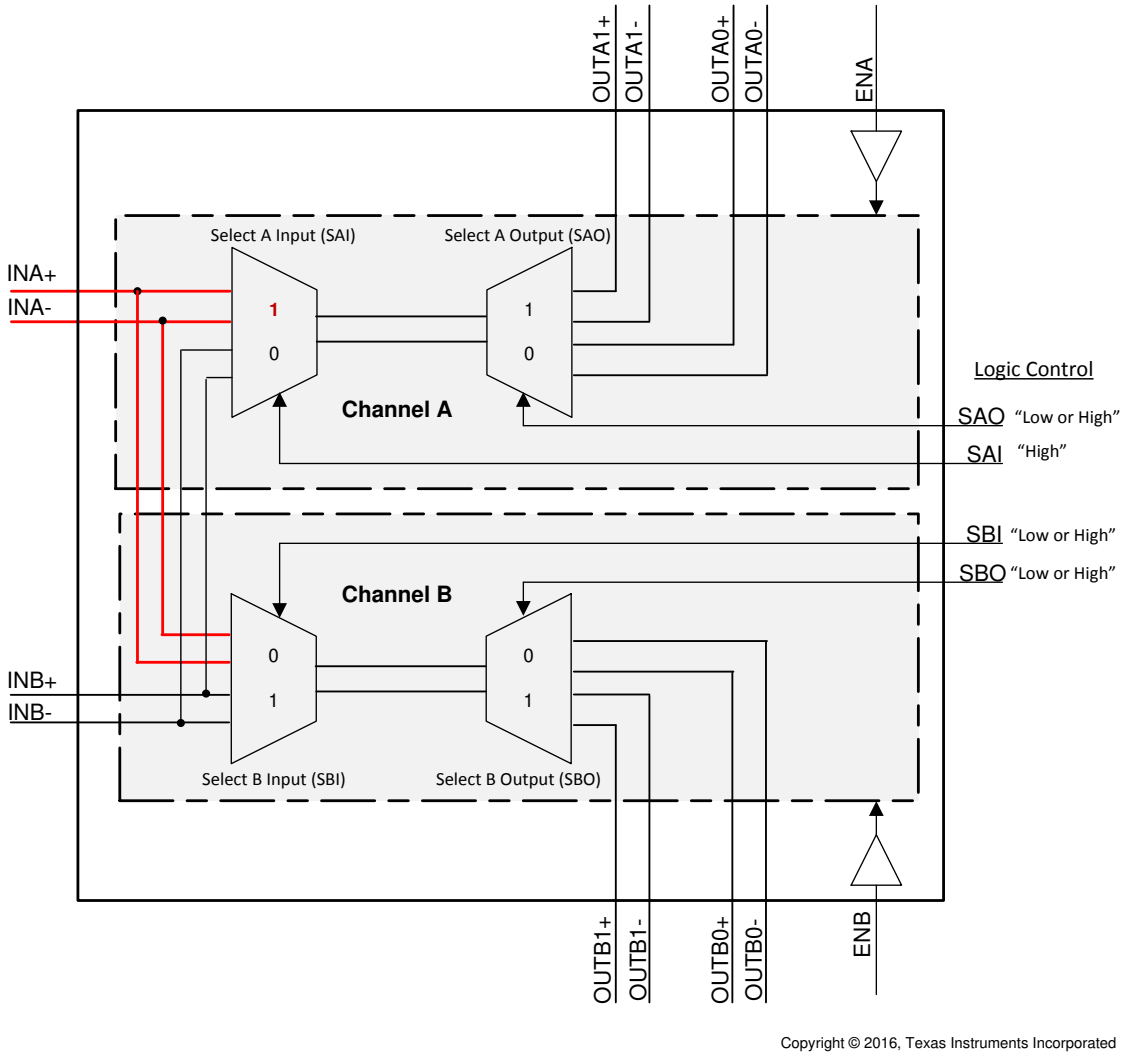


Figure 17. Fan-Out 1:2 Functional Block Diagram

Table 6.

SAI	SBI	SA0	SBO	OUTA0	OUTA1	OUTB0	OUTB1	FUNCTIONAL MODE
0	0	0	0	INB	—	INA	—	Crosspoint, 1-channel 1:4 mux
0	0	0	1	INB	—	—	INA	1-channel 1:4 mux
0	0	1	0	—	INB	INA	—	1-channel 1:4 mux
0	0	1	1	—	INB	—	INA	1-channel 1:4 mux
0	1	0	0	INB	—	INB	—	
0	1	0	1	INB	—	—	INB	
0	1	1	0	—	INB	INB	—	
0	1	1	1	—	INB	—	INB	
1	0	0	0	INA	—	INA	—	Fan-out 1:2 configuration
1	0	0	1	INA	—	—	INA	Fan-out 1:2 configuration
1	0	1	0	—	INA	INA	—	Fan-out 1:2 configuration
1	0	1	1	—	INA	—	INA	Fan-out 1:2 configuration
1	1	0	0	INA	—	INB	—	Crosspoint, 2-channel 1:2 mux, 1-channel 1:4 mux
1	1	0	1	INA	—	—	INB	2-channel 1:2 mux,1-channel 1:4 mux
1	1	1	0	—	INA	INB	—	2-channel 1:2 mux,1-channel 1:4 mux
1	1	1	1	—	INA	—	INB	2-channel 1:2 mux,1-channel 1:4 mux

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3DS10224 device can be configured for a variety of applications which makes this a great utility device. The most unique feature of this device is the ability to operate as a differential crosspoint switch.

9.2 Typical Applications

9.2.1 1-Channel Differential 1:4 Mux

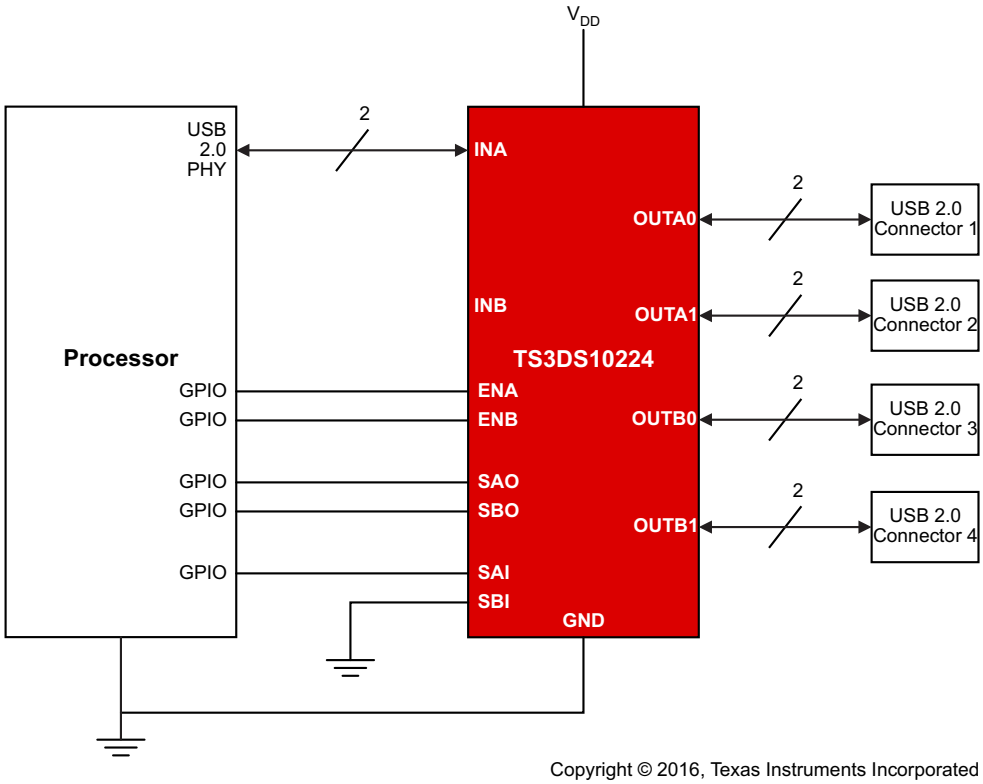


Figure 18. 1-Channel Differential 1:4 Mux Application

9.2.1.1 Design Requirements

TI recommends that the digital control pins SAI, SBI, SAO, and SBO be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from a floating pin. Unused pins for the signal paths INA, INB, OUTAx, and OUTBx must be terminated with a 50-Ω resistor to ground to reduce signal reflections in high-speed applications.

The thermal pad may be left floating or connected to ground.

9.2.1.2 Detailed Design Procedure

The TS3DS10224 can be properly operated without any external components. TI recommends placing a bypass capacitor on the VCC pin.

Typical Applications (continued)

9.2.1.3 Application Curves

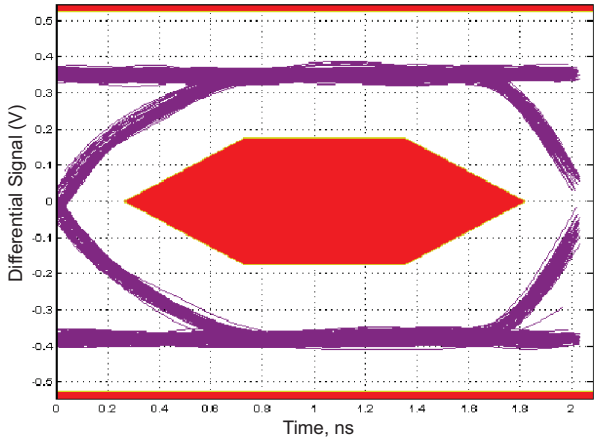


Figure 19. 480-Mbps USB 2.0 Eye Diagram Through Path With No Device

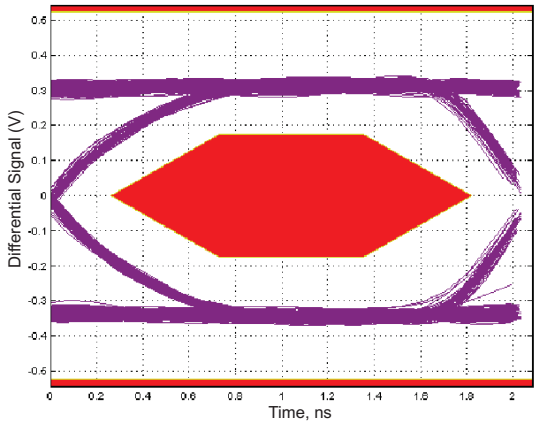


Figure 20. 480-Mbps USB 2.0 Eye Diagram With Device

9.2.2 2-Channel Differential Crosspoint Switch

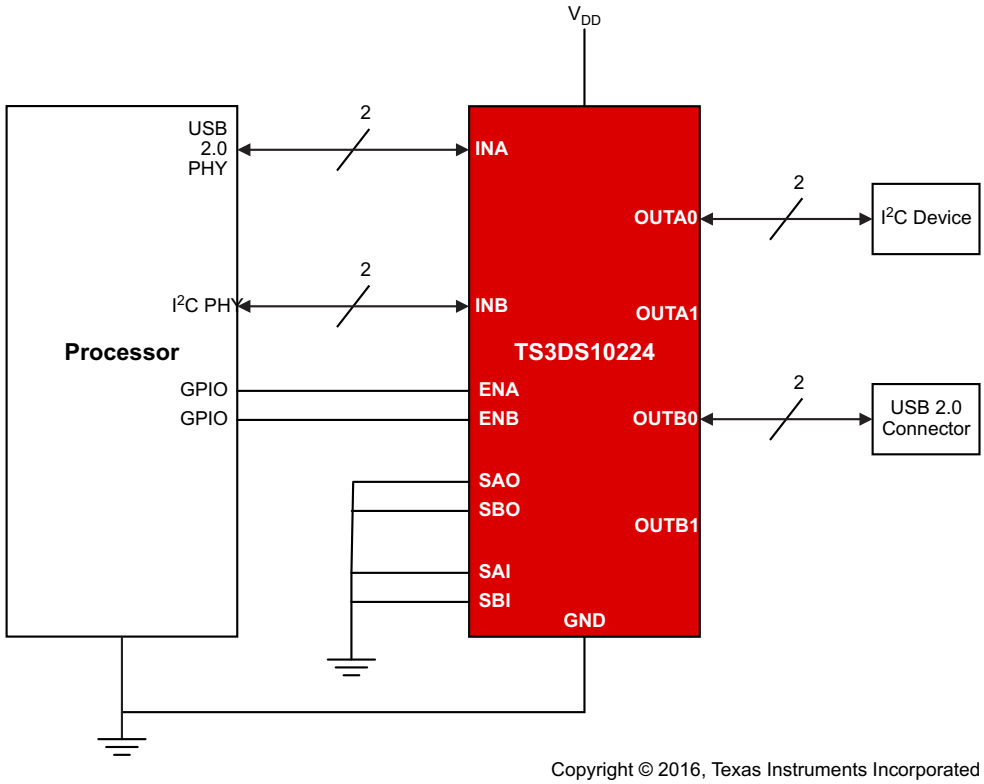


Figure 21. 2-Channel Differential Crosspoint Switch Schematic

Typical Applications (continued)

9.2.2.1 Design Requirements

TI recommends that the digital control pins SAI, SBI, SAO, and SBO be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from a floating pin. Unused pins for the signal paths INA, INB, OUTAx, and OUTBx must be terminated with a 50-Ω resistor to ground to reduce signal reflections in high-speed applications.

9.2.3 Fan-Out Switch

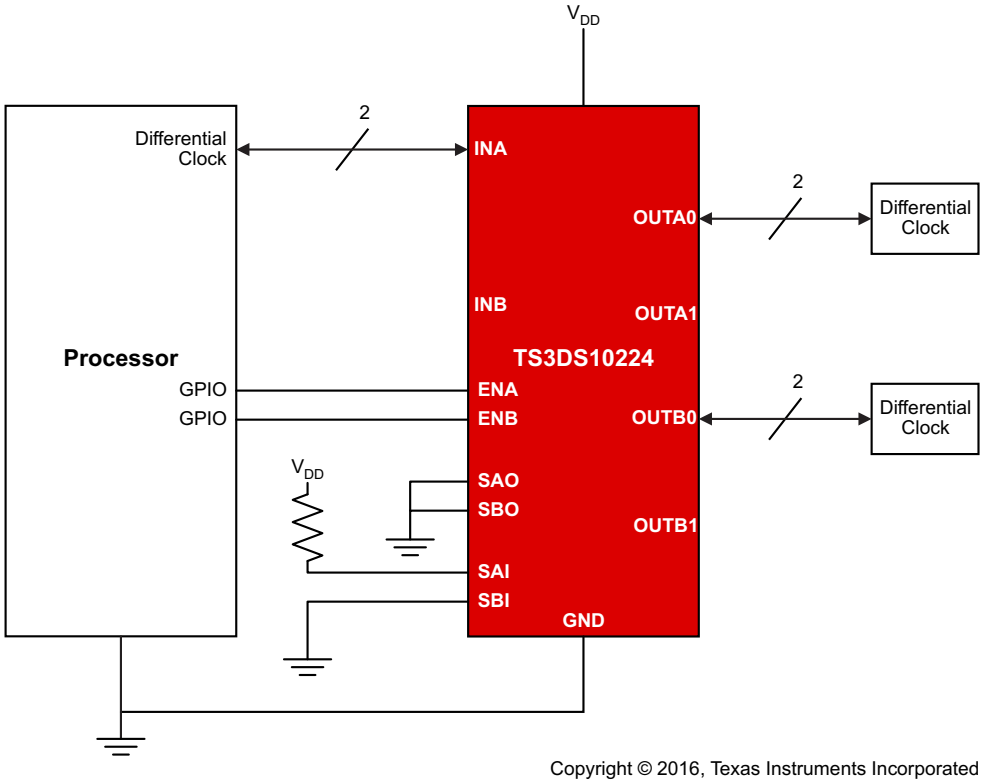


Figure 22. Fan-Out Switch Schematic

9.2.3.1 Design Requirements

TI recommends that the digital control pins SAI, SBI, SAO, and SBO be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin. Unused pins for the signal paths INA, INB, OUTAx, OUTBx must be terminated with a 50-Ω resistor to ground to reduce signal reflections in high-speed applications.

The bandwidth performance is lower in this application (500 MHz).

Typical Applications (continued)

9.2.4 2-Channel Differential 1:2 SPDT Switch

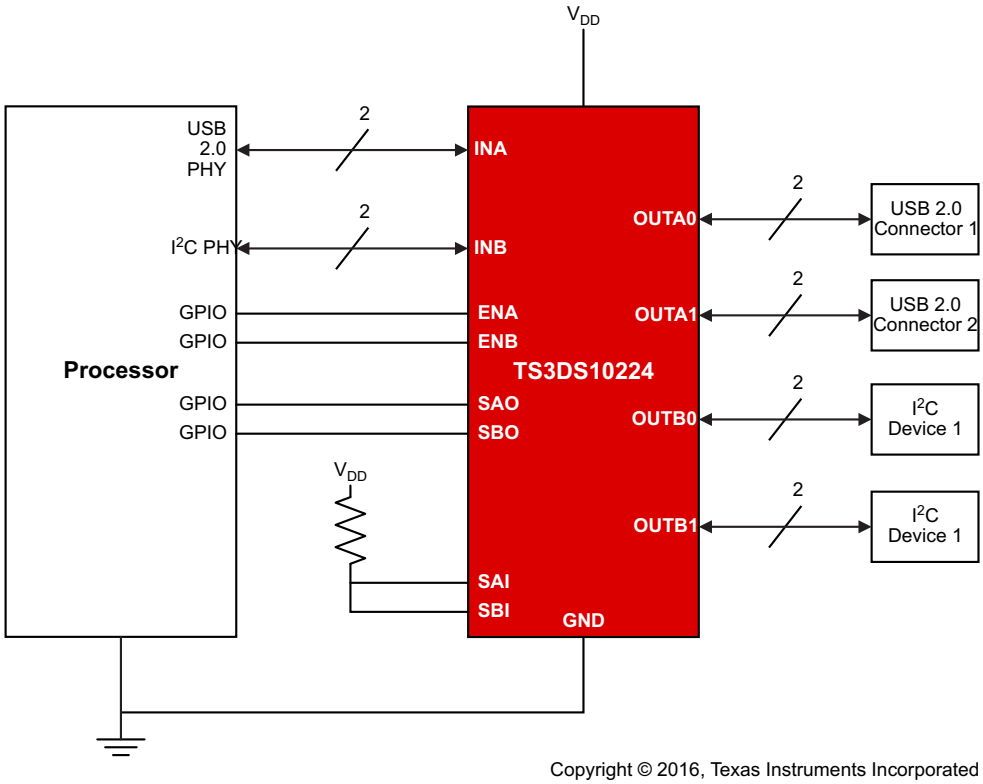


Figure 23. 2-Channel Differential 1:2 SPDT Switch Schematic

10 Power Supply Recommendations

Power to the device is supplied through the VCC pin and must be within the recommended operating voltage range. TI recommends a bypass capacitor be placed as close to the supply pin (VCC) as possible to help smooth out lower frequency noise and to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

- The thermal pad may be left floating or connected to the ground plane
- Place supply-bypass capacitors as close to the VCC pin as possible and avoid placing the bypass capacitors near the positive and negative traces.
- The high-speed positive and negative traces must always be matched and the lengths must not exceed 4 inches; otherwise, the eye diagram performance may be degraded. In layout, the impedance of positive and negative traces must match the cable characteristic differential impedance for optimal performance.
- Route the high-speed signals using a minimum of vias and corners to reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.
- Avoid stubs on the high-speed signal traces because they cause signal reflections.
- Route all high-speed signal traces over continuous GND planes, with no interruptions.
- Avoid crossing over anti-etch, commonly found with plane splits.
- Due to high-frequency signal traces, TI recommends a printed-circuit board with at least four layers; two signal layers separated by a ground and power layer as shown in Figure 24.

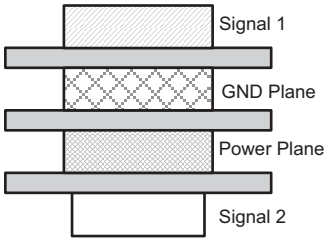


Figure 24. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

11.2 Layout Example

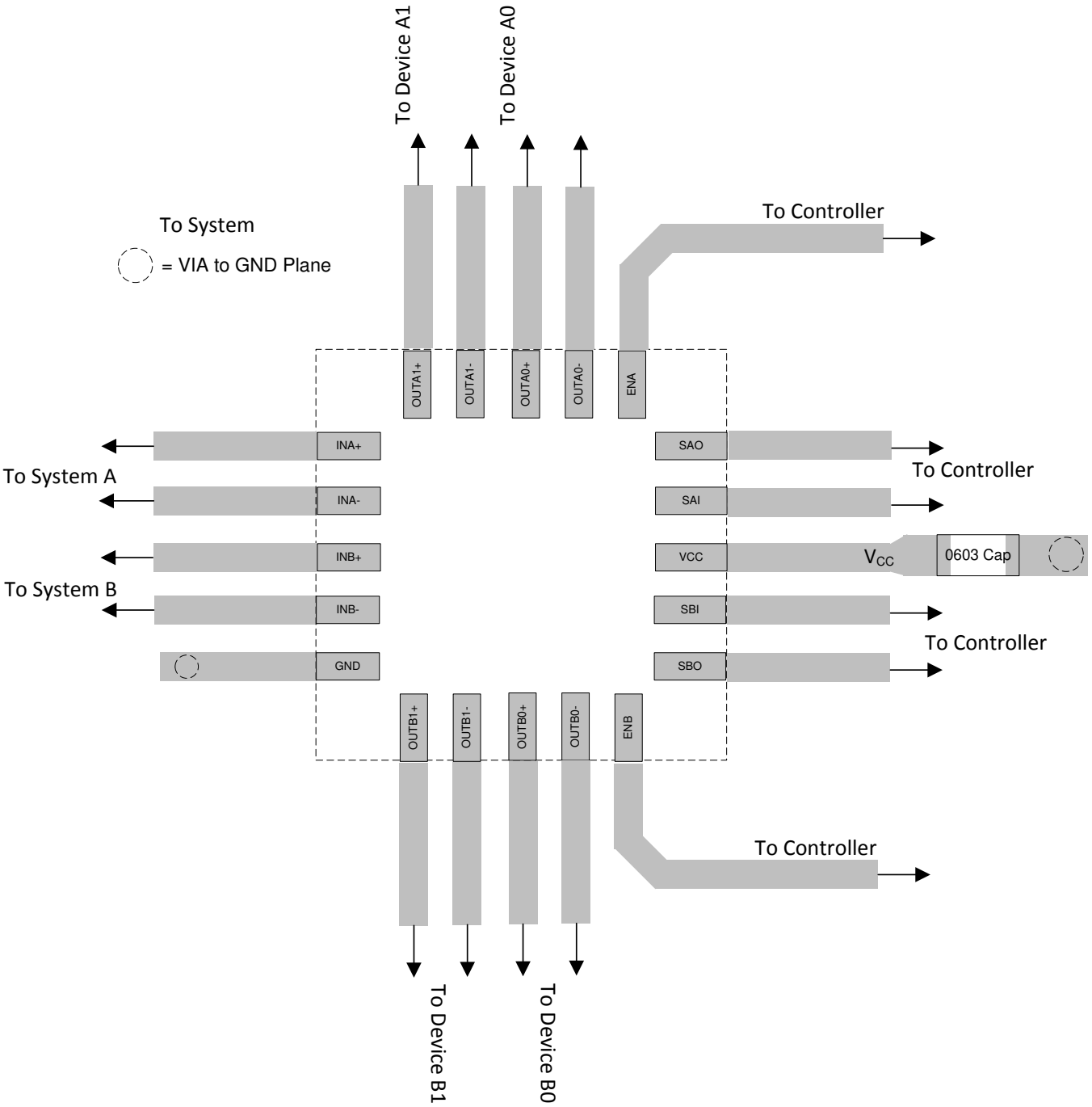


Figure 25. WQFN Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

《慢速或浮点 CMOS 输入的影响》(SCBA004)。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 商标

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12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DS10224RUKR	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

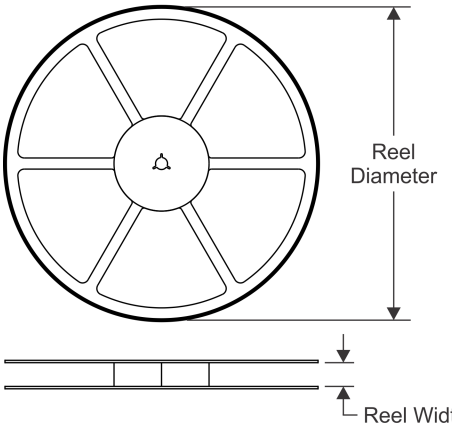
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

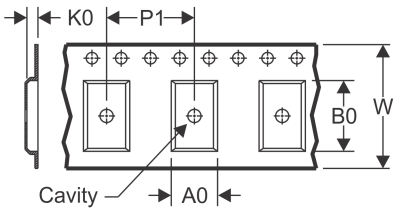
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

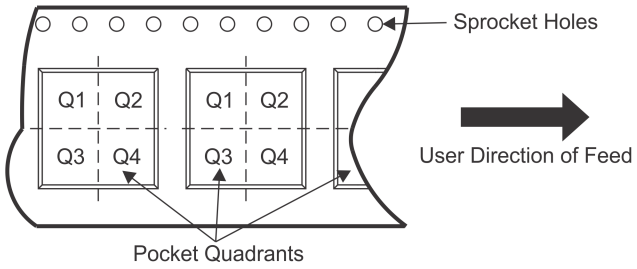


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

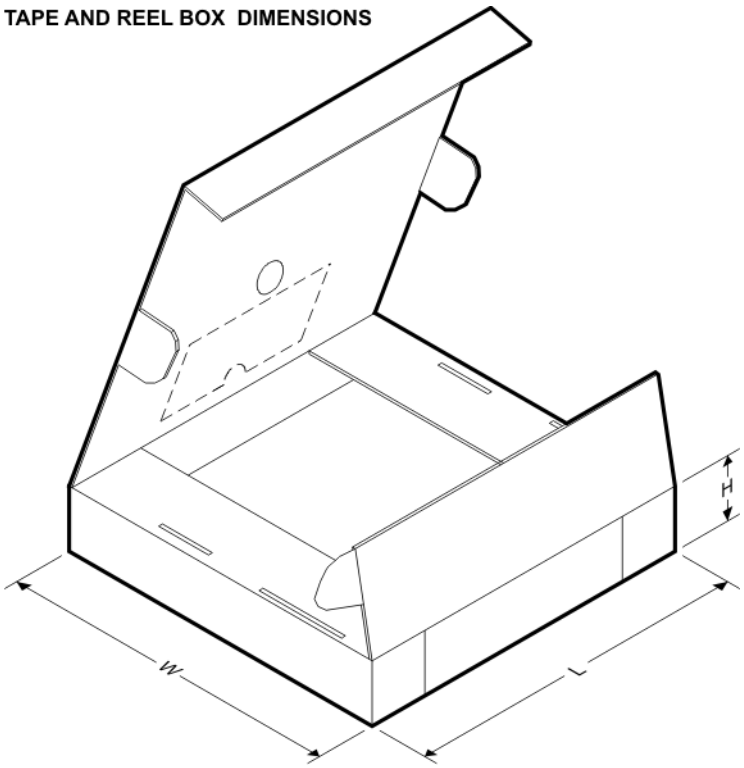
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DS10224RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

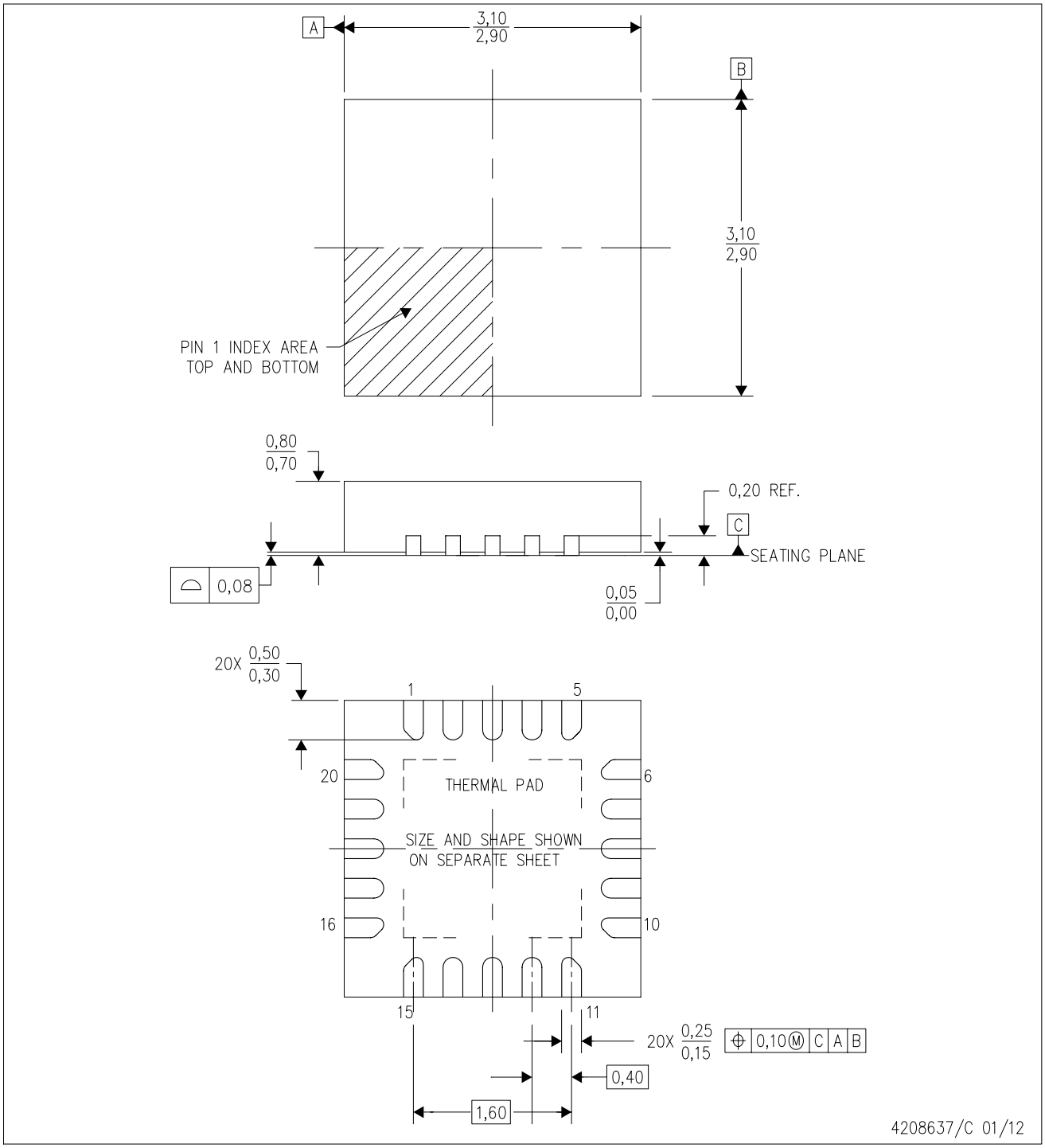
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DS10224RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

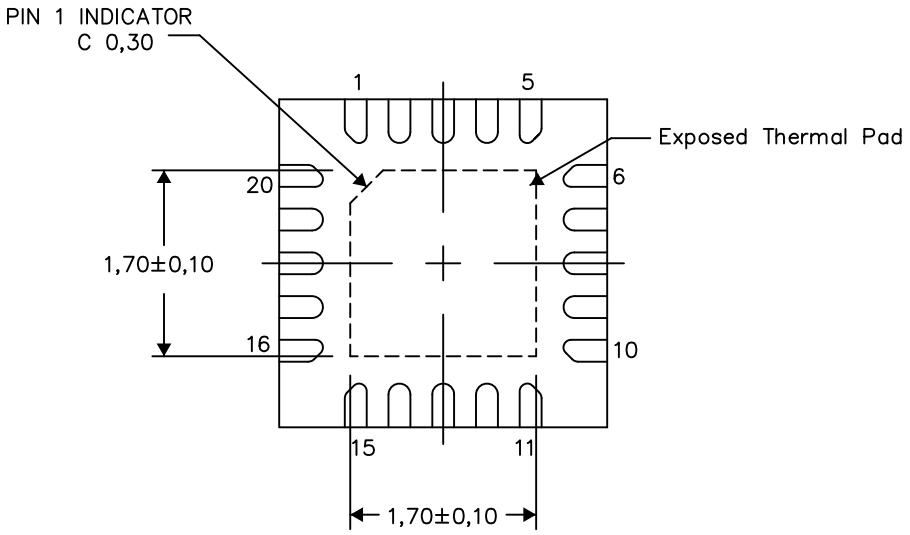
RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



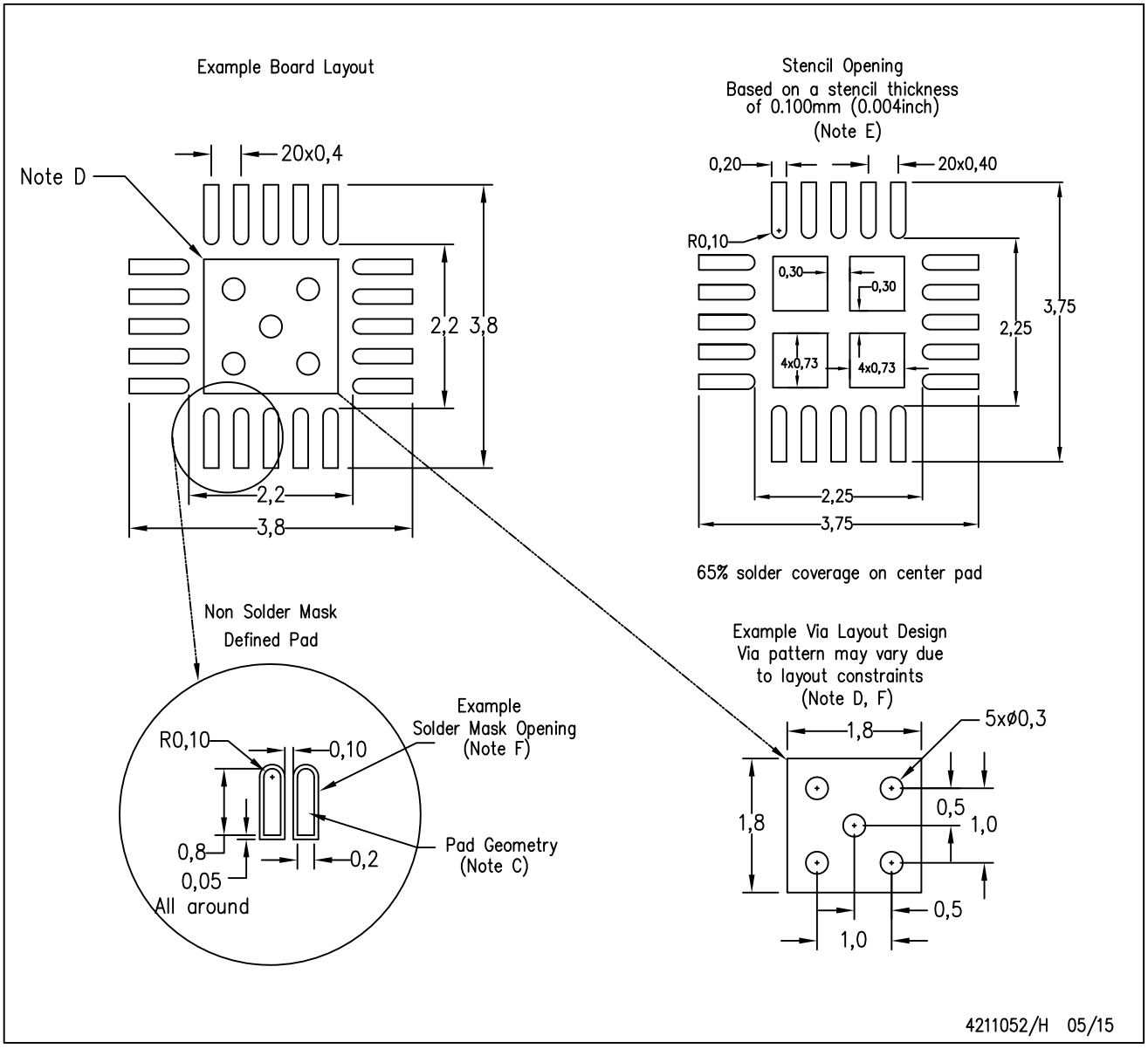
Bottom View

Exposed Thermal Pad Dimensions

4209762/I 05/15

NOTE: All linear dimensions are in millimeters

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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