SN74CBTU4411 11 位 4 选 1 多路复用器/多路信号分离器 具有电荷泵和预充电输出的 1.8V DDR-II 开关

1 特性

- 支持 SSTL_18 信号传输级别
- 适用于 DDR-II 应用
- D 端口输出由偏置电压 (V_{BIAS}) 预充
- 用于控制输入的内部终端
- 高带宽（最低 400MHz）
- 平缓的低导通电阻 (r_{on}) 特性，（r_{on} = 最大 17Ω）
- 内部 400Ω 下拉电阻器
- 低差分，上升沿或下降沿偏斜
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- ATCA 解决方案
- 自动体外除颤器
- 自适应照明
- 血液气体分析器：便携式
- 蓝牙耳机
- CT 扫描仪
- 摄像机：监控模拟
- 化学和气体传感器
- DLP 3D 机器视觉和光纤网络

3 说明

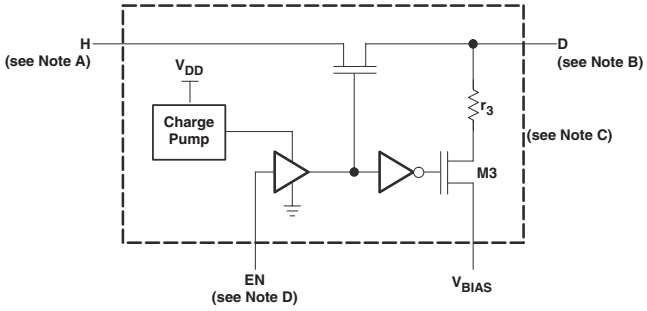
SN74CBTU4411 器件是一种具备低导通状态电阻 (r_{on}) 的高带宽 SSTL_18 兼容型 FET 多路复用器/多路信号分离器。此器件借助内部电荷泵提高通道晶体管的栅极电压，提供平缓的低 r_{on}。平缓的低 r_{on} 可实现最短传播延迟，并且支持数据输入/输出 (I/O) 端口的轨至轨信号传输。此外，该器件还 具备 极低的数据 I/O 电容，能够尽可能减少数据总线上的容性负载以及信号失真现象。通道间相互匹配的 r_{on} 和 I/O 电容会形成超低差分以及上升沿或下降沿偏斜。得益于此，该器件可在 DDR-II 应用中表现出最佳 性能。

器件信息(1)

器件型号	封装	封装尺寸
SN74CBTU4411ZST	NFBGA (72)	7.00mm × 7.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

每个 **FET** 开关 **(SW1)** 的简化原理图



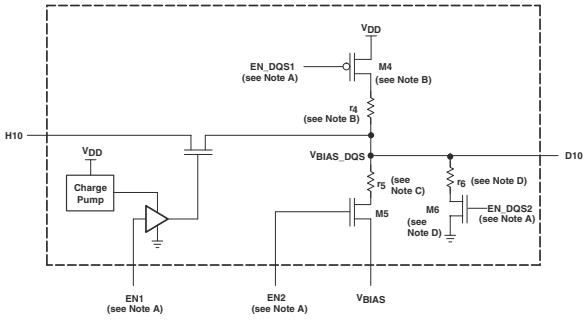
A. 适用于端口 H0 到 H9

B. 适用于端口 D0 到 D9

C. r_3 + r_{on} (M3) = 400Ω（典型值）。

D. EN 是应用于开关的内部启用信号。

每个 **FET** 开关 **(SW2)** 的简化原理图



A. EN_DQS1、EN_DQS2、EN1 和 EN2 是应用于开关的内部启用信号。

B. r_4 + r_{on} (M4) = 1kΩ（典型值）。

C. r_5 + r_{on} (M5) = 400Ω（典型值）。

D. r_6 + r_{on} (M6) = 2.3kΩ（典型值）。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (February 2016) to Revision B **Page**

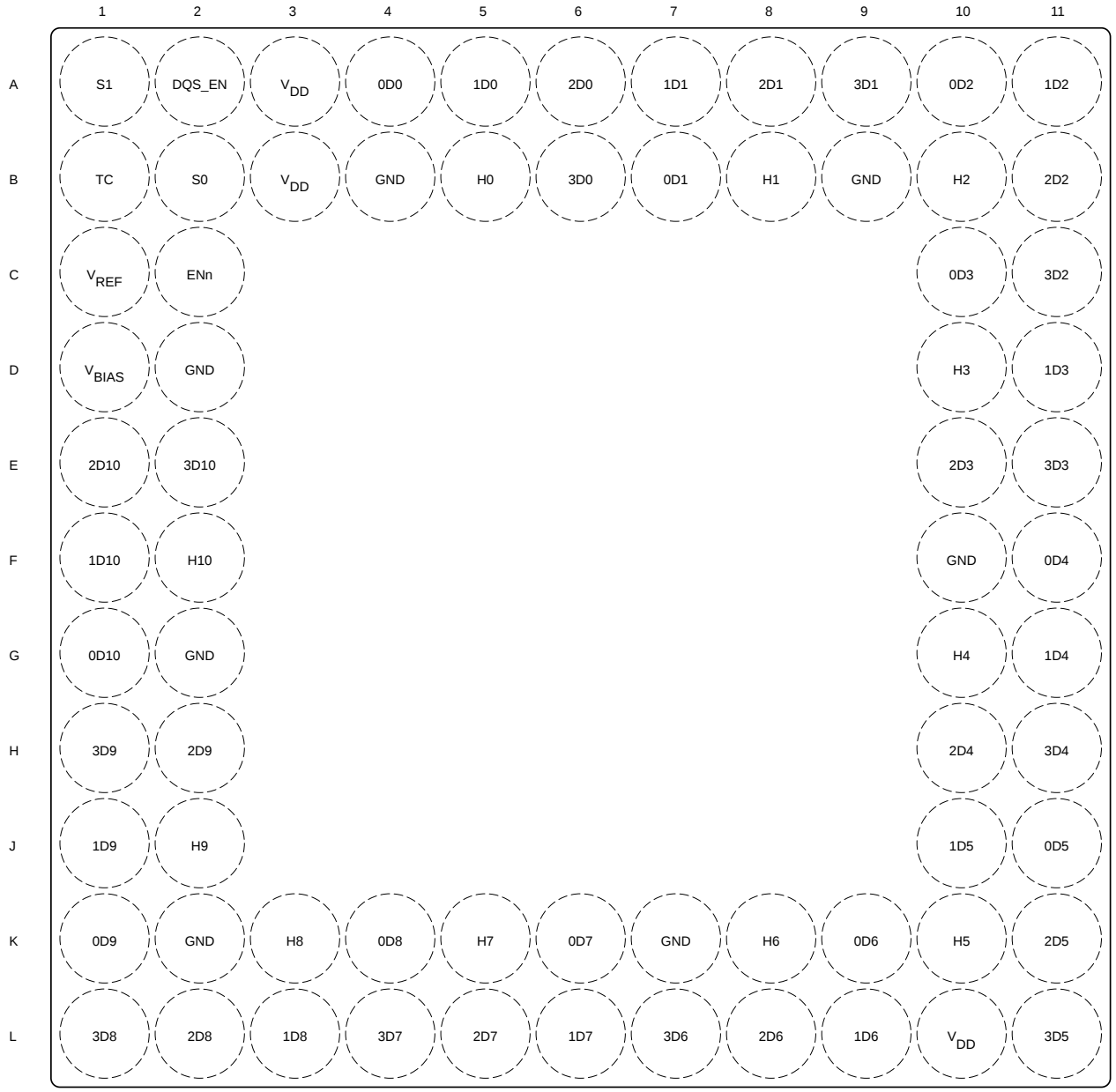
- Changed the V_{BIAS} MAX value From: 0.33 × V_{DD} To: V_{DD} in the *Recommended Operating Conditions* table ... 6

Changes from Original (April 2005) to Revision A **Page**

- 添加了 *ESD 额定值*表、*特性 说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分，*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Removed *Pin Assignments* table due to updated *Pin Out Drawing* ... 3

5 Pin Configuration and Functions

ZST Package
72-Pin NFBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
S0	B2	I	Select input control
S1	A1	I	Select input control
V_{DD}	A3, B3, L10	—	Power supply
GND	B4, B9, F10, K7, K2, G2, D2	—	Ground

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TC	B1	I	Termination control input
DQS_EN	A2	I	D10 port output voltage control
H0	B5	I/O	H port0
H1	B8	I/O	H port1
H2	B10	I/O	H port2
H3	D10	I/O	H port3
H4	G10	I/O	H port4
H5	K10	I/O	H port5
H6	K8	I/O	H port6
H7	K5	I/O	H port7
H8	K3	I/O	H port8
H9	J2	I/O	H port9
H10	F2	I/O	H port10
0D0	A4	I/O	D0 port0
1D0	A5	I/O	D0 port1
2D0	A6	I/O	D0 port2
3D0	B6	I/O	D0 port3
0D1	B7	I/O	D1 port0
1D1	A7	I/O	D1 port1
2D1	A8	I/O	D1 port2
3D1	A9	I/O	D1 port3
0D2	A10	I/O	D2 port0
1D2	A11	I/O	D2 port1
2D2	B11	I/O	D2 port2
3D2	C11	I/O	D2 port3
0D3	C10	I/O	D3 port0
1D3	D11	I/O	D3 port1
2D3	E10	I/O	D3 port2
3D3	E11	I/O	D3 port3
0D4	F11	I/O	D4 port0
1D4	G11	I/O	D4 port1
2D4	H10	I/O	D4 port2
3D4	H11	I/O	D4 port3
0D5	J11	I/O	D5 port0
1D5	J10	I/O	D5 port1
2D5	K11	I/O	D5 port2
3D5	L11	I/O	D5 port3
0D6	K9	I/O	D6 port0
1D6	L9	I/O	D6 port1
2D6	L8	I/O	D6 port2
3D6	L7	I/O	D6 port3
0D7	K6	I/O	D7 port0
1D7	L6	I/O	D7 port1
2D7	L5	I/O	D7 port2
3D7	L4	I/O	D7 port3
0D8	K4	I/O	D8 port0

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
1D8	L3	I/O	D8 port1
2D8	L2	I/O	D8 port2
3D8	L1	I/O	D8 port3
0D9	K1	I/O	D9 port0
1D9	J1	I/O	D9 port1
2D9	H2	I/O	D9 port2
3D9	H1	I/O	D9 port3
0D10	G1	I/O	D10 port0
1D10	F1	I/O	D10 port1
2D10	E1	I/O	D10 port2
3D10	E2	I/O	D10 port3
ENn	C2	I	Active low enable input
V_{BIAS}	D1	—	Bias voltage
V_{REF}	C1	—	Reference voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	2.5	V
V_{IN}	Control input voltage(2)(3)		–0.5	2.5	V
$V_{I/O}$	Switch I/O voltage(2)(3)(4)		–0.5	2.5	V
I_{IK}	Control input clamp current	$V_{IN} < 0$ or $V_{IN} > 0$		±50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$ or $V_{I/O} > 0$		±50	mA
$I_{I/O}$	ON-state switch current(5)			±100	mA
	Continuous current through V_{DD} or GND pins			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		1.7	1.8	1.9	V
V_{REF}	Reference supply voltage		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V
V_{BIAS}	BIAS supply voltage		0	0.3 × V_{DD}	V_{DD}	V
V_{IH}	High-level control input voltage	S	V_{REF} + 250 mV			V
		$\overline{EN}$, TX, DQS_EN	0.65 × V_{DD}			
V_{IL}	Low-level control input voltage	S			V_{REF} – 250 mV	V
		$\overline{EN}$, TX, DQS_EN			0.35 × V_{DD}	
$V_{I/O}$	Data input/output voltage		0		V_{DD}	V
T_A	Operating free-air temperature		0		85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC(1)		SN74CBTU4411 ZST (NFBGA) 72 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Minimum and maximum limits apply for T_A = 0°C to 85°C (unless otherwise noted). Typical limits apply for V_{DD} = 1.8 V and T_A = 25°C (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}(2)	Control inputs(3)	V_{DD} = 1.7 V, I_{IN} = –18 mA				–1.8	V
V_{BIAS_DQS}	D10	V_{DD} = 1.7 V, DQS_EN = V_{DD}		1.1		1.275	V
V_{OH}	D10	V_{DD} = 1.7 V, DQS_EN = V_{DD}, $\overline{EN}$ = V_{DD}, I_O = 100 µA			1.6	1.8	V
I_{IN}	Control inputs(3)	V_{DD} = 1.9 V, V_{IN} = V_{DD} or GND				±1	µA
I_{OZ}(4)		V_{DD} = 1.9 V, V_O = 0 to 1.9 V, V_I = 0, Switch OFF, V_{BIAS} open				±10	µA
I_{CC}		V_{DD} = 1.9 V, TC = GND, $\overline{EN}$ = GND, $I_{I/O}$ = 0, S0 or S1 input switching at 50% duty cycles, Data I/O are open			0.7	2.5	mA
		$\overline{EN}$ = V_{DD}				500	µA
I_{CCD}		V_{DD} = 1.9 V, TC = GND, $\overline{EN}$ = GND, $I_{I/O}$ = 0, S0 or S1 input switching at 50% duty cycle, Data I/O are open				0.5	mA/MHz(5)
C_{in}	S port	V_{DD} = 1.9 V, TC = GND, $\overline{EN}$ = GND, V_{IN} = V_{REF} ± 250 mV		2.5		3.5	pF
	$\overline{EN}$, TC, DQS_EN inputs	V_{DD} = 1.9 V, V_{IN} = 0 or 1.9 V			2.5		
$C_{io(OFF)}$	H port	$V_{I/O}$ = 0.5 × V_{DD} ± 0.4 V, Switch OFF, V_{BIAS} open				2.5	pF
$C_{io(ON)}$		$V_{I/O}$ = 0.5 × V_{DD} ± 0.4 V, Switch ON, V_{BIAS} = GND				4.6	pF
r_{on}(6)		V_{DD} = 1.7 V, V_I = 0.5 × V_{DD} ± 0.5 V, I_O = 10 mA		6	10	17	Ω
$\Delta r_{on(flat)}$(7)		V_{DD} = 1.7 V, DQS_EN = V_{DD}, I_O = 10 mA	V_I = 0.5 V_{DD} ± 0.25 V		1.5	3	Ω
			V_I = 0.5 V_{DD} ± 0.5 V		2.5	5	
r_{term}	S port	V_{DD} = 1.7 V		110	160	210	Ω
$r_{pulldown}$	D0–D10	V_{DD} = 1.7 V	DQS_EN = GND	280	400	520	Ω
	D10		DQS_EN = V_{DD}, $\overline{EN}$ = GND	1600	2300	3000	
r_{pullup}	D10	V_{DD} = 1.7 V, DQS_EN = V_{DD}, $\overline{EN}$ = GND		700	1000	1300	Ω

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) V_{IK} refers to the clamp voltage due to the internal diode, which is connected from each control input to GND.
(3) For the leakage current test on S0 and S1, $\overline{EN}$ and TC inputs are set to low.
(4) For I/O ports, the parameter I_{OZ} includes the input leakage current. I_{OZ} applies only to the H port.
(5) This frequency of S0 and S1 inputs, for example, for a data I/O rate of 533 Mbit/s, with a burst of 4, the required frequency is for S0 or S1 input is ≅ 66 MHz (533/8). The total I_{CC} due to switching S0, S1 will be approximately 27 mA (66 MHz × 0.4 mA/MHz).
(6) Measured by the voltage drop between the D and H pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (D or H) pins.
(7) $\Delta r_{on(flat)}$ is the difference of maximum r_{on} and minimum r_{on} for a specific channel in a specific device.

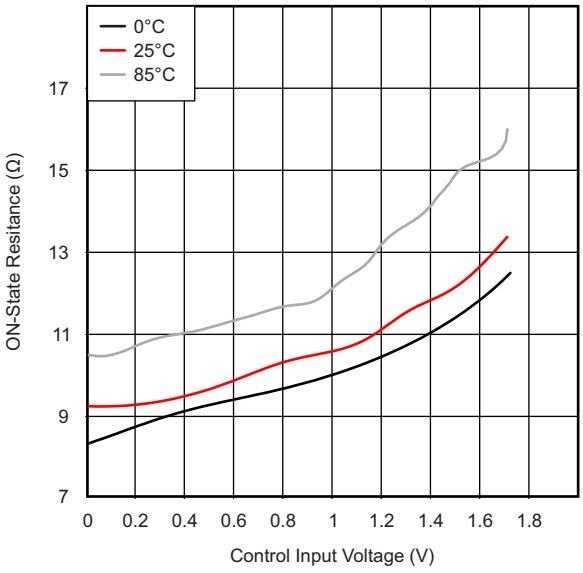
6.6 Switching Characteristics

T_A = 0°C to 85°C (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	D or H port		400			MHz
	S port(1)		84			
t_{pd}		From D or H (input) to D or H (output)		297		ps
t_{en}(t_{PZL}, t_{PZH})(2)		From S (input) to D (output)	750		2100	ps
t_{dis}(t_{PLZ}, t_{PHZ})(2)		From S (input) to D (output)	750		2100	ps
t_{osk}					85	ps
t_{esk}					40	ps
t_{start}(3)				20		µs

(1) $\overline{EN}$ = GND, TC = GND
(2) V_{BIAS} = open
(3) t_{start} is the time required for the charge-pump circuit output voltage to reach a steady state value after V_{DD} is applied.

6.7 Typical Characteristic

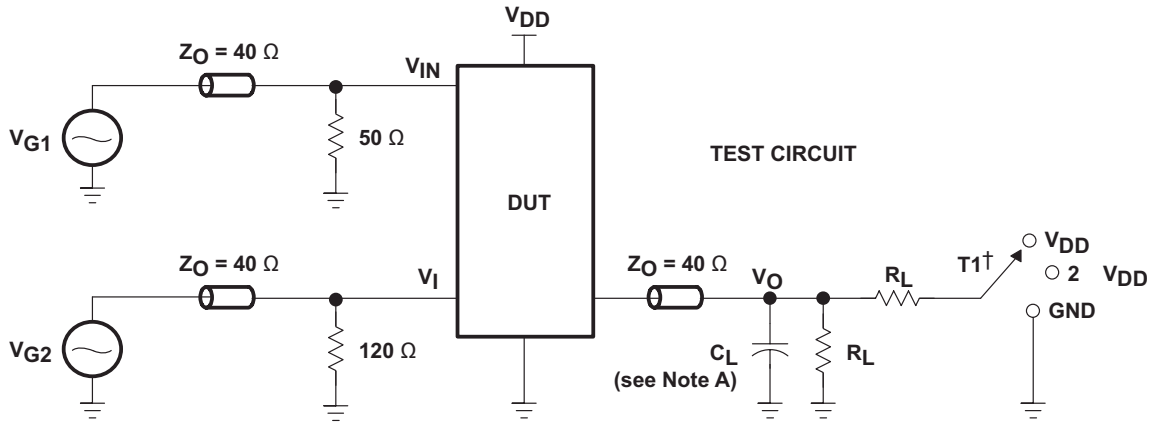


V_{IH} = 1.7 V V_{IL} = 0 V H0 to 0D0 at –10 mA

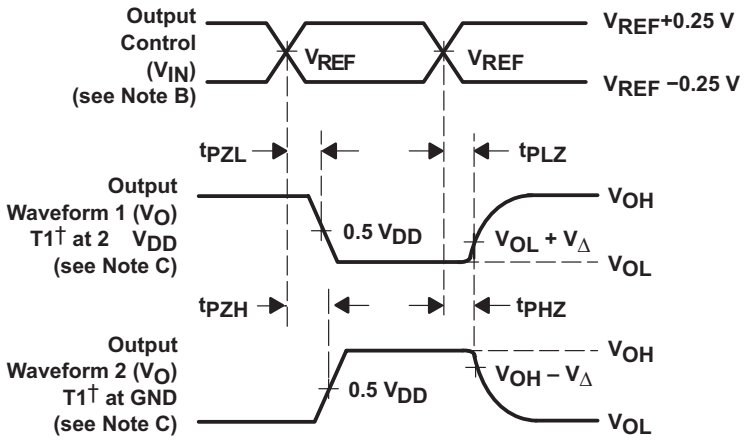
Figure 1. ON-State Resistance Across Temperature

7 Parameter Measurement Information

7.1 Enable and Disable Times



TEST	V_{DD}	T1†	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	1.8 V ± 0.1 V	2 × V_{DD}	1 kΩ	GND	6 pF	0.125 V
t_{PHZ}/t_{PZH}	1.8 V ± 0.1 V	GND	1 kΩ	V_{DD}	6 pF	0.125 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

† T1 is an external terminal.

A. C_L includes probe and jig capacitance.

B. Output control applies to select (S0, S1) inputs.

C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

D. All input pulses are supplied by generators having the following characteristics: Z_{OS} = 50 Ω, rising and falling edge rate is 1 V/ns.

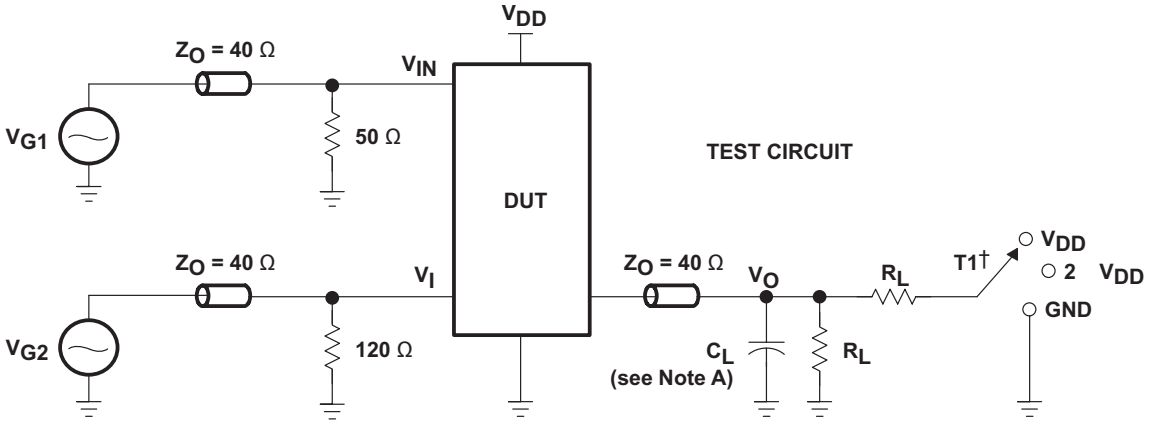
E. The outputs are measured one at a time, with one transition per measurement.

F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

G. t_{PZL} and t_{PZH} are the same as t_{en}.

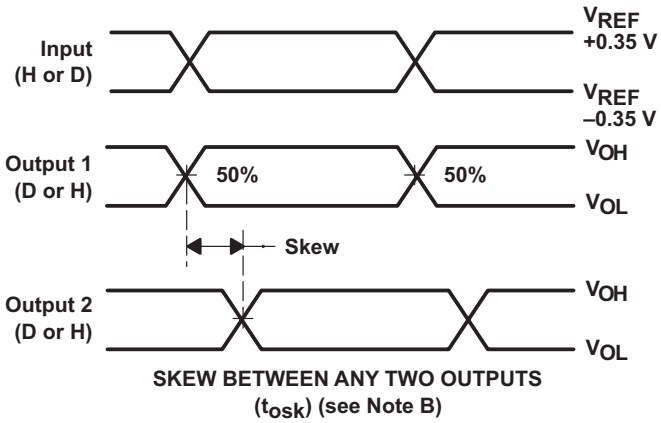
Figure 2. Test Circuit and Voltage Waveforms

7.2 Skew and Propagation Delay Times

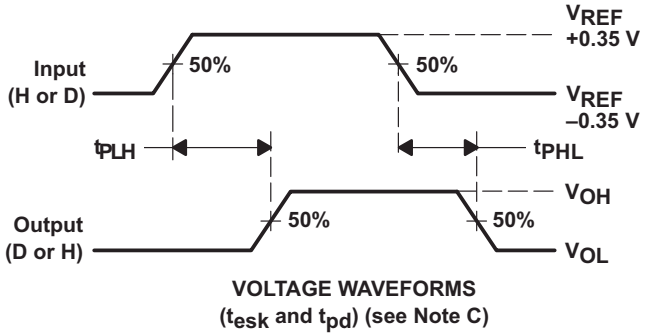


TEST	V_{DD}	T1†	R_L	V_I	C_L
t_{pd}	1.8 V ± 0.1 V	V_{DD}	150 Ω	See waveform	6 pF
t_{osk}	1.8 V ± 0.1 V	V_{DD}	150 Ω	See waveform	6 pF
t_{esk}	1.8 V ± 0.1 V	V_{DD}	150 Ω	See waveform	6 pF

† T1 is an external terminal.



SKEW BETWEEN ANY TWO OUTPUTS
(t_{osk}) (see Note B)



VOLTAGE WAVEFORMS
(t_{esk} and t_{pd}) (see Note C)

A. C_L includes probe and jig capacitance.

B. t_{osk} is the difference in output voltage from channel to channel in a specific device.

C. t_{PLH} and t_{PHL} are the same as t_{pd} and $t_{esk} = |t_{PLH} – t_{PHL}|$

D. All input pulses are supplied by generators having the following characteristics: Z_{OS} = 50 Ω, rising and falling edge rate is 1 V/ns.

E. The outputs are measured one at a time, with one transition per measurement.

Figure 3. Test Circuit and Voltage Waveforms

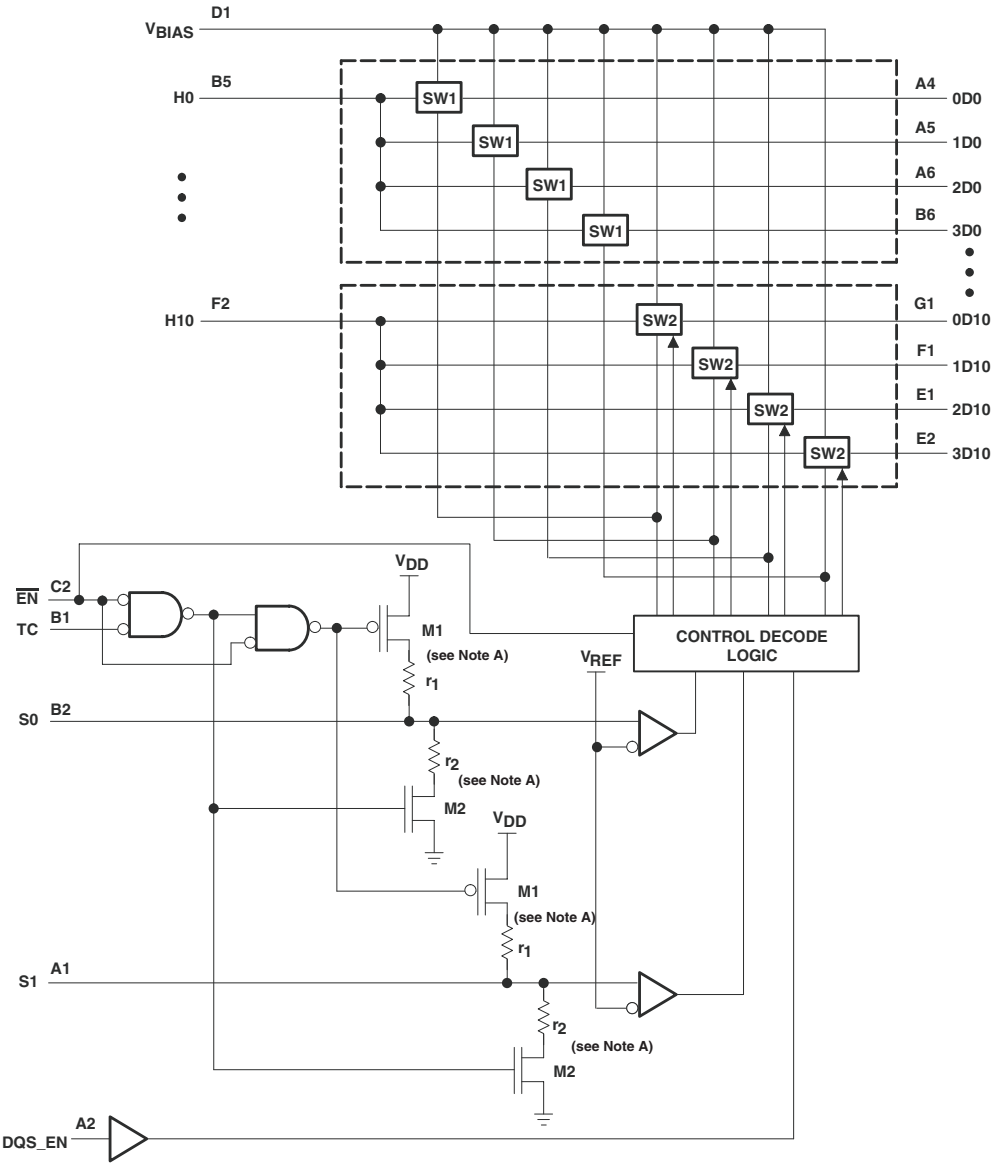
8 Detailed Description

8.1 Overview

The SN74CBTU4411 device is organized as an 11-bit 1-of-4 multiplexer/demultiplexer with a single switch-enable ($\overline{EN}$) input. When $\overline{EN}$ is low, the switch is enabled and the H port is connected to one of the D ports. Ports D0 to D9 for the disabled channels are connected to V_{BIAS} through a 400-Ω resistor. DQS_EN determines the output voltage for the disabled D10 ports. When DQS_EN is low, this voltage is V_{BIAS}. When DQS_EN is high, the disabled D10 ports are connected to an internal voltage (V_{BIAS_DQS}) source, which is approximately equal to 0.7 V_{DD}.

When $\overline{EN}$ is high, all the channels are disabled. Ports D0 to D9 are connected to V_{BIAS}. For the D10 port, the disabled output voltage is determined by the DQS_EN input. When DQS_EN is low, this voltage is V_{BIAS}. When DQS_EN is high, this voltage is V_{DD}

8.2 Functional Block Diagram



A. $r_1 + r_{on}$ (M1), $r_2 + r_{on}$(M2) = 160 Ω typical

Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. The $\overline{EN}$ and TC inputs determine the internal termination for S0 and S1 inputs. When $\overline{EN}$ is low, the termination is determined by the TC input. When both $\overline{EN}$ and TC are low, termination resistors are disconnected from the S inputs. When $\overline{EN}$ is low and TC is high, both pullup and pulldown resistors are connected to the S inputs. When $\overline{EN}$ is high, only the pulldown termination resistors are connected to the S inputs, regardless of the voltage level at the TC input.

8.4 Device Functional Modes

Table 1 and Table 2 lists the functional modes of the SN74CBTU4411.

Table 1. Function Table

INPUTS				INPUT/OUTPUT Hn	FUNCTION
$\overline{EN}$	DQS_EN	S1	S0		
L	L	L	L	0Dn	Hn = 0Dn 1Dn, 2Dn, 3Dn connected to V_{BIAS}
L	L	L	H	1Dn	Hn = 1Dn 0Dn, 2Dn, 3Dn connected to V_{BIAS}
L	L	H	L	2Dn	Hn = 2Dn 0Dn, 1Dn, 3Dn connected to V_{BIAS}
L	L	H	H	3Dn	Hn = 3Dn 0Dn, 1Dn, 2Dn connected to V_{BIAS}
L	H	L	L	0Dn	H0–H9 = 0D0–0D9 1D0–1D9, 2D0–2D9, 3D0–3D9 connected to V_{BIAS} H10 = 0D10 1D10, 2D10, 3D10 connected to V_{BIAS_DQS} (1)
L	H	L	H	1Dn	H0–H9 = 1D0–1D9 0D0–0D9, 2D0–2D9, 3D0–3D9 connected to V_{BIAS} H10 = 1D10 0D10, 2D10, 3D10 connected to V_{BIAS_DQS} (1)
L	H	H	L	2Dn	H0–H9 = 2D0–2D9 0D0–0D9, 1D0–1D9, 3D0–3D9 connected to V_{BIAS} H10 = 2D10 0D10, 1D10, 3D10 connected to V_{BIAS_DQS} (1)
L	H	H	H	3Dn	H0–H9 = 3D0–3D9 0D0–0D9, 1D0–1D9, 2D0–2D9 connected to V_{BIAS} H10 = 3D10 0D10, 1D10, 2D10 connected to V_{BIAS_DQS} (1)
H	L	X	X	Z	0Dn, 1Dn, 2Dn, 3Dn connected to V_{BIAS}
H	H	X	X	Z	0D0–0D9, 1D0–1D9, 2D0–2D9, 3D0–3D9 connected to V_{BIAS} 0D10, 1D10, 2D10, 3D10 connected to V_{DD}

(1) V_{BIAS_DQS} is an internal voltage condition.

Table 2. Function Table Continued

INPUTS		FUNCTION
$\overline{EN}$	TC	
L	L	Termination resistors disconnected from S inputs
L	H	Termination resistors connected with S inputs
H	X	Pulldown termination resistor connected and pullup termination resistor disconnected from the S inputs

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CBTU4411 is suitable for DDR-II applications where high-bandwidth is required. This device has low and flat ON resistance and have internal termination control inputs. The D-ports are precharged by Bias voltage.

9.2 Typical Application

SN74CBTU4411 is an 11 bit, 1:4 Mux and suitable for high-bandwidth applications.

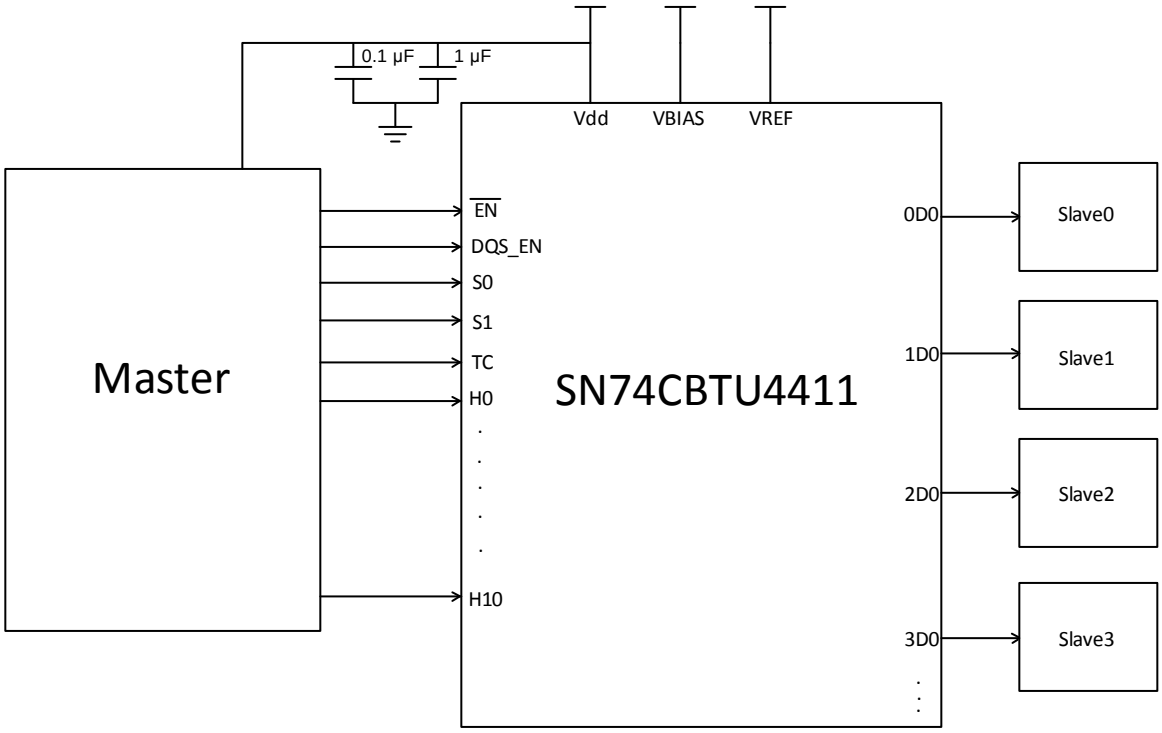


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

SN74CBTU4411 supports 400-MHz bandwidth on the D or H ports and 84 MHz on the S port. The Enable control from the master must be activated and depending on the select pins, the data is transferred into one of the slaves 0 to 3. The Enable control at high will tristate the Input / output as per the functional table. See *Recommended Operating Conditions* and *Absolute Maximum Ratings* for other voltage, current and handling parameters.

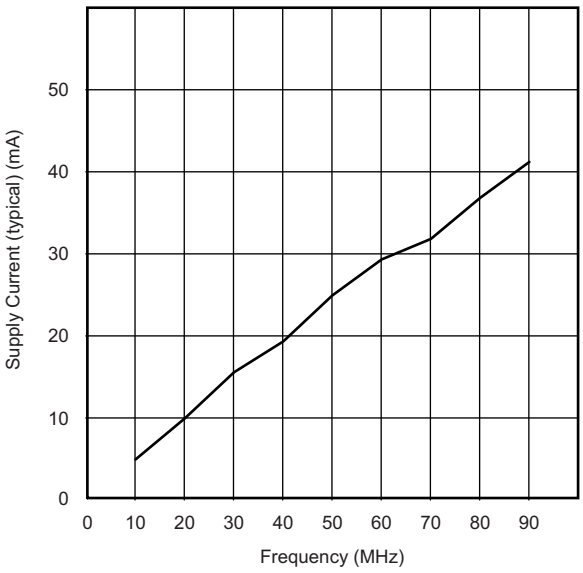
Typical Application (continued)

9.2.2 Detailed Design Procedure

The H port signal from the master can go to 1 of the 4 slave ports depending on the select inputs S0 and S1. The V_{BIAS} and V_{REF} can be determined from the *Recommended Operating Conditions*.

1. Recommended Input Conditions
   - For specified high and low levels for all the input control pins, see V_{IH} and V_{IL} in the *Recommended Operating Conditions*.
   - Inputs are not overvoltage tolerant and should be below the valid V_{DD}.
2. Recommend Input/Output Conditions
   - The absolute maximum continuous on state switch current for any I/O should not exceed ±100 mA
   - The I/O voltage range should not be above V_{DD} and below ground.

9.2.3 Application Curve



V_{CC} = 1.9 V T_A = 25°C

Figure 6. Supply Current (Typical) vs Frequency Data

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor. If there are multiple V_{CC} pins, TI recommends a 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Figure 7 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the I/Os, so they also cannot float when disabled.

11.2 Layout Example

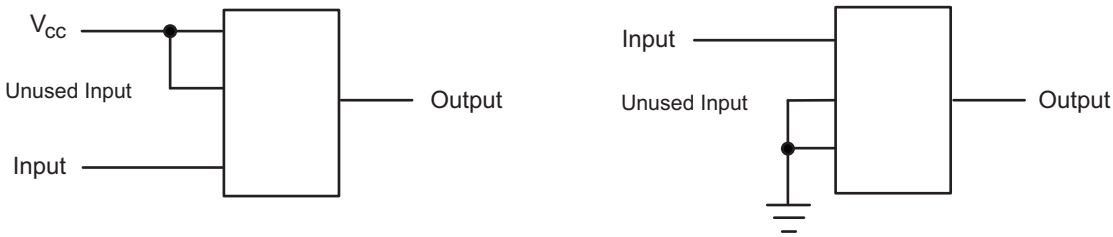


Figure 7. Layout Diagram

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

如需相关文档，请参阅应用报告《*慢速或浮点 CMOS 输入的影响*》(SCBA004)。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTU4411ZSTR	ACTIVE	NFBGA	ZST	72	2000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 85	CTU4411	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

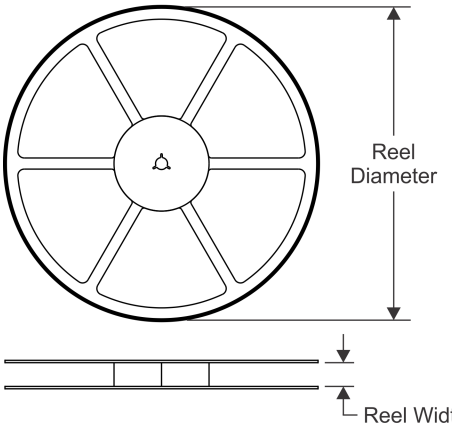
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

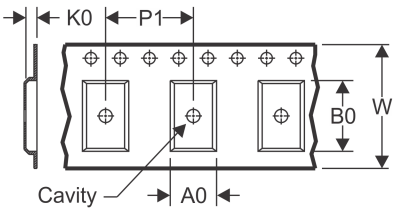
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

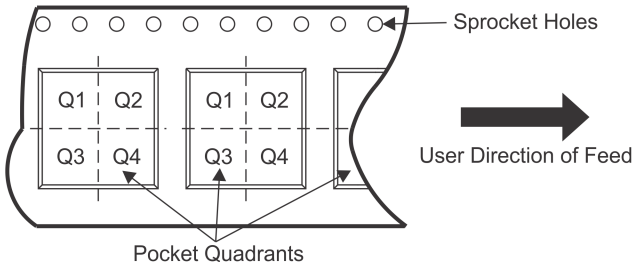


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

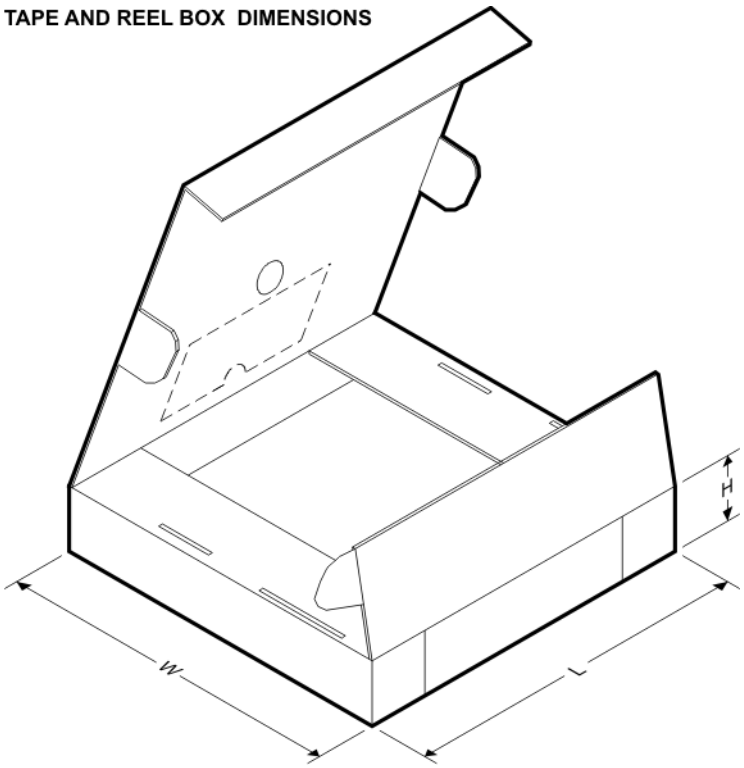
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTU4411ZSTR	NFBGA	ZST	72	2000	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

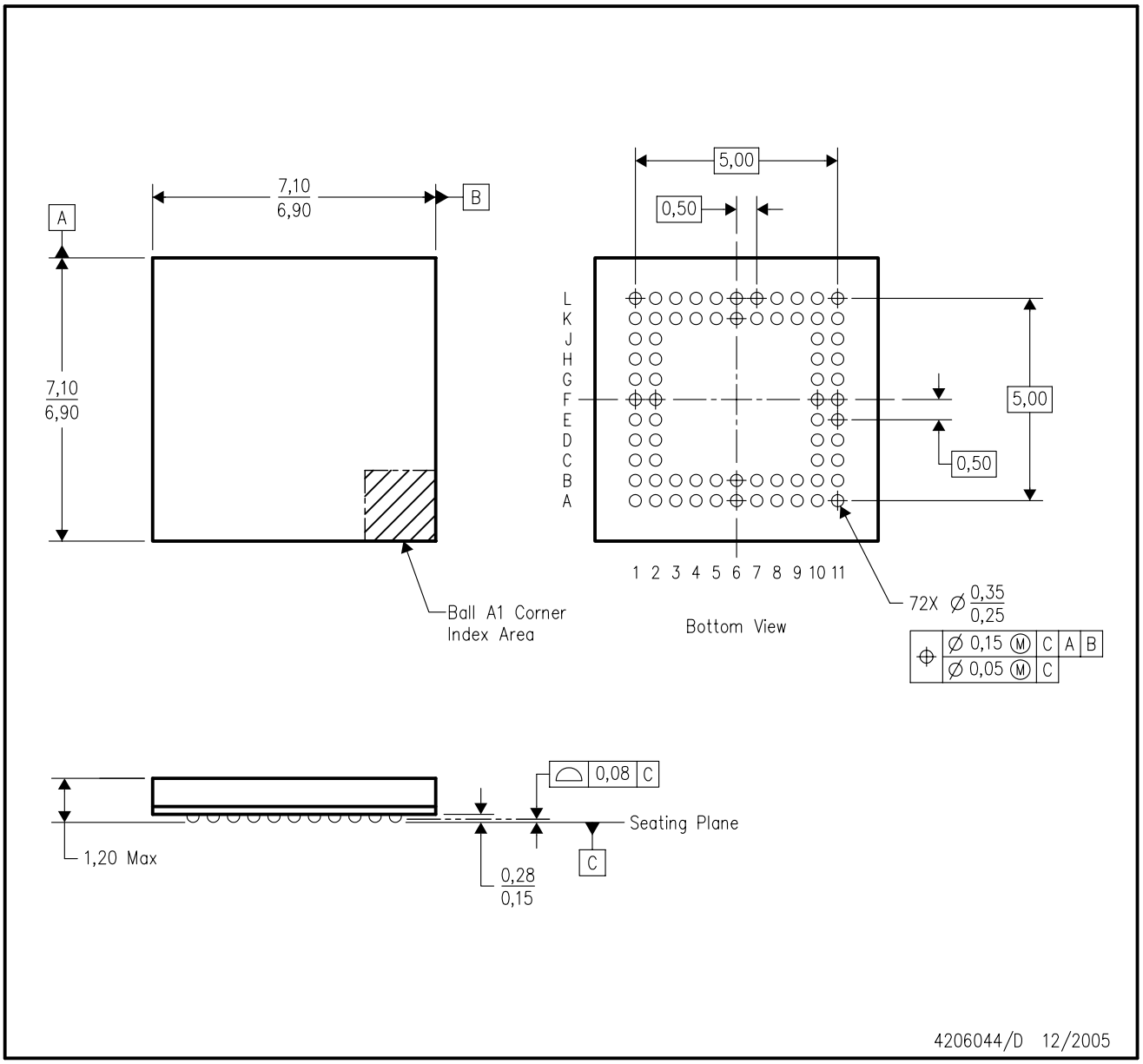
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTU4411ZSTR	NFBGA	ZST	72	2000	336.6	336.6	31.8

ZST (S–PBGA–N72) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Complies to JEDEC MO–195 variation AD (depopulated).
D. This package is lead–free. Refer to the 72 GST package (drawing 4206043) for tin–lead (SnPb).

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