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#### **TMP112-Q1**

ZHCSD10E - SEPTEMBER 2014 - REVISED DECEMBER 2018

#### **TMP112-Q1** 采用 **SOT563** 封装的汽车应用级高精度、 低功耗 数字温度传感器

#### 特性 1

- 具有符合 AEC-Q100 标准的下列特性:
  - 温度等级 1: -40°C 至 125°C 的环境工作温度 范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- SOT563 封装 (1.6mm × 1.6mm) 尺寸较 SOT23 减 小 68%
- 未经校准时的精度:
  - 0°C 到 65°C 时为 0.5°C (最大值)
  - -40°C 到 125°C 时为 1°C (最大值)
- 低静态电流:
  - 激活时 10μA (最大值)
  - 关断时 1µA(最大值)
- 电源电压范围: 1.4V 至 3.6V
- 分辨率: 12 位
- 数字输出:兼容 SMBus、双线制和 I<sup>2</sup>C 接口
- NIST 可追溯
- 应用 2
- 汽车空调
- 信息娱乐处理器管理
- 空气流量传感器
- 电池控制单元
- 引擎控制单元
- UREA 传感器
- 抽水机
- HID 灯
- 安全气囊控制单元

#### 简化原理图



## 3 说明

TMP112-Q1 器件是一款数字温度传感器,在要求高精 度的应用中是 NTC/PTC 热敏电阻的理想替代品。该器 件在未经校准或无外部组件信号调节的情况下可提供的 精度为 ±0.5℃。器件温度传感器为高度线性化产品, 无需复杂计算或查表即可得知温度。此器件还具有可提 高精度的校准功能,用户可借此功能将精度校准到 ± 0.17℃(请参阅校准以提高精度部分)。片载 12 位 模数转换器提供的分辨率低至 0.0625℃。

1.6mm x 1.6mm SOT563 封装尺寸较 SOT23 封装减 小 68%。TMP112-Q1 器件 特性 SMBus™、两线制和 I<sup>2</sup>C 接口兼容性,最多允许四个器件位于一条总线上。 此外,该器件还 特性 SMBus 报警功能。器件的额定 工作电压范围是 1.4V 至 3.6V, 整个工作范围内最大 静态电流为 10µA。

TMP112-Q1 器件非常适用于控制单元、温度控制、信 息娱乐和传感器模块等应用中的扩展温度测量。器件的 额定工作温度范围为 -40℃ 至 +125℃。

TMP112-Q1 生产单元已经过 100% 的传感器测试,具 有 NIST 可追溯的特点,并已借助 NIST 可追溯的设备 使用 ISO/IEC 17025 标准认可的校准要求进行验证。

	器件信息 <sup>(1)</sup>	
器件型号	封装	封装尺寸(标称值)
TMP112-Q1	SOT563 (6)	1.60mm x 1.20mm

(1) 如需了解所有可用封装,请参阅数据表末尾的可订购产品附 录。



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CI	hanges from Revision D (December 2015) to Revision E	Page
•	Updated description for ADD0 pin for connection to SDA and SCL	4
•	Changed supply voltage maximum value from: 5 V to: 4 V	4
•	Changed input voltage maximum value for the SCL, ADD0, and SDA pins from: 5 V to: 4 V	4
•	Changed input voltage maximum value for the ALERT pin from: (V+) + 0.5 V to: (V+) + 0.3 and ≤ 4	4
•	Updated junction-to-ambient thermal resistance from 200 °C/W to 210.3 °C/W	5
•	Updated junction-to-case (top) thermal resistance from 73.7 °C/W to 105.0 °C/W	5
•	Updated junction-to-board thermal resistance from 34.4 °C/W to 87.5 °C/W	5
•	Updated junction-to-top characterization parameter from 3.1 °C/W to 6.1 °C/W	5
•	Updated junction-to-board characterization parameter from 34.2 °C/W to 87.0 °C/W	5
•	添加了接收文档更新通知部分	28

## Changes from Revision C (March 2015) to Revision D

•	添加 NIST 特性 项目符号	1
•	己在 <i>说明</i> 部分添加了 WQFN (RUN) 封装	1

## Changes from Revision B (November 2014) to Revision C

•	更新了电路原理图上的引脚编号	1
•	Changed the Handling Ratings table to ESD Ratings and moved the storage temperature parameter to the Absolute Maximum Ratings table	4
•	Changed min, typ, max values for the Temperature Accuracy (temperature error) parameter	5
•	Changed the frequency from 2.85 to 3.4 MHz in the POWER SUPPLY section of the Electrical Characteristics table	6
•	Changed the Temperature Error at 25°C graph in the Typical Characteristics section	7
•	Changed the Temperature Error vs Temperature graph in the Typical Characteristics section	7

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## Changes from Revision A (October 2014) to Revision B

• 己更改 器件状态从 产品预览 更改为 量产数据......1

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## 5 Pin Configuration and Functions



#### **Pin Functions**

PIN		1/0	DESCRIPTION	
NO.	NAME	1/0	DESCRIPTION	
1	SCL	I	Serial clock. Open-drain output; requires a pullup resistor.	
2	GND	—	Ground	
3	ALERT	0	Overtemperature alert. Open-drain output; requires a pullup resistor.	
4	ADD0	I	Address select. Connect to V+, GND, SDA or SCL	
5	V+	I	Supply voltage, 1.4 V to 3.6 V	
6	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor.	

## 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	V+		4	V
Voltage at SCL, ADD0,	and SDA	-0.5	4	V
Voltage at ALERT		-0.5	(V+) + 0.3 and ≤ 4	V
Output voltage		-0.5	5	V
Operating temperature		-55	150	°C
Junction temperature, T <sub>J</sub>			150	°C
Storage temperature, T <sub>stg</sub>		-60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatio discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Supply Voltage	1.4	3.3	3.6	V
T <sub>A</sub>	Operating free-air temperature	-40		125	°C



#### 6.4 Thermal Information

	THERMAL METRIC <sup>(1)</sup>	TMP112-Q1 DRL (SOT563) 6 PINS	UNIT
$R_{\thetaJA}$	Junction-to-ambient thermal resistance	210.3	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	105.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.5	°C/W
ΨЈТ	Junction-to-top characterization parameter	6.1	°C/W
Ψјв	Junction-to-board characterization parameter	87.0	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

## 6.5 Electrical Characteristics

At  $T_A = 25^{\circ}C$  and V+ = 1.4 to 3.6 V, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Temperature range		-40		125	°C
		25°C, V+ = 3.3 V		±0.1	±0.5	
	Temperature accuracy (temperature error)	0°C to 65°C, V+ = 3.3 V		±0.25	±0.5	°C
		-40°C to 125°C		±0.5	±1.0	
	Accuracy vs supply	–40°C to 125°C		0.0625	±0.25	°C/V
	Long-term stability	3000 Hours		< 1		LSB
	Resolution (LSB)			0.0625		°C
DIGITAL IN	PUT/OUTPUT		i.		<u>.</u>	
	Input capacitance			3		pF
VIH	Input logic high		0.7 × (V+)		3.6	V
V <sub>IL</sub>	Input logic low		-0.5		0.3 × (V+)	V
l <sub>l</sub>	Input current	0 < V <sub>I</sub> < 3.6 V			1	μA
N/	Output logic low, SDA	$V+ > 2 V, I_{OL} = 3 mA$	0		0.4	V
VOL(SDA)		V+ < 2 V, I <sub>OL</sub> = 3 mA	0		0.2 × (V+)	
N/	Output logic low, ALERT	$V+ > 2 V, I_{OL} = 3 mA$	0		0.4	
VOL(ALERT)		V+< 2 V, I <sub>OL</sub> = 3 mA	0		0.2 × (V+)	v
	Resolution			12		Bits
	Conversion time	One-shot mode		26	35	ms
		CR1 = 0, CR0 = 0		0.25		
		CR1 = 0, CR0 = 1		1		0
	Conversion modes	CR1 = 1, $CR0 = 0$ (default)		4		CONV/S
		CR1 = 1, CR0 = 1		8		
	Timeout time			30	40	ms

## **Electrical Characteristics (continued)**

At  $T_A = 25^{\circ}$ C and V+ = 1.4 to 3.6 V, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
POWER SUPPLY									
	Operating supply range		1.4		3.6	V			
		Serial bus inactive, CR1 = 1, CR0 = 0 (default)		7 10					
IQ	Average quiescent current	Serial bus active, SCL frequency $(f_{(SCL)}) = 400 \text{ kHz}$		15		μΑ			
		Serial bus active, $f_{(SCL)} = 3.4 \text{ MHz}$		85					
I <sub>SD</sub>		Serial bus inactive		0.5	1				
	Shutdown current	Serial bus active, $f_{(SCL)} = 400 \text{ kHz}$		10		μA			
		Serial bus active, $f_{(SCL)} = 3.4 \text{ MHz}$		80					

## 6.6 Specifications for User-Calibrated Systems

For additional information on the slopes listed in this table, see the Calibrating for Improved Accuracy section.

PARAMETER	CONDITION	MIN	MAX	UNIT
	V+ = 3.3, -40°C to 25°C	-7	0	m°C/°C
Average Slope (Temperature Error vs Temperature) <sup>(1)</sup>	V+ = 3.3, 25°C to 85°C	0	5	m°C/°C
	V+ = 3.3, 85°C to 125°C	0	8	m°C/°C

(1) User-calibrated temperature accuracy can be within  $\pm 1LSB$  because of quantization noise.

## 6.7 Timing Requirements

See the *Timing Diagrams* section for timing diagrams.

			FAST M	DDE	HIGH-SI MOD	PEED )E	UNIT
			MIN	MAX	MIN	MAX	
$f_{(\rm SCL)}$	SCL operating frequency	V+	0.001	0.4	0.001	2.85	MHz
t <sub>(BUF)</sub>	Bus-free time between STOP and START condition		600		160		ns
t <sub>(HDSTA)</sub>	Hold time after repeated START condition. After this period, the first clock is generated.		600		160		ns
t <sub>(SUSTA)</sub>	repeated start condition setup time	See Two-Wire Timing Diagrams	600		160		ns
t <sub>(SUSTO)</sub>	STOP condition setup time		600		160		ns
t <sub>(HDDAT)</sub>	Data hold time		100	900	25	105	ns
t <sub>(SUDAT)</sub>	Data setup time		100		25		ns
t <sub>(LOW)</sub>	SCL-clock low period	V+ , see <i>Two-Wire Timing</i> <i>Diagrams</i>	1300		210		ns
t <sub>(HIGH)</sub>	SCL-clock high period	See Two-Wire Timing Diagrams	600		60		ns
t <sub>FD</sub>	Data fall time	See Two-Wire Timing Diagrams		300		80	ns
		See Two-Wire Timing Diagrams		300			ns
t <sub>RD</sub>	Data rise time	SCLK ≤ 100 kHz, see <i>Two-Wire</i> <i>Timing Diagrams</i>		1000			ns
t <sub>FC</sub>	Clock fall time	See Two-Wire Timing Diagrams		300		40	ns
t <sub>RC</sub>	Clock rise time	See Two-Wire Timing Diagrams		300		40	ns



## 6.8 Typical Characteristics

At  $T_A = 25^{\circ}C$  and V+ = 3.3 V, unless otherwise noted.



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# **Typical Characteristics (continued)**

At  $T_A = 25^{\circ}$ C and V+ = 3.3 V, unless otherwise noted.





## 7 Detailed Description

#### 7.1 Overview

The TMP112-Q1 device is a digital temperature sensor that is optimal for thermal-management and thermalprotection applications. The TMP112-Q1 device is two-wire, SMBus and I<sup>2</sup>C interface-compatible. The device is specified over an operating temperature range of -40°C to 125°C. Figure 8 shows a block diagram of the TMP112-Q1 device. Figure 9 illustrates the ESD protection circuitry contained in the TMP112-Q1 device.

The temperature sensor in the TMP112-Q1 device is the chip itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal.

An alternative version of the TMP112-Q1 device is available. The TMP102-Q1 device has reduced accuracy, the same micro-package, and is pin-to-pin compatible.

Device	Compatible Interfaces	Package	Supply Current	Supply Voltage (Min)	Supply Voltage (Max)	Resolution	Local Sensor Accuracy (Max)	Specified Calibration Drift Slope
TMP112-Q1	I <sup>2</sup> C SMBus	SOT563 1.2 × 1.6 × 0.6	10µA	1.4V	3.6V	12 Bit 0.0625°C	0.5°C: (0°C to 65°C) 1°C: (-40°C to 125°C)	Yes
TMP102-Q1	l <sup>2</sup> C SMBus	SOT563 1.2 × 1.6 × 0.6	10µA	1.4V	3.6V	12 Bit 0.0625°C	2°C: (25°C to 85°C) 3°C: (-40°C to 125°C)	No

Table 1. Advantages of TMP112-Q1 Versus TMP102-Q1

#### 7.2 Functional Block Diagram



Figure 8. Internal Block Diagram

#### Functional Block Diagram (continued)



Figure 9. Equivalent Internal ESD Circuitry

#### 7.3 Feature Description

#### 7.3.1 Digital Temperature Output

The digital output from each temperature measurement conversion is stored in the read-only temperature register. The temperature register of the TMP112-Q1 device is configured as a 12-bit read-only register (setting the EM bit to 0 in the configuration register; see the *Extended Mode (EM)* section), or as a 13-bit read-only register (setting the EM bit to 1 in the configuration register) that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in Table 8. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits (13 bits in extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed. The data format for temperature is listed in Table 2 and Table 3. One LSB equals 0.0625°C. Negative numbers are represented in binary twos complement format. Following power up or reset, the temperature register reads 0°C until the first conversion is complete. Bit D0 of byte 2 indicates normal mode (EM bit equals 0) or extended mode (EM bit equals 1), and can be used to distinguish between the two temperature register data formats. The unused bits in the temperature register always read 0.

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX					
128	0111 1111 1111	7FF					
127.9375	0111 1111 1111	7FF					
100	0110 0100 0000	640					
80	0101 0000 0000	500					
75	0100 1011 0000	4B0					
50	0011 0010 0000	320					
25	0001 1001 0000	190					
0.25	0000 0000 0100	004					
0	0000 0000 0000	000					
-0.25	1111 1111 1100	FFC					
-25	1110 0111 0000	E70					
-55	1100 1001 0000	C90					

#### Table 2. 12-Bit Temperature Data Format<sup>(1)</sup>

(1) The resolution for the temperature ADC in internal temperature mode is 0.0625°C/count.



Table 2 does not list all temperatures. Use the following rules to obtain the digital data format for a given temperature or the temperature for a given digital data format.

To convert positive temperatures to a digital data format:

- 1. Divide the temperature by the resolution
- 2. Convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

Example: (50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

- 1. Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number.
- 2. Multiply the decimal number by the resolution to obtain the positive temperature.

Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = 50°C

To convert negative temperatures to a digital data format:

- 1. Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format.
- 2. Generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

Example: (|-25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

- Generate the twos compliment of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature.
- Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by -1 for the negative sign.

Example: 1110 0111 0000 has twos compliment of 0001 1001 0000 = 0001 1000 1111 + 1

Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|-25°C|); (|-25°C|) × (-1) = -25°C

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
150	0 1001 0110 0000	0960
128	0 1000 0000 0000	0800
127.9375	0 0111 1111 1111	07FF
100	0 0110 0100 0000	0640
80	0 0101 0000 0000	0500
75	0 0100 1011 0000	04B0
50	0 0011 0010 0000	0320
25	0 0001 1001 0000	0190
0.25	0 0000 0000 0100	0004
0	0 0000 0000 0000	0000
-0.25	1 1111 1111 1100	1FFC
-25	1 1110 0111 0000	1E70
-55	1 1100 1001 0000	1C90

#### Table 3. 13-Bit Temperature Data Format

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#### 7.3.2 Serial Interface

The TMP112-Q1 device operates as a slave device only on the I<sup>2</sup>C, SMBus and two-wire interface-compatible bus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP112-Q1 device supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 2.85 MHz) modes. All data bytes are transmitted MSB first.

#### 7.3.2.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a highto low-logic level when the SCL pin is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge and pulling the SDA pin low.

A data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During the data transfer the SDA pin must remain stable when the SCL pin is high, because any change in the SDA pin when the SCL pin is high is interpreted as a START or STOP signal.

When all data have been transferred, the master generates a STOP condition indicated by pulling the SDA pin from low to high when the SCL pin is high.

#### 7.3.2.2 Serial Bus Address

To communicate with the TMP112-Q1 device, the master must first address slave devices through a slaveaddress byte. The slave-address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP112-Q1 device features an address pin to allow up to four devices to be addressed on a single bus. Table 4 lists the pin logic levels used to properly connect up to four devices.

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001 000	Ground
1001 001	V+
1001 010	SDA
1001 011	SCL

#### Table 4. Address Pin and Slave Addresses

#### 7.3.2.3 Writing and Reading Operation

Accessing a particular register on the TMP112-Q1 device is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the TMP112-Q1 device requires a value for the pointer register (see Figure 11).

When reading from the TMP112-Q1 device, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a slave-address byte with the R/W bit low, followed by the pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/W bit high to initiate the read command. See Figure 12 for details of this sequence. If repeated reads from the same register are desired, continuously sending the pointer register bytes is not necessary because the TMP112-Q1 device retains the pointer register value until the value is changed by the next write operation.

Register bytes are sent with the most significant byte first, followed by the least significant byte.



#### 7.3.2.4 Slave Mode Operation

The TMP112-Q1 device can operate as a slave receiver or slave transmitter. As a slave device, the TMP112-Q1 device never drives the SCL line.

#### 7.3.2.4.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address with the R/W bit low. The TMP112-Q1 device then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP112-Q1 device then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP112-Q1 device acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

#### 7.3.2.4.2 Slave Transmitter Mode

The first byte transmitted by the master is the slave address with the R/W bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a *not-acknowledge* on reception of any data byte or by generating a START or STOP condition.

#### 7.3.2.5 SMBus Alert Function

The TMP112-Q1 device supports the SMBus alert function. When the TMP112-Q1 device operates in interrupt mode (TM = 1), the ALERT pin can be connected as an SMBus alert signal. When a master senses that an alert condition is present on the alert line, the master sends an SMBus ALERT command (0001 1001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus ALERT command and responds by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the alert condition is caused by the temperature exceeding  $T_{(HIGH)}$  or falling below  $T_{(LOW)}$ . The LSB is high if the temperature is greater than  $T_{(HIGH)}$ , or low if the temperature is less than  $T_{(LOW)}$ . See *Figure 13* for details of this sequence.

If multiple devices on the bus respond to the SMBus ALERT command, arbitration during the slave address portion of the SMBus ALERT command determines which device clears the alert status of that device. The device with the lowest two-wire address wins the arbitration. If the TMP112-Q1 device wins the arbitration, the TMP112-Q1 ALERT pin becomes inactive at the completion of the SMBus ALERT command. If the TMP112-Q1 device loses the arbitration, the TMP112-Q1 ALERT pin remains active.

#### 7.3.2.6 General Call

The TMP112-Q1 device responds to a two-wire general-call address (0000 000) if the eighth bit is 0. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000 0110, the TMP112-Q1 internal registers are reset to power-up values. The TMP112-Q1 device does not support the general-address acquire command.

#### 7.3.2.7 High-Speed (Hs) Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. The TMP112-Q1 device does not acknowledge this byte, but switches the input filters on the SDA and SCL pins and the output filters on the SDA pin to operate in Hs-mode thus allowing transfers at up to 2.85 MHz. After the Hs-mode master code has been issued, the master transmits a two-wire slave address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP112-Q1 device switches the input and output filters back to fast-mode operation.

#### 7.3.2.8 Timeout Function

The TMP112-Q1 device resets the serial interface if the SCL pin is held low for 30 ms (typical) between a start and stop condition. The TMP112-Q1 releases the SDA line if the SCL pin is pulled low and waits for a start condition from the host controller. To avoid activating the timeout function, maintain a communication speed of at least 1 kHz for SCL operating frequency.



#### 7.3.2.9 Timing Diagrams

The TMP112-Q1 device is two-wire, SMBus and I<sup>2</sup>C interface-compatible. Figure 10 to Figure 13 illustrate the various operations on the TMP112-Q1 device. Parameters for Figure 10 are listed in the *Timing Requirements* table. The bus definitions are defined as follows:

Bus Idle: Both SDA and SCL lines remain high.

- Start Data Transfer: A change in the state of the SDA line, from high to low, when the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.
- **Stop Data Transfer:** A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.
- **Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. Using the TMP112-Q1 device for single byte updates is also possible. To update only the most-significant (MS) byte, terminate the communication by issuing a START or STOP communication on the bus.
- Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a *not-acknowledge (1)* on the last byte that has been transmitted by the slave.

#### 7.3.2.9.1 Two-Wire Timing Diagrams

See the *Timing Requirements* table for timing specifications.













- (1) The values of A0 and A1 are determined by the ADD0 pin.
- (2) The master must leave the SDA pin high to terminate a single-byte read operation.
- (3) The master must leave the SDA pin high to terminate a two-byte read operation.

#### Figure 12. Two-Wire Timing Diagram for Read Word Format



(1) The values of A0 and A1 are determined by the ADD0 pin.

## Figure 13. Timing Diagram for SMBus ALERT



#### 7.4 Device Functional Modes

#### 7.4.1 Continuos-Conversion Mode

The default mode of the TMP112-Q1 device is continuos conversion mode. During continuous-conversion mode, the ADC performs continuos temperature conversions and stores each results to the temperature register, overwriting the result from the previous conversion. The conversion rate bits, CR1 and CR0, configure the TMP112-Q1 device for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 8 Hz. The default rate is 4 Hz. The TMP112-Q1 device has a typical conversion time of 26 ms. To achieve different conversion rates, the TMP112-Q1 device makes a conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 5 lists the settings for CR1 and CR0.

		_
CR1	CR0	CONVERSION RATE
0	0	0.25 Hz
0	1	1 Hz
1	0	4 Hz (default)
1	1	8 Hz

Table 5.	Conversion	Rate	Settings
----------	------------	------	----------

After a power up or general-call reset, the TMP112-Q1 device immediately begins a conversion as shown in Figure 14. The first result is available after 26 ms (typical). The active quiescent current during conversion is 40  $\mu$ A (typical at 27°C). The quiescent current during delay is 2.2  $\mu$ A (typical at 27°C).



(1) The delay is set by CR1 and CR0 bits in the configuration register.

Figure 14. Conversion Start

#### 7.4.2 Extended Mode (EM)

The extended mode bit configures the device for normal mode operation (EM = 0) or extended mode operation (EM = 1). In normal mode, the temperature register and the high and low limit registers use a 12-bit data format. Normal mode is used to make the TMP112-Q1 device compatible with the TMP75 device.

Extended mode (EM = 1) allows measurement of temperatures above  $128^{\circ}$ C by configuring the temperature register and the high and low limit registers for 13-bit data format.

#### 7.4.3 Shutdown Mode (SD)

The shutdown mode bit saves maximum power by shutting down all device circuitry other than the serial interface which reduces current consumption to typically less than 0.5  $\mu$ A. Shutdown mode is enabled when the SD bit is set to 1. When this bit is set to 1 the device shuts down when current conversion is completed. When the SD bit is set to 0 the device maintains a continuous conversion state.

#### 7.4.4 One-Shot and Conversion Ready Mode (OS)

The TMP112-Q1 device features a one-shot temperature-measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit begins a single temperature conversion. During the conversion, the OS bit reads 0. The device returns to the SHUTDOWN state at the completion of the single conversion. After the conversion, the OS bit reads 1. This feature is useful for reducing power consumption in the TMP112-Q1 device when continuous temperature monitoring is not required.



As a result of the short conversion time, the TMP112-Q1 device can achieve a higher conversion rate. A single conversion typically occurs for 26 ms and a read can occur in less than 20  $\mu$ s. When using one-shot mode, 30 or more conversions per second are possible.

#### 7.4.5 Thermostat Mode (TM)

The thermostat mode bit indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1).

#### 7.4.5.1 Comparator Mode (TM = 0)

In Comparator mode (TM = 0), the Alert pin is activated when the temperature equals or exceeds the value in the  $T_{(HIGH)}$  register and remains active until the temperature falls below the value in the  $T_{(LOW)}$  register. For more information on the comparator mode, see the *High- and Low-Limit Registers* section.

#### 7.4.5.2 Interrupt Mode (TM = 1)

In Interrupt mode (TM = 1), the Alert pin is activated when the temperature exceeds  $T_{(HIGH)}$  or goes below  $T_{(LOW)}$  registers. The Alert pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High- and Low-Limit Registers* section.

#### 7.5 Programming

#### 7.5.1 Pointer Register

Figure 15 shows the internal register structure of the TMP112-Q1 device. The 8-bit pointer register of the device is used to address a given data register. The pointer register uses the two LSBs (see Table 12) to identify which of the data registers must respond to a read or write command. The power-up reset value of the P[1:0] byte is 00. By default, the TMP112-Q1 device reads the temperature on power up.



Figure 15. Internal Register Structure



#### **Programming (continued)**

Table 6 lists the pointer address of the registers available in the TMP112-Q1 device. Table 7 lists the bits of the pointer register byte. During a write command, bytes P2 through P7 must always be 0.

P1	P0	REGISTER
0	0	Temperature register (read only [R])
0	1	Configuration register (read-write [R/W])
1	0	T <sub>(LOW)</sub> register (R/W)
1	1	T <sub>(HIGH)</sub> register (R/W)

#### **Table 6. Pointer Addresses**

#### Table 7. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

#### 7.5.2 Temperature Register

The temperature register of the TMP112-Q1 device is configured as a 12-bit read-only register (setting the EM bit to 0 in the configuration register; see the *Extended Mode (EM)* section), or as a 13-bit read-only register (setting the EM bit to 1 in the configuration register) that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in Table 8. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits (13 bits in extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	T11	T10	Т9	Т8	Τ7	Т6	T5	T4
	(T12)	(T11)	(T10)	(T9)	(T8)	(T7)	(T6)	(T5)
2	Т3	T2	T1	T0	0	0	0	0
	(T4)	(T3)	(T2)	(T1)	(T0)	(0)	(0)	(1)

#### Table 8. Bytes 1 and 2 of Temperature Register<sup>(1)</sup>

(1) Extended mode 13-bit configuration shown in parentheses.

#### 7.5.3 Configuration Register

The configuration register is a 16-bit R/W register used to store bits that control the operational modes of the temperature sensor. Read-write operations are performed MSB first. Table 9 lists the format and power-up and reset values of the configuration register. For compatibility, the first byte corresponds to the configuration register in the TMP75 and TMP275 devices. All registers are updated byte by byte.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	ТМ	SD
	0	1	1	0	0	0	0	0
2	CR1	CR0	AL	EM	0	0	0	0
	1	0	1	0	0	0	0	0

#### Table 9. Configuration and Power-Up and Reset Formats

#### 7.5.3.1 Shutdown Mode (SD)

The shutdown mode bit saves maximum power by shutting down all device circuitry other than the serial interface which reduces current consumption to typically less than 0.5  $\mu$ A. Shutdown mode is enabled when the SD bit is set to 1. When this bit is set to 1 the device shuts down when current conversion is completed. When the SD bit is set to 0 the device maintains a continuous conversion state.



#### 7.5.3.2 Thermostat Mode (TM)

The thermostat mode bit indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High- and Low-Limit Registers* section.

#### 7.5.3.3 Polarity (POL)

The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When the POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is shown in Figure 16.



Figure 16. Output Transfer Function Diagrams

#### 7.5.3.4 Fault Queue (F1/F0)

A fault condition exists when the measured temperature exceeds the user-defined limits set in the  $T_{(HIGH)}$  and  $T_{(LOW)}$  registers. Additionally, the number of fault conditions required to generate an alert can be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 10 lists the number of measured faults that can be programmed to trigger an alert condition in the device. For  $T_{(HIGH)}$  and  $T_{(LOW)}$  register format and byte order, see the *High- and Low-Limit Registers* section.

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6



#### 7.5.3.5 Converter Resolution (R1 and R0)

The converter resolution bits, R1 and R0, are read-only bits. The TMP112-Q1 converter resolution is set on start up to 11 which sets the temperature register to a 12 bit-resolution.

#### 7.5.3.6 One-Shot (OS)

When the device is in shutdown mode, writing a 1 to the OS bit begins a single temperature conversion. During the conversion, the OS bit reads 0. The device returns to the SHUTDOWN state at the completion of the single conversion. For more information on the one-shot conversion mode, see the *One-Shot and Conversion Ready Mode (OS)* section.

#### 7.5.3.7 Extended Mode (EM)

The extended mode bit configures the device for normal mode operation (EM = 0) or extended mode operation (EM = 1). In normal mode, the temperature register and the high and low limit registers use a 12-bit data format. For more information on the extended mode, see the *Extended Mode (EM)* section.

#### 7.5.3.8 Alert (AL)

The AL bit is a read-only function. Reading the AL bit provides information about the comparator mode status. The state of the POL bit inverts the polarity of data returned from the AL bit. When the POL bit equals 0, the AL bit reads as 1 until the temperature equals or exceeds  $T_{(HIGH)}$  for the programmed number of consecutive faults, causing the AL bit to read as 0. The AL bit continues to read as 0 until the temperature falls below  $T_{(LOW)}$  for the programmed number of consecutive faults, when it again reads as 1. The status of the TM bit does not affect the status of the AL bit.

#### 7.5.3.9 Conversion Rate (CR)

The conversion rate bits, CR1 and CR0, configure the TMP112-Q1 device for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 8 Hz. The default rate is 4 Hz. For more information on conversion rate bits, see the *Continuos-Conversion Mode* section.

#### 7.5.4 High- and Low-Limit Registers

The temperature limits are stored in the  $T_{(LOW)}$  and  $T_{(HIGH)}$  registers in the same format as the temperature result, and their values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which operates as a comparator output or an interrupt, and is set by the TM bit in the configuration register.

In Comparator mode (TM = 0), the ALERT pin becomes active when the temperature equals or exceeds the value in the  $T_{(HIGH)}$  register and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated  $T_{(LOW)}$  value for the same number of faults.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds the value in  $T_{(HIGH)}$  for a consecutive number of fault conditions (as shown in Table 10). The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode. When the ALERT pin is cleared, it becomes active again only when temperature falls below  $T_{(LOW)}$ , and remains active until cleared by a read operation of any register or a successful response to the SMBus alert response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds  $T_{(HIGH)}$ . The ALERT pin can also be cleared by resetting the device with the general-call Reset command. This action also clears the state of the internal registers in the device, returning the device to comparator mode (TM = 0).



Both operating modes are represented in Figure 16. Table 11 and Table 12 list the format for the  $T_{(HIGH)}$  and  $T_{(LOW)}$  registers. The most significant byte is sent first, followed by the least significant byte. The power-up reset values for  $T_{(HIGH)}$  and  $T_{(LOW)}$  are:

- $T_{(HIGH)} = 80^{\circ}C$
- T<sub>(LOW)</sub> = 75°C

The format of the data for  $T_{(HIGH)}$  and  $T_{(LOW)}$  is the same as for the temperature register.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
4	H11	H10	H9	H8	H7	H6	H5	H4
1	(H12)	(H11)	(H10)	(H9)	(H8)	(H7)	(H6)	(H5)
	H3	H2	H1	H0	0	0	0	0
2	(H4)	(H3)	(H2)	(H1)	(H0)	(0)	(0)	(0)

#### Table 11. Bytes 1 and 2 of T<sub>(HIGH)</sub> Register<sup>(1)</sup>

(1) Extended mode 13-bit configuration shown in parenthesis.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4
1	(L12)	(L11)	(L10)	(L9)	(L8)	(L7)	(L6)	(L5)
2 -	L3	L2	L1	LO	0	0	0	0
	(L4)	(L3)	(L2)	(L1)	(L0)	(0)	(0)	(0)

## Table 12. Bytes 1 and 2 of T<sub>(LOW)</sub> Register<sup>(1)</sup>

(1) Extended mode 13-bit configuration shown in parenthesis.

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#### 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 8.1 Application Information

#### 8.1.1 Calibrating for Improved Accuracy

Many temperature monitoring applications require better than 0.5°C accuracy over a limited temperature range. Knowing the offset of a temperature sensor at a given temperature in conjunction with the average temperature span (slope) error over a fixed range makes achieving this improved accuracy possible.

The TMP112-Q1 device has three distinct slope regions that conservatively approximate the inherent curvature. The following lists the three distinct slope regions:

- 1. Slope1 applies over -40°C to 25°C
- 2. Slope2 applies over 25°C to 85°C
- 3. Slope3 applies over 85°C to 125°C

The Specifications for User-Calibrated Systems table defines these slopes which are also shown in Figure 17.



Figure 17. Accuracy and Slope Curves versus Temperature

Use Equation 1 to calculate the worst-case accuracy at a specific temperature. Accuracy<sub>(worst-case)</sub> = Accuracy<sub>(25°C)</sub> +  $\Delta$ T × Slope

(1)



#### **Application Information (continued)**

#### 8.1.1.1 Example 1: Finding Worst-Case Accuracy From –15°C to 50°C

As an example, if the user is concerned only about the temperature accuracy between -15°C to 50°C, the worstcase accuracy could be determined by using the two slope calculations shown in Equation 2 and Equation 4:

Accuracy(worst-case) = Accuracy(25°C) + $\Delta$ T × Slope	(2)
Accuracy(MAX[-15°C to 25°C]) = $0.3°C + (-15°C - 25°C) \times (-7 \frac{m°C}{°C}) = 0.58°C$	(3)
Accuracy(MAX[25°C to 50°C]) = Accuracy(25°C) + $\Delta$ T × Slope2(MAX)	(4)
Accuracy(MAX[25°C to 50°C]) = $0.3°C + (50°C - 25°C) \times \left(5\frac{m°C}{°C}\right) = 0.425°C$	(5)
The same calculations must be applied to the minimum case: Accuracy(MIN[-15°C to 25°C]) = Accuracy(25°C) + ΔT × Slope1(MIN)	(6)
Accuracy(MIN[-15°C to 25°C]) = -0.5°C + $\left[ (-15°C - 25°C) \times \left( 0 \frac{m°C}{°C} \right) \right] = -0.5°C$	(7)

<sup>Accuracy</sup>(MIN[25°C to 50°C])<sup>= Accuracy</sup>(25°C)<sup>+ ∆T × Slope2</sup>(MIN)

Accuracy(MIN[25°C to 50°C]) = 
$$-0.5°C + \left[ (50°C - 25°C) \times \left( 0 \frac{m°C}{°C} \right) \right] = -0.5°C$$
 (9)

Based on these calculations, a user can expect a worst-case accuracy of  $0.58^{\circ}$ C to  $-0.5^{\circ}$ C in the temperature range of  $-15^{\circ}$ C to  $50^{\circ}$ C.

#### 8.1.1.2 Example 2: Finding Worst-Case Accuracy From 25°C to 100°C

If the desired temperature range falls in the region of slope 3, first calculate the worst-case value from 25°C to 85°C and add it to the change in temperature multiplied by the span error of slope 3. As an example, consider the temperature range of 25°C to 125°C as shown in Equation 10:

 $Accuracy(MAX[25^{\circ}C \text{ to } 100^{\circ}C]) = Accuracy(25^{\circ}C) + \Delta T \times Slope2(MAX) + \Delta T \times Slope3(MAX)$ (10)

Accuracy (MAX[25°C to 100°C]) = 
$$0.3°C + (85°C - 25°C) \times (4.5 \frac{m^{\circ}C}{°C}) + (100°C - 85°C) \times (8\frac{m^{\circ}C}{°C}) = 0.69°C$$
 (11)

Then perform the same calculation for the minimum case as shown in Equation 12:

 $Accuracy(MIN[25^{\circ}C \text{ to } 100^{\circ}C]) = Accuracy(25^{\circ}C) + \Delta T \times Slope2(MIN) + \Delta T \times Slope3(MIN)$ (12)

Accuracy(MIN[25°C to 100°C]) = 
$$-0.5°C + \left[ (85°C - 25°C) \times \left( 0 \frac{m°C}{°C} \right) \right] + \left[ (100°C - 85°C) \times \left( 0 \frac{m°C}{°C} \right) \right] = -0.5°C$$
 (13)

(8)

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#### **Application Information (continued)**

#### 8.1.2 Using The Slope Specifications With a 1-Point Calibration

The initial accuracy assurance at 25°C with the slope regions provides an accuracy that is high enough for most applications. However, if higher accuracy is desired, this increase can be achieved with a 1-point calibration at 25°C. This calibration removes the offset at room temperature, thereby reducing the source of error in a TMP112-Q1 temperature reading down to the curvature. Figure 18 shows the error of a calibrated TMP112-Q1 device.



Figure 18. Calibrated Accuracy and Slope Curves versus Temperature

Using the previous example temperature range of 0°C to 50°C, the worst-case temperature error is now reduced to the worst-case slopes because the offset at 25°C (that is, the maximum and minimum temperature errors of  $0.3^{\circ}$ C and  $-0.5^{\circ}$ C) is removed. Therefore, a user can expect the worst-case accuracy to improve to  $0.175^{\circ}$ C.

#### 8.1.2.1 Power Supply-Level Contribution to Accuracy

The superior accuracy that can be achieved with the TMP112-Q1 device is complemented by the immunity-to-DC variations from a 3.3-V supply voltage. This immunity is important because it spares the user from having to use another LDO regulator to produce 3.3 V to achieve accuracy. Nevertheless, the noise quantization that results from changing supply can add some slight change in temperature measurement accuracy. As an example, if the user chooses to operate the device at 1.8 V, the worst-case expected change in accuracy can be calculated with Equation 14:

$$Accuracy(PSR) = \pm (V + -3.3 V) \times \left[ \frac{0.25^{\circ}C}{V} \right]$$

$$Accuracy(PSR)^{=\pm} (1.8 V - 3.3 V) \times \left[ \frac{0.25^{\circ}C}{V} \right] = \pm 0.375^{\circ}C$$
(15)

This example is a worst-case accuracy contribution as a result of variation in power supply that must be added to the accuracy plus the slope maximum.



#### 8.2 Typical Application

The TMP112-Q1 device is used to measure the PCB temperature of the board location where the device is mounted. The programmable address options allow up to four locations on the board to be monitored on a single serial bus.



NOTE: The SCL, SDA, and ALERT pins require pullup resistors.

#### Figure 19. Typical Connections

#### 8.2.1 Design Requirements

The TMP112-Q1 device requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistors is 5-k $\Omega$ . In some applications the pullup resistor can be lower or higher than 5 k $\Omega$  but must not exceed 3 mA of current on any of those pins. A 0.01- $\mu$ F bypass capacitor on the supply is recommended as shown in Figure 19. The SCL and SDA lines can be pulled up to a supply that is equal to or higher than V+ through the pullup resistors. To configure one of four different addresses on the bus, connect the ADD0 pin to either the GND, V+, SDA, or SCL pin.

#### 8.2.2 Detailed Design Procedure

Place the TMP7112-Q1 device in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, care must be taken to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

The TMP112-Q1 device is a very low-power device and generates very low noise on the supply bus. Applying an RC filter to the V+ pin of the TMP112-Q1 device can further reduce any noise that the TMP112-Q1 device might propagate to other components.  $R_{(F)}$  in Figure 20 must be less than 5 k $\Omega$  and  $C_{(F)}$  must be greater than 10 nF.



## **Typical Application (continued)**



Figure 20. Noise Reduction Techniques

#### 8.2.3 Application Curves

Figure 21 shows the step response of the TMP112-Q1 device to a submersion in an oil bath of 100°C from room temperature (27°C). The time-constant, or the time for the output to reach 63% of the input step, is 0.8 s. The time-constant result depends on the printed circuit board (PCB) that the TMP112-Q1 device is mounted. For this test, the TMP112-Q1 device was soldered to a two-layer PCB that measured 0.375 in × 0.437 in.



Figure 21. Temperature Step Response

## 9 Power Supply Recommendations

The TMP112-Q1 device operates with power supply in the range of 1.4 to 3.6 V. The device is optimized for operation at 3.3-V supply but can measure temperature accurately in the full supply range. Refer to the *Power Supply-Level Contribution to Accuracy* section for more information about the power supply impact on the accuracy of the device.

A power-supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01  $\mu$ F. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.



## 10 Layout

#### 10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01  $\mu\text{F}$ . Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins (SDA , SCL and ALERT) through 5- $k\Omega$  pullup resistors.

#### **10.2 Layout Example**



Figure 22. Layout Example

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#### 11 器件和文档支持

#### 11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档:

TMP112 产品说明书, SBOS473

或访问 http://www.ti.com.cn/product/cn/TMP112, 查看 TMP112 产品文件夹

#### 11.2 接收文档更新通知

要接收文档更新通知,请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的通知我 进行注册,即可每周接收产品信息更改摘要。有关更改的详细信息,请查看任何已修订文档中包含的修订历史记录。

#### 11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点;请参阅 TI 的 《使用条款》。

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设计支持 **7I 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

#### 11.4 商标

E2E is a trademark of Texas Instruments. SMBus is a trademark of Intel, Inc. All other trademarks are the property of their respective owners.

#### 11.5 静电放电警告

▲ 这些装置包含有限的内置 ESD 保护。存储或装卸时,应将导线一起截短或将装置放置于导电泡棉中,以防止 MOS 门极遭受静电损 伤。

## 11.6 术语表

SLYZ022 — TI 术语表。 这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更,恕不另行通知,且 不会对此文档进行修订。如需获取此数据表的浏览器版本,请查阅左侧的导航栏。

#### 重要声明和免责声明

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10-Dec-2020

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins F	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP112AQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SLP	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(<sup>6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	
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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP112AQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TEXAS INSTRUMENTS

www.ti.com

# PACKAGE MATERIALS INFORMATION

20-Dec-2018



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP112AQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0

# **DRL0006A**



# **PACKAGE OUTLINE**

# SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side. 4. Reference JEDEC registration MO-293 Variation UAAD



# **DRL0006A**

# **EXAMPLE BOARD LAYOUT**

# SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# **DRL0006A**

# **EXAMPLE STENCIL DESIGN**

# SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

8. Board assembly site may have different recommendations for stencil design.



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