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TEXAS INSTRUMENTS

TMP1075
ZHCSHX1D – MARCH 2018 – REVISED OCTOBER 2019

具有 I²C 和 SMBus 接口且采用行业标准 LM75 外形尺寸和引脚输出的 TMP1075 温度传感器

1 特性

- TMP1075DGK/TMP1075D 的精度：
  - −40°C 至 +110°C 范围内为 ±1°C（最大值）
  - −55°C 至 +125°C 范围内为 ±2°C（最大值）
- TMP1075DSG 的精度
  - −40°C 至 +75°C 范围内为 ±1°C（最大值）
  - −55°C 至 +125°C 范围内为 ±2°C（最大值）
- 低功耗：
  - 2.7µA 平均电流
  - 0.37µA 关断电流
- 宽电源电压范围：1.7V 至 5.5V
- 温度与电源无关
- 数字接口：SMBus，I²C
- 软件与业界通用的 LM75 和 TMP75 完全兼容
- 可兼容 I³C 混合快速模式总线
- 分辨率：12 位
- 支持高达 32 个设备地址
- 警报引脚功能
- NIST 可追溯性

2 应用

- 电源温度监控
- 计算机外设过热保护
- 笔记本电脑
- 手机
- 电池管理
- 办公机器
- 恒温器控制
- 环境监测和供热通风与空气调节 (HVAC)
- 机电器件温度

3 说明

TMP1075 精度最高，功耗最低，是行业标准 LM75 和 TMP75 数字温度传感器的替代产品。TMP1075 采用 SOIC-8 和 VSSOP-8 封装，可提供引脚对引脚及软件兼容，以便快速升级任何现有 xx75 设计。TMP1075 还新增了一个 2x2mm DFN 封装，与 SOIC 封装相比，该封装将 PCB 空间占用减小了 79%。

TMP1075 可在较宽的工作温度范围内实现 ±1°C 的精度，它还具有一个可提供 0.0625°C 温度分辨率的片上 12 位模数转换器 (ADC)。

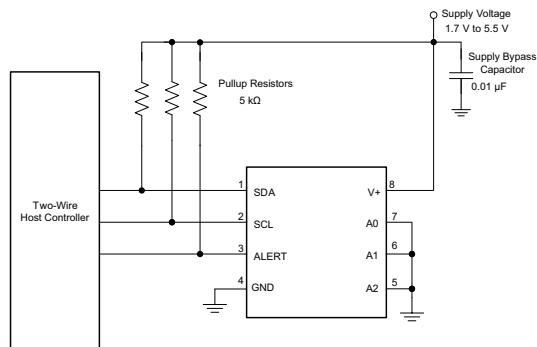TMP1075 兼容两线制 SMBus 接口和 I²C 接口，支持高达 32 个器件地址并提供 SMBus 复位和警报功能。

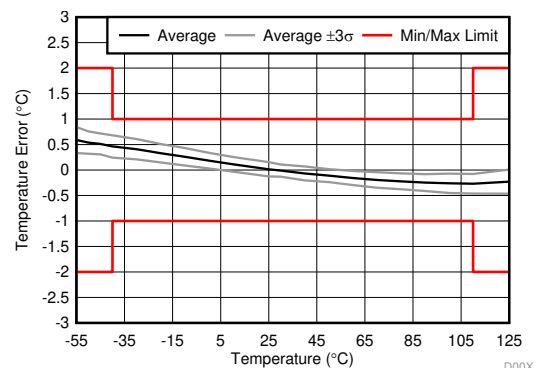TMP1075 设计用于提供精确且具有成本效益的温度测量，可适用于几乎所有电信、企业、工业和个人电子设备。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMP1075	VSSOP/DGK (8)	3.00mm × 3.00mm
	SOIC/D (8)	4.90mm × 3.91mm
	WSON/DSG (8)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图

温度精度 (DGK & D)

English Data Sheet: SBOS854

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

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Changes from Revision B (December 2018) to Revision C   **Page**

Changes from Revision A (June 2018) to Revision B   **Page**

Changes from Original (March 2018) to Revision A   **Page**

5 说明 （续）

TMP1075 器件的额定工作温度范围为 −55°C 至 +125°C。

TMP1075 装置在生产调试阶段经过 100% 测试，可通过 NIST 进行追溯，且使用经 ISO/IEC 17025 认证标准校准的设备进行了验证。

6 Pin Configuration and Functions

DGK, D, and DSG Packages
8-Pin VSSOP, SOIC, and WSON
Top View

SDA	1	8	V+
SCL	2	7	A0
ALERT	3	6	A1
GND	4	5	A2
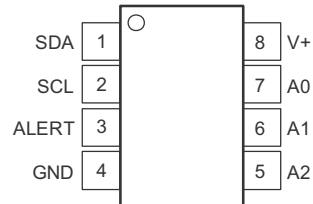
NOTE: Pin 1 is determined by orienting the package marking as indicated in the diagram.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SDA	I/O	Serial data. Open-drain output that requires a pullup resistor
2	SCL	I	Serial clock
3	ALERT	O	Overtemperature alert; Open-drain output that requires a pullup resistor
4	GND	—	Ground
5	A2	I	Address select A2: Connect to GND or V+
6	A1	I	Address select A1: Connect to GND, V+, SDA, or SCL
7	A0	I	Address select A0: Connect to GND, V+, SDA, or SCL
8	V+	I	Supply voltage, 1.7 V to 5.5 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Power supply, V+		6.5	V
Input voltage SCL, SDA, A1, A0	−0.3	6.5	V
Input voltage A2 pin	−0.3	(V+) + 0.3	V
Operating temperature	−55	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	−60	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	1.7		5.5	V
Operating free-air temperature, T_A	−55		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TMP1075	TMP1075	TMP1075	UNIT
		DGK (VSSOP)	D (SOIC)	DSG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	202.5	130.4	87.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82	76.9	111.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	124.4	72.3	54	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.9	32	9.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	122.6	71.9	54.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	__	__	28.1	°C/W
M_T	Thermal mass	16.6	64.2	5.0	mJ/°C

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = −55°C to +125°C and V+ = 1.7 V to 5.5 V (unless noted); typical specification are at T_A = 25°C and V+=3.3 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT							
	Range			−55		125	°C
	Accuracy (temperature error)	DGK, D	−40°C to +110°C		±0.25	±1	°C
			−55°C to +125°C		±0.25	±2	
		DSG	−40°C to +75°C		±0.25	±1	°C
			−55°C to +125°C		±0.25	±2	°C
	Accuracy (temperature error) vs supply		PSRR			±0.03	°C/V
	Resolution		1 LSB (12 bit)		0.0625		°C
	Repeatability[1]		25°C, V+= 3.3 V [2]		0.0625		°C
	Long-term drift[3]		500 hours at 150°C, 5.5V		0.0625		°C
DIGITAL INPUT/OUTPUT							
	Input capacitance				5		pF
V_{IH}	High-level input logic			0.7(V+)			V
V_{IL}	Low-level input logic					0.3(V+)	V
I_{IN}	Leakage input current			-0.25	0	0.25	µA
	Input voltage hysteresis		SCL and SDA pins		600		mV
V_{OL}	Low-level output logic		I_{OL} = -3 mA, SDA and ALERT pins	0	0.15	0.4	V
	ADC Conversion time		one-shot mode	4.5	5.5	7	ms
T_C	Conversion Time		R1 = 0, R0 = 0 (default)		27.5		ms
			R1 = 0, R0 = 1		55		
			R1 = 1, R0 = 0		110		
			R1 = 1, R0 = 1		220		
	Reset time		The time between reset till ADC conversion start		0.3		ms
	Conversion Rate Variation			-10	0	10	%
POWER SUPPLY							
	Operating voltage range			1.7	3.3	5.5	V
I_Q	Quiescent current (serial bus inactive)		R1 = 0, R0 = 0 (default)		10	20	µA
			R1 = 0, R0 = 1		5.5	9	µA
			R1 = 1, R0 = 0		4	6	
			R1 = 1, R0 = 1		2.7	4	
			During 5.5 ms active conversion		52	85	µA
I_{SD}	Shutdown current		Serial bus active, SCL frequency = 400 kHz, A0=A1=A2=GND		13		µA
			Serial bus inactive, A0=A1=A2=SCL=SDA=V+, 25°C		0.37	0.65	µA
			Serial bus inactive, A0=A1=A2=SCL=SDA=V+		0.37	3.5	µA
	Power supply thresholds		Supply rising, Power-on Reset		1.22		V
			Supply failing, Brown-out Detect		1.1		

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) One-shot mode setup, 1 sample per minute for 24 hours.
(3) Long-term drift is determined using accelerated operational life testing at a junction temperature of 150°C.

7.6 Timing Requirements

minimum and maximum specifications are over –55°C to 125°C and V+ = 1.7 V to 5.5 V (unless otherwise noted)[1]

		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	2.56	MHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time	600		160		ns
$t_{(SUSTO)}$	STOP condition setup time	600		160		ns
$t_{(HDDAT)}$	Data hold time[2]	0		0	130	ns
$t_{(SUDAT)}$	Data setup time	100		20		ns
$t_{(LOW)}$	SCL clock low period	1300		250		ns
$t_{(HIGH)}$	SCL clock high period	600		60		ns
$t_{(VDAT)}$	Data valid time (data response time)[3]		900		130	ns
t_{FDA}	Data fall time		300		100	ns
t_R	Clock rise time		300		40	ns
t_F	Clock fall time		300		40	ns
$t_{timeout}$	Timeout (SCL = SDA = GND)	20	30	20	30	ms
t_{RC}	Clock/ data rise time for SCL = 100 kHz		1000			ns

(1) The host and device have the same V+ value. Values are based on statistical analysis of samples tested during initial release.
(2) The maximum $t_{(HDDAT)}$ can be 0.9 μs for fast mode, and is less than the maximum $t_{(VDAT)}$ by a transition time.
(3) $t_{(VDAT)}$ = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse). = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
t_{LPF}	Spike filter for I³C compatibility	SCL= 12.5 MHz		50		ns
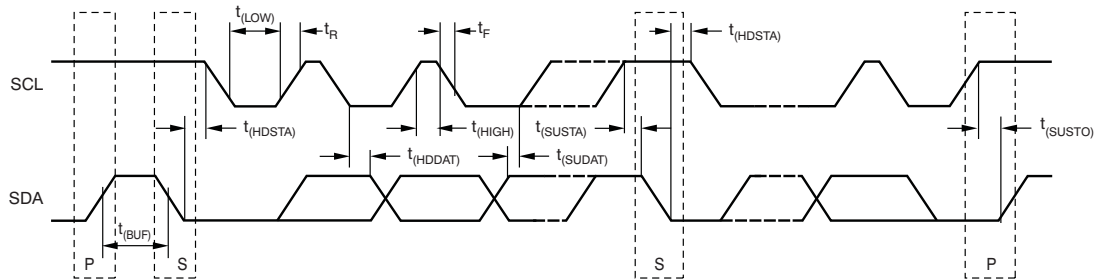
图 1. Two-Wire Timing Diagram

7.8 Typical Characteristics

at T_A = 25°C and V+ = 3.3 V (unless otherwise noted)
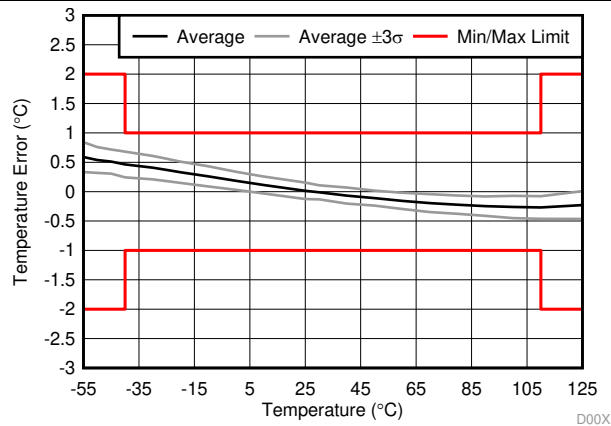
图 2. DGK & D Temperature Error vs Temperature
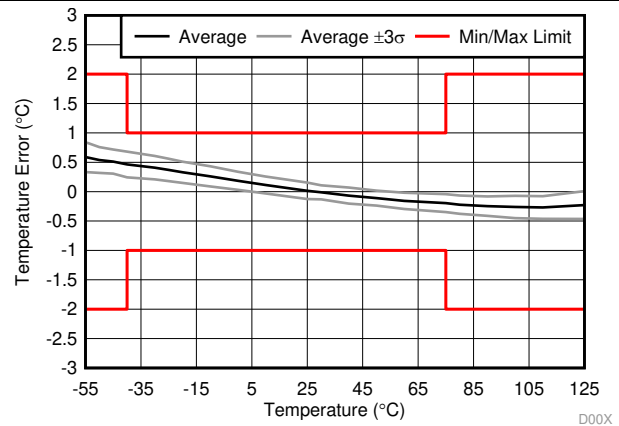
图 3. DSG Temperature Error vs Temperature
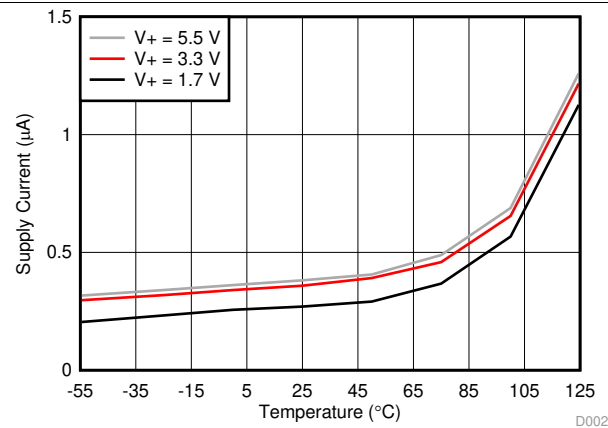
图 4. Shutdown Current vs Temperature
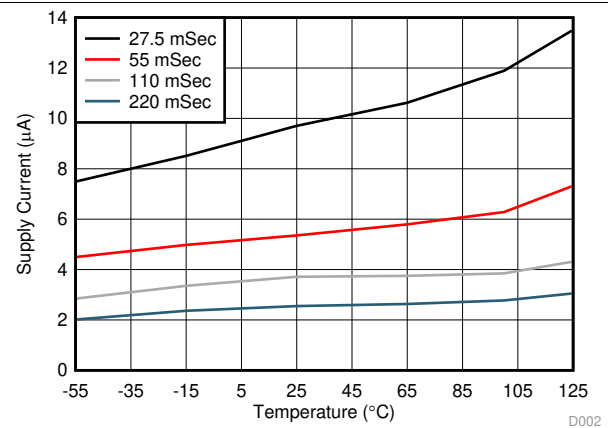
图 5. Average Current vs Conversion Rates and Temperature
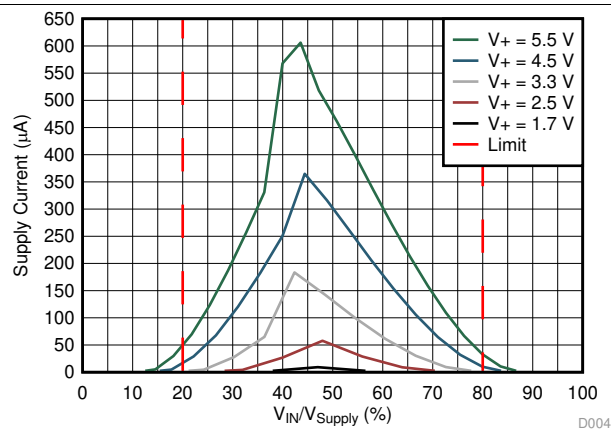
图 6. Supply Current vs Input Cell Voltage
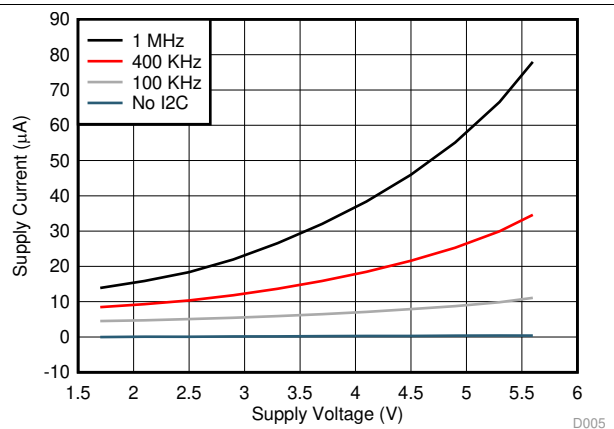
图 7. Supply Current vs I²C Bus Clock and Supply Voltage in Shutdown Mode

Typical Characteristics (接下页)

at T_A = 25°C and V+ = 3.3 V (unless otherwise noted)
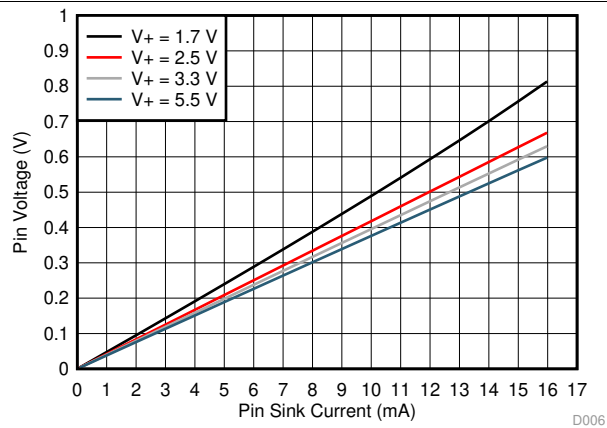
图 8. ALERT Pin Output Voltage vs Sink Current
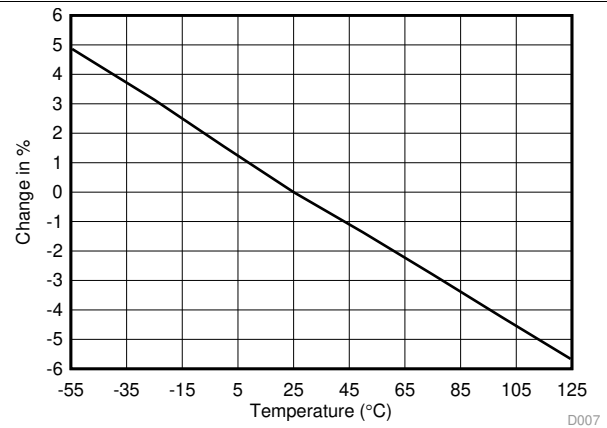
图 9. Sampling Period Change vs Temperature (1.7 V to 5.5 V)

8 Detailed Description

8.1 Overview

The TMP1075 device is a digital temperature sensor that is optimal for thermal management and thermal protection applications. The TMP1075 is a SMBus and is I^{2}C interface-compatible. It is also capable of coexisting in an I^{3}C bus when in Mixed Fast Mode. The device is specified over a temperature range of −55°C to +125°C. The *Functional Block Diagram* section shows an internal block diagram of TMP1075 device.

The temperature sensor thermal path runs through the package leads as well as the plastic package. The leads provide the primary thermal path due to the lower thermal resistance of the metal.

8.2 Functional Block Diagram
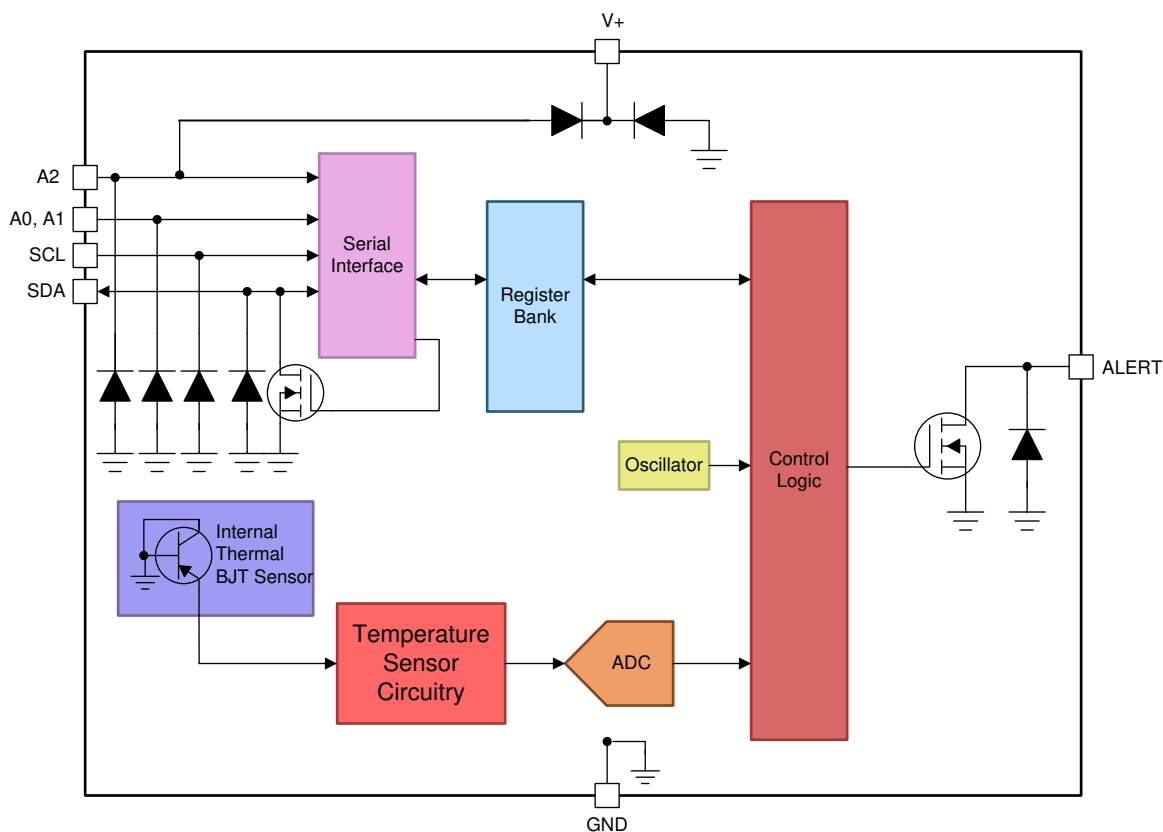
图 10. **Functional Block Diagram**

8.3 Feature Description

8.3.1 Digital Temperature Output

The digital output from each temperature measurement conversion is stored in the read-only Temperature register. Which is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data. However, only the first 12 MSBs are used to indicate temperature while the remaining 4 LSB are set to zero. Data format for the temperature is listed in 表 1. Negative numbers are represented in binary two's-complement format. After power-up or reset, the Temperature register reads 0°C until the first conversion is complete.

表 1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
127.9375	0111 1111 1111 0000	7FF0
100	0110 0100 0000 0000	6400
80	0101 0000 0000 0000	5000
75	0100 1011 0000 0000	4B00
50	0011 0010 0000 0000	3200
25	0001 1001 0000 0000	1900
0.25	0000 0000 0100 0000	0040
0.0625	0000 0000 0001 0000	0010
0	0000 0000 0000 0000	0000
−0.0625	1111 1111 1111 0000	FFF0
−0.25	1111 1111 1100 0000	FFC0
−25	1110 0111 0000 0000	E700
−50	1100 1110 0000 0000	CE00
−128	1000 000 0000 0000	8000

8.3.2 I²C and SMBus Serial Interface

The TMP1075 operates as a target device on the two-wire, SMBus and I²C interface-compatible bus. Connections to the bus are made through the open-drain I/O line SDA and SCL input pin. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP1075 supports the transmission protocol for fast mode up to 400 kHz and high-speed mode up to 2.56 MHz. All data bytes are transmitted MSB first.

8.3.2.1 Bus Overview

The device that initiates the data transfer is called a host, and the devices controlled by the host are the target. The bus must be controlled by a host device that generates the SCL that controls the bus access and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. This is indicated by the host pulling the data line SDA from a high to low logic level when SCL is high. All target devices on the bus shift in the device address byte on the rising edge of the clock with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the device being addressed responds to the host by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer, SDA must remain stable when SCL is high because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the host generates a STOP condition indicated by pulling SDA from low to high logic level when SCL is high.

8.3.2.2 Serial Bus Address

To communicate with the TMP1075, the host must first address devices through an address byte. The device address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP1075 features three address pins to allow up to 32 devices to be addressed on a single bus interface. 表 2 describes the pin logic levels used to connect up to 32 devices. The state of pins A0, A1, and A2 is sampled on every bus communication and must be set prior to any activity on the interface.

表 2. Address Pins State

A2	A1	A0	7-BIT ADDRESS	A2	A1	A0	7-BIT ADDRESS
0	0	SDA	1000000	0	SDA	SDA	1010000
0	0	SCL	1000001	0	SDA	SCL	1010001
0	1	SDA	1000010	0	SCL	SDA	1010010
0	1	SCL	1000011	0	SCL	SCL	1010011
1	0	SDA	1000100	1	SDA	SDA	1010100
1	0	SCL	1000101	1	SDA	SCL	1010101
1	1	SDA	1000110	1	SCL	SDA	1010110
1	1	SCL	1000111	1	SCL	SCL	1010111
0	0	0	1001000	0	SDA	0	1011000
0	0	1	1001001	0	SDA	1	1011001
0	1	0	1001010	0	SCL	0	1011010
0	1	1	1001011	0	SCL	1	1011011
1	0	0	1001100	1	SDA	0	1011100
1	0	1	1001101	1	SDA	1	1011101
1	1	0	1001110	1	SCL	0	1011110
1	1	1	1001111	1	SCL	1	1011111

8.3.2.3 Pointer Register

图 11 shows the internal register structure of the TMP1075, and 表 4 lists the pointer addresses of the register map. 表 3 shows that the register map reset value of the pointer register is 00h.
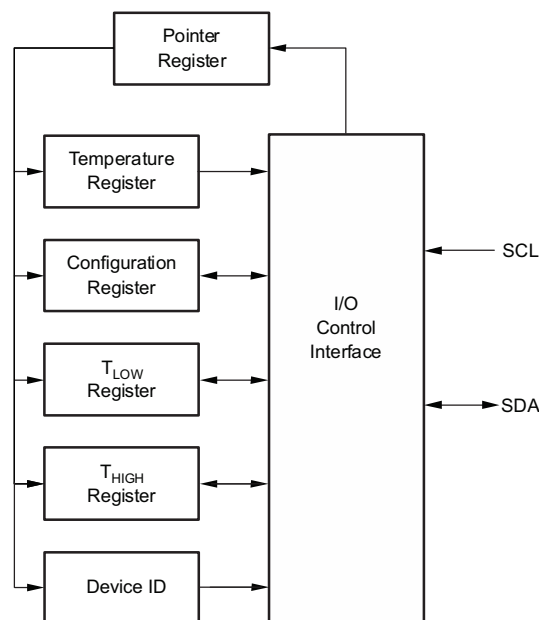

图 11. Internal Register Structure

8.3.2.3.1 Pointer Register Byte [reset = 00h]

表 3. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	Register Bits			

8.3.2.4 Writing and Reading to the TMP1075

Accessing a particular register on the TMP1075 device is accomplished by writing the appropriate value to the Pointer register. After Reset, the register value is set to zero. The value for the Pointer register is the first byte transferred after the device address byte with the R/W bit low. Every write operation to the TMP1075 requires a value for the Pointer register (see 图 12).

When reading from the TMP1075 device, the last value stored in the Pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer register. This action is accomplished by issuing a device address byte with the R/$\overline{W}$ bit low, followed by the Pointer register byte. No additional data are required. The host can then generate a START condition and send the device address byte with the R/$\overline{W}$ bit high to initiate the read command. See 图 14 for details of this sequence. If repeated reads from the same register are desired, the Pointer register bytes do not have to be continually sent because the TMP1075 remembers the Pointer register value until the value is changed by the next write operation.

Register bytes are sent MSB first.

8.3.2.5 Operation Mode

The TMP1075 can operate as a receiver or transmitter. As a target device, the TMP1075 never drives the SCL line.

8.3.2.5.1 Receiver Mode

The first byte transmitted by the host is the device address with the R/$\overline{W}$ bit low. The TMP1075 then acknowledges reception of a valid address. The next byte transmitted by the host is the Pointer register. The TMP1075 then acknowledges reception of the Pointer register byte. The next byte or bytes are written to the register addressed by the Pointer register. The TMP1075 acknowledges reception of each data byte. The host can terminate data transfer by generating a START or STOP condition.

8.3.2.5.2 Transmitter Mode

The first byte is transmitted by the host and is the device address, with the R/$\overline{W}$ bit high. The target device acknowledges reception of a valid device address. The next byte is transmitted by the device and is the most significant byte of the register indicated by the Pointer register. The host acknowledges reception of the data byte. The next byte transmitted by the device is the least significant byte. The host acknowledges reception of the data byte. The host can terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

8.3.2.6 SMBus Alert Function

The TMP1075 supports the SMBus Alert function. When the TMP1075 is operating in interrupt mode (TM = 1), the ALERT pin of the TMP1075 can be connected as an SMBus Alert signal. When a host senses that an alert condition is present on the ALERT line, the host sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP1075 is active, the devices acknowledge the SMBus Alert command and respond by returning the device address on the SDA line. The eighth bit (LSB) of the device address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the alert condition. This bit is equal to POL if the temperature is greater than or equal to T_{HIGH}. This bit is equal to $\overline{POL}$ if the temperature is less than T_{LOW}. See 图 17 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the device address portion of the SMBus Alert command determines which device clears the alert status. If the TMP1075 wins the arbitration, the ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP1075 loses the arbitration, the ALERT pin remains active.

8.3.2.7 General Call- Reset Function

The TMP1075 responds to the two-wire general call address (0000 000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000 110, the TMP1075 resets the internal registers to the power-up reset values.

8.3.2.8 High-Speed Mode (HS)

For the two-wire bus to operate at frequencies above 400 kHz, the host device must issue an HS mode host code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP1075 device does not acknowledge this byte, but it does switch the input filters on the SDA and SCL and the output filters on the SDA to operate in HS mode. After the HS mode host code is issued, the host transmits a two-wire device address to initiate a data transfer operation. The bus continues to operate in HS mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP1075 switches the input and output filters back to fast-mode operation.

8.3.2.9 Coexists in I^{3}C Mixed Fast Mode

A bus with both I^{3}C and I^{2}C interfaces is referred to as a mixed fast mode with clock speeds up to 12.5 MHz. In order for the TMP1075, which is an I^{2}C device, to coexist in the same bus, the device incorporated a spike suppression filter of 50 ns on the SDA and SCL pins to avoid any interference to the bus when communicating with I^{3}C devices.

8.3.2.10 Time-Out Function

The TMP1075 resets the serial interface if SDA is held low for 25 ms (typical) between a START and STOP condition. The TMP1075 releases the SDA bus is held low and waits for a START condition. To avoid activating the time-out function, a communication speed of at least 1 kHz must be maintained.

8.3.3 Timing Diagrams

The TMP1075 is two-wire SMBus and I^{2}C interface-compatible. 图 12 to 图 17 describe the various operations on the TMP1075. The following list provides bus definitions.

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the host device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a host receive, the termination of the data transfer can be signaled by the host generating a Not-Acknowledge on the last byte that is transmitted by the target device.

8.3.4 Two-Wire Timing Diagrams
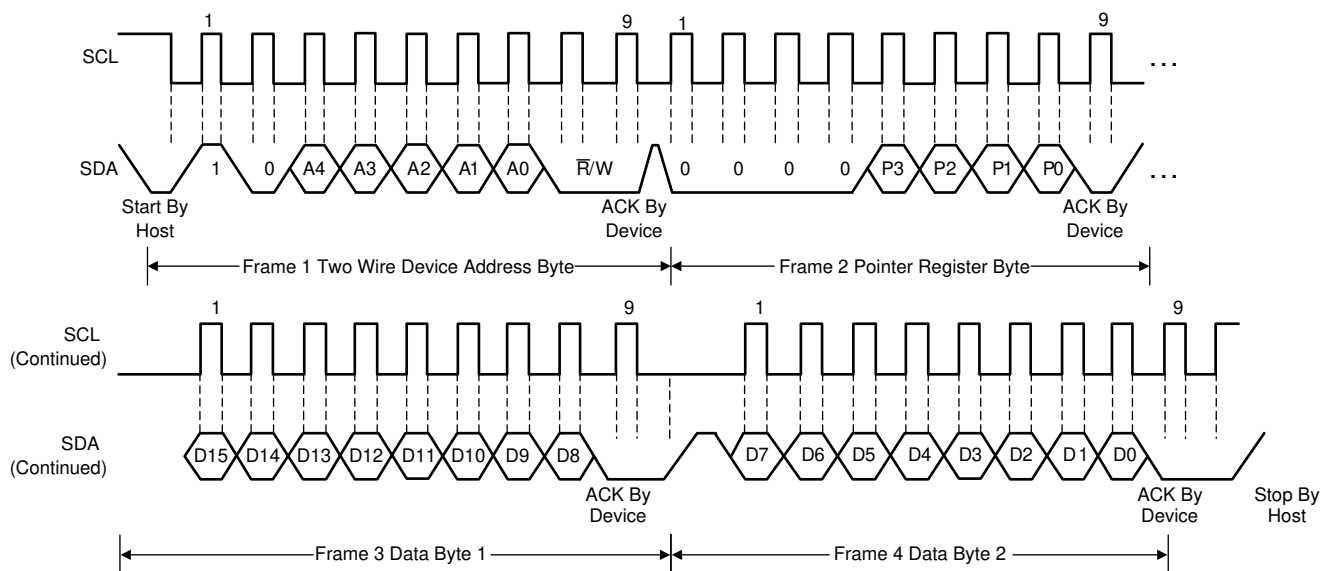
图 12. **Two-Wire Timing Diagram for Write Word Format**
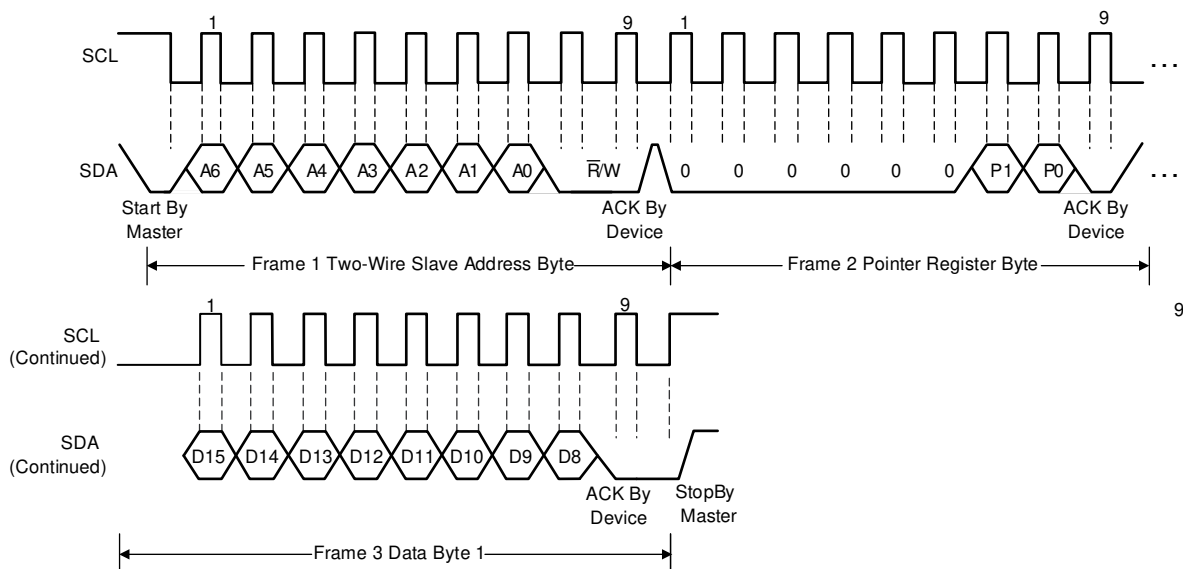
图 13. **Two-Wire Timing Diagram for Write Single Byte Format**
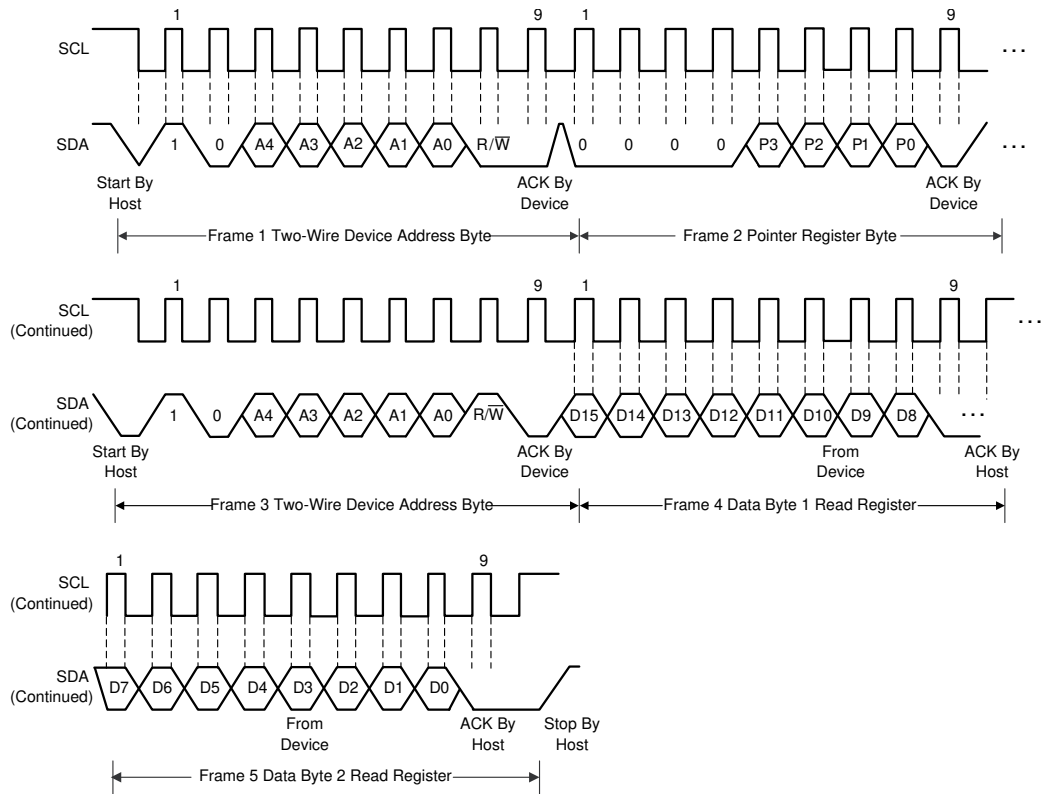
图 14. Two-Wire Timing Diagram for Read Word Format
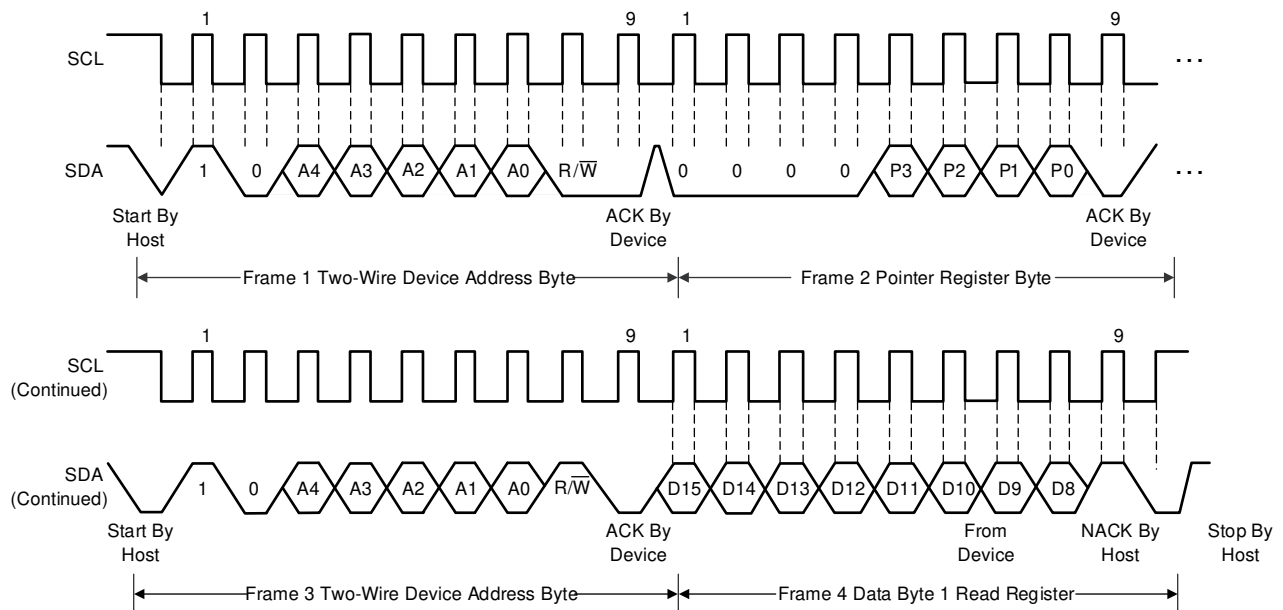
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图 15. Two-Wire Timing Diagram for Read Single Byte Format
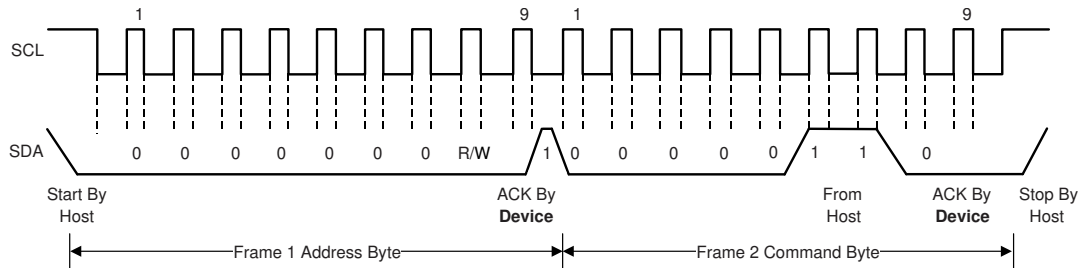
图 16. **General-Call Reset Command Timing Diagram**
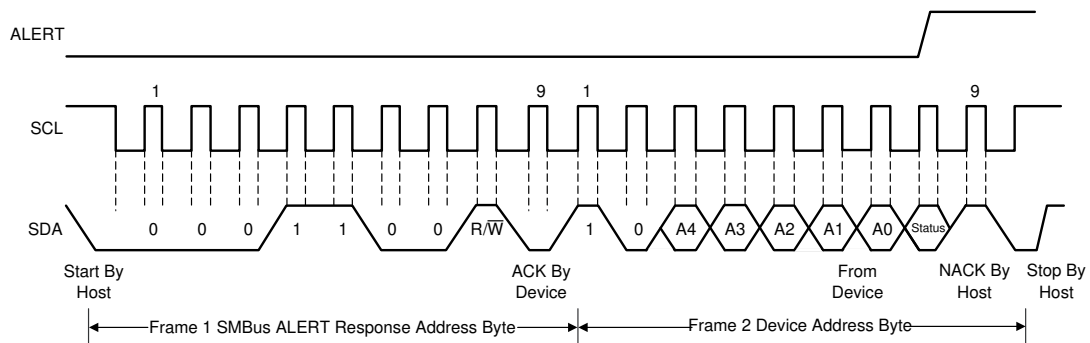
图 17. **Timing Diagram for SMBus Alert**

8.4 Device Functional Modes

8.4.1 Shutdown Mode (SD)

Shutdown mode (SD) of the TMP1075 device allows the user to conserve power by shutting down all device circuitry except the serial interface, which reduces current consumption to 0.37 μA (typical). SD is initiated when the SD bit in the configuration register is set to 1. When SD is equal to 0, the device stays in continuous conversion mode.

8.4.2 One-Shot Mode (OS)

The TMP1075 features a one-shot mode (OS) temperature measurement. When the device is in shutdown mode, writing 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP1075 when continuous temperature monitoring is not required. When the configuration register is read, the OS bit always reads zero.

8.4.3 Continuous Conversion Mode (CC)

When the device is operating in continuous conversion mode (SD=0), every conversion cycle consists of an active conversion, followed by a standby as shown in 图 18. The device consumes 52 μA (typical) during active conversion, while the low-power standby consumes 0.3 μA. Active conversion time is 5.5 ms before the part goes on standby. 表 7 shows the list of conversion cycle configured using [R1:R0] bits in the configuration register.

Device Functional Modes (接下页)
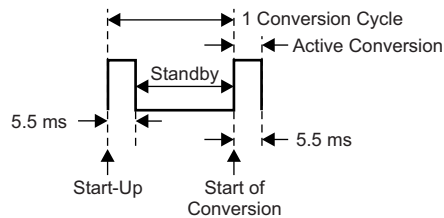
图 18. **Conversion Rate Diagram**

8.4.4 Thermostat Mode (TM)

The thermostat mode bit indicates whether ALERT pin operates in comparator mode (TM = 0) or interrupt mode (TM = 1). ALERT pin mode is controlled by TM (bit 9) of the configuration register. Any write to the TM bit changes the ALERT pin to a none active condition, clears the faults count, and clears the alert interrupt history. The ALERT pin can be disabled in both comparator and interrupt modes if both limit registers are set to the rail values T_{LOW} = −128°C and T_{HIGH} = +127.9375°C.

8.4.4.1 Comparator Mode (TM = 0)

In comparator mode (TM = 0), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of Fault Queue bits [F1:F0]. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

The difference between the two limits acts as a hysteresis on the comparator output, and a fault counter prevents false alerts as a result of system noise. The SMBus Alert response function is ignored in the comparator mode.

8.4.4.2 Interrupt Mode (TM = 1)

In interrupt mode (TM = 1), the device starts to compare temperature readings with the High Limit register value. The ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of conversions as set by the Fault Queue bits [F1:F0]. The ALERT pin remains active until it is cleared by one of three events: a read of any register, a successful SMBus Alert response, or a shutdown command. After the ALERT pin is cleared, the device starts to compare temperature readings with the T_{LOW}. The ALERT pin becomes active again only when the temperature drops below T_{LOW} for a consecutive number of conversions as set by the Fault Queue bits. The ALERT pin remains active until cleared by any of the same three clearing events. After the ALERT pin is cleared by one of the events, the cycle repeats and the device resumes to compare the temperature to T_{HIGH}. The interrupt mode history is cleared by a change in the TM=0 bit, setting the device to SD mode, or resetting the device.

8.4.4.3 Polarity Mode (POL)

The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is shown in 图 19.

Device Functional Modes (接下页)
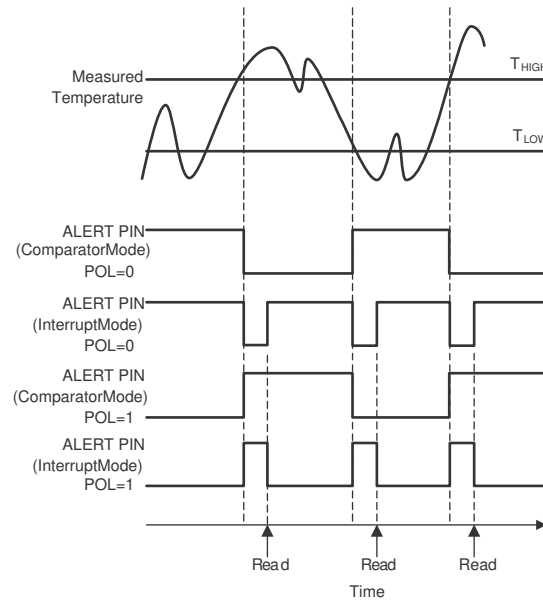
图 19. Output Transfer Function Diagrams

8.5 Register Map

表 4. TMP1075 Register Map

ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
00h	R	0000h	TEMP	Temperature result register	Go
01h	R/W	00FFh	CFGR	Configuration register	Go
02h	R/W	4B00h	LLIM	Low limit register	Go
03h	R/W	5000h	HLIM	High limit register	Go
0Fh	R	7500h	DIEID	Device ID register	Go

注

TMP1075 Configuration register supports single byte read and write for software compatibility with xx75 standard temperature sensors.

8.5.1 Register Descriptions

表 5. TMP1075 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.5.1.1 Temperature Register (address = 00h) [default reset = 0000h]

The Temperature register of the TMP1075 is a 12-bit, read-only register that stores the result of the most recent conversion (see 图 20). Data is represented in binary two's complement format. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Following power-up or reset, the Temperature register value is 0°C until the first conversion is complete.

图 20. Temperature Register

15	14	13	12	11	10	9	8
T11	T10	T9	T8	T7	T6	T5	T4
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

7	6	5	4	3	2	1	0
T3	T2	T1	T0	0	0	0	0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

表 6. Temperature Register Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:4	T[11:0]	R	000h	12-bit, read-only register that stores the most recent temperature conversion results.
3:0	—	R	0h	Not used

8.5.1.2 *Configuration Register (address = 01h) [default reset = 00FFh]*

The Configuration register is an 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format of the Configuration register for the TMP1075 is shown in 图 21 followed by a breakdown of the register bits. The power-up or reset value of the Configuration register are all bits equal to 00FFh.

图 21. Configuration Register

15	14	13	12	11	10	9	8
OS	R1	R0	F1	F0	POL	TM	SD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

表 7. Configuration Register Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	OS	R/W	0	One-shot conversion mode. Writing 1, starts a single temperature conversion. Read returns 0.
14:13	R[1:0]	R/W	0	Conversion rate setting when device is in continuos conversion mode 00: 27.5 ms conversion rate 01: 55 ms conversion rate 10: 110 ms conversion rate 11: 220 ms conversion rate
12:11	F[1:0]	R/W	0	Consecutive fault measurements to trigger the alert function 00: 1 fault 01: 2 faults 10: 3 faults 11: 4 faults
10	POL	R/W	0	Polarity of the output pin 0: Active low ALERT pin 1: Active high ALERT pin
9	TM	R/W	0	Selects the function of the ALERT pin 0: ALERT pin functions in comparator mode 1: ALERT pin functions in interrupt mode
8	SD	R/W	0	Sets the device in shutdown mode to conserve power 0: Device is in continuos conversion 1: Device is in shutdown mode
7:0	—	R/W	FFh	Not used

注

Configuration register supports single byte read and write over I^{2}C bus to ensure software compatibility with other xx75 standard temperature sensors like TMP75 and LM75. When a single byte write is performed, the data byte on the I^{2}C bus updates the register bits 15-8. Similarly when a single byte read is performed, the data bits 15-8 is transferred over the I^{2}C bus.

8.5.1.3 Low Limit Register (address = 02h) [default reset = 4B00h]

The register is configured as a 12-bit, read/write register and data is represented in two's complement format. The layout for T_{LOW} is the same as for the Temperature register and is shown in 图 22. The default reset value is 4B00h and corresponds to 75°C.

图 22. **Low Limit Register**

15	14	13	12	11	10	9	8
L11	L10	L9	L8	L7	L6	L5	L4
R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1
7	6	5	4	3	2	1	0
L3	L2	L1	L0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8. **Low Limit Register Field Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:4	L[11:0]	R/W	4B0h	12-bit, read-write register that stores the low limit for comparison with temperature results.
3:0	—	R/W	0h	Not used

8.5.1.4 High Limit Register (address = 03h) [default reset = 5000h]

The register is configured as a 12-bit, read/write register and data is represented in two's complement format. The layout for T_{HIGH} is the same as for the Temperature register and is shown in 图 23. The default reset value is 5000h and corresponds to 80°C.

图 23. **High Limit Register**

15	14	13	12	11	10	9	8
H11	H10	H9	H8	H7	H6	H5	H4
R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
H3	H2	H1	H0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9. **High Limit Register Field Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:4	H[11:0]	R/W	500h	12-bit, read-write register that stores the high limit for comparison with temperature results.
3:0	—	R/W	0h	Not used

8.5.1.5 *Device ID Register (address = 0Fh) [default reset = 7500]*

This read only register reads the device ID as shown in 图 24.

图 24. Device ID Register

15	14	13	12	11	10	9	8
DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
R-0	R-1	R-1	R-1	R-0	R-1	R-0	R-1
7	6	5	4	3	2	1	0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

表 10. Device ID Register Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	DID[15:0]	R/W	7500h	16-bit, read-only register that stores the die ID for the device. The MSB reads the static value 75h to indicate the device name for TMP1075

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMP1075 can measure the PCB temperature of the location where the user mounts the device. The TMP1075 features two-wire SMBus and I^{2}C interface compatibility, with the TMP1075 allowing up to 32 devices on one bus. The TMP1075 requires a pullup resistor on the SDA pin, and if needed, on the SCL and ALERT pins. A 0.01-μF bypass capacitor is also required as shown in 图 25.

9.2 Typical Application
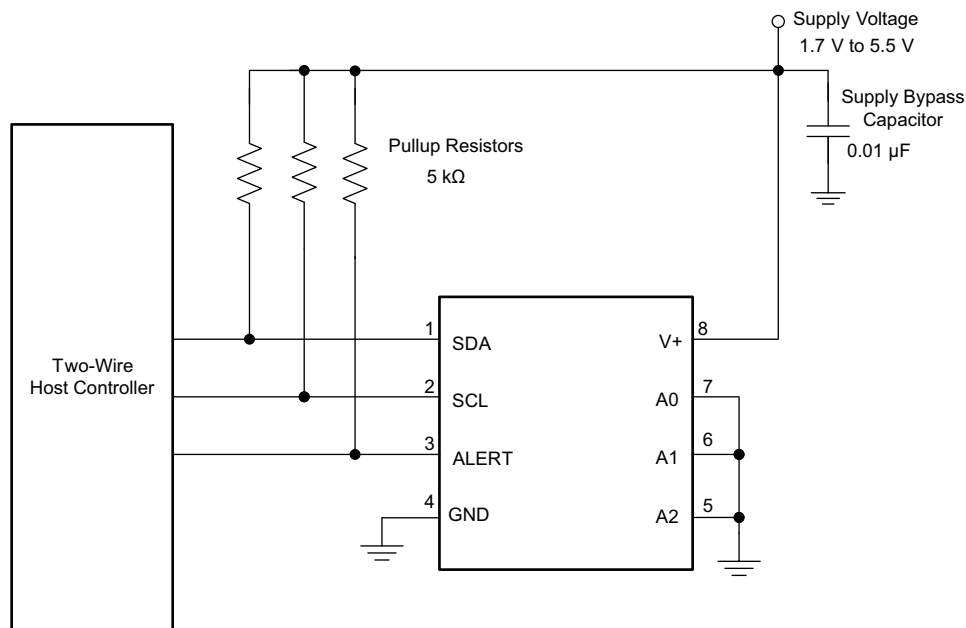
图 25. Typical Connections

9.2.1 Design Requirements

The recommended value for the pullup resistor is 5 kΩ. In some applications, the pullup resistor can be lower or higher than 5 kΩ, but the maximum current through the pullup current is recommended to not exceed 3 mA on the SCL and SDA pins. The SCL, SDA, A0, A1, and ALERT lines can be pulled up to a supply that is higher than V+. The A2 pin can only be connected to GND or V+. When the ALERT pin is not used, it can either be connected GND or left floating.

9.2.2 Detailed Design Procedure

Place the TMP1075 device in close proximity to the heat source that must be monitored with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

Typical Application (接下页)

9.2.2.1 Migrating From the xx75 Device Family

The TMP1075 is designed specifically to be a pin-to-pin compatible replacement with xx75 family of devices. This includes considerations for software compatibility. The two byte registers of the TMP1075 dynamically support single byte read or write, meaning that replacing older xx75 standard temperature sensors should not require any updates to existing code.

9.2.3 Application Curve

For application curves, see 表 11:

表 11. Table of Graphs

FIGURE	TITLE
图 9	Sampling Period Change vs Temperature (1.7V to 5.5V)

10 Power Supply Recommendations

The TMP1075 operates with a power supply in the range of 1.7 V to 5.5 V. A power-supply bypass capacitor is required for precision and stability. Place this power-supply bypass capacitor as close to the supply and ground pins of the device as possible. A typical value for this supply bypass capacitor is 0.01 μF. Applications with noisy or high-impedance power supplies can require a bigger bypass capacitor to reject power-supply noise.

To minimize device self-heating and improve temperature precision, it is recommended to:

- Use the minimum supply voltage rail available
- Avoid communication over I^2C bus during ADC conversion
- Use one-shot mode to minimize power consumption
- Set I^2C signal levels V_{IL} close to ground and V_{IH} above 90% of V+
- Maintain the I2C bus signals positive edge less than 1 μs by using a pull-up resistor < 10 kΩ
- Connect the address pins A_0 and A_1 to either ground or V+

11 Layout

11.1 Layout Guidelines

Place the power-supply bypass capacitor as close to the supply and ground pins as possible. The recommended value of this bypass capacitor is 0.01 μF. Pullup the open-drain output pins SDA and ALERT through 5 kΩ pullup resistors. The SCL requires a pullup resistor only if the microprocessor output is open drain.

11.2 Layout Example
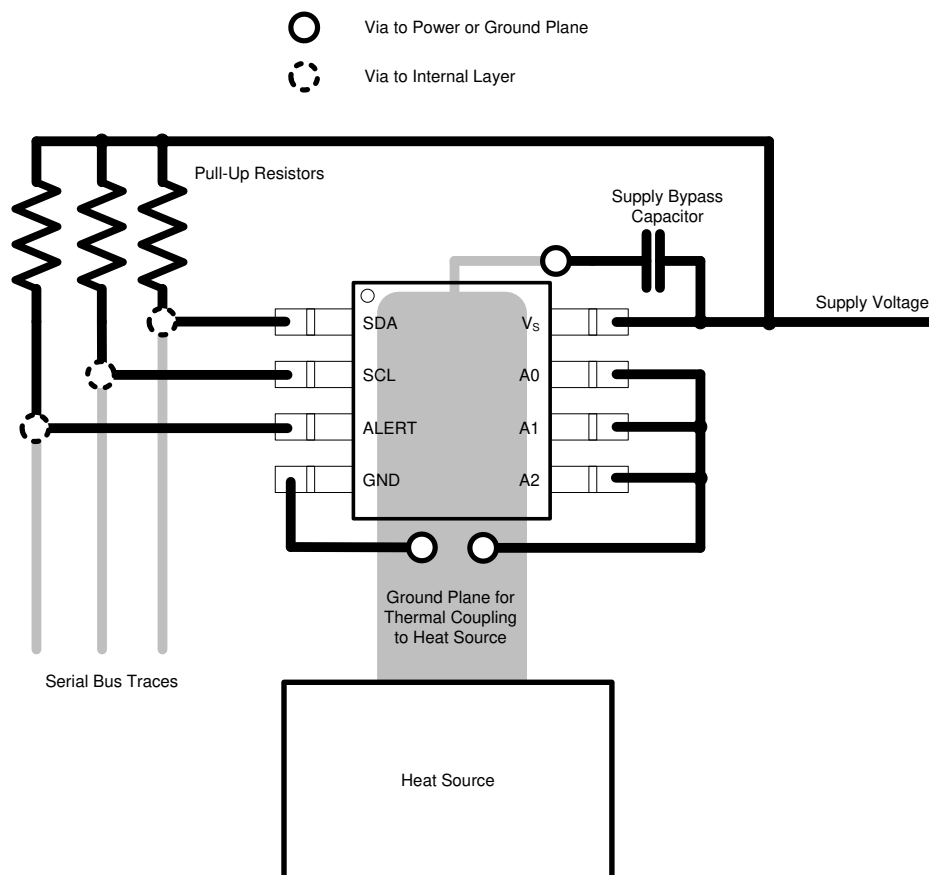
图 26. **Layout Example**

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP1075DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	1075	Samples
TMP1075DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	1075	Samples
TMP1075DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1075	Samples
TMP1075DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1AE	Samples
TMP1075DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1AE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP1075DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP1075DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP1075DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP1075DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TMP1075DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP1075DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP1075DGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP1075DR	SOIC	D	8	2500	853.0	449.0	35.0
TMP1075DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TMP1075DSGT	WSON	DSG	8	250	210.0	185.0	35.0

.228-.244 TYP
[5.80-6.19]

A

PIN 1 ID AREA

1

.189-.197
[4.81-5.00]
NOTE 3

4

B

.150-.157
[3.81-3.98]
NOTE 4

6X .050
[1.27]

8

2X

.150
[3.81]

5

8X .012-.020
[0.31-0.51]

⊕ | .010 [0.25] Ⓜ | C | A | B

C ◄

SEATING PLANE

⌒ | .004 [0.1] | C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010 TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

1

8X (.024)
[0.6]

SYMM
℄

SEE
DETAILS

8

SYMM
℄

6X (.050)
[1.27]

4

5

(R.002) TYP
[0.05]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

.0028 MIN
[0.07]
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SYMM

8X (.061)
[1.55]

1

8X (.024)
[0.6]

SYMM

8

6X (.050)
[1.27]

4

5

(R.002) TYP
[0.05]

(.213)
[5.4]

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
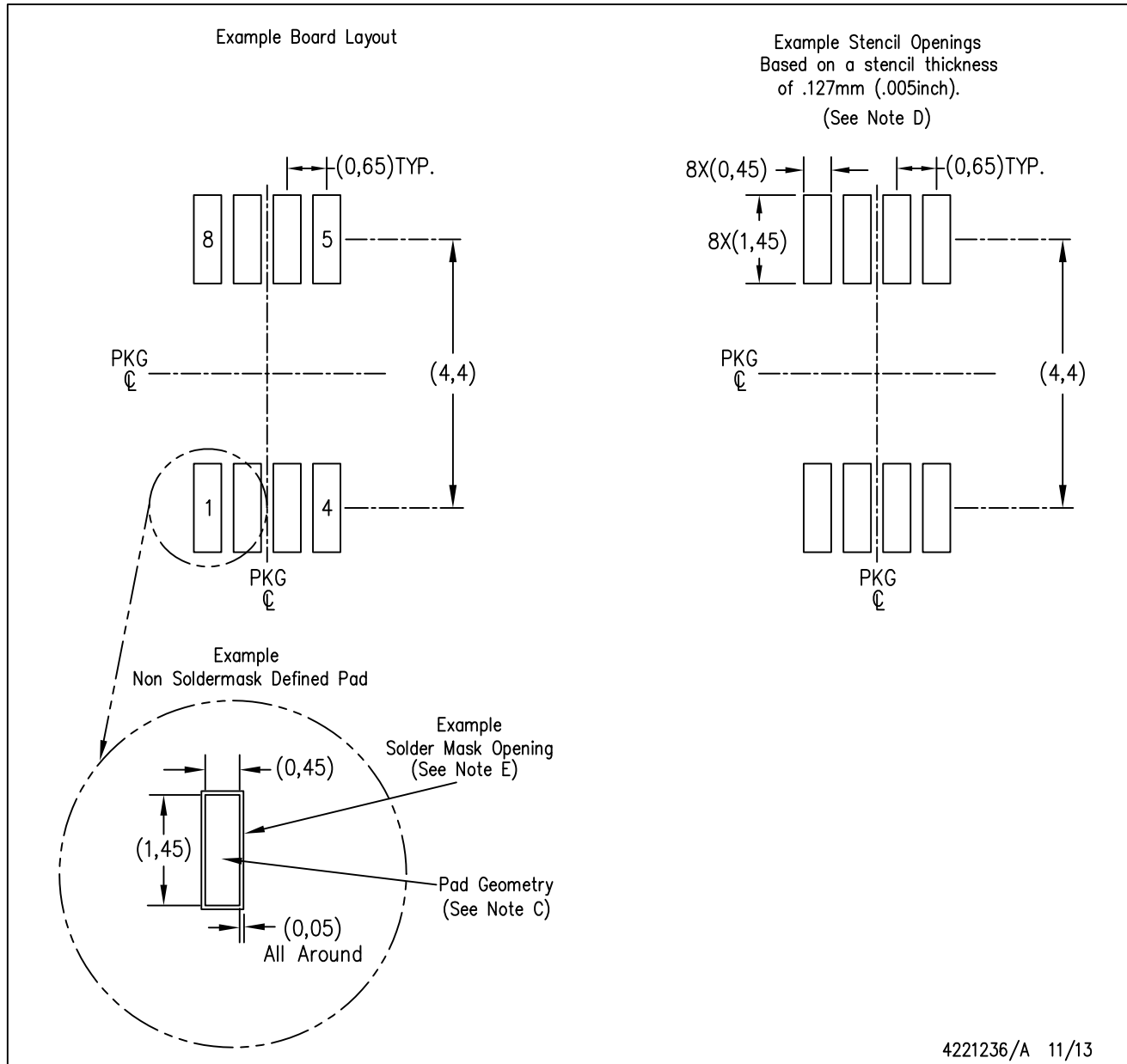9. Board assembly site may have different recommendations for stencil design.

DGK (S−PDSO−G8) PLASTIC SMALL−OUTLINE PACKAGE

0,65

8

5

0,38
0,25

⊕ | 0,13 Ⓜ

⟨D| 3,10
2,90

5,05
4,75

1

4

⟨C|
3,10
2,90

0,23
0,13

Gauge Plane

0°−8°

0,25

0,70
0,40

1,10 MAX

0,15
0,05

Seating Plane

◠ | 0,10

4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
       not exceed 0.15 per end.
   ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
   E. Falls within JEDEC MO−187 variation AA, except interlead flash.

DGK (S-PDSO-G8)   PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

(0,65)TYP.

8   5

PKG
℄

(4,4)

1   4

PKG
℄

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

(0,45)

(1,45)

(0,05)
All Around

Pad Geometry
(See Note C)

8X(0,45)   (0,65)TYP.

8X(1,45)

PKG
℄

(4,4)

PKG
℄

4221236/A 11/13

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC-7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

This image is a representation of the package family, actual package may vary.
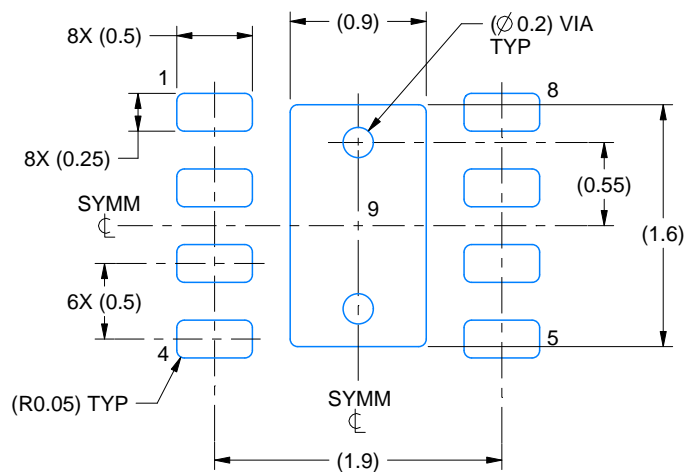Refer to the product data sheet for package details.

4224783/A

A 2.1 / 1.9 B

PIN 1 INDEX AREA

2.1 / 1.9

0.32 / 0.18

0.4 / 0.2

ALTERNATIVE TERMINAL SHAPE
TYPICAL

0.8 MAX

0.05 / 0.00

C

SEATING PLANE

0.08 C

EXPOSED THERMAL PAD

0.9 ± 0.1

4

5

6X 0.5

2X 1.5

9

1.6 ± 0.1

1

8

PIN 1 ID

8X 0.4 / 0.2

8X 0.32 / 0.18

(0.2) TYP

0.1 Ⓜ C A B
0.05 Ⓜ C
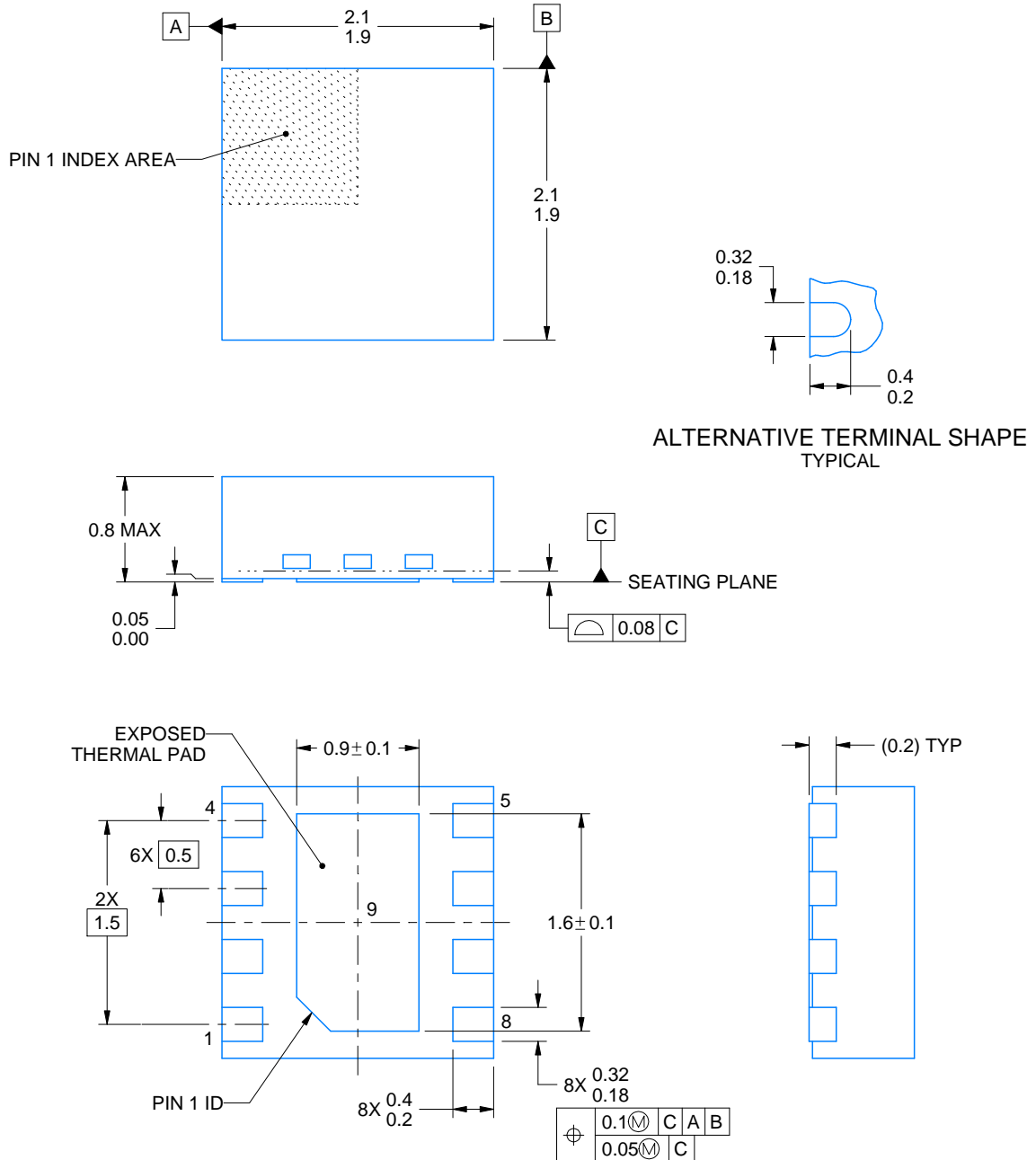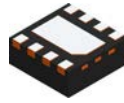
4218900/D   04/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

8X (0.5)

(0.9)

($\emptyset$ 0.2) VIA
TYP

1

8

8X (0.25)

SYMM
℄

9

(0.55)

(1.6)

6X (0.5)

4

5

(R0.05) TYP

SYMM
℄

(1.9)

LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
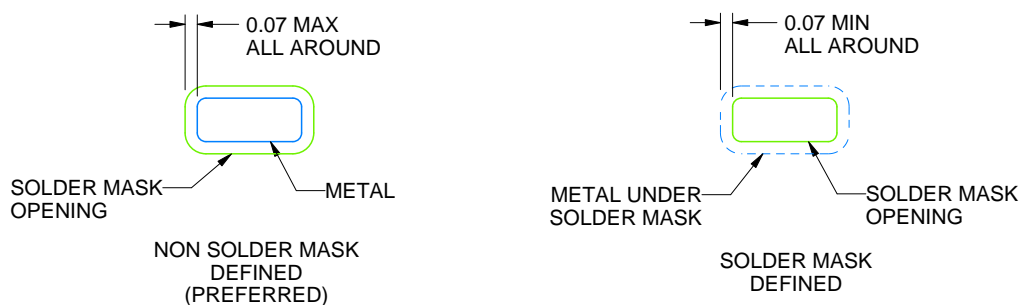
SOLDER MASK DETAILS

4218900/D   04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
   on this view. It is recommended that vias under paste be filled, plugged or tented.

DSG0008A
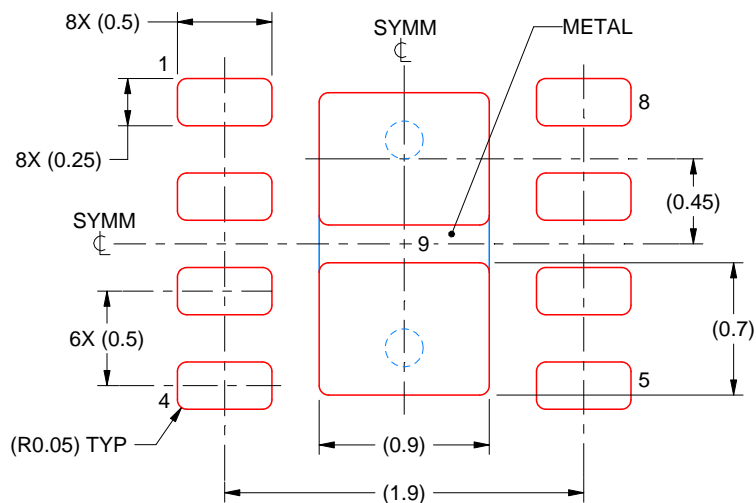
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D   04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.