TEXAS INSTRUMENTS
TMP126-Q1
SNIS227 – MAY 2021

TMP126-Q1 High-Accuracy, Low-Power SPI Temperature Sensor with 175 °C Operation, CRC and Slew Rate Alert

1 Features

- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade-0: –55 °C to 175 °C Ambient Operating Temperature
  - Device HBM Classification Level 2
  - Device CDM Classification Level C2b
- High accuracy
  - ±0.3 °C (maximum) from –20 °C to 85 °C
  - ±0.4 °C (maximum) from –40 °C to 125 °C
  - ±0.5 °C (maximum) from –55 °C to 150 °C
  - ±1 °C (maximum) from 150 °C to 175 °C
- Operating temperature range –55 °C to 175 °C
- Supply range: 1.62 V to 5.5 V
- Factory-calibrated
  - NIST traceability
- Low power consumption
- Programmable temperature alert limits
- Temperature slew rate alert
- Optional Cyclic Redundancy Check (CRC)
- 3-wire SPI interface

2 Applications

- Transmission Control Units
- On-board Chargers (OBC)
- Brake Systems
- Traction Inverters
- Vehicle Control Units (VCU)
- DC/DC Converters
- Power Distribution Units (PDU)
- Powertrain Exhaust Sensors

3 Description

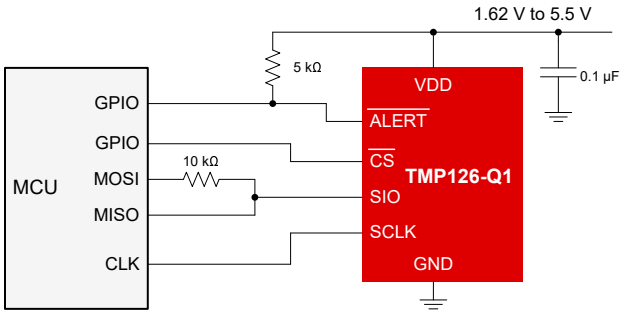
The TMP126-Q1 is a high 0.3 °C accuracy digital temperature that supports an ambient temperature range of –55 °C to 175 °C. The TMP126-Q1 features a 14-bit signed temperature resolution (0.03125 °C per LSB) while operating over a supply range of 1.62 V to 5.5 V. With a fast conversion rate, low supply current, and a simple 3-wire SPI compatible interface, the TMP126-Q1 is designed for a wide range of applications.

The TMP126-Q1 includes additional advanced features for increased reliability in harsh environments such as optional CRC checksum for data integrity, programmable alert limits, a temperature slew rate warning, and an enhanced operational temperature range. The device utilizes a NIST traceable factory calibration for guaranteed accuracy and comes in a small SOT package for close placement to heat sources along with fast response times.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TMP126-Q1	SOT-23 (6)	2.90 mm × 1.60 mm
	SOT-SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2021	*	Initial release.

5 Device Comparison

Table 5-1. Device Comparison

Feature	TMP126-Q1	TMP127-Q1
Accuracy	0.3 °C	0.8 °C
Packages	DBV, DCK	DBV
Continuous and shutdown mode	•	•
175 °C operation	•	•
Grade-0	•	•
NIST Traceable	•	
Alert pin functionality	•	
Slew rate warning	•	
CRC option	•	

6 Pin Configuration and Functions

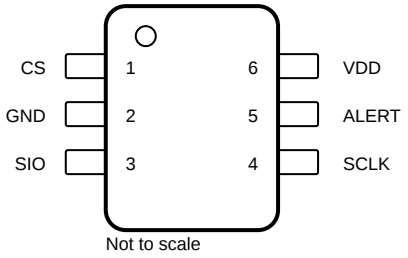

Figure 6-1. DBV 6-pin SOT-23 Top View

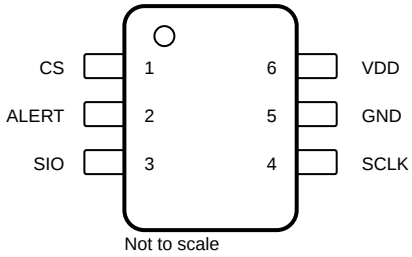

Figure 6-2. DCK 6-pin SC70 Top View

Table 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBV	DCK		
$\overline{CS}$	1	1	I	Chip select signal to activate SPI interface
GND	2	5	-	Ground
SIO	3	3	I/O	System input/output
SCLK	4	4	I	System clock input
$\overline{ALERT}$	5	2	O	Alert open-drain output. Can be left floating or grounded when not used.
VDD	6	6	-	Supply voltage

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7 Specifications

7.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	6	V
I/O voltage	SIO	–0.3	V_{DD} + 0.2 V	V
I/O voltage	$\overline{CS}$, $\overline{ALERT}$, SCLK	–0.3	6	V
Operating junction temperature, T_J		–65	180	°C
Storage temperature, T_{stg}		–65	180	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C2b	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.62	3.3	5.5	V
$V_{I/O}$	SIO	0		V_{DD}	V
$V_{I/O}$	$\overline{CS}$, $\overline{ALERT}$, SCLK	0		5.5	V
T_A	Operating ambient temperature	-55		175	°C

7.4 Thermal Information

THERMAL METRIC		TMP126-Q1	
		DBV	DCK
		6-pins	6-pins
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168.2	183.4
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.5	136.4
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–
$R_{\theta JB}$	Junction-to-board thermal resistance	48.1	74.2
ψ_{JT}	Junction-to-top characterization parameter	27.5	57.9
ψ_{JB}	Junction-to-board characterization parameter	47.9	74.0
M_T	Thermal Mass	TBD	TBD

7.5 Electrical Characteristics

Over free-air temperature range and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR}	Temperature accuracy	-20 °C to 85 °C	1-Hz conversion cycle	-0.3		0.3	°C
		-40 °C to 125°C		-0.4		0.4	°C
		-55 °C to 150°C		-0.5		0.5	°C
		-55 °C to 175°C		-1		1	°C
PSR	DC power supply rejection	One-shot mode			TBD		m°C/V
T_{RES}	Temperature resolution	Including sign bit			14		Bits
		LSB			31.25		m°C
T_{REPEAT}	Repeatability(1)	V_{DD} = 3.3 V 1-Hz conversion cycle			TBD		LSB
	Long-term stability and drift	1000 hours at 150°C(2)			TBD		°C
	Temperature cycling and hysteresis(3)				TBD		LSB
t_{CONV}	Conversion time			4.5	5.5	7	ms
t_{VAR}	Timing variation of all device settings			TBD		TBD	%
DIGITAL INPUT/OUTPUT							
C_{IN}	Input capacitance	f = 1 MHz			4		pF
V_{IH}	Input logic high level	SCLK, SIO, $\overline{CS}$		0.7 * (V_{DD})			V
V_{IL}	Input logic low level	SCLK, SIO, $\overline{ALERT}$, $\overline{CS}$				0.3 * (V_{DD})	V
I_{IN}	Input leakage current	SCLK, SIO, $\overline{ALERT}$, $\overline{CS}$		-1		1	µA
V_{OH}	SIO output high level	I_{OH} = 3 mA		V_{DD} - 0.4		V_{DD}	V
V_{OL}	SIO output low level	I_{OL} = -3 mA		0		0.4	V
	$\overline{ALERT}$ output logic low level	I_{OL} = -3 mA		0		0.4	V

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Over free-air temperature range and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD_ACTIVE}	Supply current during active conversion	Active Conversion, $\overline{CS}$ = V_{DD} T_A = -55 °C to 150 °C			75	100	µA
I_{DD_ACTIVE}	Supply current during active conversion	Active Conversion, $\overline{CS}$ = V_{DD} T_A = 150 °C to 175 °C				TBD	µA
I_{DD}	Average current consumption	T_A = 25 °C Conversion cycle time: 1 Hz	$\overline{CS}$ = V_{DD}		1	TBD	µA
			f_{SCLK} = 10 MHz			TBD	
		T_A = -55 °C to 150 °C Conversion cycle time: 1 Hz	$\overline{CS}$ = V_{DD}			6	
			f_{SCLK} = 10 MHz			TBD	
		T_A = 175 °C Conversion cycle time: 1 Hz	$\overline{CS}$ = V_{DD}			TBD	
			f_{SCLK} = 10 MHz			TBD	
I_{SB}	Standby current(4)	$\overline{CS}$ = V_{DD}	T_A = 25 °C		1	TBD	µA
			T_A = -55 °C to 150 °C			5	
			T_A = -55 °C to 175 °C			TBD	
I_{SD}	Shutdown current	$\overline{CS}$ = V_{DD} T_A = 25 °C			0.35	1.5	µA
	Shutdown current	$\overline{CS}$ = V_{DD} T_A = 150 °C				3.5	µA
	Shutdown current	$\overline{CS}$ = V_{DD} T_A = 175 °C				TBD	µA
V_{POR}	Power-on reset threshold voltage	Supply rising			1.3		V
	Brownout detect	Supply falling			1.1		V
t_{RAPM_VDD}	V_{DD} ramp time requirements	Supply rising or falling					µs/V
t_{RESET}	Reset Time	Time required by device to reset			1.5		ms

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) Long term stability is determined using accelerated operational life testing at a junction temperature of 150 °C.
(3) Hysteresis is defined as the ability to reproduce a temperature reading as the temperature varies from room → hot →room→cold→room. The temperatures used for this test are -40 °C, 25 °C, and 150 °C.
(4) Quiescent current between conversions

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7.6 SPI Interface Timing

Over free-air temperature range and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted)

		SPI BUS		UNIT
		MIN	MAX	
f_{CLK}	SCLK frequency		10	MHz
t_{CLK}	SCLK Period	100		ns
t_{LEAD}	Falling edge of $\overline{CS}$ to rising edge of SCLK setup time	100		ns
t_{LAG}	Rising edge of SCLK to rising edge of /CS setup time	20		ns
t_{SU}	SIO to SCLK rising edge setup time	10		ns
t_{HOLD}	SIO hold time after rising edge of SCLK	20		ns
t_{VALID}	Time from falling edge of SLCK to valid SIO data		35	ns
$t_{SIO(DIS)}$	Time from rising edge of $\overline{CS}$ to SIO high-impedance		20	ns
t_{RISE}	SIO, SCLK, $\overline{CS}$ rise time		100	ns
t_{FALL}	SIO, SCLK, $\overline{CS}$ fall time		100	ns
$t_{INTERFRAME}$	Delay between two SPI communication sequences ($\overline{CS}$ high)	700 (3.5 ns)		ns
$t_{INITIATION}$	Delay between valid V_{DD} volage and initial SPI communication	50		µs

7.7 Timing Diagram

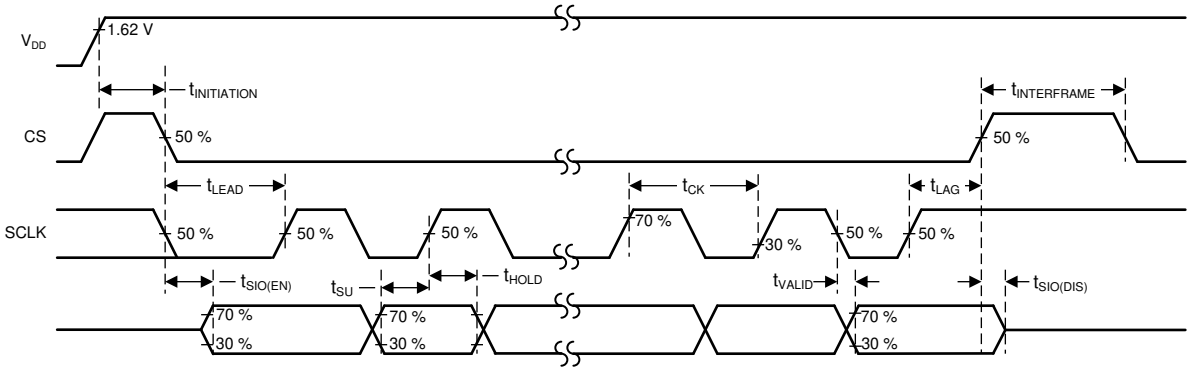

Figure 7-1. Two-Wire Timing Diagram

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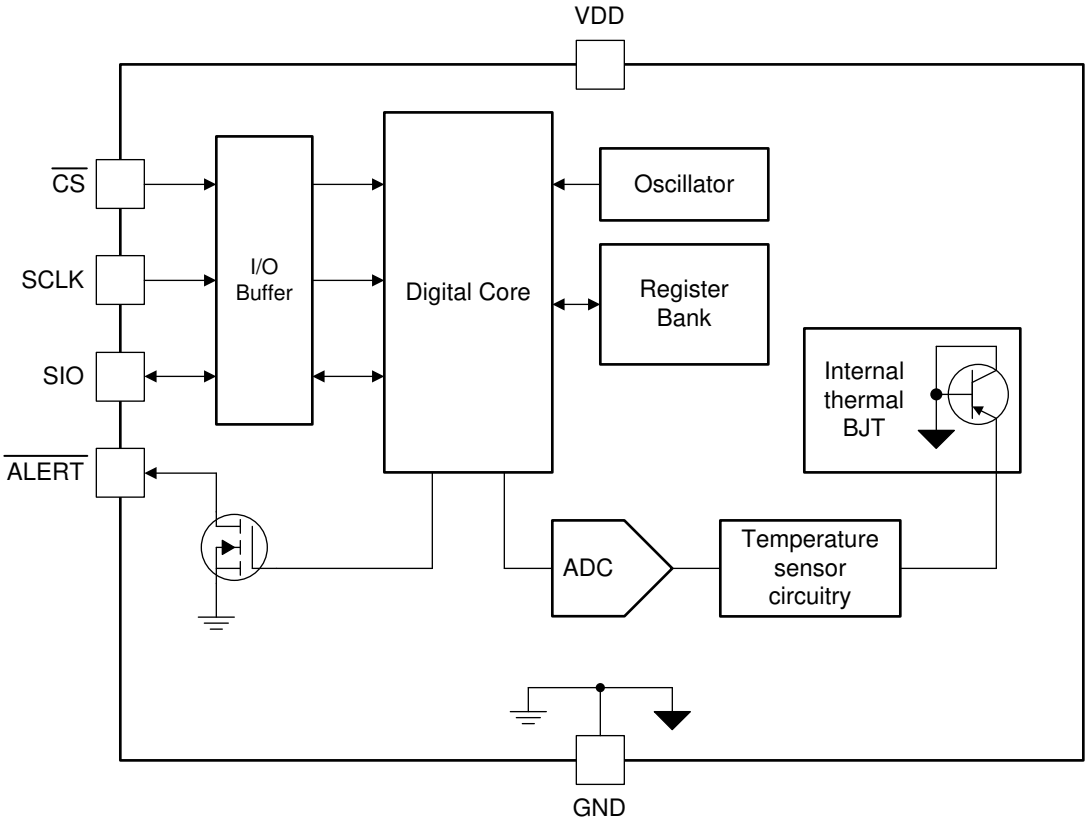
8 Detailed Description

8.1 Overview

The TMP126-Q1 is a factory calibrated digital output temperature sensor designed for thermal management and thermal protection applications. The device has a 3-wire SPI compatible interface with multiple operating modes including continuous, one-shot, and shutdown mode. The TMP126-Q1 features an $\overline{\text{ALERT}}$ output with temperature threshold settings for autonomous monitoring and system alerts. In addition the TMP126-Q1 also includes a temperature slew rate warning feature that alerts the system to temperature spikes, allowing for corrective action before reaching thermal limits.

For data integrity an optional Cyclic Redundancy Check (CRC) is available that will validate communication with the device.

8.2 Functional Block Diagram



8.3 Feature Descriptions

8.3.1 Temperature Limits

The TMP126-Q1 includes a temperature limit warning that can be enabled or disabled in the configuration register. If enabled, at the end of every completed conversion the TMP126-Q1 will compare the result against the limits stored in the low limit register and the high limit register. When exceeding these limits the $\overline{\text{ALERT}}$ pin will be set. The $\overline{\text{ALERT}}$ pin behavior will change depending on which mode the device is configured to as described in the Interrupt and Comparator Mode section.

The Alert functionality can allow the system to set the desired operating thermal limits of the system with the TMP126-Q1 and allow autonomous monitoring of temperature without the need for the system to read the temperature. When a thermal limit is exceeded the system will receive a warning through the $\overline{\text{ALERT}}$ pin and can react accordingly to adjust the operating temperature back to within normal system operation.

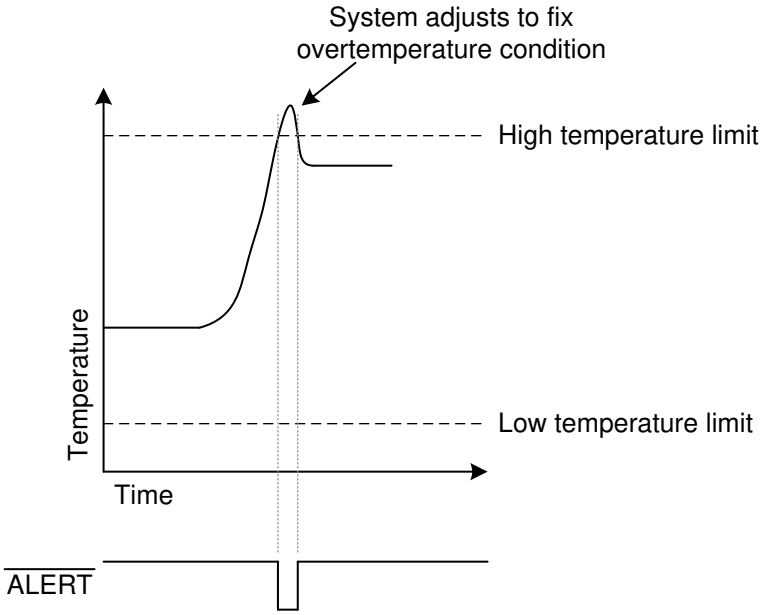


Figure 8-1. Temperature Limit Alert

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8.3.2 Slew Rate Warning

The slew rate warning is an adjustable alert option that can be adjusted with the Slew_Limit register.

The slew rate warning will notify the system of temperature spikes as they occur, allowing the system to react and correct for the increase in temperature before reaching thermal operating limits. Compared to throttling a system after crossing a thermal limit, the slew rate warning will allow a more safe system operation and greater reliability by not exceeding specified system operating conditions.

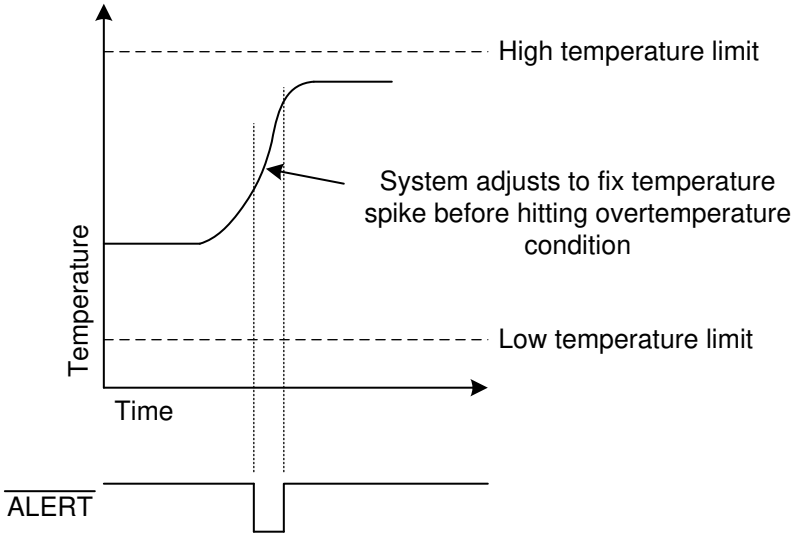

Figure 8-2. Slew Rate Alert

Calculating the slew rate requires a fixed time period and is only available in continuous mode. The Slew_Limit register is used to set the unsigned limit. The TMP126-Q1 will monitor the temperature slew rate and compare the positive change of temperature from the current conversion to the previous against the Slew_Limit. If the slew rate exceeds the Slew_Limit, the respective bits in the Alert_Status register will be set to indicate the warning. Figure 8-3 depicts the timing of the Slew Rate Warning relative to the temperature conversions. The slew rate check is always applied to the current temperature conversion and the previous temperature conversion.

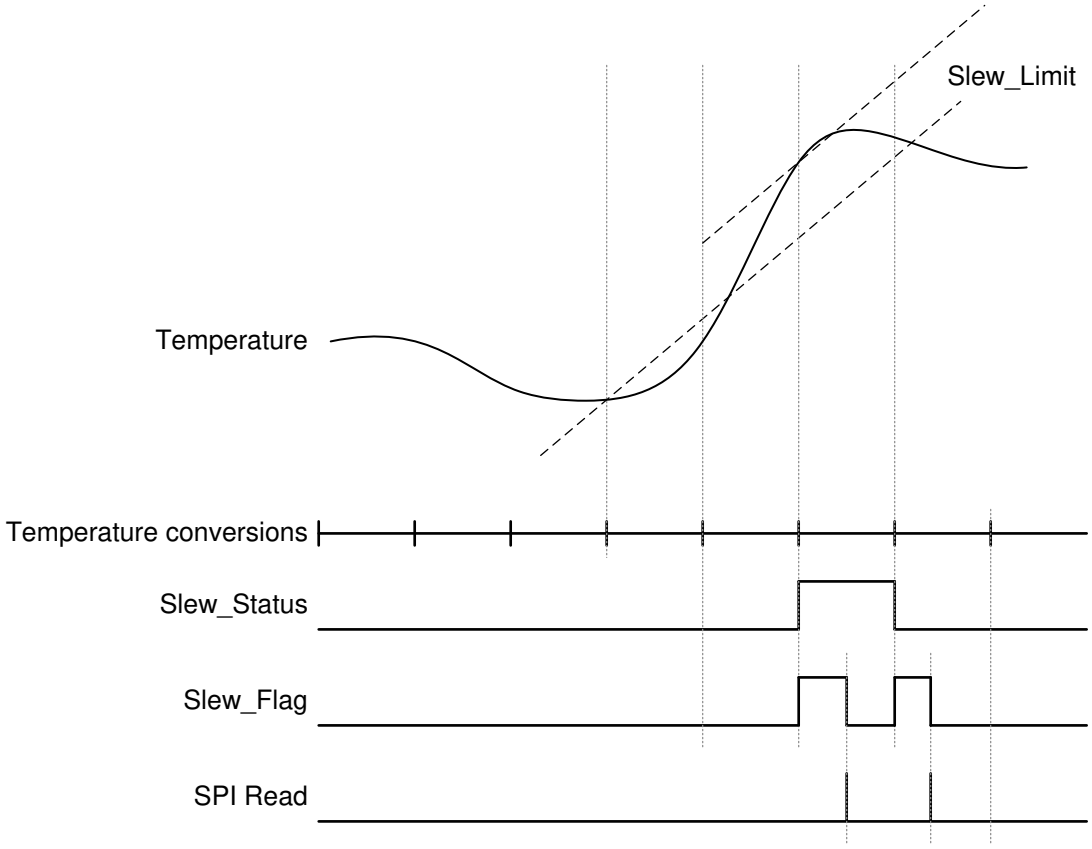

Figure 8-3. Slew Rate Warning Timing Diagram

The TMP126-Q1 does not support negative slew rate value reporting.

8.3.3 Cyclic Redundancy Check (CRC)

The TMP126-Q1 has integrated optional CRC that can be used to determine the integrity of the SPI communication to the TMP126-Q1. The CRC is enabled by setting the CRC_Enable bit in the command word to '1' with an appropriate data block length. During a read, the TMP126-Q1 will append a 16 bit CRC checksum to the data block for the host to compare with its own checksum. In this manner the host can validate the data sent by TMP126-Q1 and read from the device again if necessary. During write operations, the host will send the CRC word that the TMP126-Q1 will compare against its own checksum. If the TMP126-Q1 determines that the data sent during the write transaction was corrupted, the TMP126-Q1 will discard the write and set the CRC_Flag in the Alert_Status register to alert the host that the register settings must be sent again.

This allows the system to ensure the data integrity of the SPI communication in both write and read operations.

Writing to the configuration register with a CRC enabled transaction is currently not supported.

8.3.4 NIST Traceability

During production a unique ID is programmed into the OTP memory of the TMP126-Q1. This unique ID is used to support NIST traceability. The TMP126-Q1 units are 100% tested on a production setup that is NIST traceable and verified with equipment that is calibrated to ISO/IEC 17025 accredited standards.

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8.4 Device Functional Modes

The TMP126-Q1 can be configured to operate in various conversion modes by using the Mode bit in the configuration register. These modes provide flexibility to operate the device in the most power efficient way necessary for the intended application.

8.4.1 Continuous Conversion Mode

When the Mode bit is set to 0b in the Configuration register, the device operates in continuous conversion mode. Figure 8-4 shows that the device continuously performs temperature conversions in this mode. The TMP126-Q1 does not wait until the end of the conversion period to update the temperature, instead the temperature result register is updated at the end of the temperature conversion. After a completed active conversion, the Data_Ready flag bit is set to '1'. The user can read the interrupt/status register or the temperature result register to clear the Data_Ready flag. Therefore, the Data_Ready_Flag can be used to determine when the conversion completes so that an external controller can synchronize reading the result register with conversion result updates. The user can set the Data_Ready_Flag_En bit in the configuration register to monitor the state of the Data_Ready_Flag on the ALERT pin.

Every conversion period consists of an active temperature conversion followed by a standby period. During standby the TMP126-Q1 will de-activate all measurement circuitry to conserve power but will remain available for any SPI communication. The device typically consumes 75 µA during the temperature conversion and only 1 µA during the low-power standby period. The duration of the temperature conversion will remain fixed, but the conversion period can be configured using the Conv_Period[2:0] bit field in the Configuration register, allowing the average current consumption of the device to be optimized based on the application requirements. Changing the conversion period also affects the temperature result update rate due to the temperature result register being updated at the end of every temperature conversion.

Use Equation 1 to calculate the average current consumption of the device in continuous conversion mode.

$$I_{DD\_AVG} = \left(\frac{(I_{ACTIVE} * t_{CONV}) + (I_{SB} * t_{STANDBY})}{Conversion\ Period} \right) \quad (1)$$

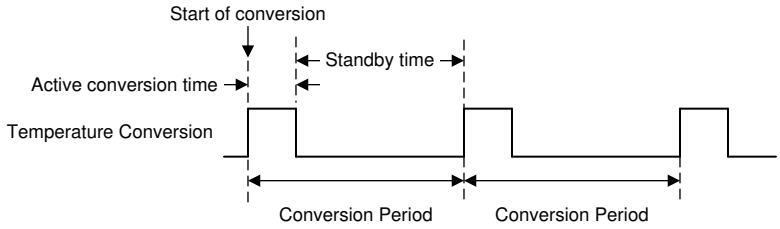

Figure 8-4. Conversion Period Timing Diagram

8.4.2 Shutdown Mode

When the Mode bit is set to 1b in the Configuration register, the device immediately enters the low-power shutdown mode. If the TMP126-Q1 is making a temperature conversion, the device will stop the conversion and discard the partial result. In this mode, the device powers down all active circuitry and can be used in conjunction with the One_Shot bit to perform temperature conversions. Engineers can use the TMP126-Q1 for battery-operated systems and other low-power consumption applications because the device typically only consumes 350 nA in Shutdown Mode.

Changing between continuous and shutdown will not clear any active alerts in the Alert_Status register register and the $\overline{\text{ALERT}}$ pin will continue to be asserted until cleared by the host. The slew rate alert will not be triggered again in shutdown mode but will not clear until read if it is already set.

8.4.3 One-Shot Mode

When One_Shot bit is set to 1b in the Configuration register the TMP126-Q1 will immediately start a new temperature conversion, referred to as a one-shot conversion, and discard any partial conversion results. After the device completes a one-shot conversion, the device will enter the low power shutdown mode. The Mode bit will be set to 1b and the One_Shot bit will be set to 0b automatically. Figure 8-5 shows a current consumption timing diagram for this mode. At the end of a one-shot conversion, the Data_Ready_Flag in the Alert_Status register is set and can be used to determine when the conversion completes.

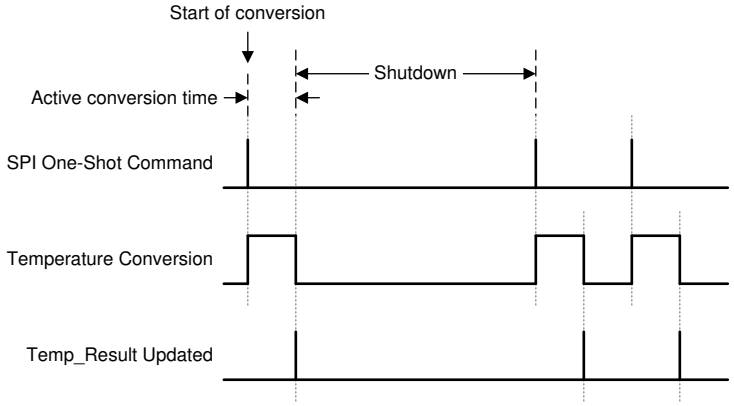

Figure 8-5. One-Shot Timing Diagram

If the One_Shot bit is continuously written to faster than the active conversion time of the TMP126, the device will continue to restart the temperature conversion with each new write. It is recommended to avoid this behavior as the temperature result does not update until a conversion finishes. If continuous one-shots are being triggered by the system Figure 8-6 depicts how the device would continually partially finish new conversions and not update the Temp_Result register.

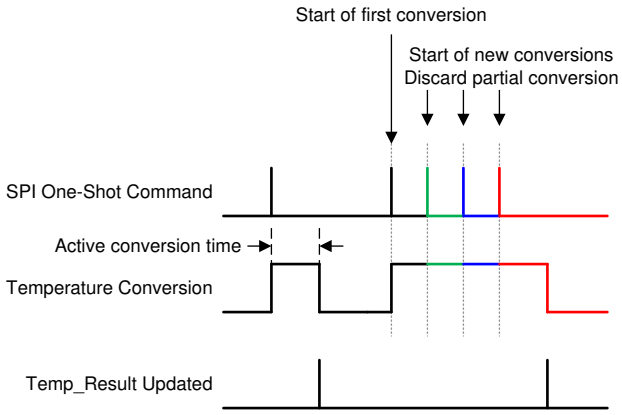

Figure 8-6. One-Shot Continuous Trigger Timing Diagram

8.4.4 Interrupt and Comparator Mode

The $\overline{\text{ALERT}}$ pin of the TMP126-Q1 can be programmed to operate in two different modes. In the interrupt mode the TMP126-Q1 will assert the $\overline{\text{ALERT}}$ pin if the temperature exceeds the limits set by temperature limit registers and the flags are enabled. After the Alert_Status is read and the interrupt bits cleared, the $\overline{\text{ALERT}}$ pin will be de-asserted. In the Comparator mode, the $\overline{\text{ALERT}}$ pin will assert if any enabled status bits of the Alert_Status are set. Changes to the Alert_Enable register will be reflected on the $\overline{\text{ALERT}}$ pin after the completed conversion or device read.

8.4.4.1 Interrupt Mode

When the INT_COMP bit in the Configuration Register is set to 0, the device is in interrupt mode. Changing the device to Interrupt mode from Comparator mode will immediately clear the Alert_Status register and reset the $\overline{\text{ALERT}}$ pin. The TMP126-Q1 will then behave as described in this section at the next temperature conversion. In this mode, the device compares the temperature result at the end of every conversion with the values in the TLow_Limit register and THigh_Limit register. If the temperature result is higher the value in the THigh_Limit register, the THigh_Status and THigh_Flag bits in the Alert_Status register will be set and the $\overline{\text{ALERT}}$ pin will assert. After a read of the Alert_Status register the flag bit will clear and the $\overline{\text{ALERT}}$ pin will de-assert. Subsequent temperature results above the hysteresis value (THigh_Limit - THigh_Hysteresis), where THigh_Hysteresis is the Most Significant Byte (MSB) in the Hysteresis register, will not set the THigh_Flag bit. The status bit will not clear until a temperature result is below (THigh_Limit - THigh_Hysteresis).

After a temperature result below (THigh_Limit - THigh_Hysteresis), the THigh_Status bit will clear, the THigh_Flag bit will be set, and the $\overline{\text{ALERT}}$ pin will be asserted to indicate the change.

If the THigh_Flag bit is not enabled in the Alert_Enable register, the flag bit will be set when the measured temperature crosses the THigh_Limit or hysteresis but the $\overline{\text{ALERT}}$ pin will not assert. The behavior for the TLow_Limit and Slew rate will be the same as the previously described high limit. Figure 8-7 shows a diagram depicting the behavior.

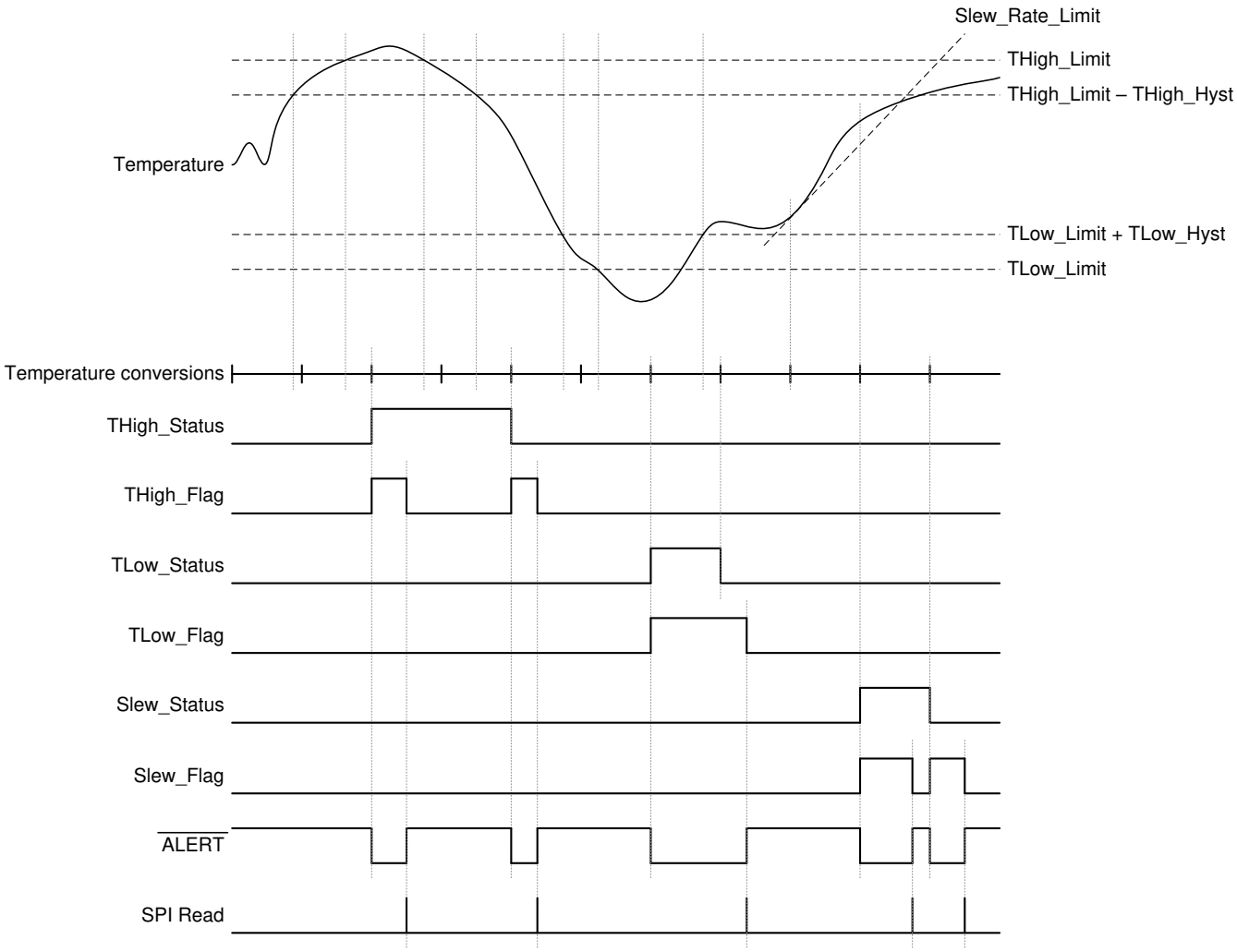

Figure 8-7. Interrupt Mode Diagram

8.4.4.2 Comparator Mode

When the INT_COMP bit in the Configuration Register is set to 0, the device is in comparator mode. Changing the device to Comparator mode from Interrupt mode will immediately clear the Alert_Status register and reset the $\overline{\text{ALERT}}$ pin. The TMP126-Q1 will then behave as described in this section at the next temperature conversion. In this mode, the device compares the temperature result at the end of every conversion with the limit registers. If the flag is enabled to assert the $\overline{\text{ALERT}}$, the $\overline{\text{ALERT}}$ will reflect the status bit of the limits. For example, if the THigh_Flag alert is enabled and the THigh_Limit is exceeded, the $\overline{\text{ALERT}}$ will assert while the THigh_Status bit is '1'. If the THigh_Flag alert is not enabled in the Alert_Enable register, the $\overline{\text{ALERT}}$ will not assert when THigh_Status bit is '1'.

After a conversion below the Hysteresis the Status bit will be set to '0' and the $\overline{\text{ALERT}}$ will de-assert. Unlike the interrupt mode, the $\overline{\text{ALERT}}$ behavior is not affected when reading the Alert_Status register. If the Alert flag is disabled in the Alert_Enable register, the $\overline{\text{ALERT}}$ pin will de-assert immediately if the respective bit is causing an alert. If there are two statuses that are affecting the $\overline{\text{ALERT}}$ such as a THigh_Limit and Slew_Rate_Limit and one of the alerts is disabled, the $\overline{\text{ALERT}}$ will remain asserted until the other limit is not exceeded. For example, if the $\overline{\text{ALERT}}$ has asserted due to a high slew rate and a high temperature and the slew rate alert is then disabled, the $\overline{\text{ALERT}}$ will only de-assert when the temperature drops below the hysteresis value. If both alerts were disabled the $\overline{\text{ALERT}}$ would then de-assert.

Thus, this mode effectively makes the device behave like a high-limit threshold detector. This mode can be used in applications where detecting if the temperature has exceeded a desired threshold is necessary. Figure 8-8 shows a timing diagram of this mode.

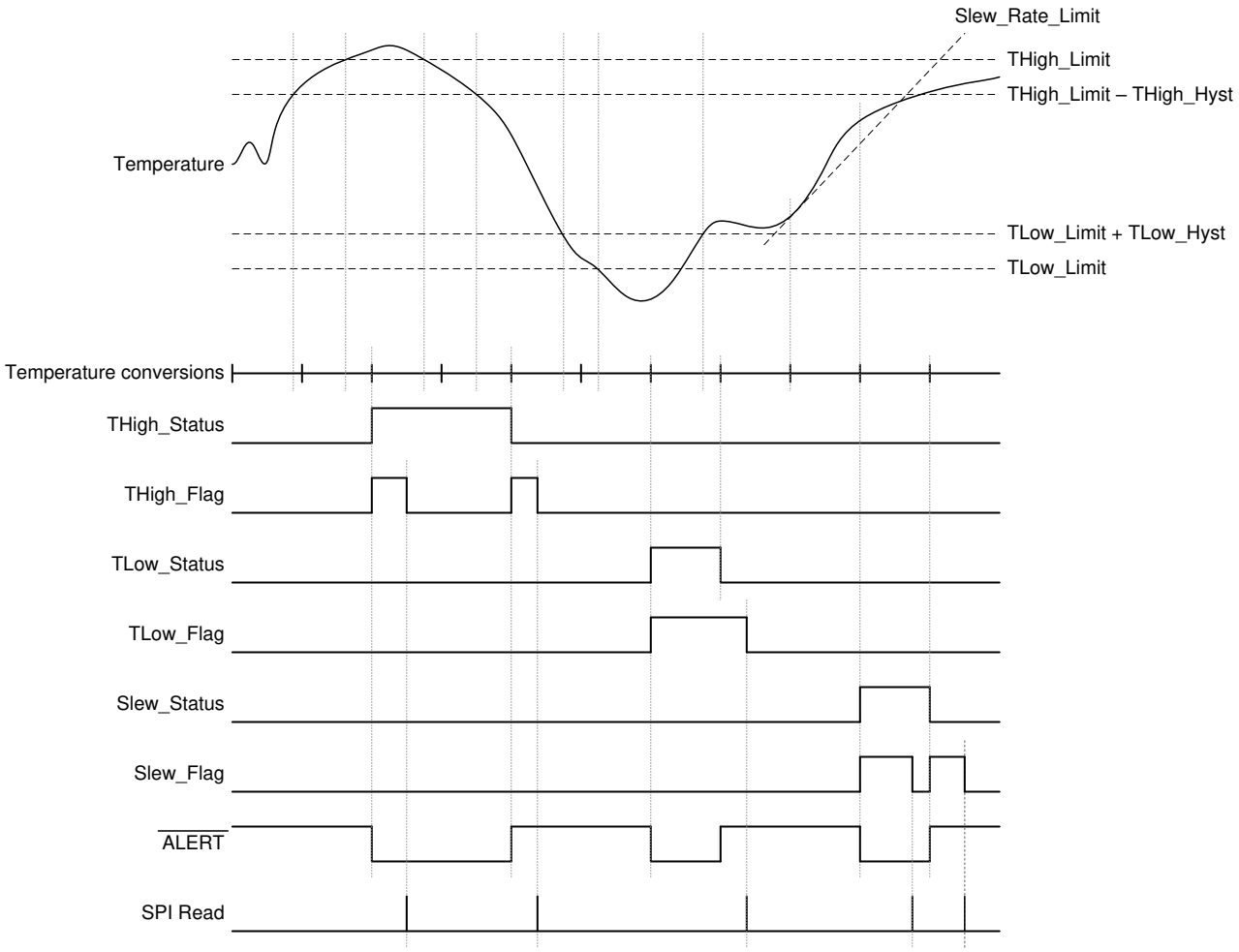

Figure 8-8. Comparator Mode Timing Diagram

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8.5 Programming

8.5.1 Temperature Data Format

Temperature data is represented by a 14-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.03125 °C. The last two bits of the register are always 00b.

Table 8-1. 14-Bit Temperature Data Format

Temperature	Digital Output	
	Binary	Hex
175 °C	0100 1011 0000 0000	5780
150 °C	0100 1011 0000 0000	4B00
125 °C	0011 1110 1000 0000	3E80
25 °C	0000 1100 1000 0000	0C80
0.03125 °C	0000 0000 0000 0100	0004
0 °C	0000 0000 0000 0000	0000
−0.03125 °C	1111 1111 1111 1100	FFFC
−25 °C	1111 0011 1000 0000	F380
−40 °C	1110 1100 0000 0000	EC00
−55 °C	1110 0100 1000 0000	E480

The first data byte is the most significant byte with most significant bit first, permitting only as much data as necessary to be read to determine temperature condition. For example, if the first four bits of the temperature data indicate an over temperature condition, the host controller could immediately abort communication and take action to remedy the excessive temperature condition.

8.5.2 Serial Bus Interface

Figure 8-9 shows an overview of the TMP126-Q1 protocol. The /CS pin must be taken low between communication transactions. Data is clocked out on the falling edge of the serial clock (SCLK), while data is clocked in on the rising edge of SCLK. The 16-bit write words are latched to the respective registers after the 16th rising clock edge including during burst write mode. If a software reset is enabled, the device will immediately reset after the 16th rising clock edge and will not respond to SPI communication until a new falling edge of the $\overline{CS}$ is observed. If a software reset is triggered during burst write, any data after the configuration register write will be ignored. The SIO buffer is tri-state during reset.

Each transaction with the TMP126-Q1 will consist of a command word, followed by the data block, and the optional CRC that is enabled in the command word.

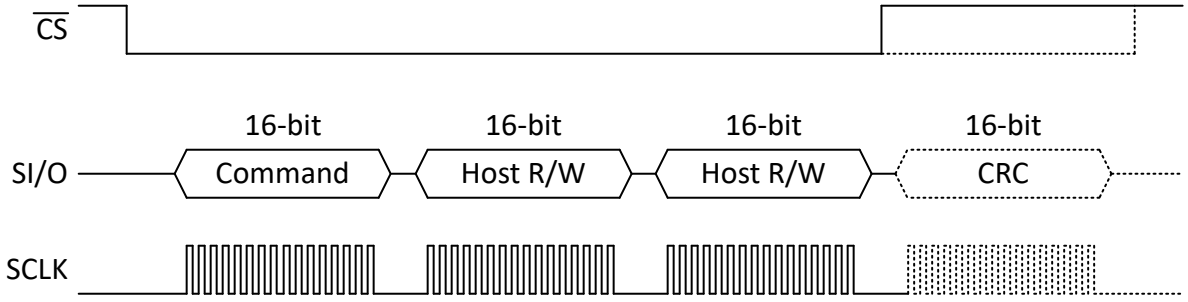

Figure 8-9. TMP126-Q1 Communication Overview

8.5.2.1 Command Word Structure

Figure 8-10 shows that the command word can be divided into 6 discrete sections detailed below.

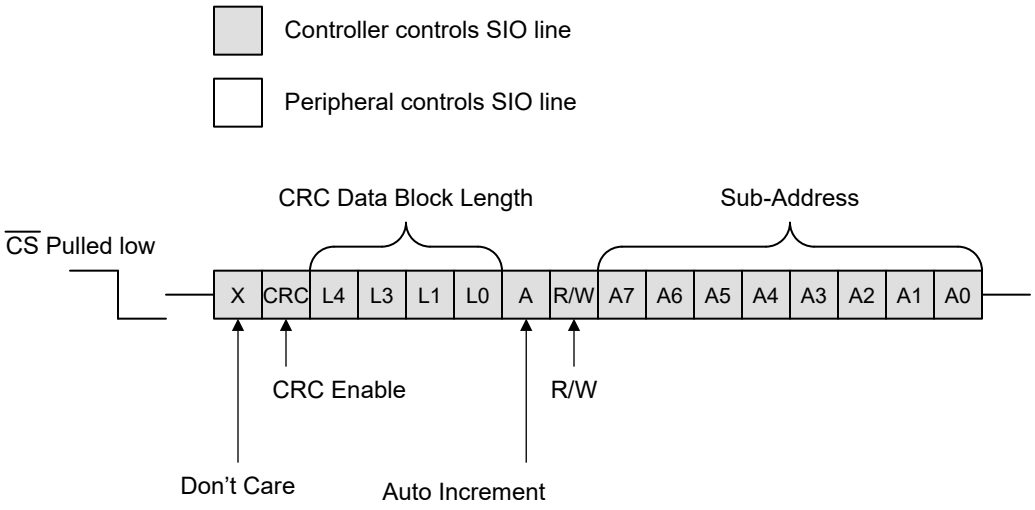

Figure 8-10. TMP126 Command Word

8.5.2.1.1 Don't Care

Bit15 of the command word is a don't care and the TMP126-Q1 will ignore this bit.

8.5.2.1.2 CRC Enable

Bit14 of the command word is the CRC enable bit. Setting this bit to 1b will enable the CRC checksum at the end of the communication as described in the CRC section.

8.5.2.1.3 CRC Data Block Length

Bits[13:10] of the command word is the CRC data block length. These bits are used to indicate how long the transaction will be when the CRC checksum is used. If this field is set to 0h or a value larger than Ah, the CRC enable will be ignored.

8.5.2.1.4 Auto Increment

Bit9 of the command word is the auto-increment bit.

Setting this bit to '1' will cause the address pointer of the TMP126-Q1 to increment by after every word of data on a read or write transaction. If the bit is set to '0', the address pointer is not incremented and reads/writes will continue to only apply the Sub-Address specified in the command word.

8.5.2.1.5 Read/Write

Bit8 of the command word is the read/write bit.

Setting this bit to '1' will issue a read command. During a read command the TMP126-Q1 will control the SI/O pin after the command word. Setting this bit to '0' will issue a write command. During a write command the controller will control the SI/O pin and the TMP126-Q1 will tri-state the SI/O pin.

8.5.2.1.6 Sub-Address

Bits[7:0] of the command word make up the register Sub-Address.

This is the register map address that will be used for reading or writing data depending on the read/write bit. Writes to Sub-Addresses outside the register map will be ignored. Reads from Sub-Addresses outside the register map will return all '0's.

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8.5.2.2 Communication

Communication is initiated by taking the $\overline{CS}$ pin low and clocking the SCLK pin. The first 16 bits of the communication are the command word for the TMP126-Q1. The following data will depend on the command byte. If a write command is issued, the TMP126-Q1 will store the data input during the next 16 bits into the appropriate Sub-Address set in the command byte. If the auto-increment bit is set to '1', the address pointer is incremented after every 16-bit word. This allows the system to program all the registers of the TMP126-Q1 in a single burst write command. If the auto-increment is set to '1' for a read command, after each 16-bit word the address pointer is incremented and the next word of data will be from the next Sub-Address.

The following sections denote example write and read operations with the TMP126-Q1.

8.5.2.3 Write Operations

Data is transmitted to the TMP126-Q1 by setting the R/W bit of the command word to logic '0'. Data can be continuously written to a single register by setting the auto-increment bit to '0' in the command register. Figure 8-11 shows an example of a repeated data write to a single register.

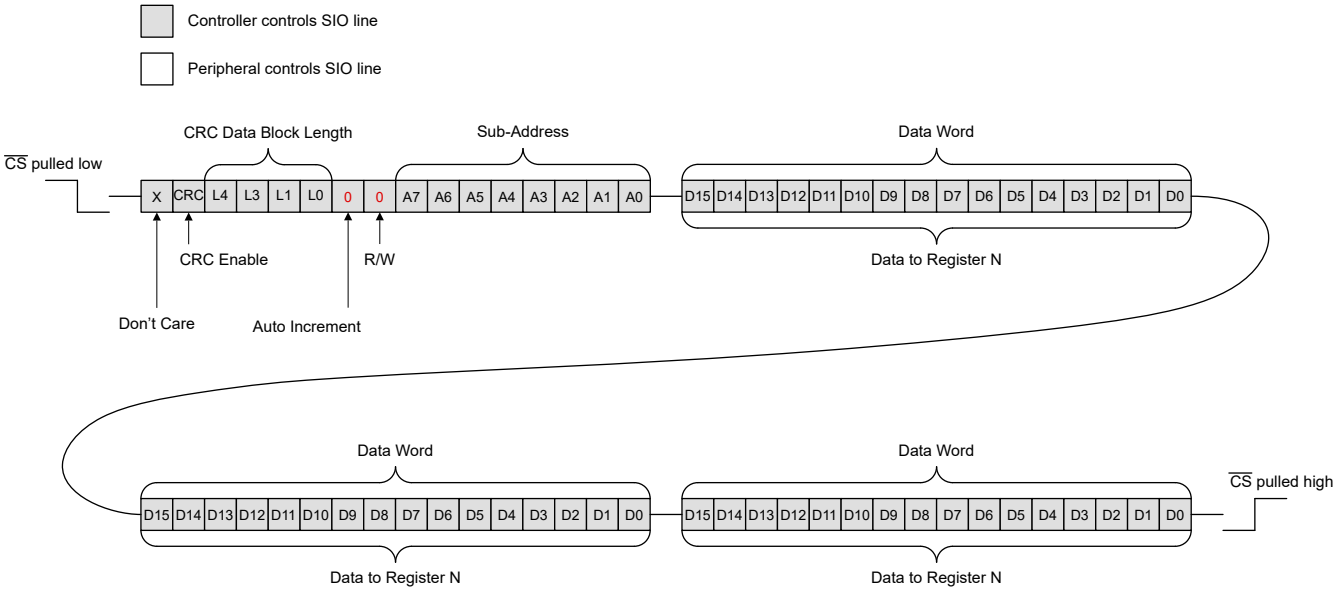

Figure 8-11. Repeated Data Write to a Single Register

Figure 8-12 shows how setting the auto increment to logic '1' to can enable a write from multiple registers in a single transaction.

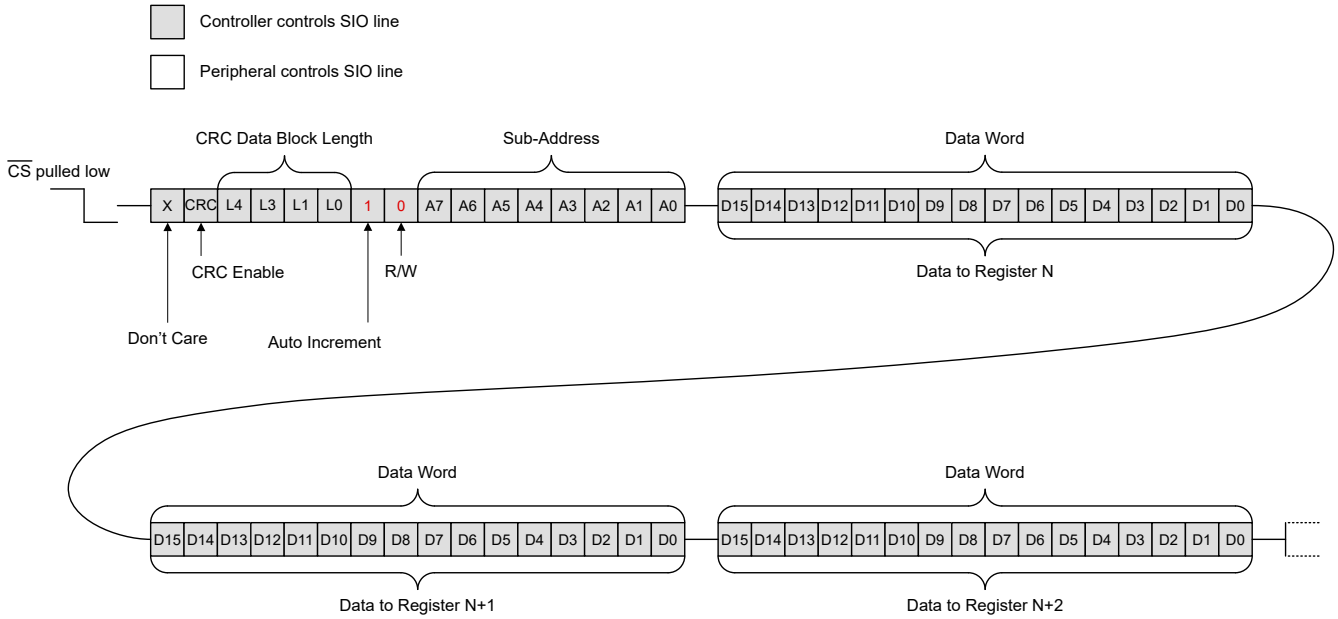

Figure 8-12. Burst Data Write to Multiple Registers

Configuration register changes will not be accepted when using auto increment writes. For configuration register changes it is recommended to use a single register write without auto increment.

8.5.2.4 Read Operations

Data is read from the TMP126-Q1 by setting the R/W bit of the command word to logic '1'. Data can be continuously read from a single register by setting the auto-increment bit to '0' in the command register. Figure 8-13 shows an example of a repeated data read from a single register. Repeated temperature reads are not supported.

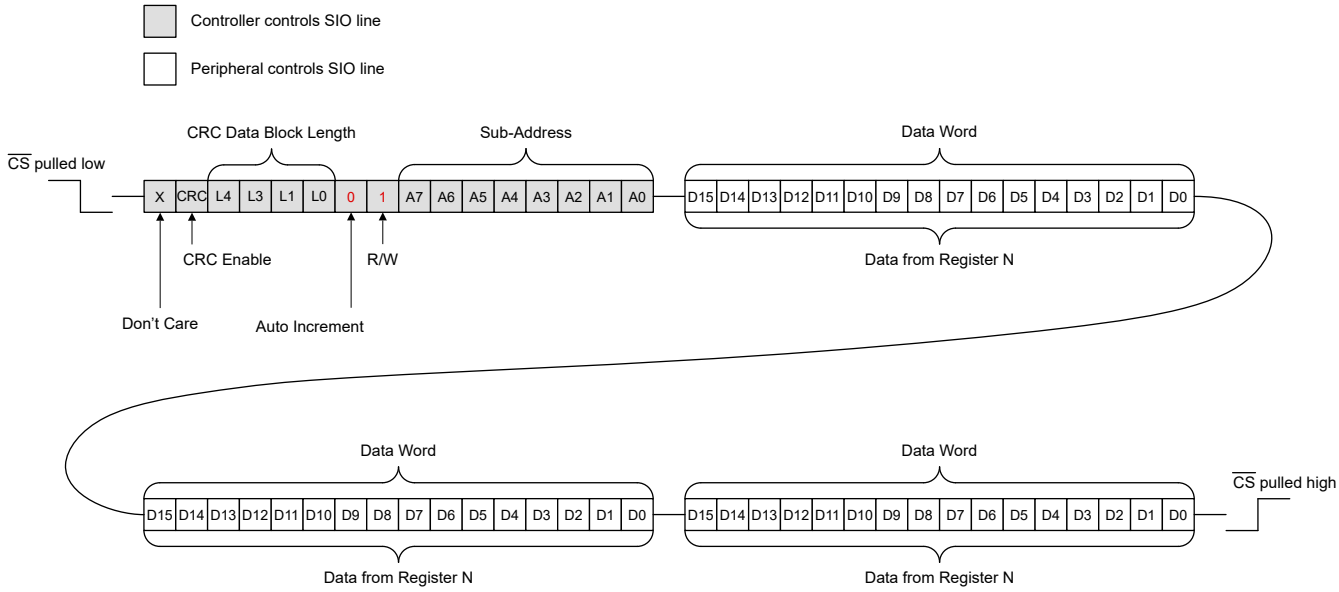

Figure 8-13. Repeated Data Read from a Single Register

Figure 8-14 shows how setting the auto increment to logic '1' to can enable a read from multiple registers in a single transaction. The status register of the TMP126-Q1 will not be cleared in burst data read mode. To clear status register contents, TI recommends to use single register reads without auto increment.

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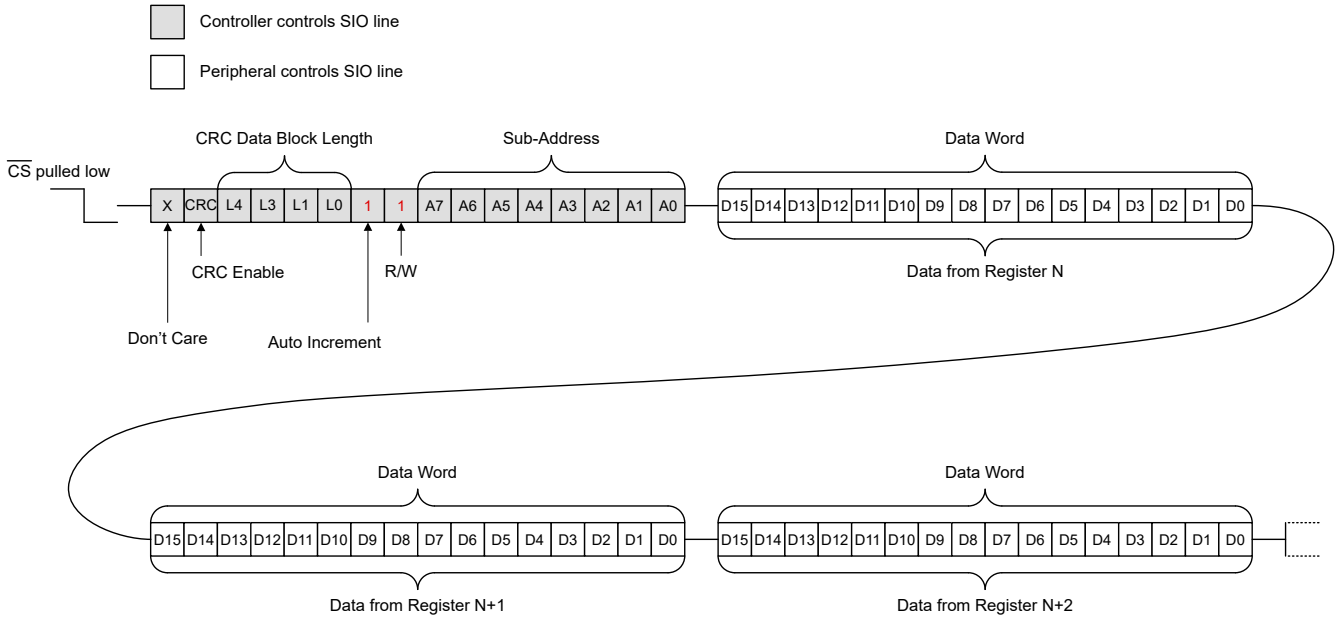

Figure 8-14. Burst Data Read from Multiple Registers

8.5.2.5 Cyclic Redundancy Check (CRC)

The TMP126-Q1 has an optional CRC feature to determine the integrity of the data that has been transmitted across the SPI communication interface. The CRC for the TMP126-Q1 is enabled by setting the CRC bit in the command word to 1b. When enabled, the TMP126-Q1 will append a 16 bit CRC checksum to the end the data block for read transactions. The controller can then compare this checksum to their own calculation and determine if the transaction was valid. During a write transaction, the host will append the 16-bit CRC checksum. The TMP126-Q1 will compare this to its own checksum. If there is a mismatch, the TMP126 will discard the write transaction and set a CRC fault ALERT to indicate to the host that the transaction failed. The host will need to send the register settings again to correctly program the TMP126-Q1. Reading the Alert_Status register will clear the CRC_Fault bit and de-assert the ALERT pin.

An overview of a CRC enabled write transaction is shown below with a data block length of 2.

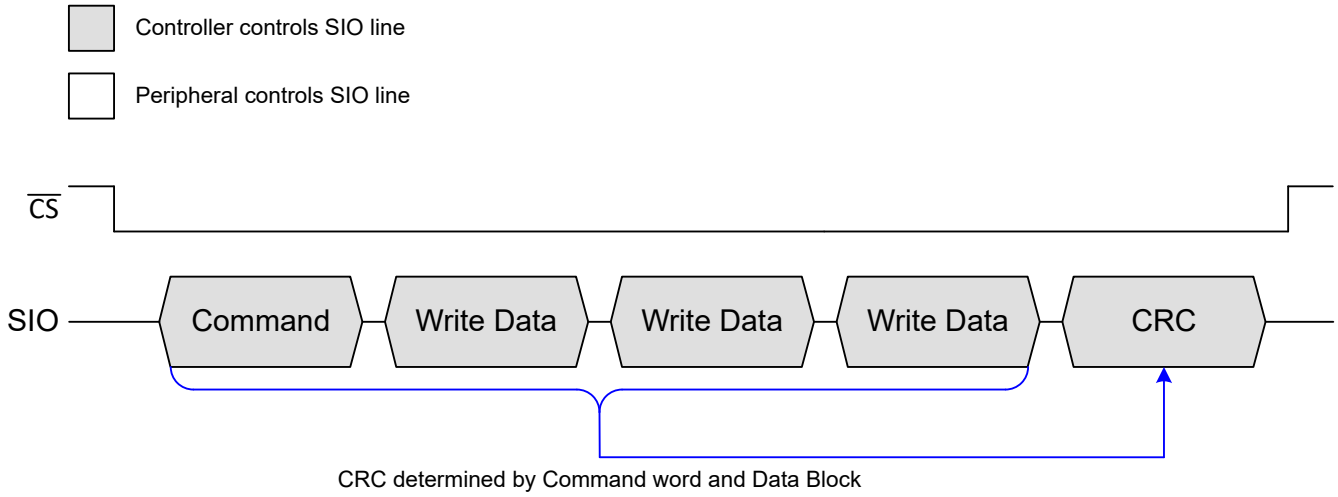

Figure 8-15. CRC Enabled Write

An overview of a CRC enabled read transaction is shown below with a data block length of 2.

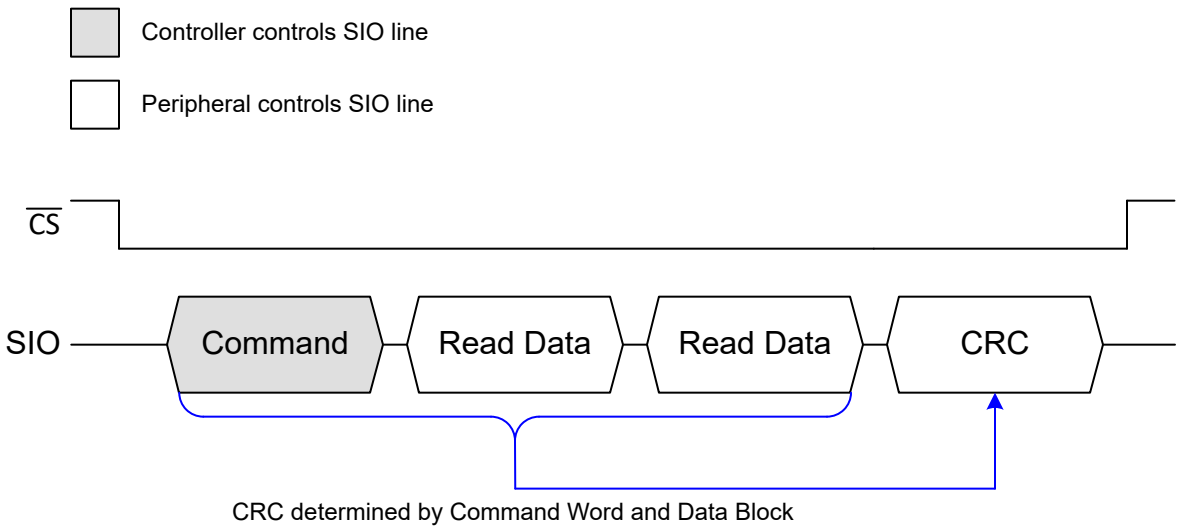

Figure 8-16. CRC Enabled Read

8.5.2.5.1 Cyclic Redundancy Check Implementation

Table 8-2 defines the CRC calculation rule.

Table 8-2. CRC Rule Table

Temperature	Digital Output
CRC Width	16 bits
Polynomial	$X^{16} + X^{12} + X^5 + 1$ (1021h)
Initial seed value	FFFFh
Input data reflected	No
Result data reflected	No
XOR value	0000h

Figure 8-17 shows the CRC Module block diagram. The CRC calculation is done on the command word and the data block. The module consists of a 16-bit shift register and 3 exclusive-OR gates. The register starts with the seed value FFFFh and the module performs an XOR function and shifts its content until the last bit of the register string is used. The final value of the shift register checksum is output onto the SIO line by the TMP126-Q1at the end of the data block for the host to validate the transaction.

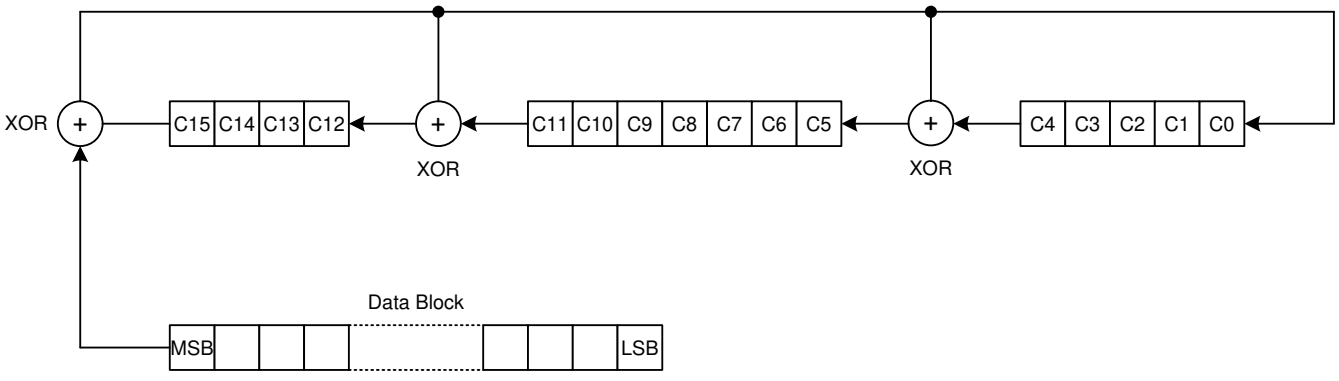

Figure 8-17. CRC Module

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8.6 Register Map

Table 8-3. TMP126-Q1 Registers

ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
00h	R	0000h	Temp_Result	Temperature result register	Go
01h	R	0000h	Slew_Result	Slew rate result register	Go
02h	R/RC	0000h	Alert_Status	Alert status register	Go
03h	R/W	0006h	Configuration	Configuration register	Go
04h	R/W	0016h	Alert_Enable	Alert enable register	Go
05h	R/W	F380h	TLow_Limit	Temperature low limit register	Go
06h	R/W	2A80h	THigh_Limit	Temperature high limit register	Go
07h	R/W	0A0Ah	Hysteresis	Hysteresis register	Go
08h	R/W	0500h	Slew_Limit	Temperature slew rate limit register	Go
09h	R	xxxxh	Unique_ID1	Unique_ID1 register	Go
0Ah	R	xxxxh	Unique_ID2	Unique_ID2 register	Go
0Bh	R	xxxxh	Unique_ID3	Unique_ID3 register	Go
0Ch	R	1126h	Device_ID	Device ID register	Go
10h-2Ah	R	xxxxh	Reserved	Reserved	

Table 8-4. TMP126-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

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8.6.1 Temp_Result Register (Address = 00h) [reset = 0000h]

This register stores the latest temperature conversion result in a 14-bit two's complement format with a LSB (Least Significant Bit) equal to 0.03125 °C.

Return to Register Map.

Figure 8-18. Temp_Result Register

15	14	13	12	11	10	9	8
Temp_Result[13:6]							
R-00h							
7	6	5	4	3	2	1	0
Temp_Result[5:0]						**Reserved**	
R-00h						R-0h	

Table 8-5. Temp_Result Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	Temp_Result[13:0]	R	0000h	14-bit temperature conversion result. Temperature data is represented by a 14-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.03125 °C.
1:0	Reserved	R	0h	These two bits will always read 0h

8.6.2 Slew_Result Register (Address = 01h) [reset = 0000h]

This register shows the latest slew rate calculation. Two consecutive measurements in continuous conversion mode are required before a result is shown. When not in continuous conversion mode the register will return to the default value.

The slew rate result is depicted in 14-bit twos-complement format with the LSB equal to 0.03125 °C/s. The TMP126 does not accurately report negative slew rate values and bit 13 of the output result can be used to indicate a negative slew rate but the output value cannot be guaranteed.

Return to Register Map.

Figure 8-19. Slew_Result Register

15	14	13	12	11	10	9	8
Slew_Rate_Result[13:6]							
R-00h							
7	6	5	4	3	2	1	0
Slew_Rate_Result[5:0]						**Reserved**	
R-00h						R-0h	

Table 8-6. Slew_Result Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	Slew_Rate_Result[13:0]	R	0000h	Temperature slew rate result. Temperature slew rate is represented by a 14-bit, twos-complement word with an LSB (Least Significant Bit) equal to 0.03125 °C/s. Format is °C/s.
1:0	Reserved	R	0h	Reserved

8.6.3 Alert_Status Register(Address = 02h) [reset = 0000h]

This register show the current alert status of the TMP126-Q1. This register will currently only clear with a single register read without auto increment.

Return to Register Map.

Figure 8-20. Alert_Status Register

15	14	13	12	11	10	9	8
Reserved							
R-00h							
7	6	5	4	3	2	1	0
CRC_Flag	Slew_Status	Slew_Flag	THigh_Status	TLow_Status	THigh_Flag	TLow_Flag	Data_Ready_Flag
RC-0h	R-0h	RC-0h	R-0h	R-0h	RC-0h	RC-0h	RC-0h

Table 8-7. Alert_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R	00h	Reserved
7	CRC_Flag	RC	0h	CRC checksum error flag indicator. This indicates that the write transaction CRC checksum failed and the register settings were discarded. 0h = The most recent CRC enabled write transaction was successful. 1h = The most recent CRC enabled write transaction failed.
6	Slew_Pos_Status	R	0h	Positive slew rate status indicator. This bit is set if there is a positive slew rate exceeding the Slew_Rate_Limit. 0h: The most recent temperature conversion result is below the Slew_Rate_Limit. 1h: The most recent temperature conversion result is above the Slew_Rate_Limit.
5	Slew_Flag	RC	0h	Slew rate flag indicator. This indicates that the current there was a temperature slew rate beyond the slew rate limit threshold. Reading Alert_Status register will clear this bit. 0h = The most recent temperature conversion has not crossed the Slew_Rate_Limit threshold. 1h = A temperature conversion has crossed the Slew_Rate_Limit threshold.
4	THigh_Status	R	0h	High temperature status indicator. 0h: The most recent temperature conversion result is below the Thigh_Limit 1h: The most recent temperature conversion is above the THigh_Limit. Once set, this bit will not clear until a temperature conversion is below THigh_Limit - THigh_Hyst
3	TLow_Status	R	0h	Low temperature status indicator. 0h: The most recent temperature conversion result is above the TLow_Limit 1h: The most recent temperature conversion is below the THigh_Limit. Once set, this bit will not clear until a temperature conversion is above TLow_Limit + TLow_Hyst

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Table 8-7. Alert_Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	THigh_Flag	RC	0h	High temperature flag indicator. This indicates that the latest temperature conversion has cross above the THigh_Limit register threshold or crossed below the THigh_Limit - THigh_Hyst threshold. Reading Alert_Status register will clear this bit. 0h = The most recent temperature conversion has not crossed the THigh_Limit or the hysteresis threshold. 1h: A temperature conversion crossed the THigh_Limit or crossed below the THigh_Limit - THigh_Hyst threshold. Once the THigh_Flag is set, THigh_Flag will not be set again until a temperature conversion is below THigh_Limit - THigh_Hyst
1	TLow_Flag	RC	0h	Low temperature flag indicator. This indicates that the latest temperature conversion has cross below the TLow_Limit register threshold or crossed above the Tlow_Limit + TLow_Hyst threshold. Reading Alert_Status register will clear this bit. 0h = The most recent temperature conversion has not crossed the TLow_Limit or the hysteresis threshold. 1h: A temperature conversion crossed below the TLow_Limit. Once the TLow_Flag is set, TLow_Flag will not be set again until temperature conversion is above TLow_Limit + TLow_Hyst
0	Data_Ready_Flag	RC	0h	Data Ready flag indicator. This indicates that there is an unread temperature conversion. Reading Alert_Status register or the Temperature Results register will clear this bit. 0h = Data in Temp_Result has been read already 1h = Data in Temp_Result is unread

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8.6.4 Configuration Register (Address = 03h) [reset = 0006h]

This register is used to configuration the operation of the TMP126-Q1.

Return to Register Map.

Figure 8-21. Configuration Register

15	14	13	12	11	10	9	8
Reserved							Reset
R-00h							R/W-0h
7	6	5	4	3	2	1	0
AVG	**Reserved**	Int_Comp	One_Shot	Mode	Conv_Period[2:0]		
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-6h		

Table 8-8. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R	00h	Reserved
8	Reset	R/W	0h	Software reset bit. When set to 1 it triggers software reset with a duration of X ms. This bit will always read back 0
7	AVG	R/W	0h	Averaging enable bit. Averaging will force every measurement including one-shot measurements to be averaged with eight conversions. 0h: Averaging is disabled 1h: Averaging is enabled
6	Reserved	R	0h	Reserved
5	Int_Comp	R/W	0h	Interrupt or comparator mode select 0h = Interrupt mode 1h = Comparator mode
4	One_Shot	R/W	0h	One-shot conversion trigger. Triggering a one-shot conversion will place the TMP126-Q1 into shutdown mode after the conversion completes. This bit will always read 0h. 0h = Default 1h = Trigger a one-shot conversion
3	Mode	R/W	0h	Conversion mode selection bit. 0h = Continuous conversion mode 1h = Shutdown mode
2:0	Conv_Period[2:0]	R/W	6h	Conversion period setting. This bit field changes the conversion period of the TMP126-Q1. 0h = 5.5 ms 1h = 31.25 ms / 32 Hz 2h = 62.5 ms / 16 Hz 3h = 125 ms / 8 Hz 4h = 250 ms / 4 Hz 5h = 500 ms / 2 Hz 6h = 1 s / 1 Hz 7h = 2 s / 0.5 Hz

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8.6.5 Alert_Enable Register(Address = 04h) [reset = 0016h]

This register configures which flags of the Alert_Status register are enabled or disabled. Disabling an Alert flag will cause the $\overline{\text{ALERT}}$ pin to not assert when that flag bit is set. If the flag is enabled the $\overline{\text{ALERT}}$ pin will assert when that flag is set. The flag bit will still be set in the register when the Alert functionality is disabled for that bit.

Currently if there is an active alert on the $\overline{\text{ALERT}}$ pin and the enable for that alert is set to 0h, the TMP126-Q1 will not the de-assert the pin until the status register is read or a new conversion occurs.

Return to Register Map.

Figure 8-22. Alert_Enable Register

15	14	13	12	11	10	9	8
Reserved							
R-00h							
7	6	5	4	3	2	1	0
Reserved			CRC_Alert_En	Slew_Alert_En	THigh_Alert_En	TLow_Alert_En	Data_Ready_Alert_En
R-0h			R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-0h

Table 8-9. Alert_Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	Reserved	R	000h	Reserved
4	CRC_Alert_En	R/W	1h	Enables the CRC_Flag alert to assert the $\overline{\text{ALERT}}$ pin. 0h = CRC_Flag $\overline{\text{ALERT}}$ disabled 1h = CRC_Flag $\overline{\text{ALERT}}$ enabled
3	Slew_Alert_En	R/W	0h	Enables the Slew_Flag assert the $\overline{\text{ALERT}}$ pin while in interrupt mode. When in comparator mode, enables the Slew_Status to assert the $\overline{\text{ALERT}}$. 0h = Slew_Flag $\overline{\text{ALERT}}$ disabled 1h = Slew_Flag $\overline{\text{ALERT}}$ enabled
2	THigh_Alert_En	R/W	1h	Enables the THigh_Flag assert the $\overline{\text{ALERT}}$ pin while in interrupt mode. When in comparator mode, enables the THigh_Status to assert the $\overline{\text{ALERT}}$. 0h = THigh_Flag Alert disabled 1h = THigh_Flag Alert enabled
1	TLow_Alert_En	R/W	1h	Enables the TLow_Flag assert the $\overline{\text{ALERT}}$ pin while in interrupt mode. When in comparator mode, enables the TLow_Status to assert the $\overline{\text{ALERT}}$. 0h = TLow_Flag Alert disabled 1h = TLow_Flag Alert enabled
0	Data_Ready_Alert_En	R/W	0h	Enables the Data_Ready_Flag to assert the $\overline{\text{ALERT}}$ pin. 0h = Data_Ready Alert disabled 1h = Data_Ready Alert enabled

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8.6.6 TLow_Limit Register(Address = 05h) [reset = F380h]

This register is used to configuration the low temperature limit of the TMP126-Q1. The limit is formatted in a 14-bit two's complement format with a LSB (Least Significant Bit) equal to 0.03125 °C. This is the same format as the TEMP_RESULT register. The range of the register is ±256 °C. The default value on startup is F380h or -25 °C. If the THigh_Limit register is equal to or less than the TLow_Limit register the temperature limits will be ignored until configured such that THigh_Limit is greater than TLow_Limit.

Return to Register Map.

Figure 8-23. TLow_Limit Register

15	14	13	12	11	10	9	8
TLow_Limit[13:6]							
R/W-F3h							
7	6	5	4	3	2	1	0
TLow_Limit[5:0]						**Reserved**	
R/W-20h						R-0h	

Table 8-10. TLow_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	TLow_Limit[13:0]	R/W	3CE0h	14-bit temperature low limit setting. Temperature low limit is represented by a 14-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.03125°C. The default setting for this is -25°C.
1:0	Reserved	R	0h	These two bits will always read 0h

8.6.7 THigh_Limit Register(Address = 06h) [reset = 2A80h]

This register is used to configuration the high temperature limit of the TMP126-Q1. The limit is formatted in a 14-bit two's complement format with a LSB (Least Significant Bit) equal to 0.03125 °C. This is the same format as the Temp_Result register. The range of the register is ±256 °C. The default value on startup is 2A80h or 85 °C. If the THigh_Limit register is equal to or less than the TLow_Limit register the temperature limits will be ignored until configured such that THigh_Limit is greater than TLow_Limit.

Return to Register Map.

Figure 8-24. THigh_Limit Register

15	14	13	12	11	10	9	8
THigh_Limit[13:6]							
R/W-2Ah							
7	6	5	4	3	2	1	0
THigh_Limit[5:0]						**Reserved**	
R/W-20h						R-0h	

Table 8-11. THigh_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	THigh_Limit[13:0]	R/W	0AA0h	14-bit temperature high limit setting. Temperature high limit is represented by a 14-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.03125°C.
1:0	Reserved	R	0h	These two bits will always read 0h

8.6.8 Hysteresis Register (Address = 07h) [reset = 0A0Ah]

This register sets the hysteresis for the THigh_Limit threshold and the TLow_Limit threshold. The default hysteresis value for both the high and low limits is equal to 5 °C.

The Hystersis is in a 8-bit unsigned format with the LSB equal to 0.5 °C. This gives a maximum value of 127.5 °C of hysteresis.

Return to Register Map.

Figure 8-25. Hysteresis Register

15	14	13	12	11	10	9	8
THigh_Hyst[7:0]							
R/W-0Ah							
7	6	5	4	3	2	1	0
TLow_Hyst[7:0]							
R/W-0Ah							

Table 8-12. Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	THigh_Hyst[7:0]	R/W	0Ah	THigh_Limit Hysteresis setting. Hysteresis value is represented by a unsigned Byte with the LSB equal to 0.5 °C. The High temperature limit hysteresis threshold is equal to (THigh_Limit - THigh_Hyst). The default hysteresis value is 5 °C.
7:0	TLow_Hyst[7:0]	R/W	0Ah	TLow_Limit Hysteresis setting. Hysteresis value is represented by a unsigned Byte with the LSB equal to 0.5 °C. The Low temperature limit hysteresis threshold is equal to (TLow_Limit + TLow_Hyst). The default hysteresis value is 5 °C.

ADVANCE INFORMATION

8.6.9 Slew_Limit Register (Address = 08h) [reset = 0500h]

This register is used to configure the temperature slew rate limit of the TMP126-Q1. The limit is formatted in a 13-bit unsigned format with the LSB (Least Significant Bit) equal to 0.03125 °C/s. The range of the register is 0 °C to +256 °C. The default value on startup is 0140h or 10 °C/s. The slew rate limit will trigger a slew rate alert on positive slew rates that are greater than the unsigned limit as enabled by the Alert_Enable register.

Return to Register Map.

Figure 8-26. Slew_Limit Register

15	14	13	12	11	10	9	8
Reserved	Slew_Rate_Limit[12:6]						
R-0h	R/W-05h						
7	6	5	4	3	2	1	0
Slew_Rate_Limit[5:0]						**Reserved**	
R/W-00h						R-0h	

Table 8-13. Slew_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved
14:2	Slew_Rate_Limit[12:0]	R/W	0140h	13-bit temperature slew rate limit setting. Temperature low limit is represented by a 13-bit unsigned word with a LSB (Least Significant Bit) equal to 0.03125 °C/s. The default setting for this is 10 °C/s.
1:0	Reserved	R	0h	Reserved

8.6.10 Unique_ID1 register (Address = 09h) [reset = xxxxh]

This register contains bits 47:32 of the Unique ID for the device. The Unique ID of the device is used for NIST traceability purposes.

Return to Register Map.

Figure 8-27. Unique_ID1 Register

15	14	13	12	11	10	9	8
Unique_ID[47:40]							
R-xxh							
7	6	5	4	3	2	1	0
Unique_ID[39:32]							
R-xxh							

Table 8-14. Unique_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Unique_ID[47:32]	R	xxxxh	Bits 47:32 of the device Unique ID

ADVANCE INFORMATION

8.6.11 Unique_ID2 register (Address = 0Ah) [reset = xxxxh]

This register contains bits 31:16 of the Unique ID for the device.

Return to Register Map.

Figure 8-28. Unique_ID2 Register

15	14	13	12	11	10	9	8
Unique_ID[31:24]							
R-xxh							
7	6	5	4	3	2	1	0
Unique_ID[23:16]							
R-xxh							

Table 8-15. Unique_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Unique_ID[31:16]	R	xxxxh	Bits 31:16 of the device Unique ID

8.6.12 Unique_ID3 register (Address = 0Bh) [reset = xxxxh]

This register contains bits 15:0 of the Unique ID for the device.

Return to Register Map.

Figure 8-29. Unique_ID3 Register

15	14	13	12	11	10	9	8
Unique_ID[15:8]							
R-xxh							
7	6	5	4	3	2	1	0
Unique_ID[7:0]							
R-xxh							

Table 8-16. Unique_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Unique_ID[15:0]	R	xxxxh	Bits 15:0 of the device Unique ID.

8.6.13 Device_ID register (Address = 0Ch) [reset = 0126h]

This register indicates the device ID and device revision.

Return to Register Map.

Figure 8-30. Device_ID Register

15	14	13	12	11	10	9	8
Rev[3:0]				ID[11:8]			
R-1h				R-1h			
7	6	5	4	3	2	1	0
ID[7:0]							
R-26h							

Table 8-17. Device_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	Rev[3:0]	R	1h	Device revision indicator.
11:0	ID[11:0]	R	126h	Device ID indicator.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMP126-Q1 can be operated with a 4-wire SPI bus in a 3-wire bus configuration with the use of a isolation resistor for a typical application. The wide supply and temperature range support of the TMP126-Q1 allow the device to support a wide variety of use cases. The integrated optional CRC ensures data integrity during communication and the slew rate alert allows the device to autonomously monitor for rapid temperature changes.

9.2 Typical Application

The TMP126-Q1 features a 3-wire SPI interface that can easily be connected to a 4-wire SPI MCU with the use of a isolation resistor.

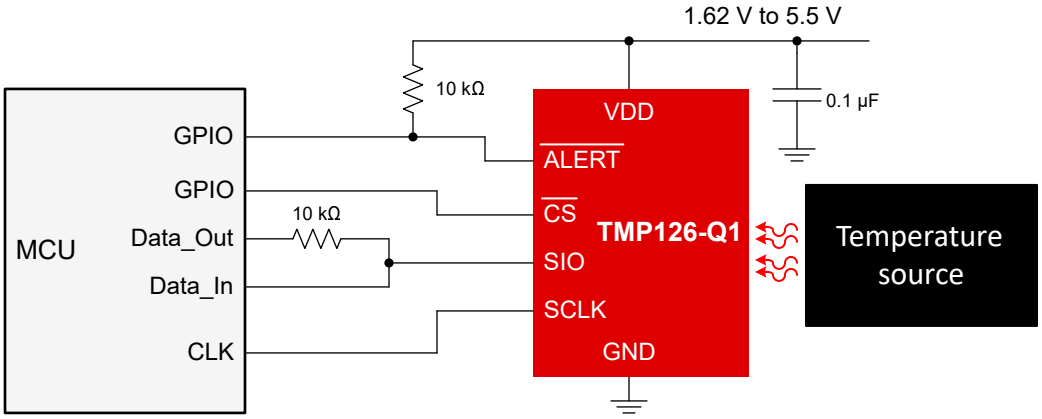

Figure 9-1. TMP126-Q1 Typical Connections

9.2.1 Design Requirements

For this design example, use the parameters listed below.

PARAMETER	Value
Supply (V_{DD})	1.62 V to 5.5 V
Isolation Resistor	10 kΩ

9.2.2 Detailed Design Procedure

The TMP126-Q1 will convert temperature at a default 1 s interval with an adjustable conversion period between 5.5 ms and 2 s. Reading faster than the conversion period will not disrupt device operation and can safely be done if desired.

The TMP126-Q1 should be placed as close to the temperature source as possible with a proper layout for thermal coupling. Placing the device as close as possible ensures that temperature changes are captured in the shortest possible time interval.

ADVANCE INFORMATION

ADVANCE INFORMATION

10 Power Supply Recommendations

The operates from a single supply VDD. This pin operates with a wide range of 1.62 V to 5.5 V and maintains accuracy across the entire supply range. A de-coupling capacitor of 0.1 µF is recommended for the VDD pin. Place the capacitor as close to the pin as possible.

11 Layout

11.1 Layout Guidelines

Place the power-supply de-coupling capacitor as close as possible to the supply and ground pins. The recommended value of this de-coupling capacitor is 0.1 µF. Separation between the SCLK trace and the SI/O traces is recommended to reduce coupling of the clock onto the data line.

11.2 Layout Example

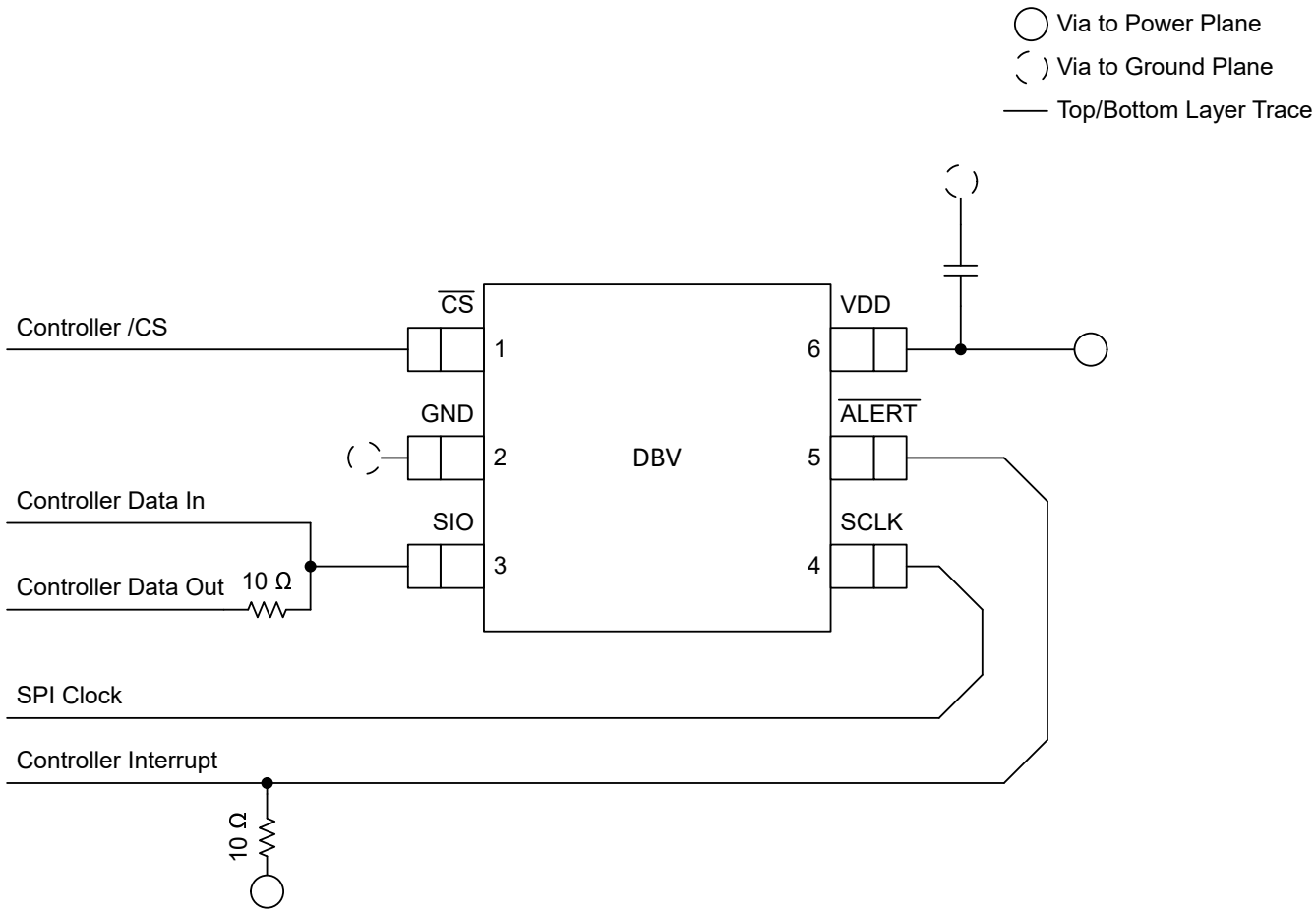

Figure 11-1. DBV Package Layout Example

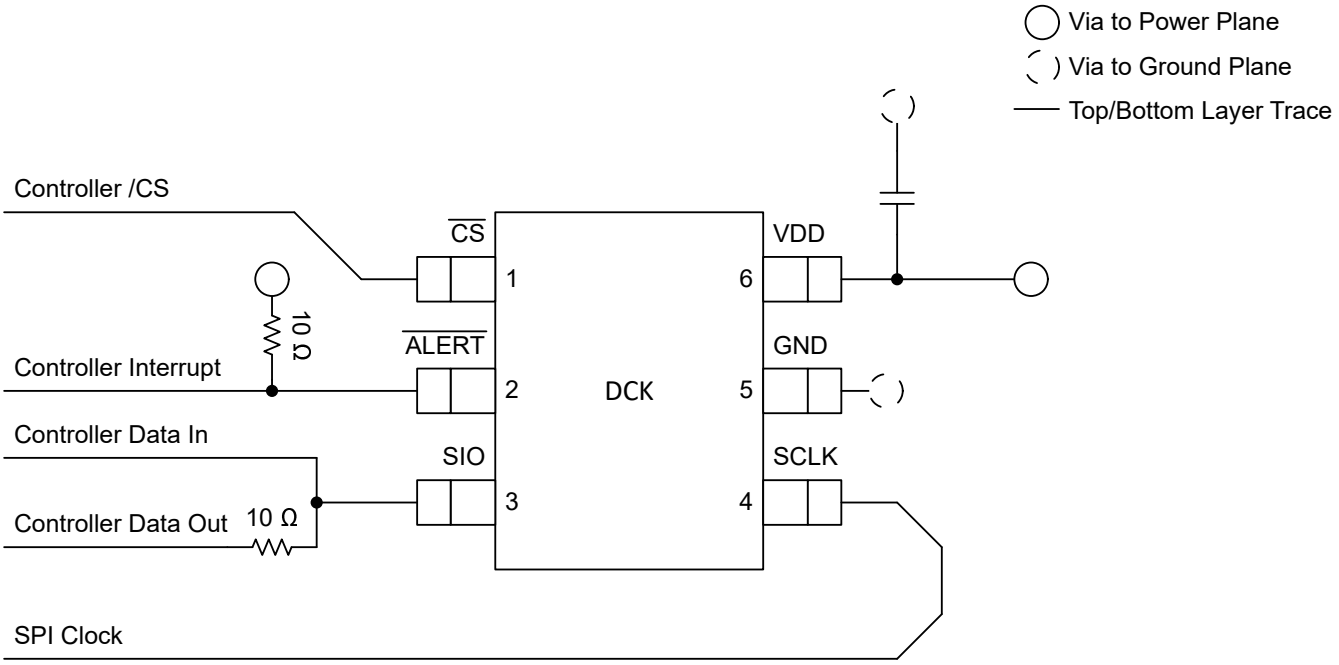

Figure 11-2. DCK Package Layout Example

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following: Texas Instruments, *TMP126EVM User's Guide* (SNIU049)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

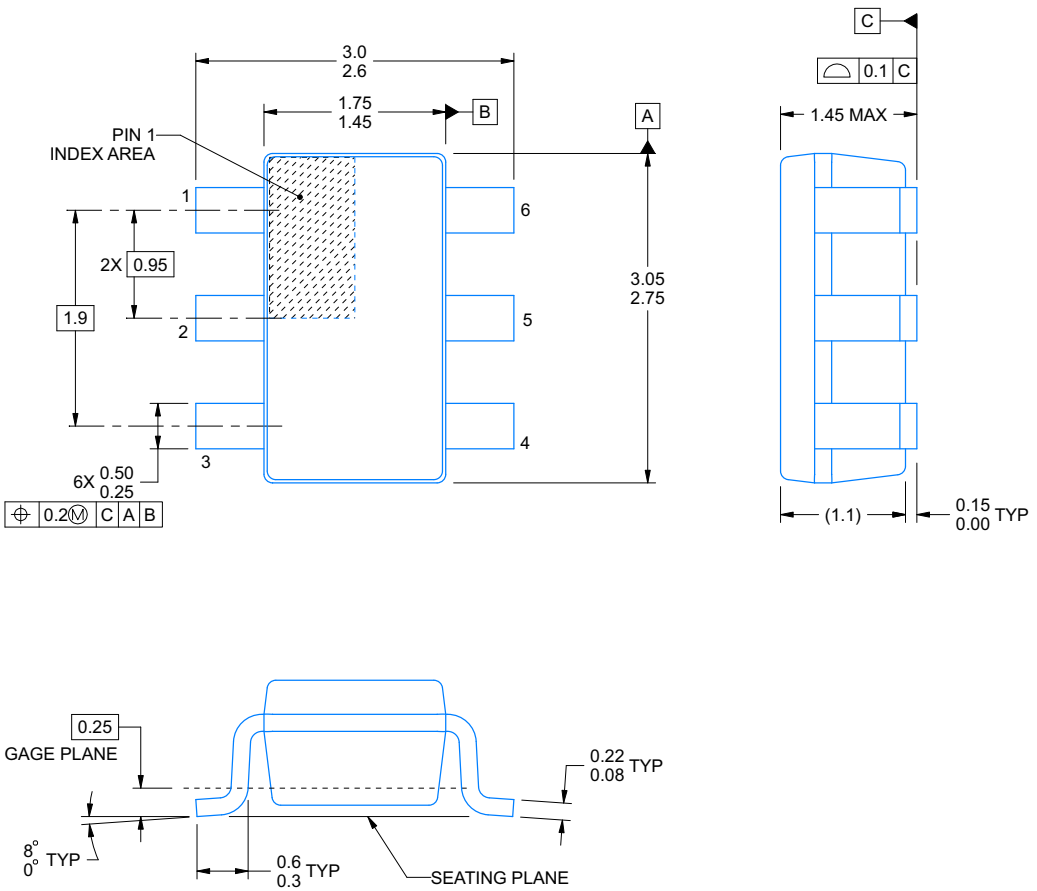
ADVANCE INFORMATION

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

ADVANCE INFORMATION

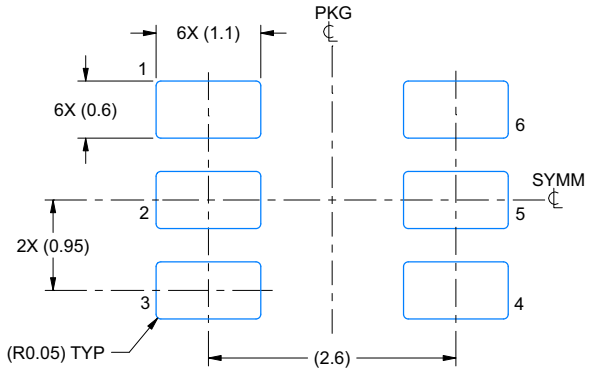
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

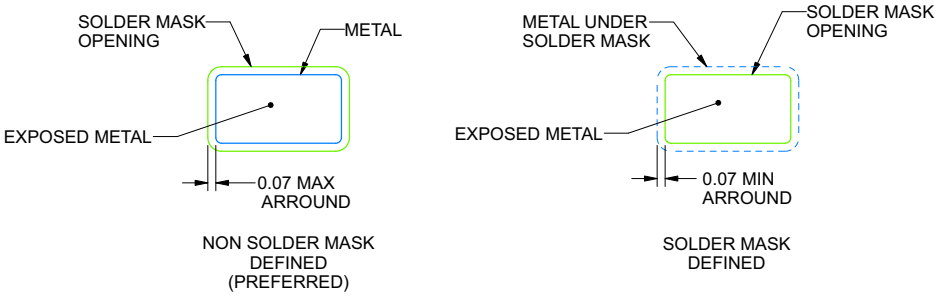
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

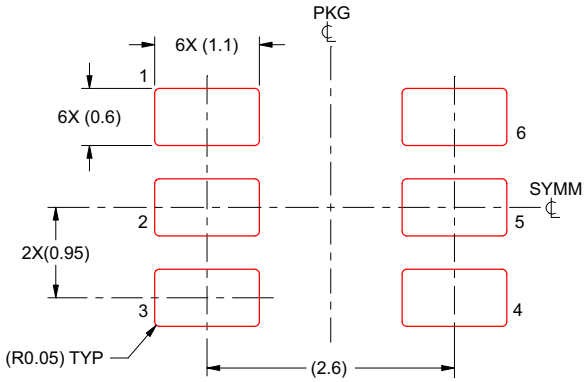
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

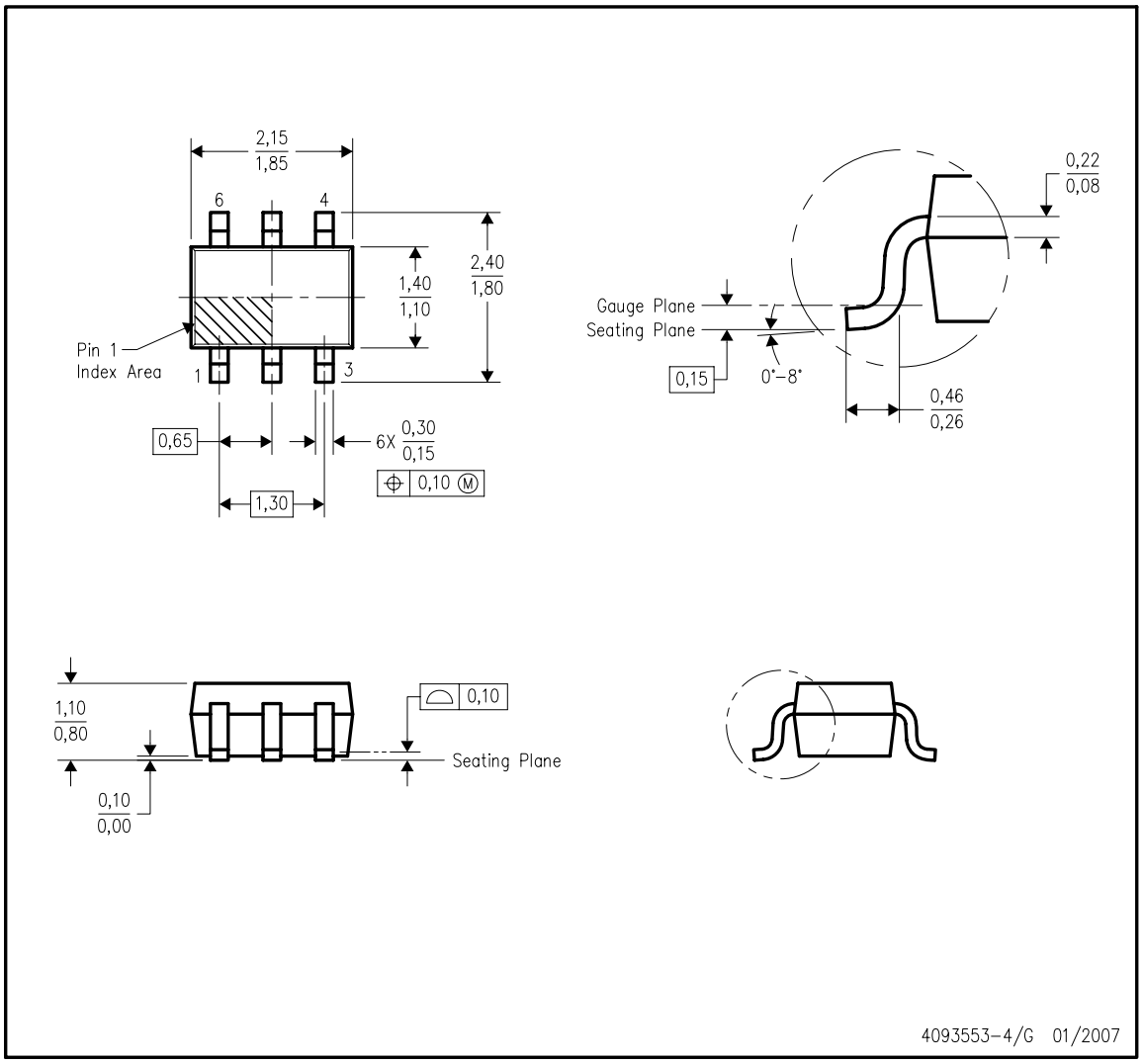
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

MECHANICAL DATA

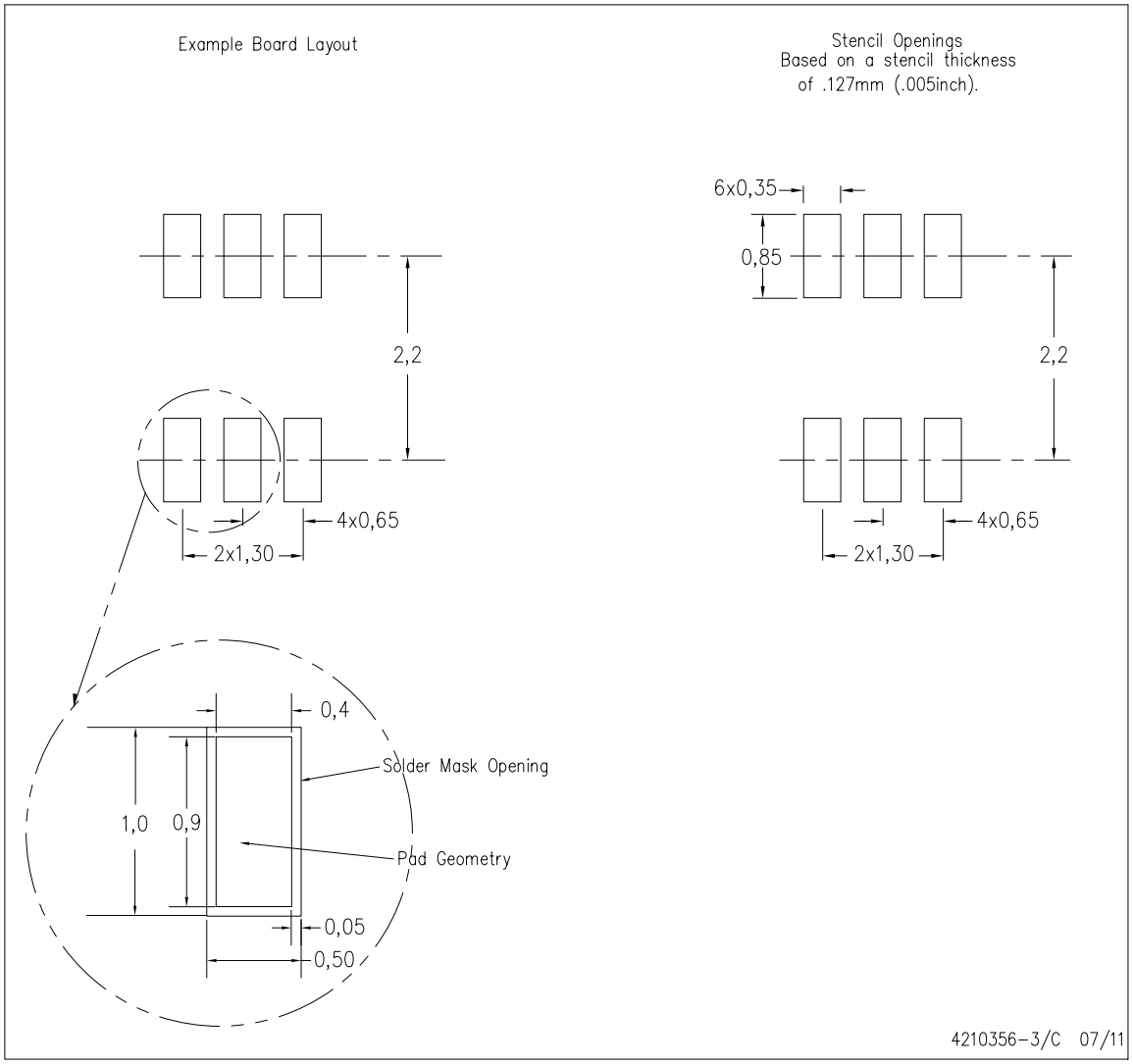
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

LAND PATTERN DATA

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE

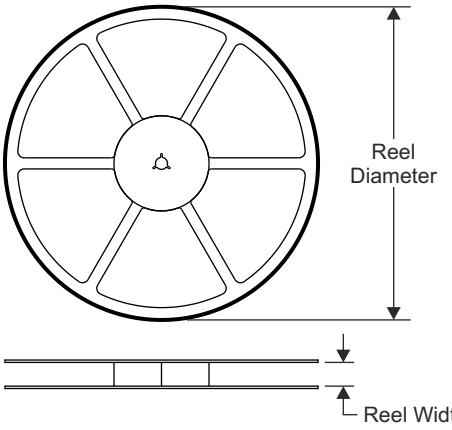


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

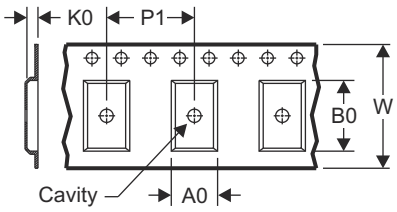
ADVANCE INFORMATION

13.1 Tape and Reel Information

REEL DIMENSIONS

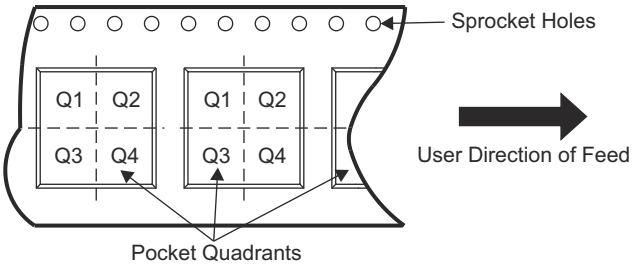


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

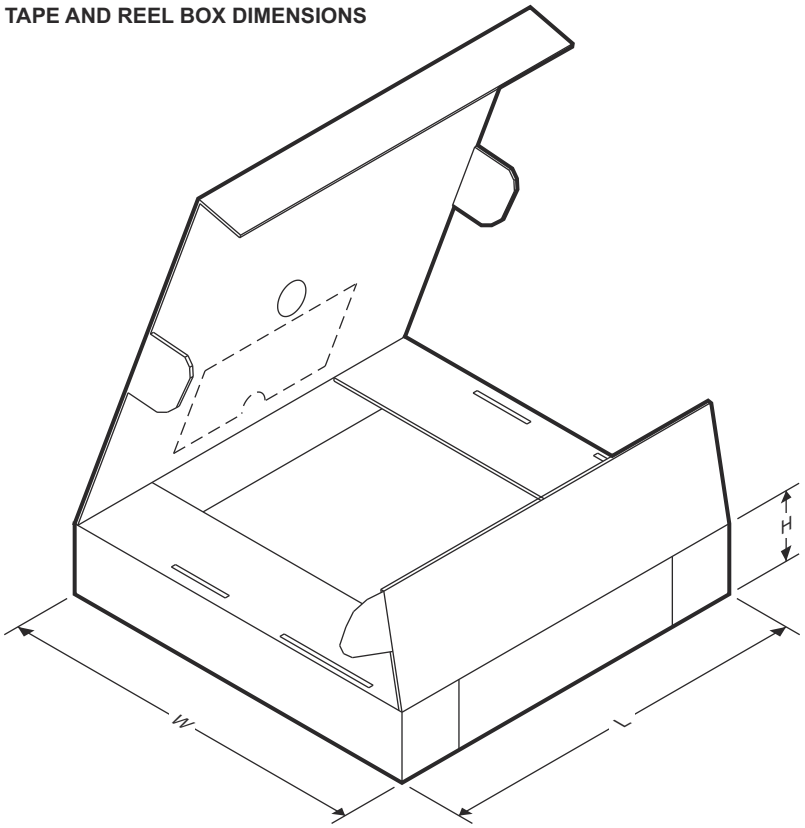
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTMP126EDBVTQ1	SOT-23	DBV	6	250	178.00	9.00	3.3	3.2	1.4	4	8	Q3

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTMP126EDBVTQ1	SOT-23	DBV	6	250	190	190	30

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMP126EDBVTQ1	ACTIVE	SOT-23	DBV	6	250	Non-RoHS & Non-Green	Call TI	Call TI	-55 to 175		Samples
PTMP126EDCKTQ1	ACTIVE	SC70	DCK	6	250	Non-RoHS & Non-Green	Call TI	Call TI	-55 to 175		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

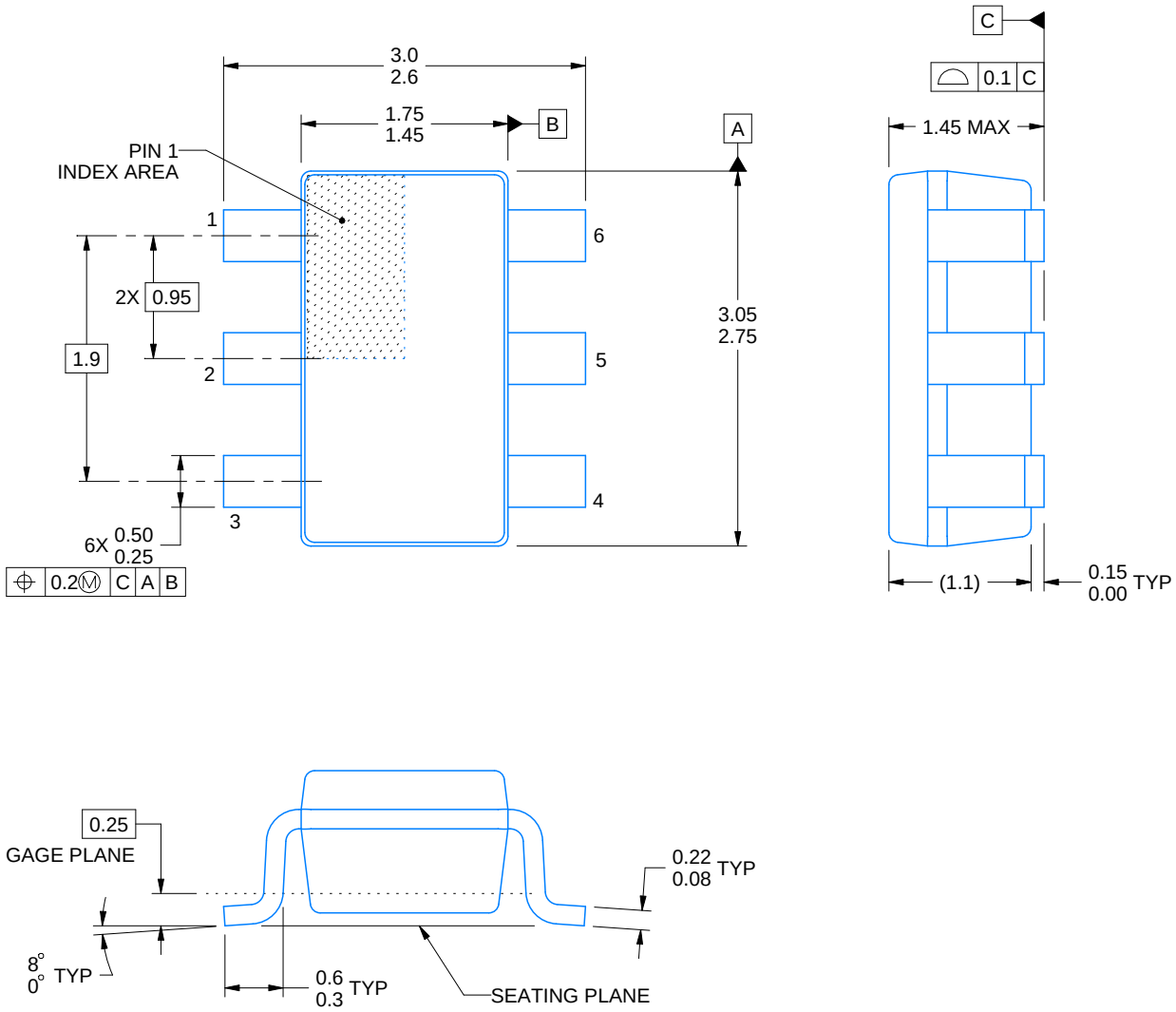
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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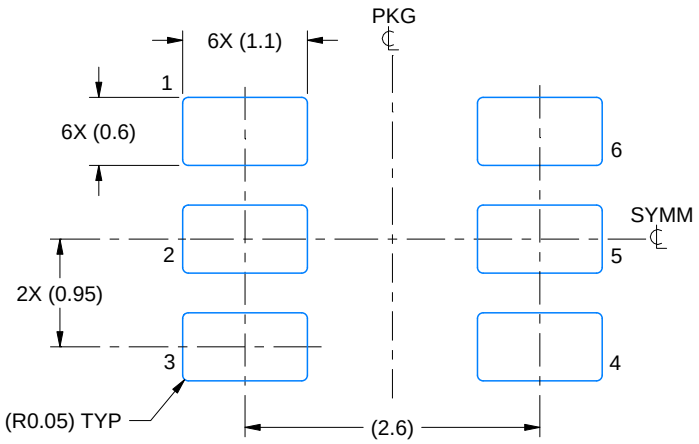
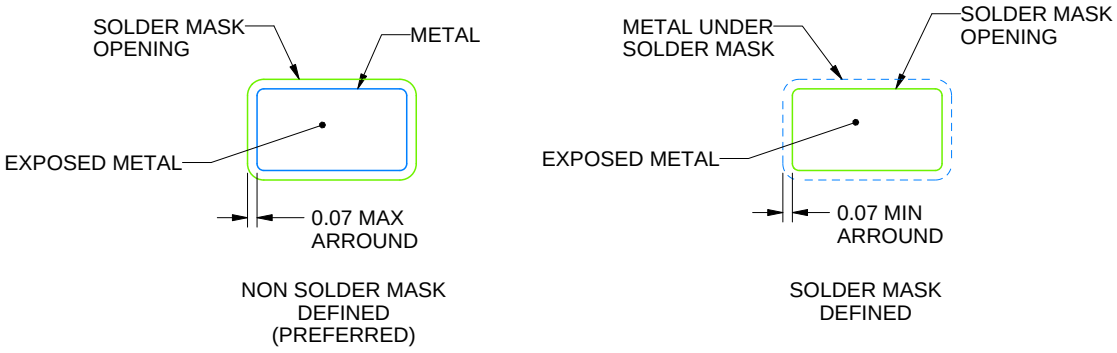
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

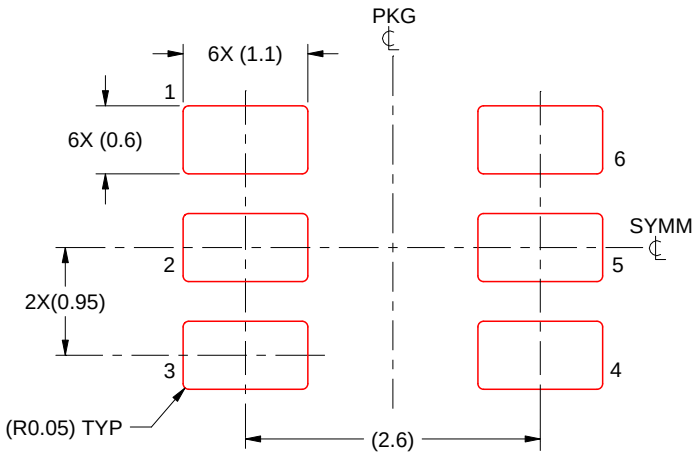


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



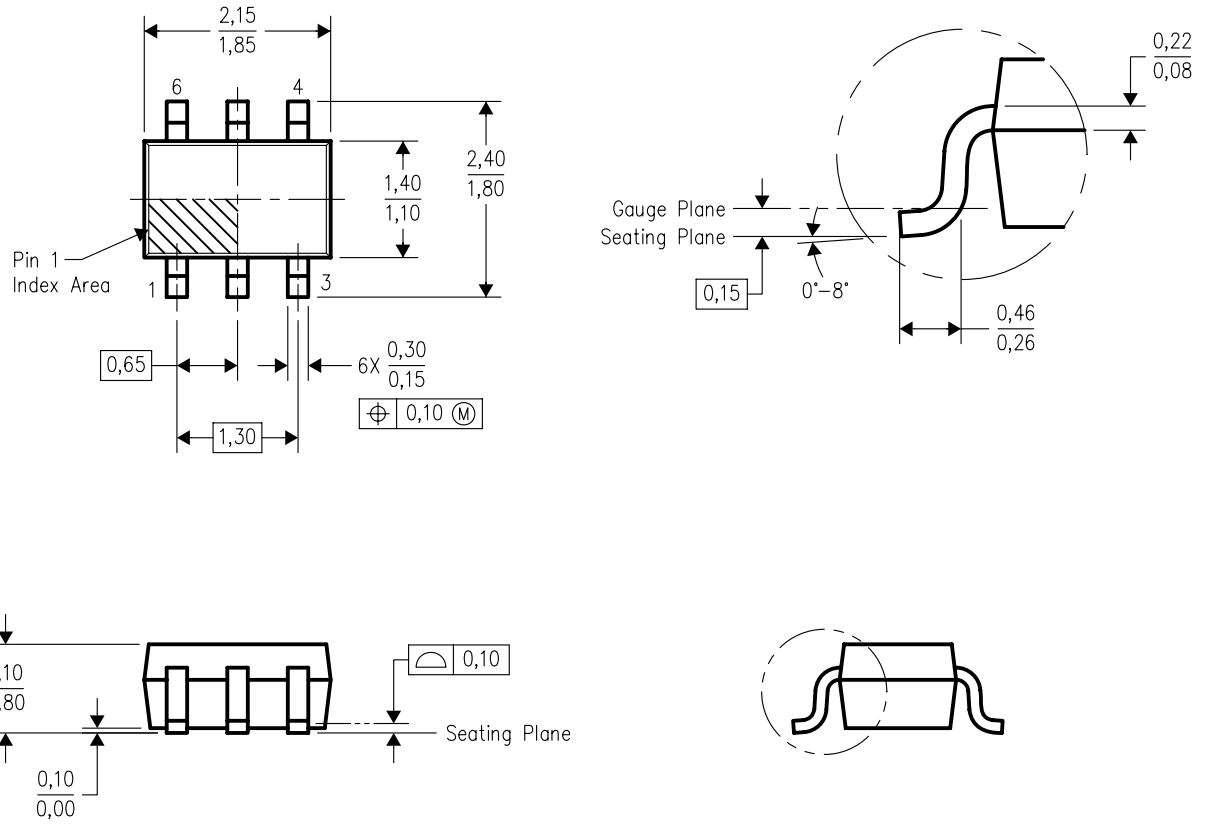
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

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