TMP708 采用 SOT 封装的电阻可编程温度开关

1 特性

- 阈值精度：
  - 典型值 ±0.5°C
  - 最大值 ±3°C（60°C 至 100°C）
- 由 1% 外部电阻设定的温度阈值
- 低静态电流：40μA（典型值）
- 开漏、低电平有效输出级
- 可通过引脚选择的 10°C 或者 30°C 温度滞后
- V_{CC} = 0.8 V 上指定的复位操作
- 电源范围：2.7V 至 5.5V
- 封装：5 引脚小外形尺寸晶体管 (SOT)-23

2 应用

- 计算机（笔记本和台式机）
- 服务器
- 工业用和医疗用设备
- 存储区域网络
- 汽车用

3 说明

TMP708 是一款全集成式电阻可编程温度开关，其温度阈值仅由一个外部电阻在整个运行范围内进行设定。TMP708 提供一个低电平有效的开漏输出，可由电压介于 2.7V 至 5.5V 范围内的电源供电。

温度阈值精度通常为 ±0.5°C，最大值为 ±3°C（60°C 至 100°C）。静态消耗电流的典型值为 40μA。可通过选择引脚来确定 10°C 或者 30°C 的温度滞后。

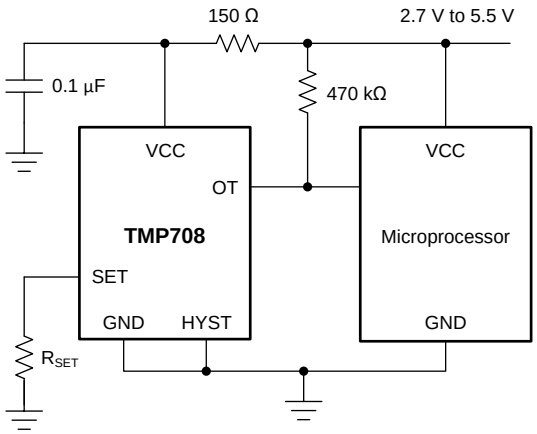
TMP708 采用 5 引脚小外形尺寸晶体管 (SOT-23) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMP708	SOT-23 (5)	2.90mm x 1.60mm

(1) 要了解所有可用封装，请见数据表末尾的封装选项附录。

典型应用



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (February 2012) to Revision B **Page**

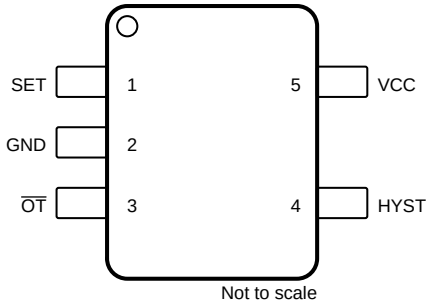
- 已添加 *器件信息*，*ESD 额定值*和*建议运行条件表*，*详细 说明*，*应用和实施*，*电源相关建议*，*布局*，*器件和文档支持*以及*机械、封装和可订购信息*部分 ... 1
- Deleted *Package and Ordering Information* table; information now available in package option addendum located at the end of this data sheet ... 2

Changes from Original (December 2011) to Revision A **Page**

- 最新的阈值精度特性着着重号 ... 1
- 更新了*说明*部分第二段中有关阈值精度的文本 ... 1
- Updated temperature error parameter in the Electrical Characteristics ... 5

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	Analog power	Device ground
HYST	4	Digital input	Hysteresis selection. For 10°C, HYST = VCC; for 30°C, HYST = GND.
$\overline{OT}$	3	Digital output	Open-drain, active low output
SET	1	Analog input	Temperature set point. Connect an external 1% resistor between SET and GND.
VCC	5	Analog power	Power-supply voltage (2.7 V to 5.5 V)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	Supply, VCC	–0.3	6	V
	Input, SET and HYST	–0.3	V_{CC} + 0.3	
	Output, OT	–0.3	6	
Current	Input		20	mA
	Output		20	
Temperature	Operating, T_A	–40	125	°C
	Junction, T_J		150	
	Storatge, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7		5.5	V
T_A	Operating temperature	0		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMP708 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	217.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 0°C to 125°C and V_{CC} = 2.7 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{CC}	Supply current	V_{CC} = 5 V		40	55	µA
		V_{CC} = 2.7 V		40	55	µA
TEMPERATURE						
T_E	Temperature error	T_A = 60°C to 100°C		±0.5	±3	°C
DIGITAL INPUT (HYST)						
V_{IH}	High-level input voltage		0.7 × V_{CC}			V
V_{IL}	Low-level input voltage				0.3 × V_{CC}	V
I_{lkg_in}	Input leakage current			1		µA
C_{IN}	Input capacitance			10		pF
ANALOG INPUT (SET)						
V_{IN}	Input voltage range		0		V_{CC}	V
DIGITAL OPEN-DRAIN OUTPUT ($\overline{OT}$)						
$I_{(OT\_SINK)}$	Output sink current	V_{OT} = 0.3 V	5	12		mA
$I_{lkg(OT)}$	Output leakage current	V_{OT} = V_{CC}		1		µA

6.6 Typical Characteristics

at T_A = 25°C and V_{CC} = 2.7 V to 5.5 V (unless otherwise noted)

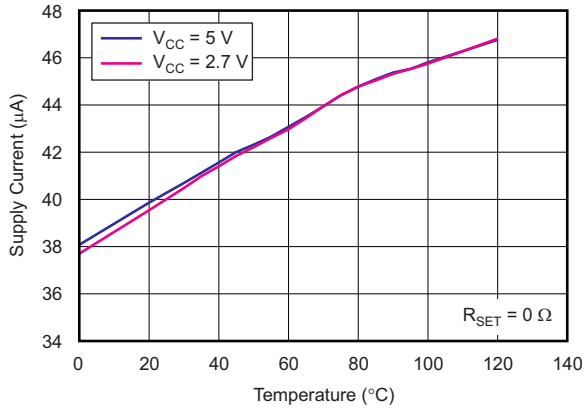


Figure 1. Supply Current vs Temperature

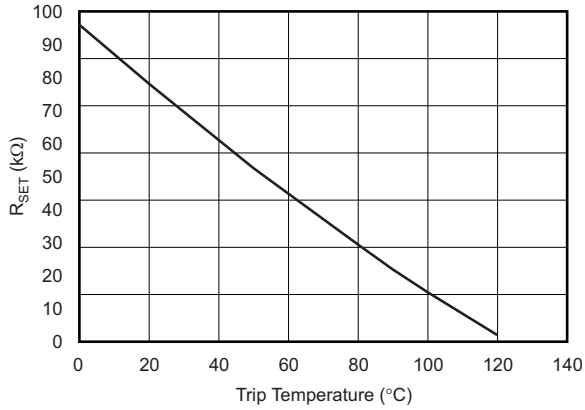


Figure 2. R_{SET} vs Trip Temperature

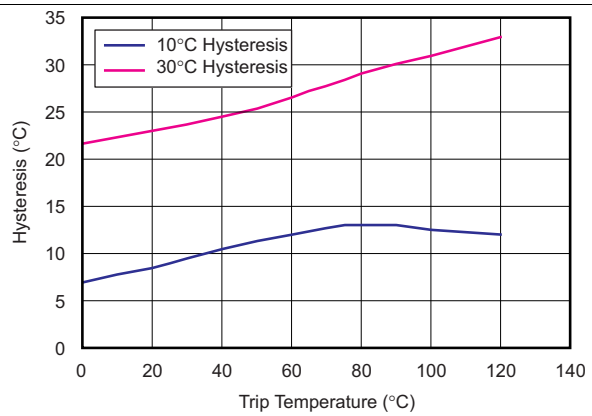


Figure 3. Hysteresis vs Trip Temperature

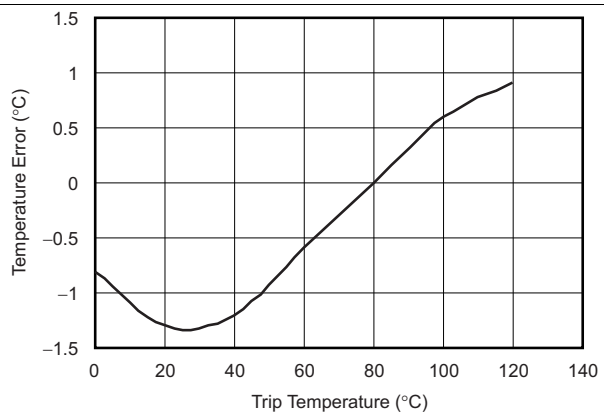


Figure 4. Temperature Error vs Trip Temperature

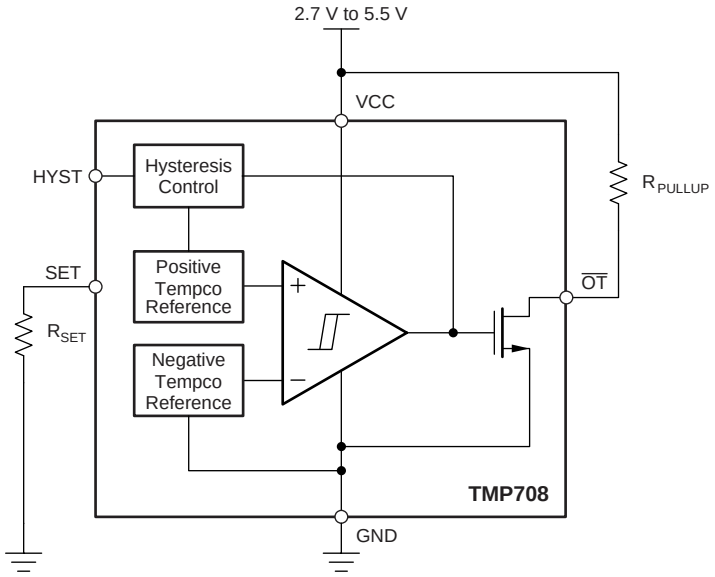
7 Detailed Description

7.1 Overview

The TMP708 is a fully-integrated, resistor-programmable temperature switch that incorporates two temperature-dependent voltage references and one comparator. One voltage reference exhibits a positive temperature coefficient (tempco), and the other voltage reference exhibits a negative tempco. The temperature at which both voltage references are equal determines the temperature trip point.

The Functional Block Diagram shows the comparator, the NFET open-drain device connected to the $\overline{OT}$ pin, the positive tempco reference using the external R_{SET} resistor, the negative tempco reference, and the hysteresis control. The voltage of the positive tempco reference is controlled by external resistor R_{SET}.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Temperature Switch

The TMP708 temperature threshold is programmable from 0°C to 125°C and is set by an external 1% resistor from the SET pin to the GND pin. The TMP708 has an open-drain, active-low output structure that easily interfaces with a microprocessor.

The TMP708 reaches the temperature trip point when the voltage from the positive tempco reference exceeds the voltage from the negative tempco reference. This difference causes the output of the comparator to switch from logic 0 to logic 1. The comparator output drives the gate of the NFET open-drain device, and pulls the voltage on the $\overline{OT}$ pin from logic 1 to logic 0 under these conditions; in other words, the output *trips*. Furthermore, the logic 1 output from the comparator causes the hysteresis control to increase the voltage of the positive tempco reference by an amount set by the logic setting on the HYST pin (10°C for logic 1 on the HYST pin; 30°C for logic 0 on the HYST pin). Increase the voltage of the positive tempco reference after the TMP708 trips to stop the TMP708 from untripping (voltage on the $\overline{OT}$ pin changing from logic 0 to logic 1) until the local temperature reduces by the amount set by the HYST pin. After the local temperature reduces, and the voltage from the positive tempco reference is less than the voltage from the negative tempco reference, the output of the comparator switches from logic 1 to logic 0. This condition causes the voltage on the $\overline{OT}$ pin to change from logic 0 to logic 1 (device untrips).

7.3.2 Hysteresis Input

The HYST pin is a digital input that allows the input hysteresis to be set at either 10°C (when HYST = VCC) or 30°C (when HYST = GND). The hysteresis function keeps the $\overline{OT}$ pin from oscillating when the temperature is near the threshold. Thus, always connect the HYST pin to either VCC or GND. Other input voltages on this pin can cause abnormal supply currents or a device malfunction.

7.3.3 Set-Point Resistor (R_{SET})

Set the temperature threshold by connecting R_{SET} from the SET pin to GND. The value of R_{SET} is determined using either Figure 2 or Equation 1:

$$R_{SET}\ (k\Omega) = 0.0012T^2 - 0.9308T + 96.147 \quad (1)$$

where

- T = temperature threshold in degrees Celsius.

7.4 Device Functional Modes

The TMP708 device has a single functional mode. Normal operation for the TMP708 device occurs when the power-supply voltage applied across the VCC and GND pins is within the specified operating range of 2.7 V to 5.5 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP708 device is simple to configure. The only external components that the device requires are a bypass capacitor and pullup resistor. Power-supply bypassing is strongly recommended. Use a 0.1-µF capacitor placed as close as possible to the VCC supply pin. To minimize the internal power dissipation of the TMP708 family of devices, use a pullup resistor value greater than 10 kΩ from the $\overline{OT}$ pin to the VCC pin. See the *Hysteresis Input* section for hysteresis configuration, and the *Set-Point Resistor (R_{SET})* section for configuring the temperature threshold.

8.2 Typical Application

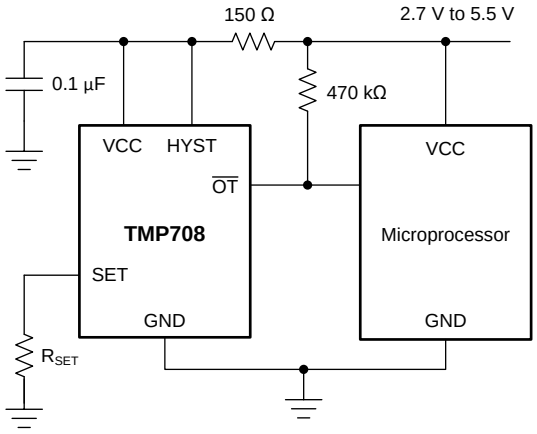


Figure 5. Overtemperature Protection for a 60°C Trip Point

8.2.1 Design Requirements

For this design example, a 2.7-V to 5.5-V power supply, 60°C trip point, and 10°C hysteresis are used.

Typical Application (continued)

8.2.2 Detailed Design Procedure

Connect the HYST pin to VCC for 10°C hysteresis. For a 60°C temperature threshold, see the *Set-Point Resistor (R_{SET})* section to compute an ideal R_{SET} resistor value of 44.619 kΩ. Select the closest standard value resistor available; in this case, 44.2 kΩ. Use a 10-kΩ pullup resistor from the $\overline{OT}$ pin to the VCC pin. To minimize power, a larger-value pullup resistor can be used, but must not exceed 470 kΩ. Place a 0.1-μF bypass capacitor close to the TMP708 device in order to reduce noise coupled from the power supply.

8.2.3 Application Curves

Figure 6 shows an example of the hysteresis feature. The HYST pin is connected to VCC, so the TMP708 device is configured for 10°C of hysteresis. The device is configured for a 60°C trip temperature by the R_{SET} resistor value; therefore, the $\overline{OT}$ output asserts low when the 60°C threshold is exceeded. The $\overline{OT}$ output remains asserted low until the sensor reaches 50°C.

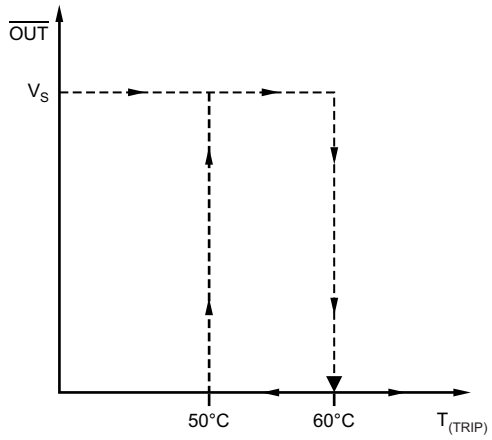


Figure 6. TMP708 Hysteresis Function

9 Power Supply Recommendations

The TMP708 low supply current and supply range allow this device to be powered from many sources. Any significant noise on the VCC pin can result in a trip-point error. Minimize this noise by low-pass filtering the device supply (V_{CC}) using a 150-Ω resistor and a 0.1-μF capacitor.

10 Layout

10.1 Layout Guidelines

The TMP708 is extremely simple to lay out. Figure 7 shows the recommended board layout.

10.2 Layout Example

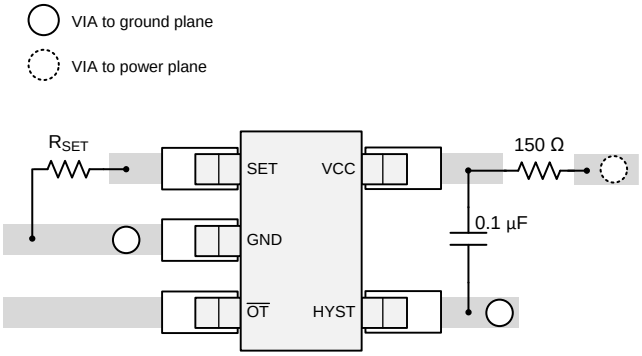


Figure 7. Recommended Layout

10.3 Thermal Considerations

The TMP708 quiescent current is typically 40 μA. The device dissipates negligible power when the output drives a high-impedance load. Thus, the die temperature is the same as the package temperature. In order to maintain accurate temperature monitoring, provide a good thermal contact between the TMP708 package and the device being monitored. The rise in die temperature as a result of self-heating is given by Equation 2:

$$\Delta T_J = P_{DISS} \times \theta_{JA} \quad (2)$$

where

- P_{DISS} = power dissipated by the device.
- θ_{JA} = package thermal resistance. Typical thermal resistance for SOT-23 package is 217.9°C/W.

To limit the effects of self-heating, keep the output current at a minimum level.

11 器件和文档支持

11.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.2 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP708AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBI	Samples
TMP708AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

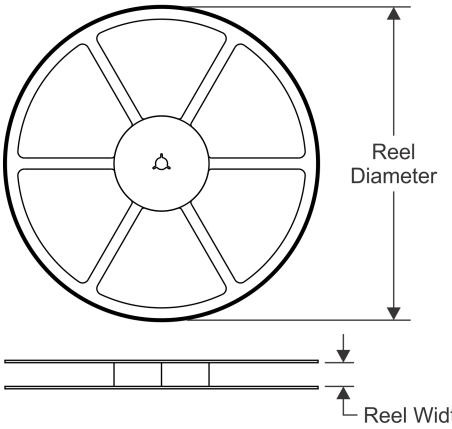
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

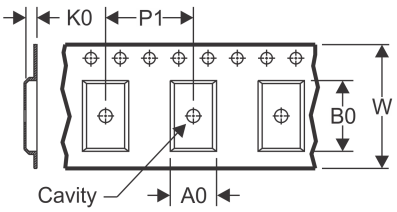
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

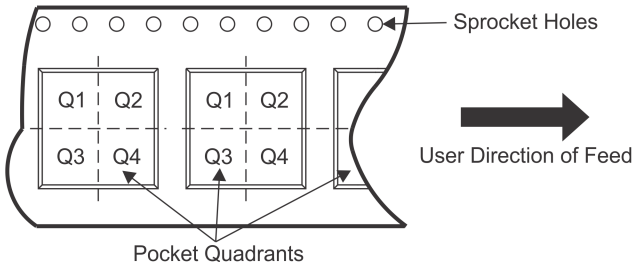


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

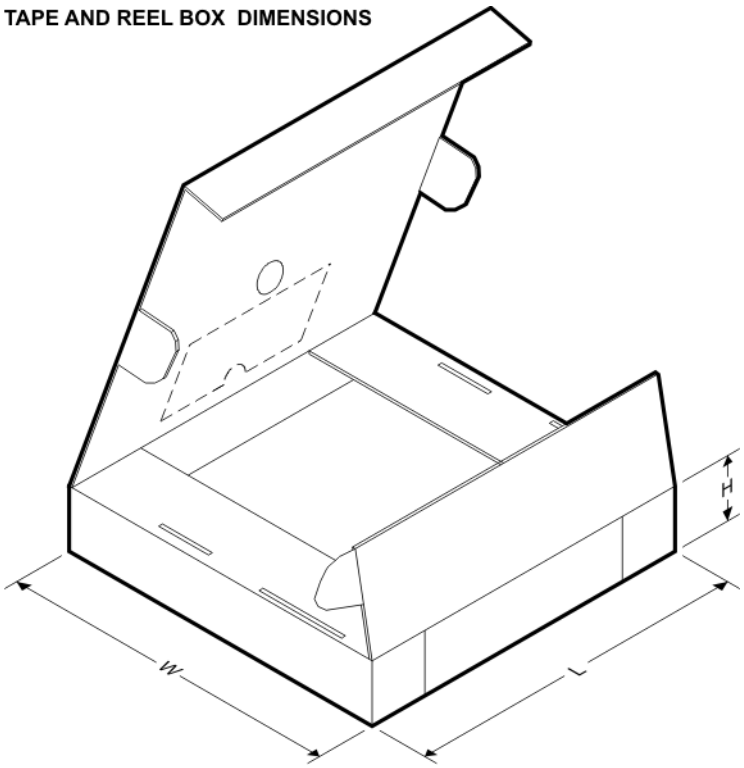
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP708AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TMP708AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

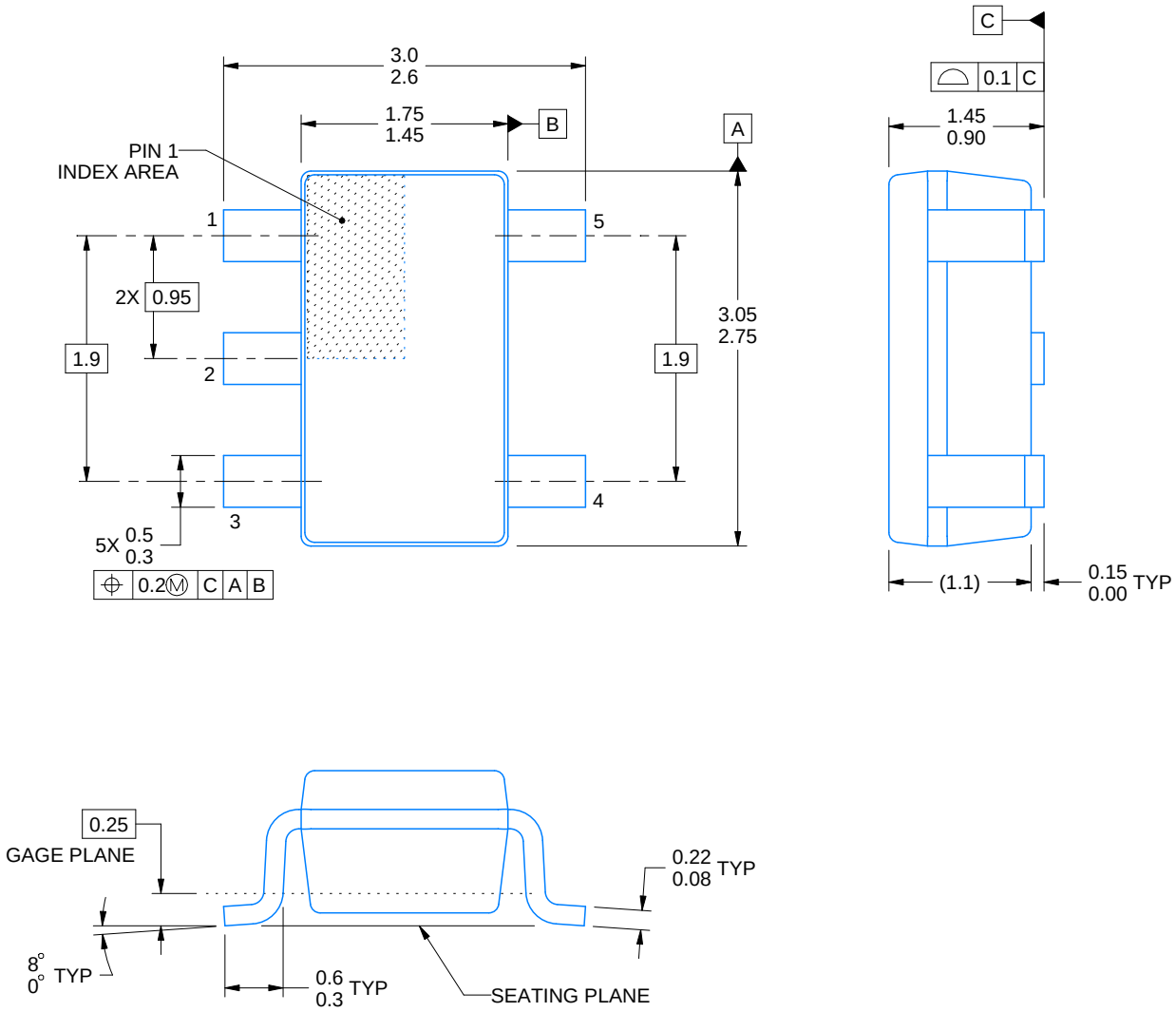
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP708AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TMP708AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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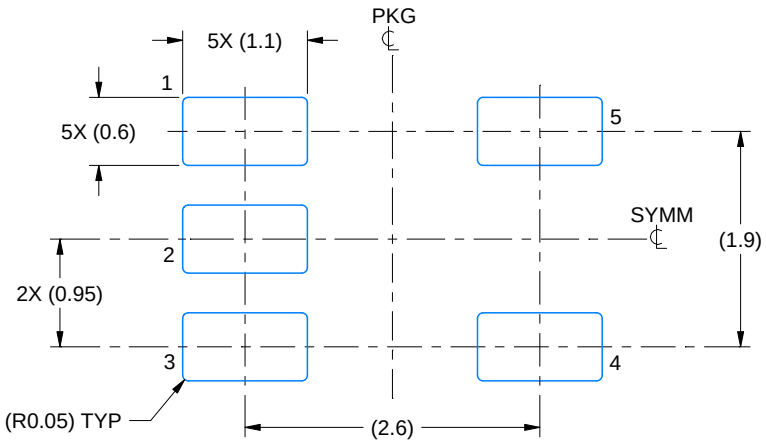
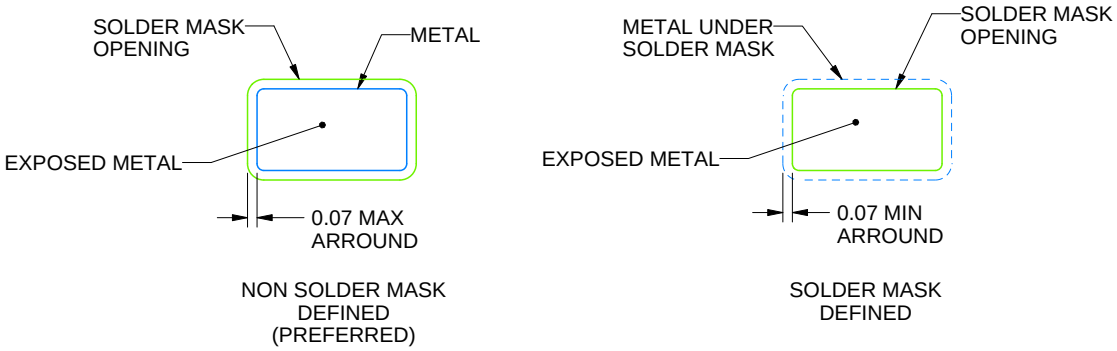
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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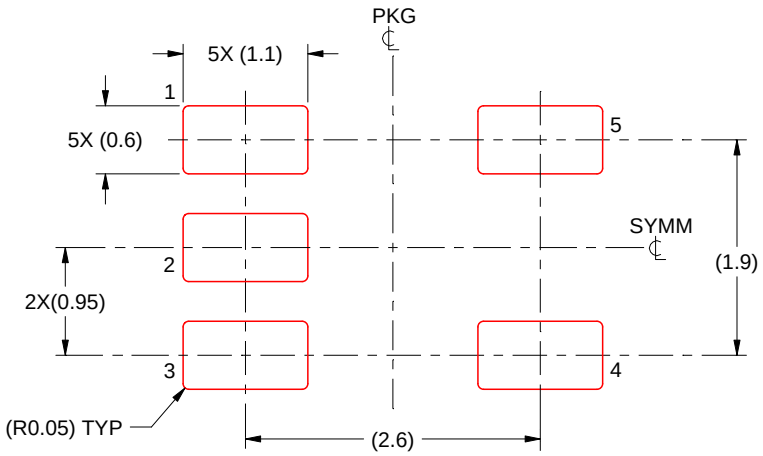
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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